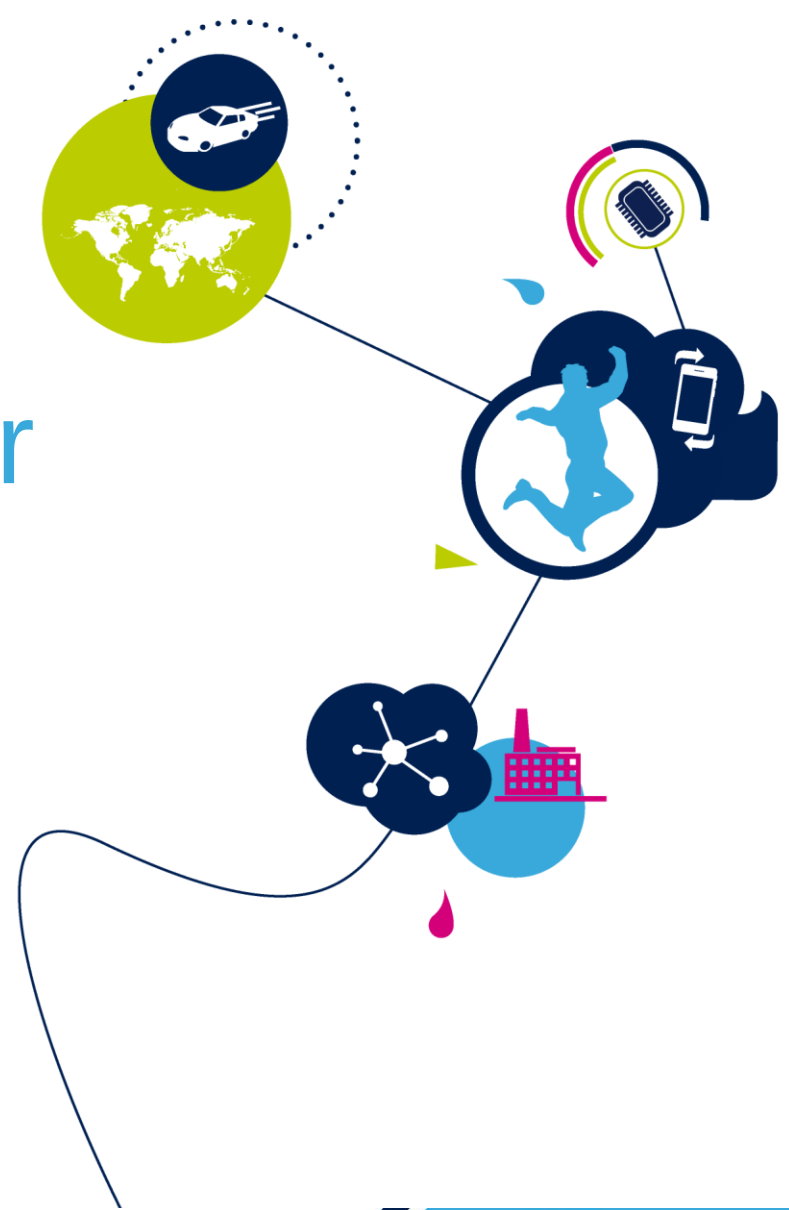
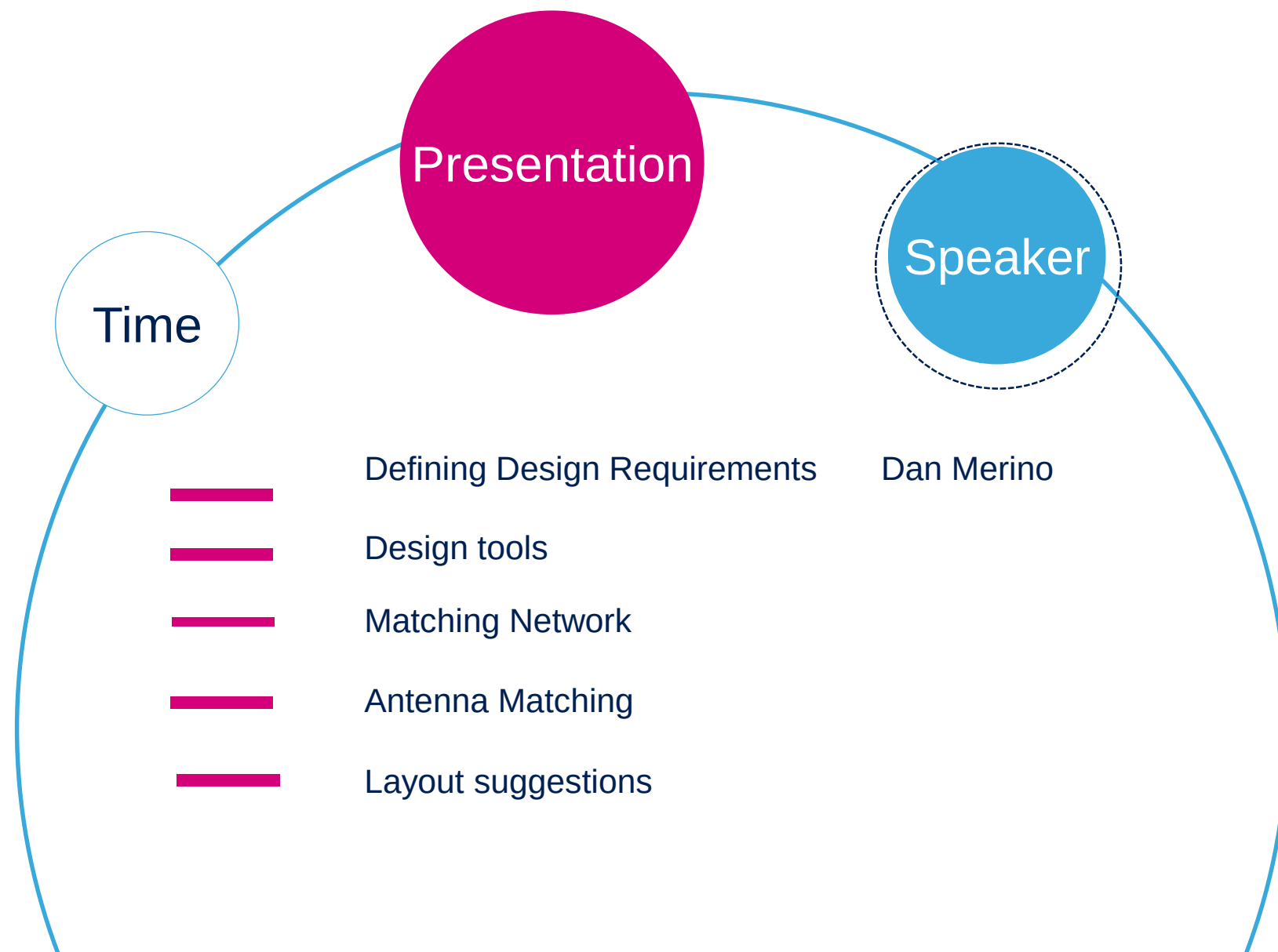


How to Design a NFC Reader Application

A Step by Step Approach

Daniel Merino







Defining Design Requirements

Defining Design Requirements

4

- End Product
 - Payment
 - General Purpose
- Communication Protocol
 - ISO 14443 A/B
 - ISO 15693
 - Felica
 - AP2P.

Defining Design Requirements

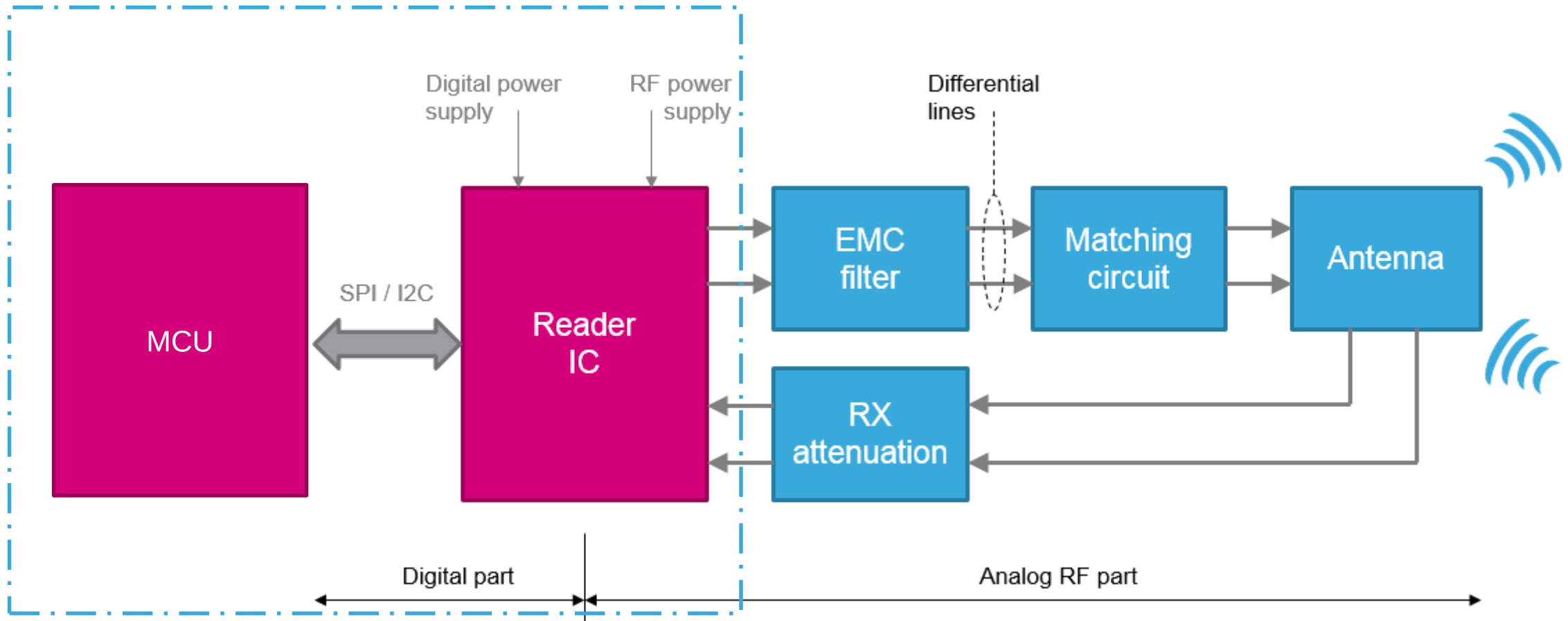
5

- System constraints
 - Antenna Size
 - Environmental Conditions
 - Metal
 - LCD screen
 - Antenna placement
- Design Trade-offs
 - Antenna size
 - Read Range
 - Current Consumption



System Block Diagram

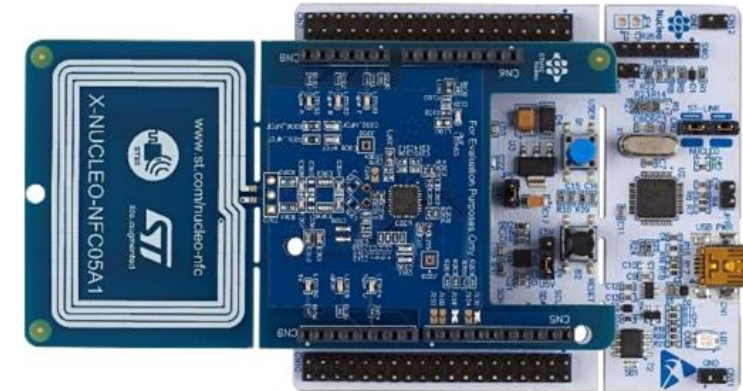
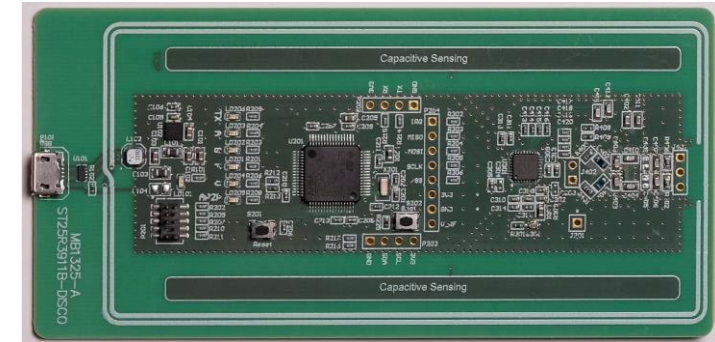
System Block Diagram 7



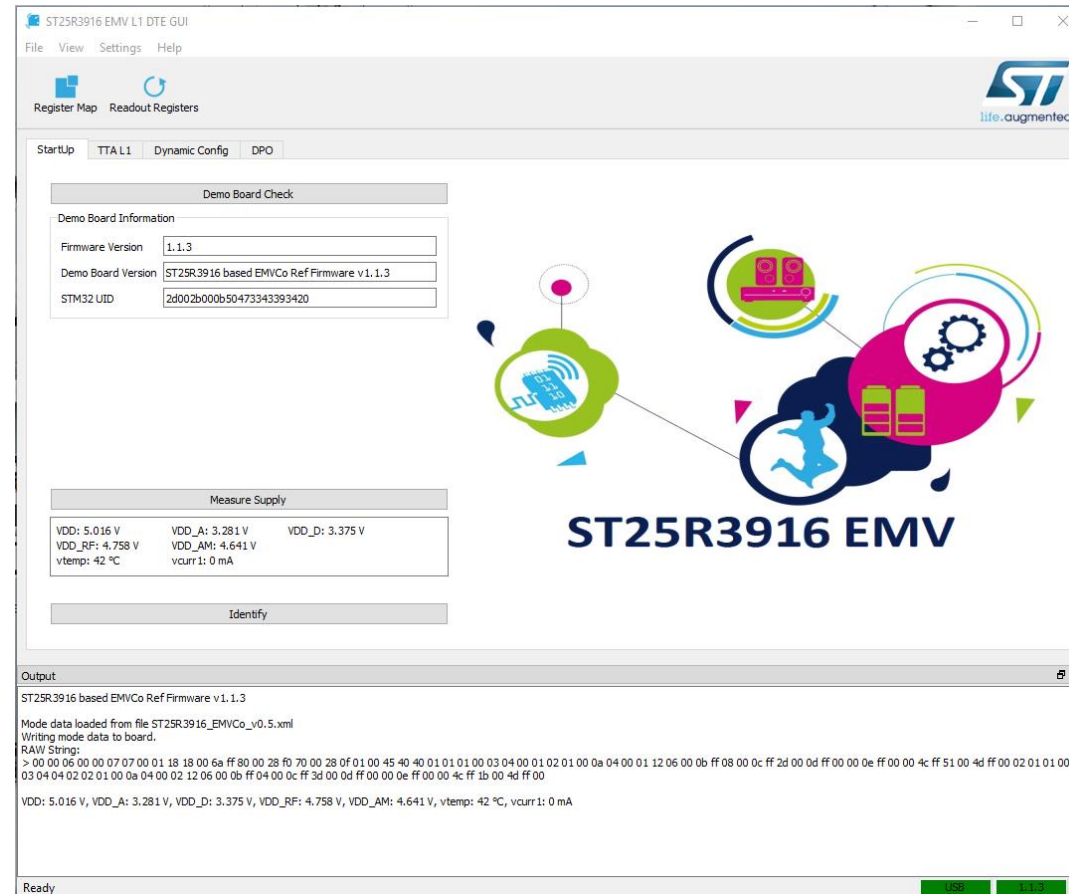


Design Tools

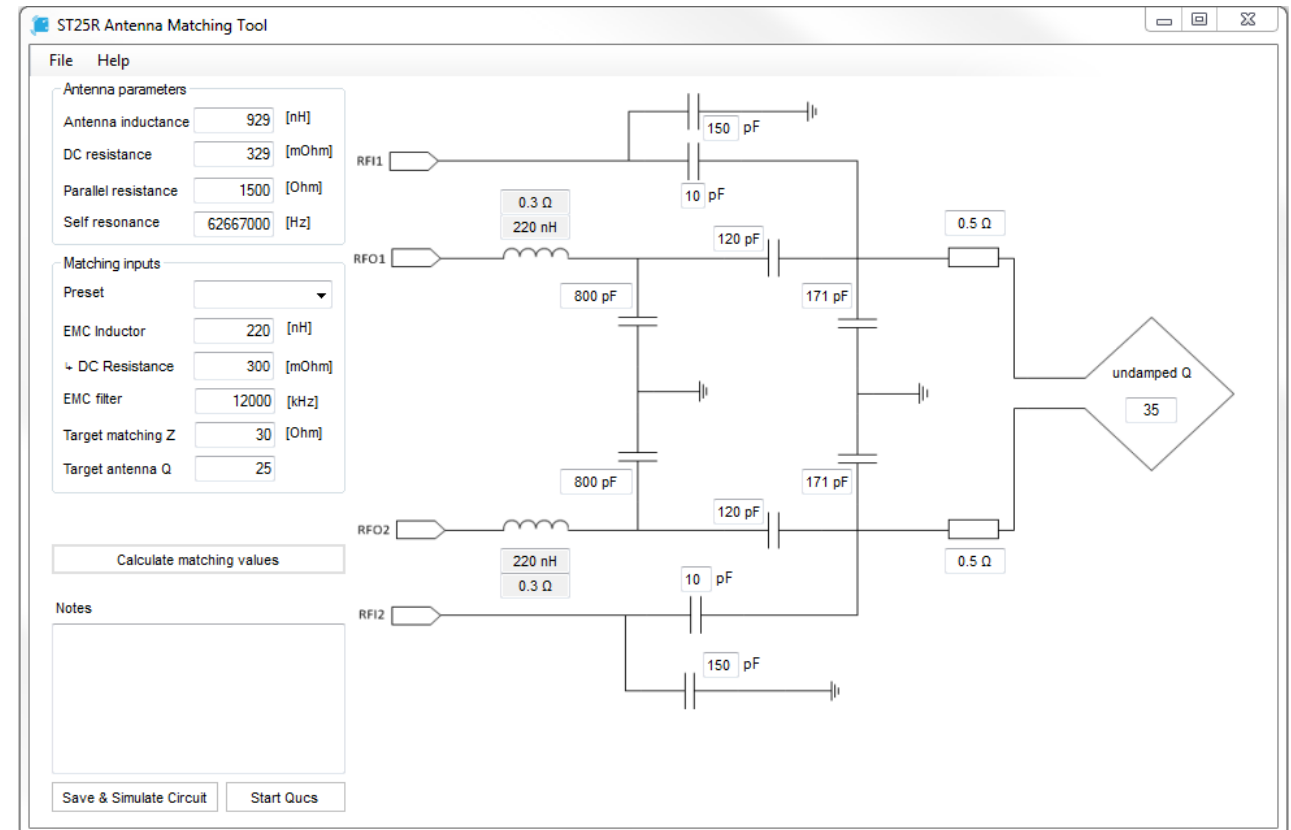
- ST25R3911B Discovery
 - Software GUI
 - Source code downloadable
 - Design files downloadable
- ST25R3911B Nucleo Shield
 - Firmware available
 - Design files downloadable
- ST25R3916 Discovery
 - Software GUI
 - Source code downloadable
 - Design files downloadable



- EMVCo Reference design
 - Hardware eval board
 - Software GUI
 - L1 Stack
 - Available only by Request



- Antenna Design Matching tool
 - Calculates matching components
 - Includes simulation program
 - Available on ST25R3911B landing page

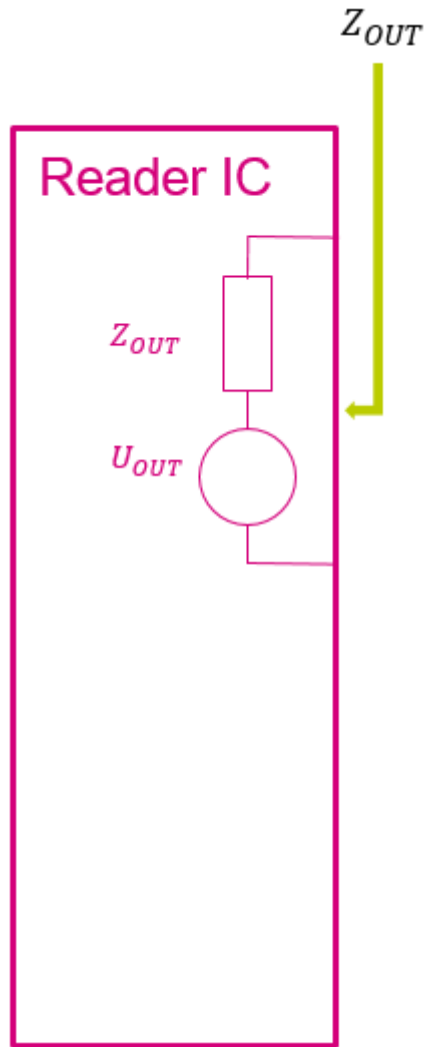




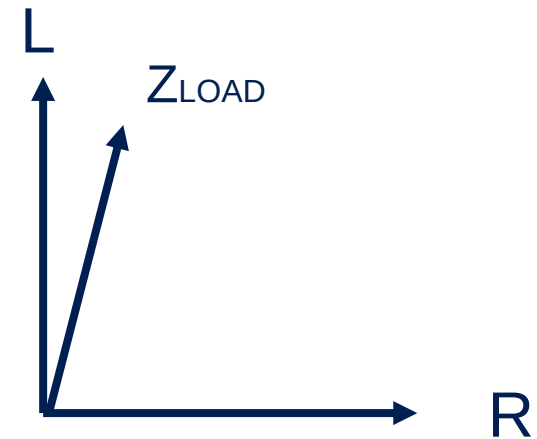
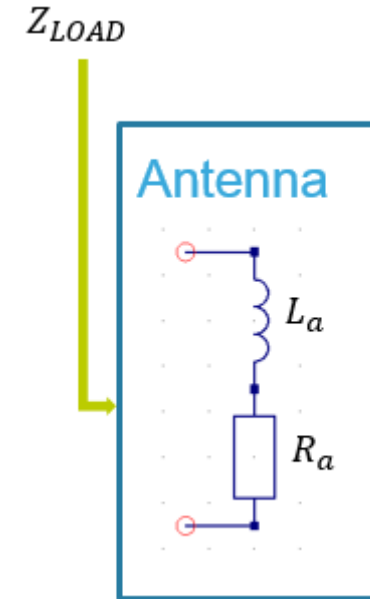
Matching Network

Matching Circuit

14

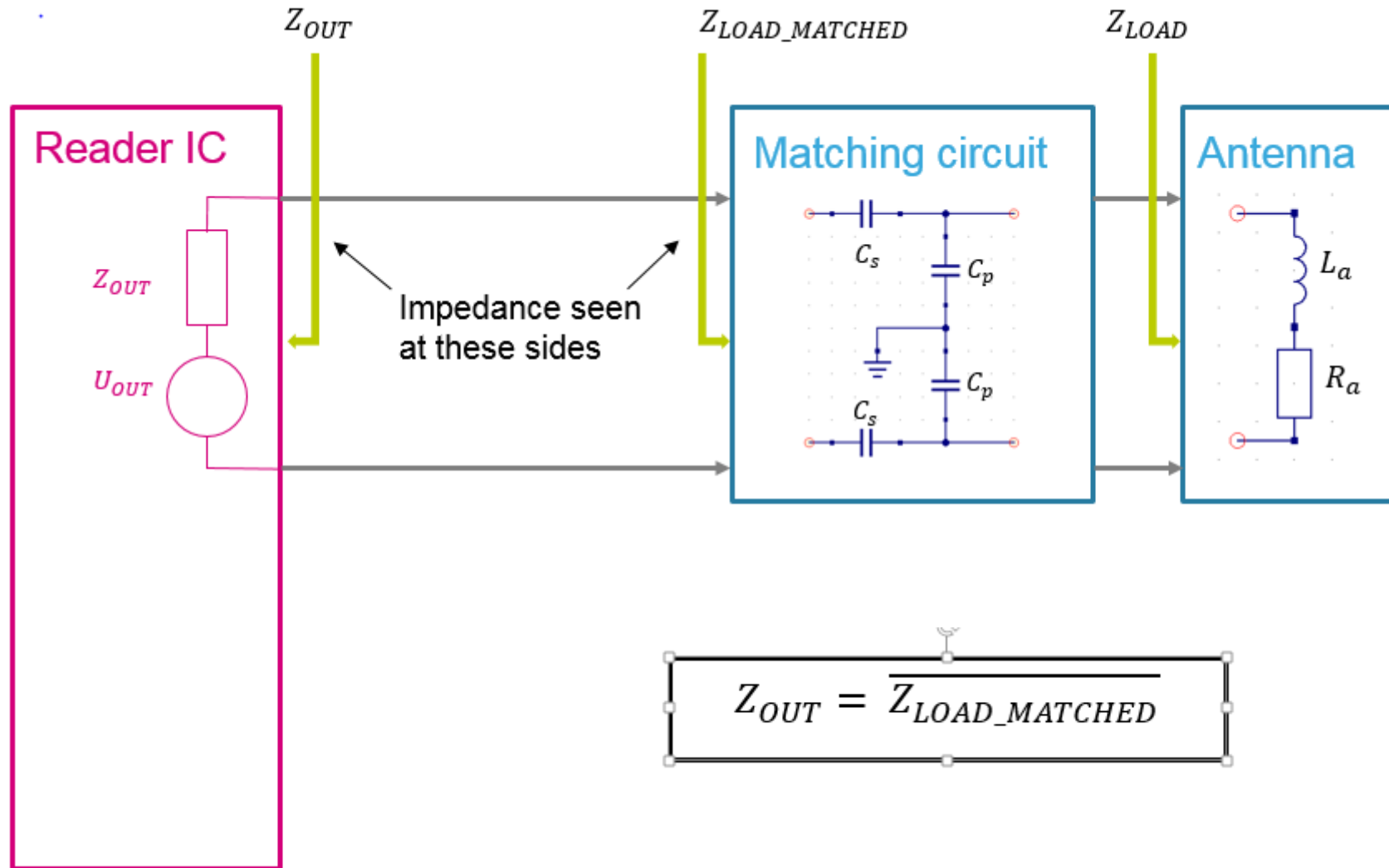


$$Z_{out} = \overline{Z_{LOAD}}$$



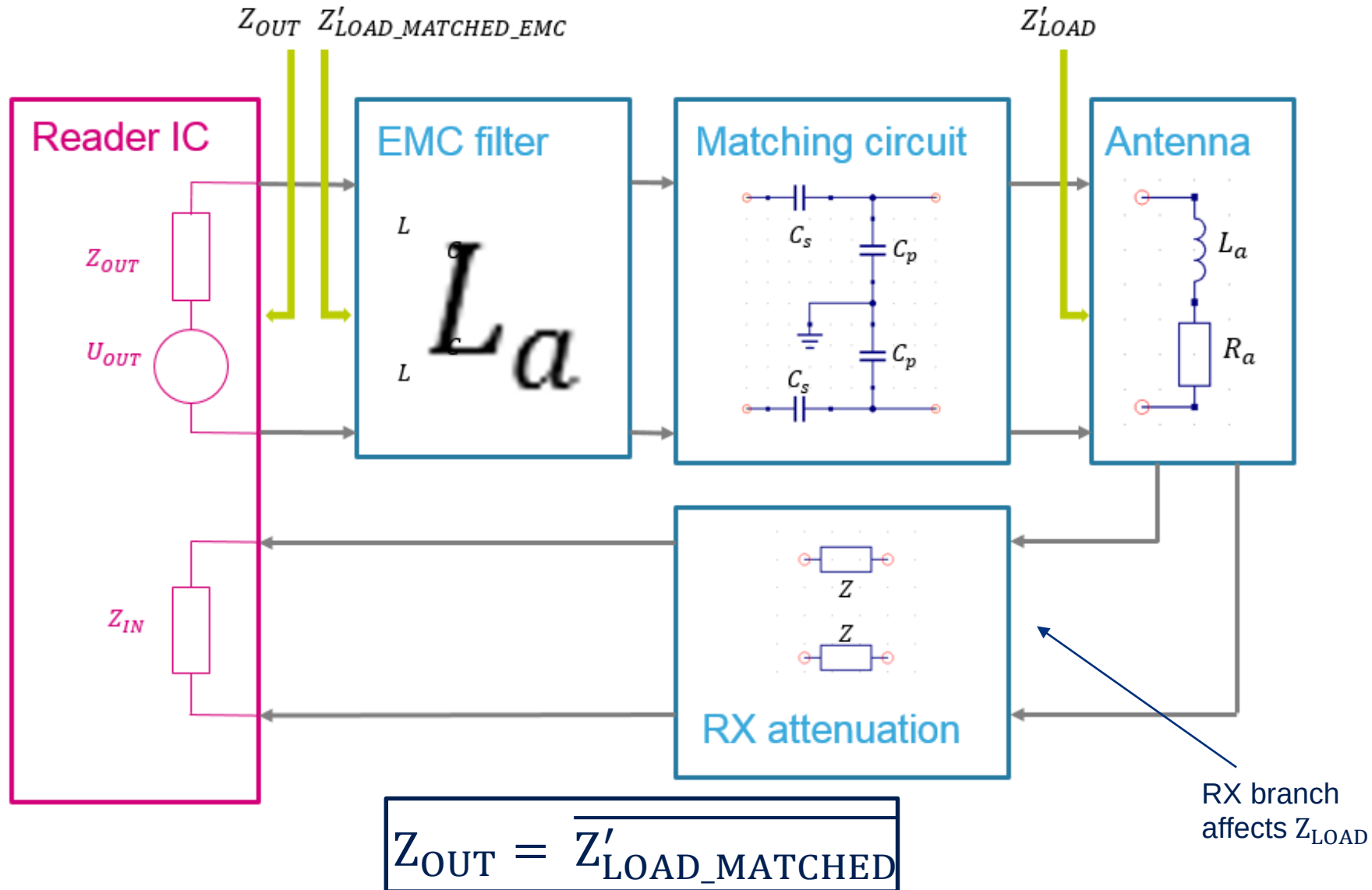
Matching Circuit

15



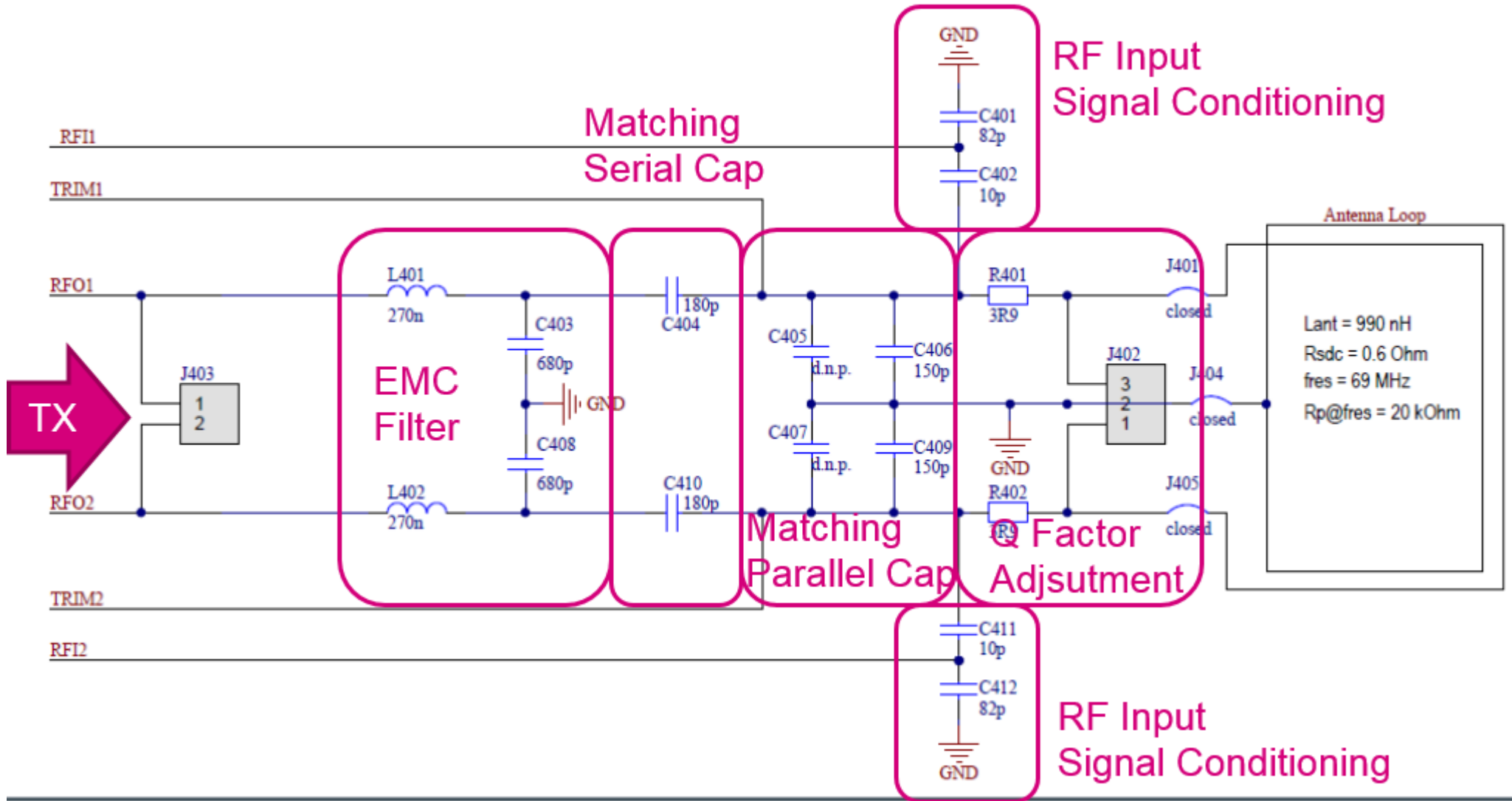
Matching Circuit

16



Matching Circuit

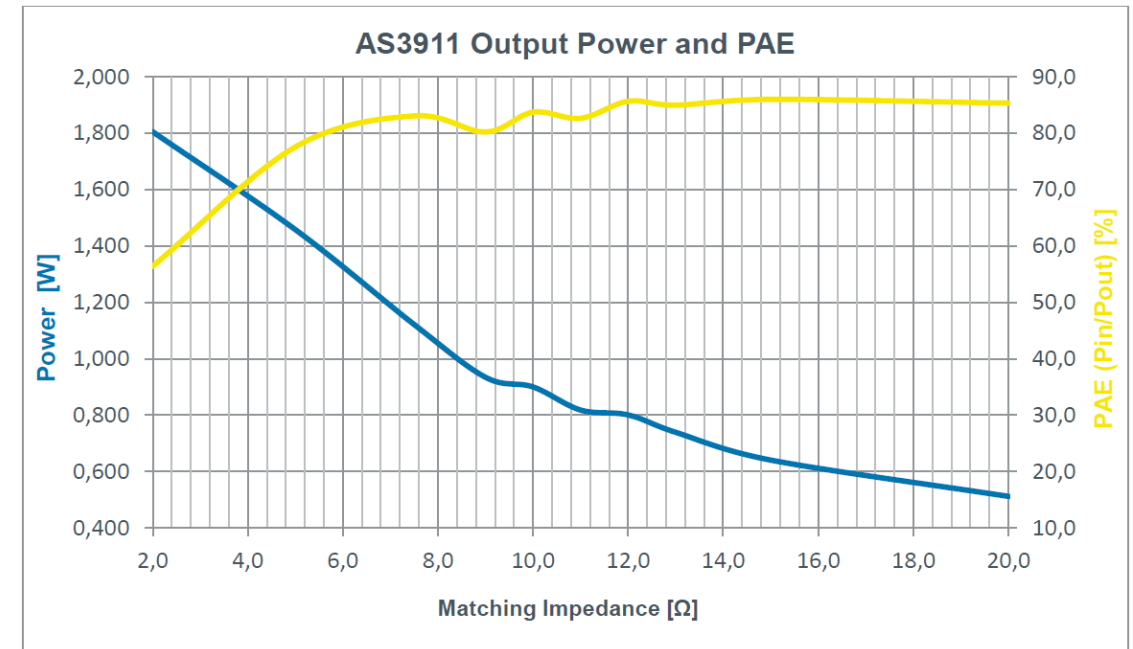
17



- Antenna
 - Two Turn
 - Typical Inductance 200nH – 2uH
- EMC Filter
 - Reduces harmonics of the RFO output stage
 - Target Cutoff Frequency about 13.56Mhz
- Matching Serial Cap
 - Impedance match from EMC filter to antenna resonator circuit
 - Cuts DC path from RFO1 to RFO2

- Q Factor adjustment
 - Sets System Q (antenna Q should always be higher than System Q)
 - Higher Q > More Field Strength > Lower Datarate
 - Lower Q > Faster rise/fall times > Higher Datarate
 - Target Values
 - Up to 106kbps – 25
 - Up to 848kbps – 12-16
 - Up to 3.4Mbps - 8
- RFI Input Conditioning
 - Reduces Antenna Voltage to < 3.0Vpp for RFI input

- Target Matching impedance
 - Higher > less field strength > less power consumption > higher efficiency
 - Lower > higher field strength > higher power consumption > less efficiency
 - Range 8 – 120 ohms
 - Typically between 10 – 30 ohms



Antenna Parameters

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Parameter	Action	Effect on parameter	Q factor
Q factor	Increase trace width	-	Increases
	Increase gap width		
Inductance	Larger antenna	Increases	Decreases
	Decrease trace width		
	Decrease gap width		
Series DC resistance	Larger antenna	Increases	Decreases
	Decrease trace width		
	Decrease gap width		
Parallel resistance	Decrease trace width	Increases	Increases
	Increase gap width		
Resonance frequency	Smaller antenna	Increases	Increases
	increase gap width		



Antenna Matching

Antenna Measurements

23

- Measure the following Parameters with a VNA
 - DC resistance
 - Inductance
 - Self resonance frequency
 - Parallel R @ F_{SR}

1:	1,000,000Hz
RL	-0.24dB
RP	164.79°
Z	6.7Ω
Rs	0.7Ω
Xs	6.7Ω
Swr	71.2:1
Mag	0.972
2:	13,563,694Hz
RL	-0.23dB
RP	55.51°
Z	95.0Ω
Rs	3.1Ω
Xs	94.9Ω
Swr	74.7:1
Mag	0.974
3:	53,729,443Hz
RL	-0.40dB
RP	0.08°
Z	2196.1Ω
Rs	2195.1Ω
Xs	65.1Ω
Swr	43.9:1
Mag	0.955

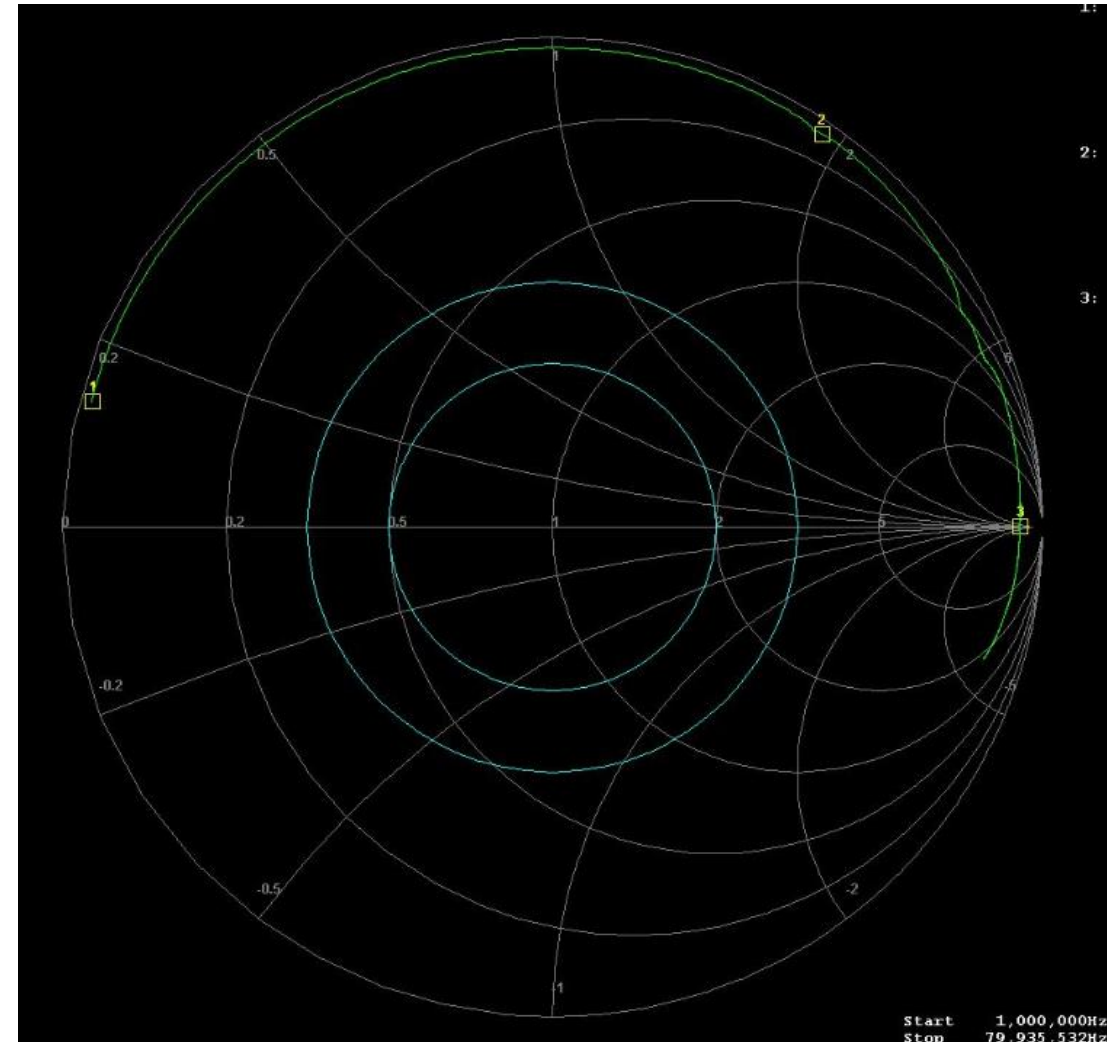
DC Resistance

Xs @13.56MHz
used to
calculate
inductance

Self Resonant
Frequency

Parallel
Resistance

$$Xs = j\omega L$$
$$L = \frac{Xs}{j\omega}$$



Antenna Measurements

24

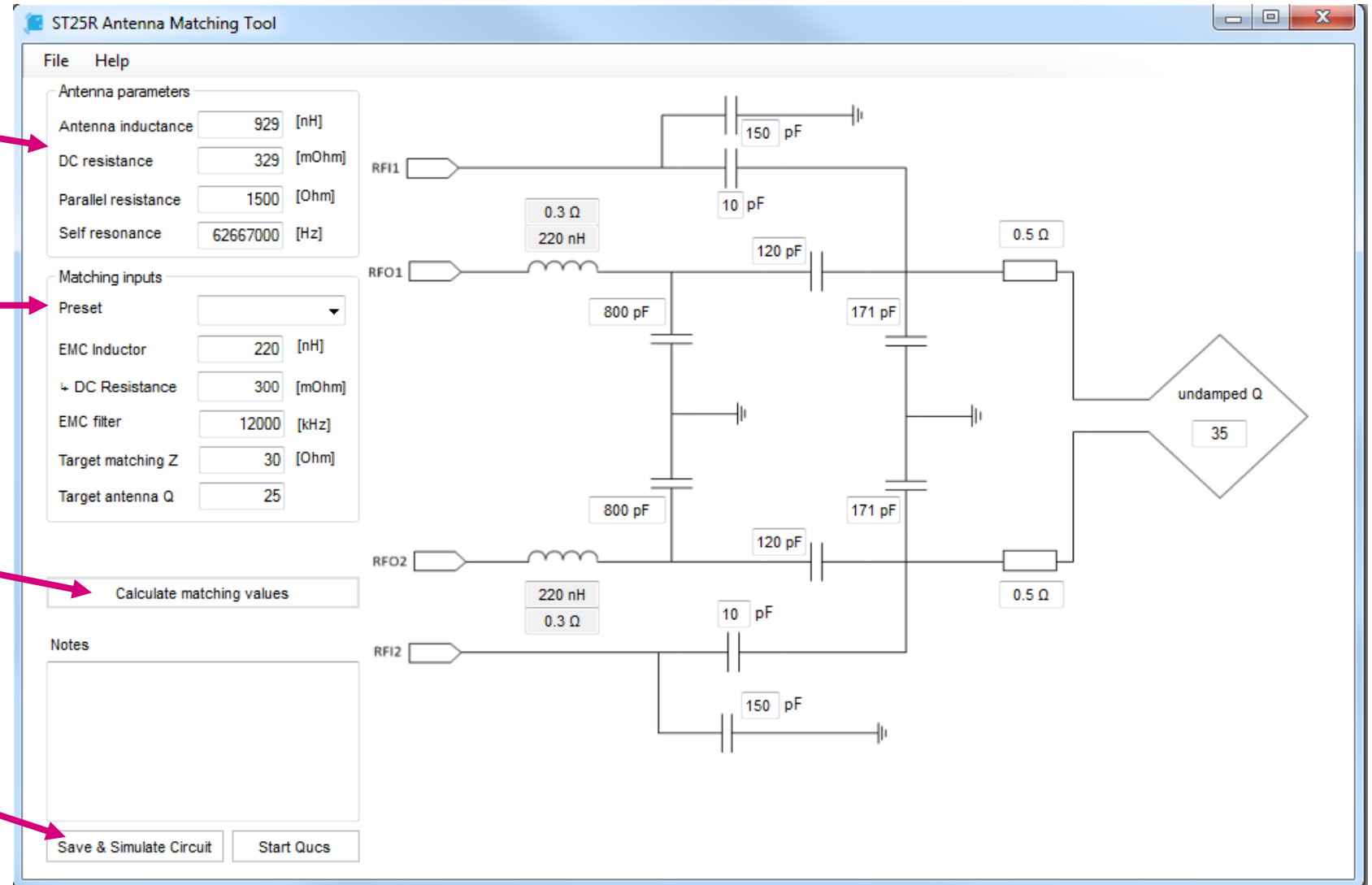
Input antenna parameters

Set pre-conditions

- EMVCo
- General Purpose
- VHBR

Calculate matching values

Simulate (opens QUCS)



Antenna Simulation

25

Simulations

ac simulation

AC1
Type=lin
Start=1 MHz
Stop=28 MHz
Points=1001
Noise=no

transient simulation

TR1
Type=lin
Start=0
Stop=4 us
Points=1024

S parameter simulation

SP1
Type=lin
Start=1 MHz
Stop=30 MHz
Points=1001

Component- Values

Equation	Equation	Equation	Equation	Equation
Eqn17 Zmatch=50 Zchip=3 Zchiphalf=1.5 AnalogSupplyVoltage=4.5	Eqn20 Lemc1=220 n RLemc1=0 Cemc1=749 p	Eqn22 Cs1=99 p Cp1=157 p Rdamp=0.50	Eqn18 Cvdrl=10 p Cvdr2=150 p	Eqn23 Cant1=7.88 p Lant1=1114 n Rant1=3262

AC Equations

Equation	Equation
Eqn7 magZin=mag((V_in_ac.v)/Pr13.i)	Eqn5 phaseZin=phase((V_in_ac.v)/Pr9.i) phaseCapDiff=phase((V_rfi_ac.v)/Pr13.i) phaseDiff=phaseCapDiff - phaseZin+180 phaseZemc=phase((V_emc_ac.v)/Pr9.i) phaseZout=phase((V_out_ac.v)/Pr9.i)
Eqn3 mag_V_out=mag((V_out_ac.v))	

Antenna - Trim

Equation	Equation	Equation
Eqn10 trim3=56 p trim2=27 p trim1=12 p trim0=5.6 p	Eqn9 Ctrimpara3=1.5 p Ctrimpara2=1.5 p Ctrimpara1=1.5 p Ctrimpara0=1.5 p	Eqn8 Rontrim3=5e5 Rontrim2=5e5 Rontrim1=5e5 Rontrim0=5e5 on = 14; off = 5e5 on = 25; off = 5e5 on = 50; off = 5e5 on = 100; off = 5e5

Capacitive Voltage Divider

Equation
Eqn2
 $V_{rfin} = V_{rfi} \cdot V_t + 1.5$

Impedance Calculation

Equation
Eqn1
 $Z_{rtot} = yvalue(rtot(S[1,1], P1, Z), 13500000)$

S-Parameter Equations

Equation	Equation
Eqn4 dBS11=db(S[3,3]) dBS21=db(S[4,3])	Eqn24 myphase=pt mymag=ma
Eqn16 $Q = xvalue(dBS21, max(dBS21)) / (abs(xvalue(dBS21, (max(dBS21)-3)) - (xvalue(dBS21, max(dBS21))))^2)$	

Component- Values

Equation
Eqn17
Zmatch=50
Zchip=3
Zchiphalf=1.5
AnalogSupplyVoltage=4.5

Equation
Eqn20
Lemc1=220 n
RLemc1=0.3
Cemc1=749 p

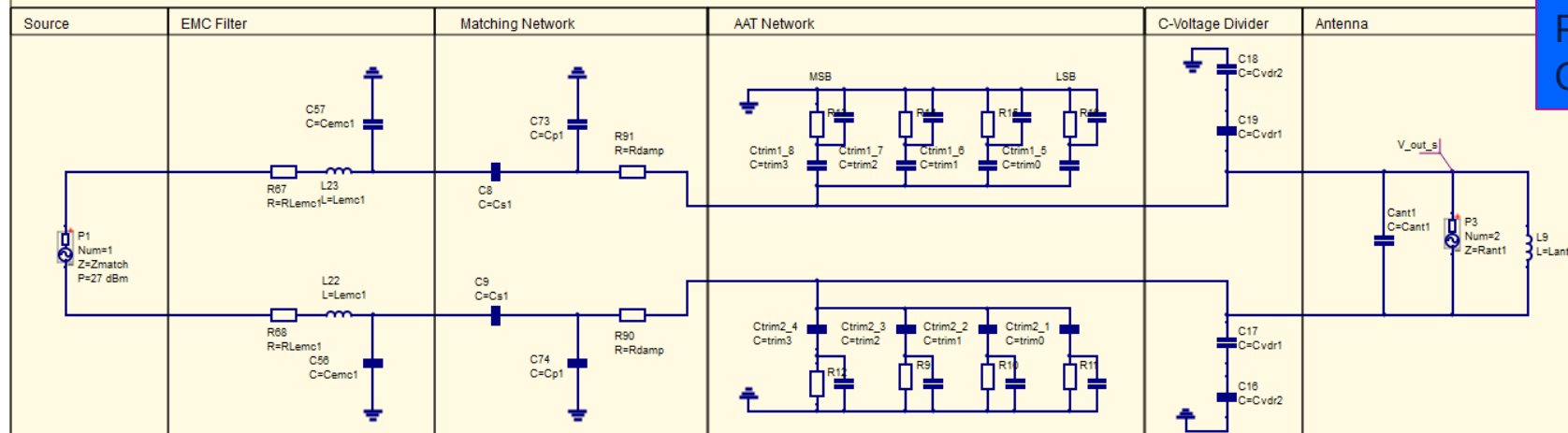
Equation
Eqn22
Cs1=106 p
Cp1=157 p
Rdamp=0.45

Equation
Eqn18
Cvdrl=10 p
Cvdr2=150 p

Equation
Eqn23
Cant1=9.02 p
Lant1=1000 n
Rant1=2863

Template Version: 1.2

S-Parameter [ZMatch]



Parameters from circuit calculator

Receiver input divider

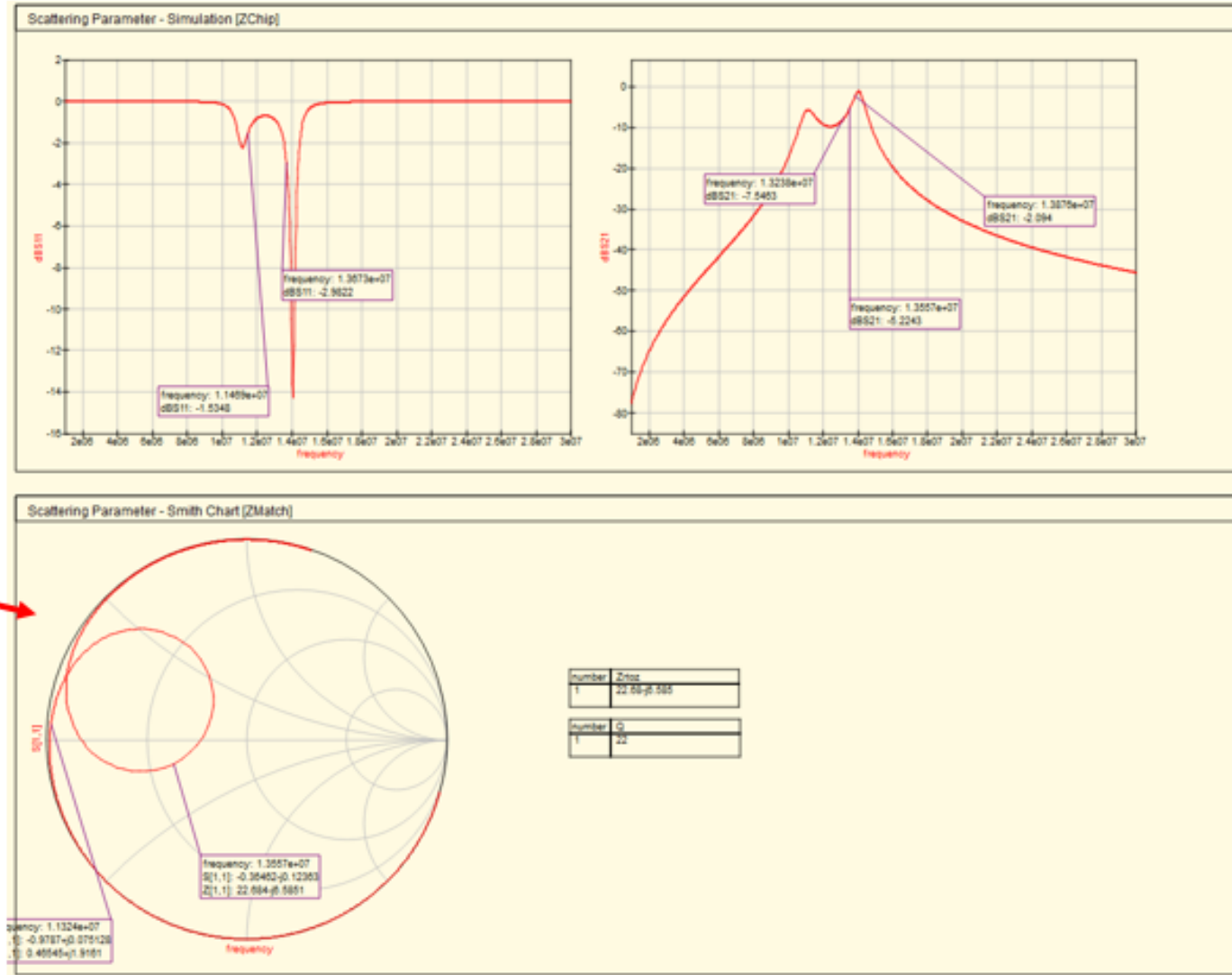
Series Cap
Parallel Cap
Q adjust

Calculated antenna parameters

Antenna Simulation

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Impedance
match info



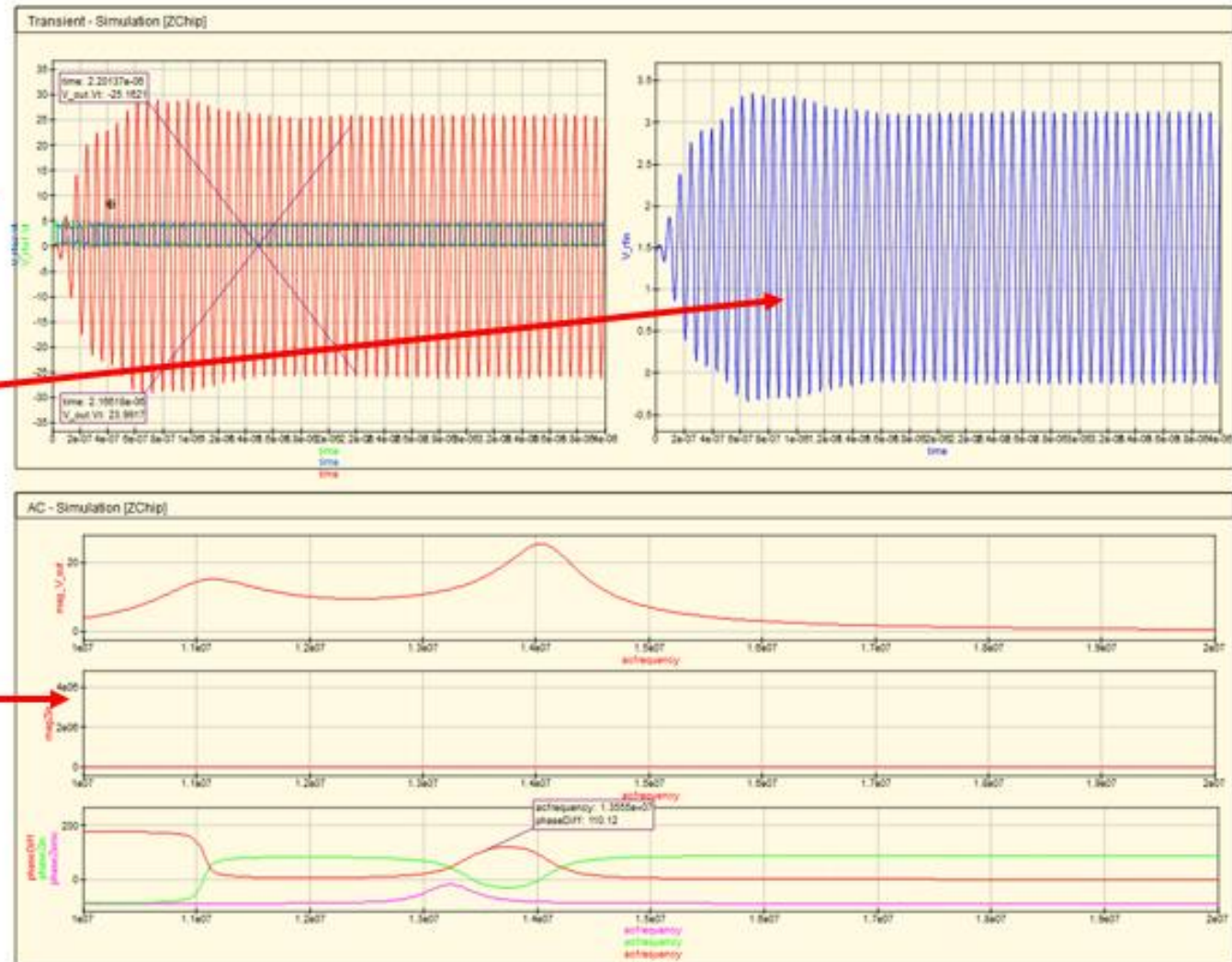
Antenna Simulation

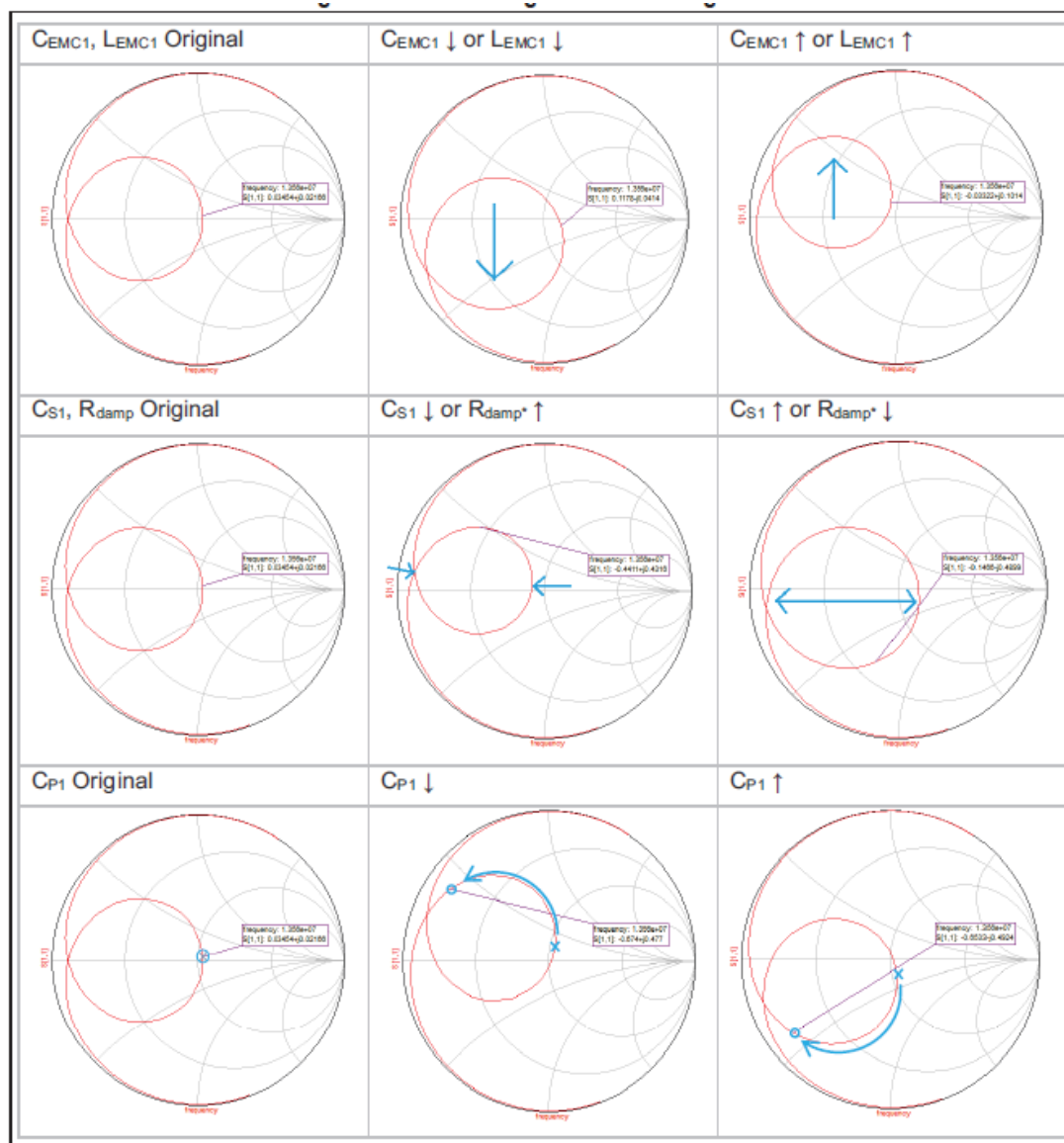
27

Antenna
voltage

Receiver input

Phase and
Amplitude info





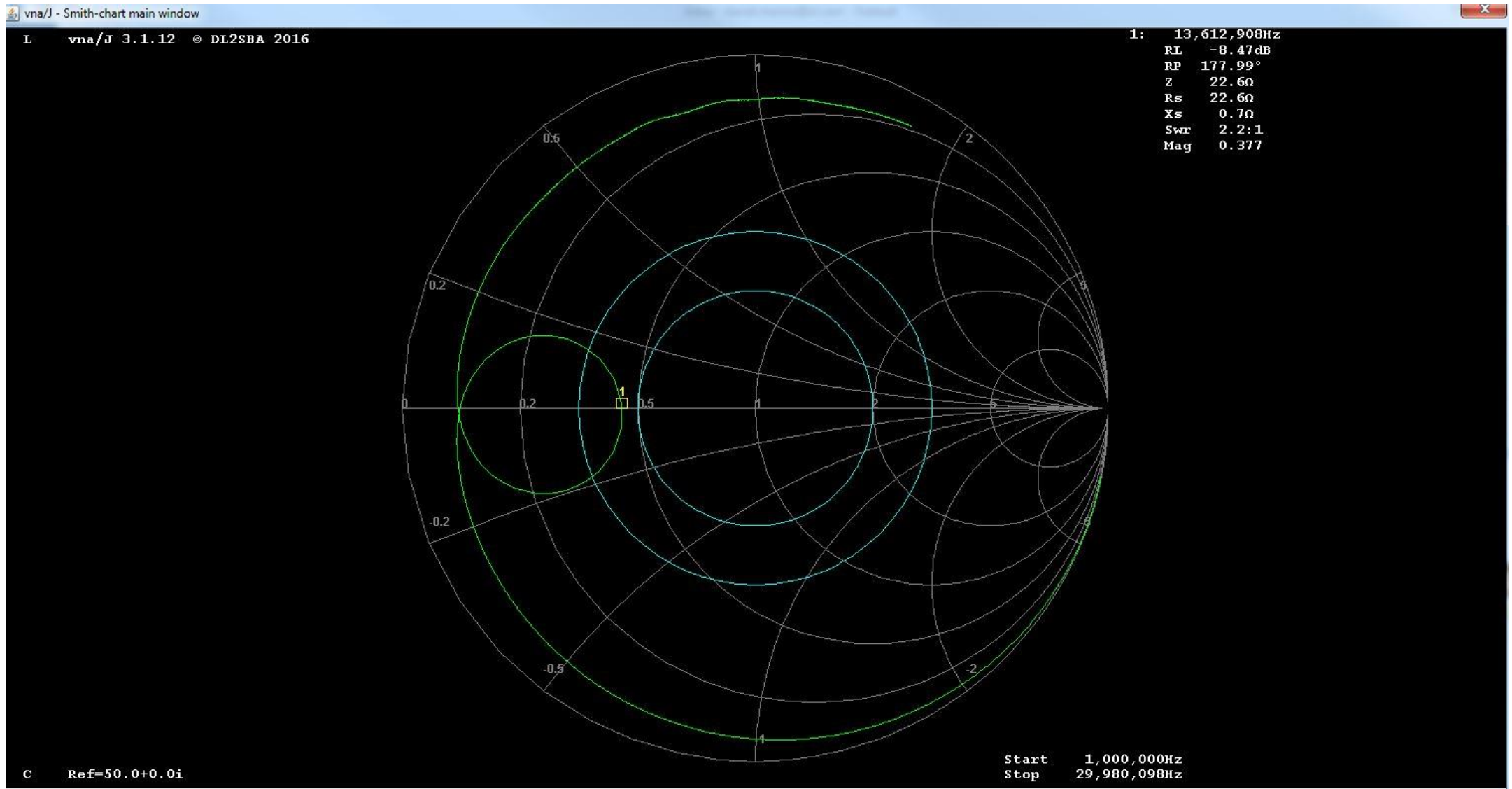
EMC
Components

- Serial Cap
- Damping Resistor

Parallel Cap

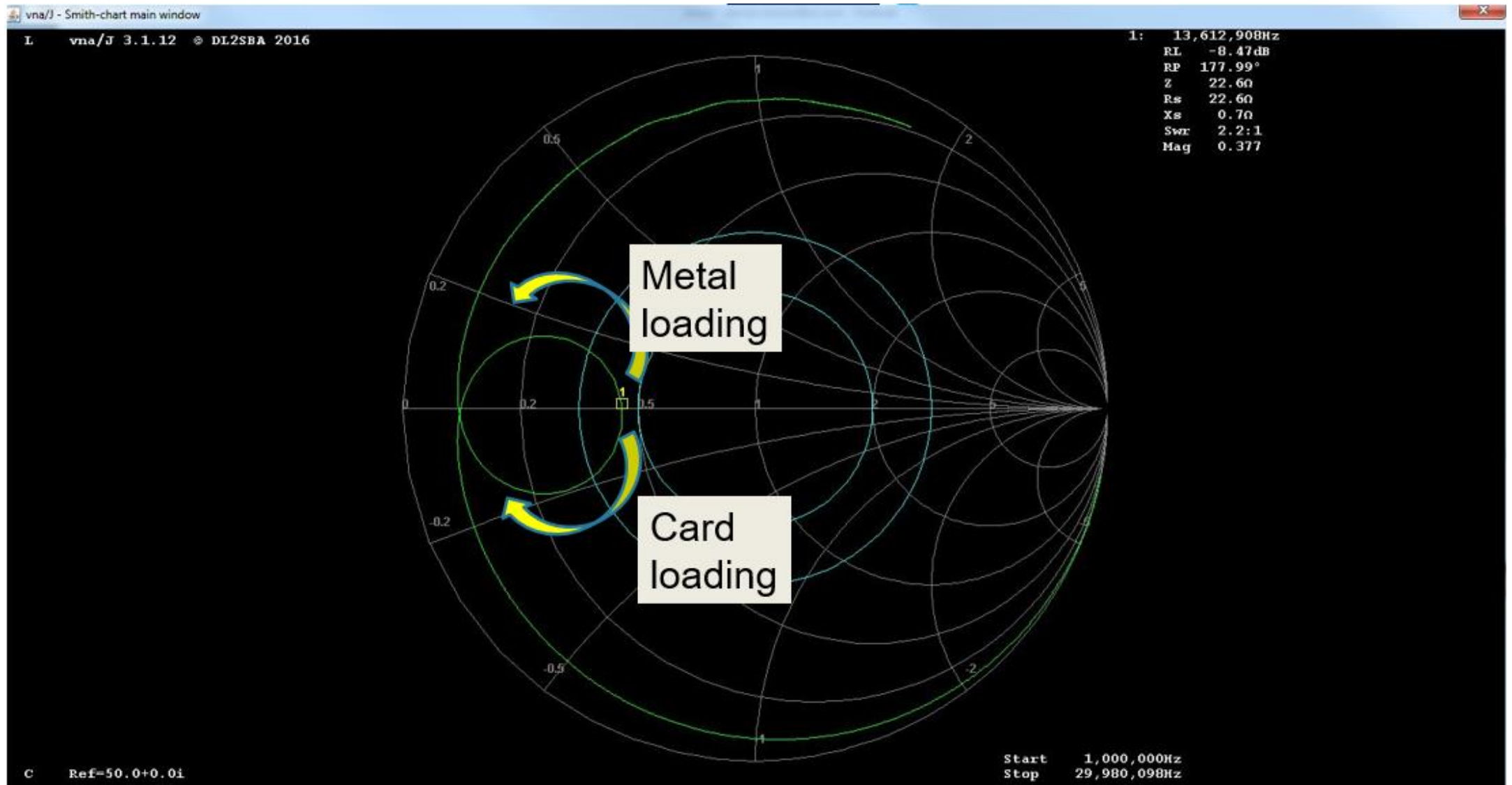
- Populate values on circuit board
- Measure match on RFO pins with VNA
- Re-adjust values as required
- Test
- Optimize read range vs current consumption

30

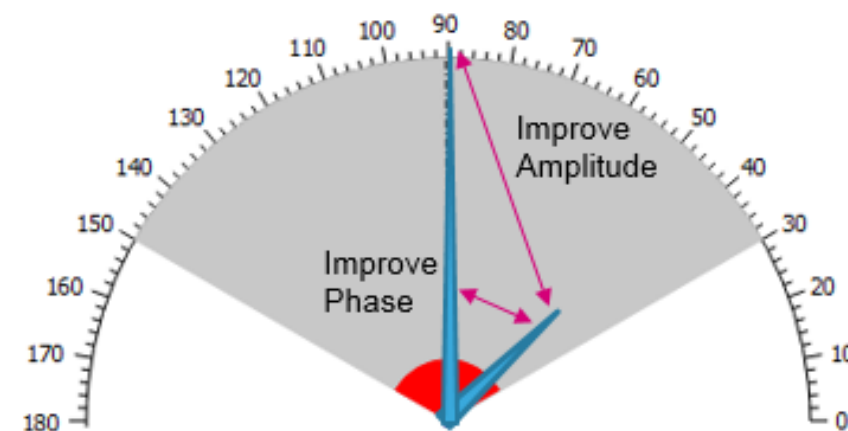


Antenna Loading

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- Automatic Antenna Tuning
 - Allows the matching circuit to be adjusted on the fly
 - Adjustment range dependent on values used
 - Larger Values > Larger range > less granularity
 - Smaller Values > Smaller range > more granularity
 - Must be compensated for in the matching circuit

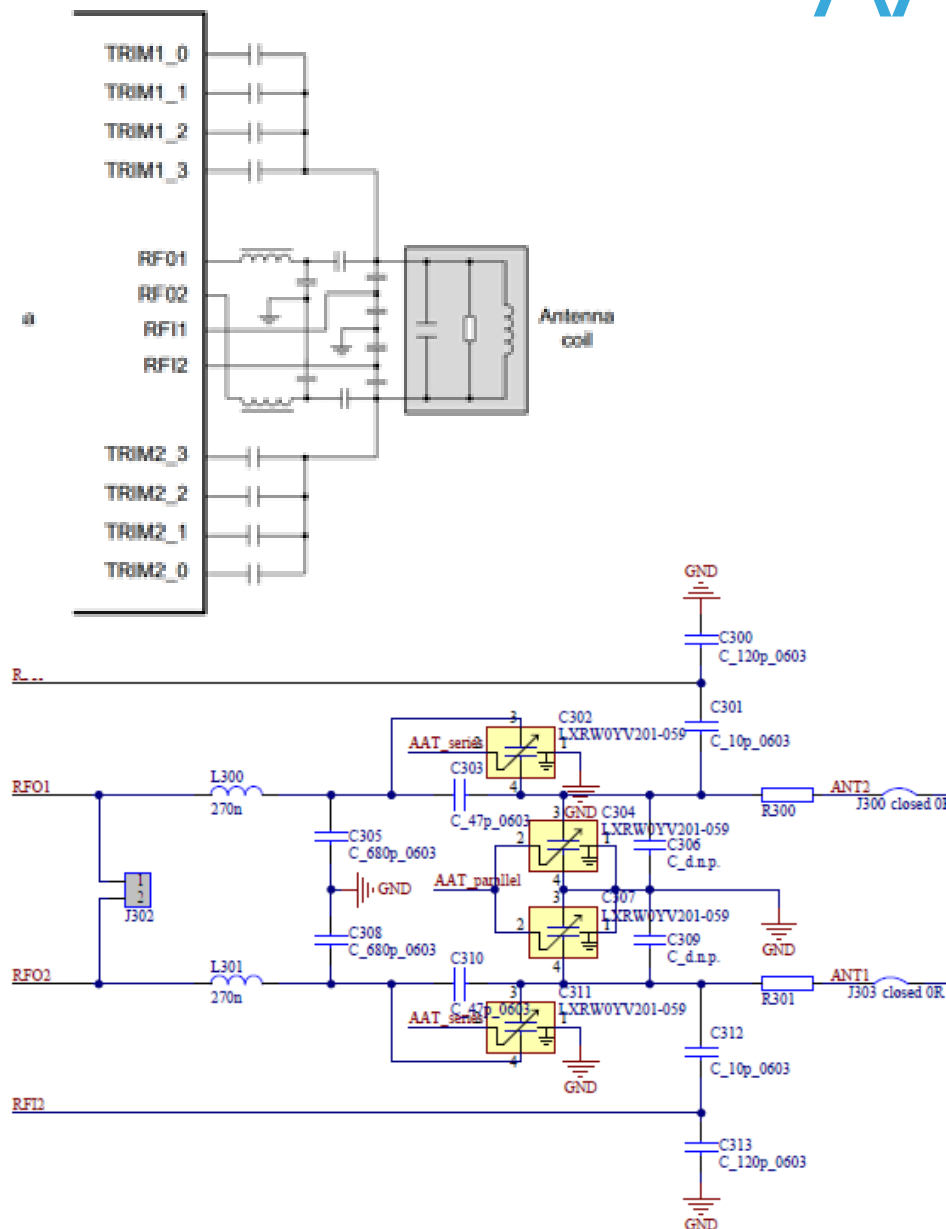


- ST25R3911B

- 8 External Binary weighted capacitors (4 per RFO)
- Switches internal to reader

- ST25R3916

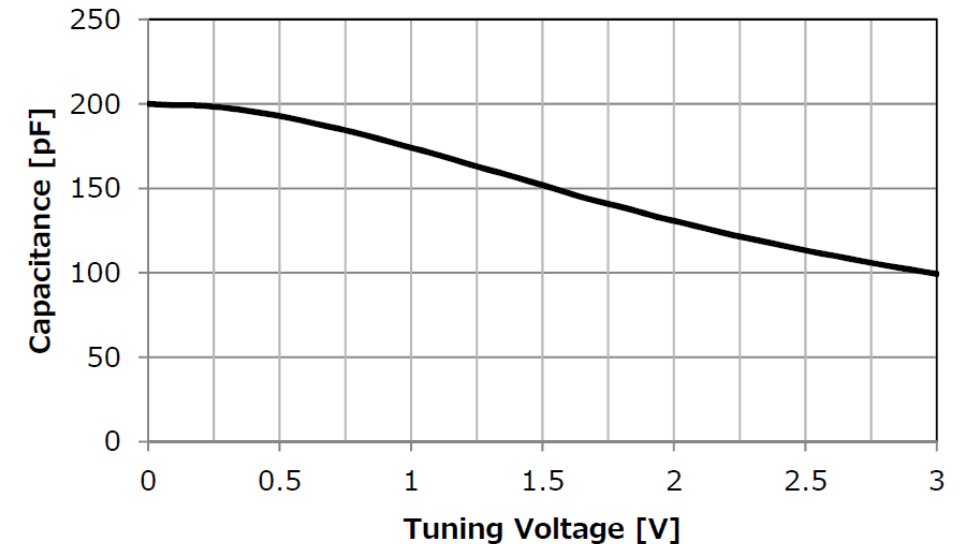
- Uses variable capacitors
- Internal DAC's use to control variable capacitors
- Can be used to control both Serial and Parallel Caps



- Match antenna as before
- Determine serial/parallel capacitors
- ST25R3916
 - Subtract $\frac{3}{4}$ Variable cap value from C_p
 - This becomes new parallel capacitor
- ST25R3911B
 - Subtract Highest trim value cap from C_p
 - This becomes new parallel capacitor



Capacitance characteristics (Typical)



- ST25R3911B

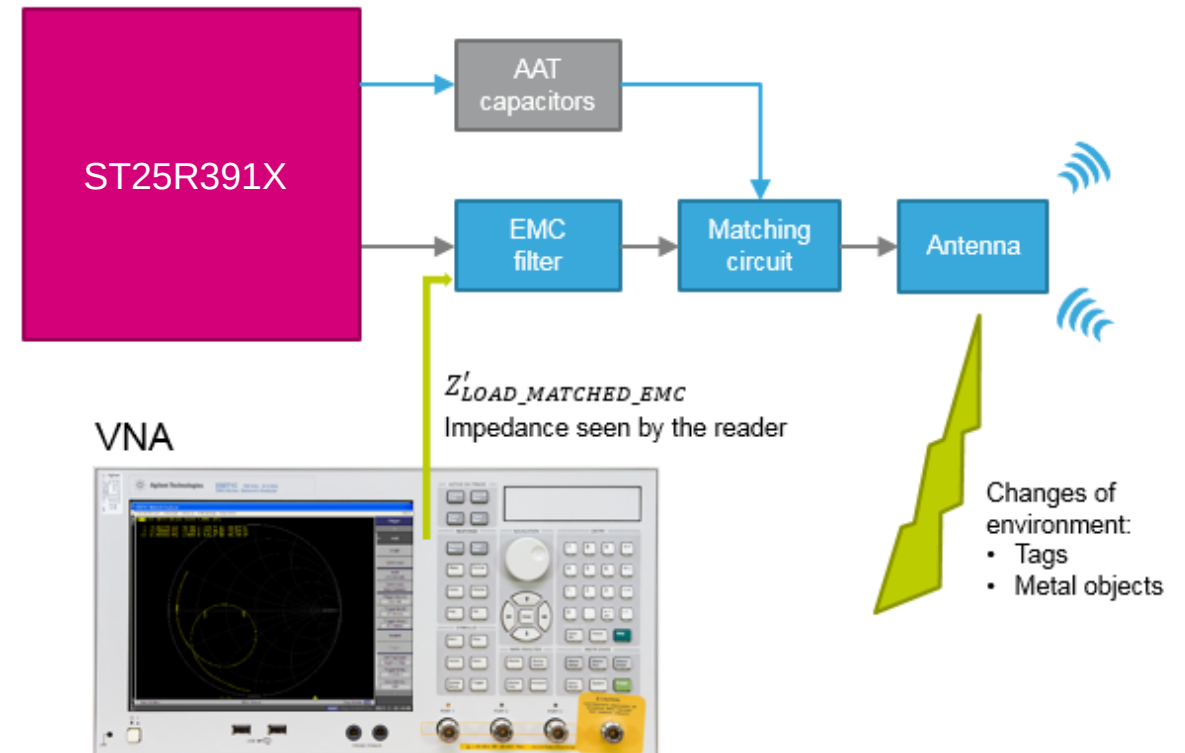
- Set reg 27 to 0xff (double check that no field is being generated)
- Adjust AAT trim to 8 (Antenna Tab in GUI)
- Match should be in center of range

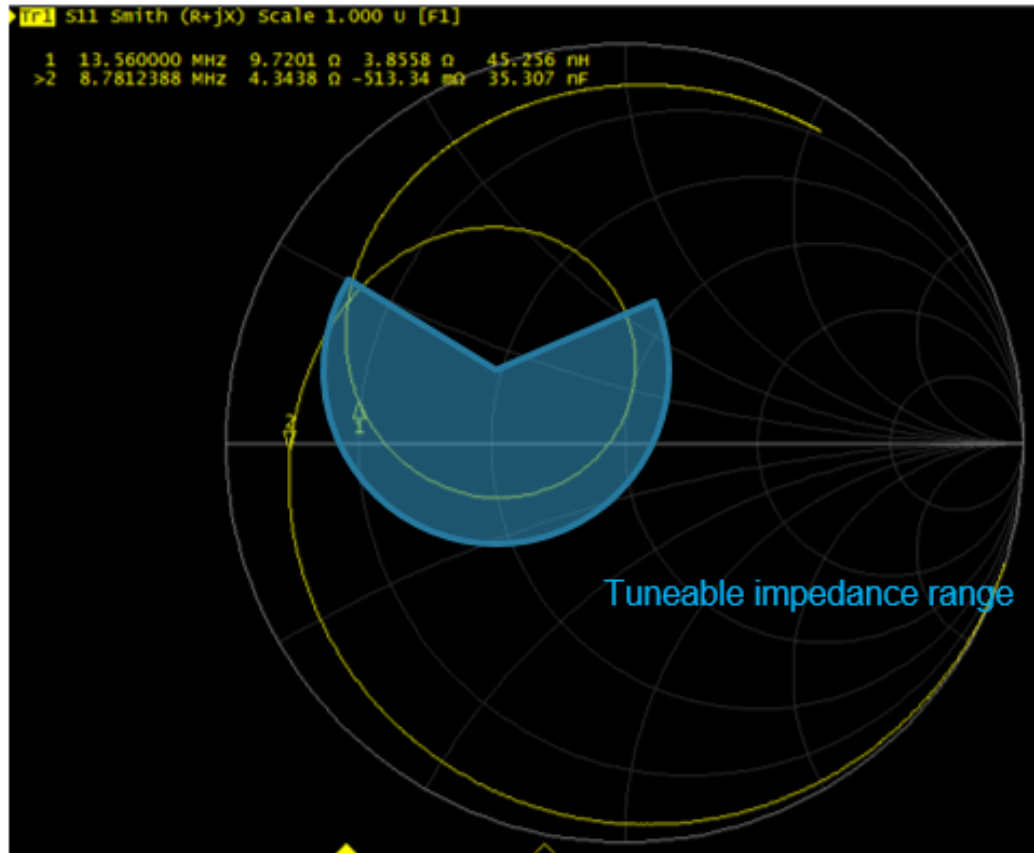
- ST25R3916

- Set reg 28 to 0x7f (double check that no field is being generated)
- Adjust AAT trim mid (Antenna Tab in GUI)
- Match should be in center of range

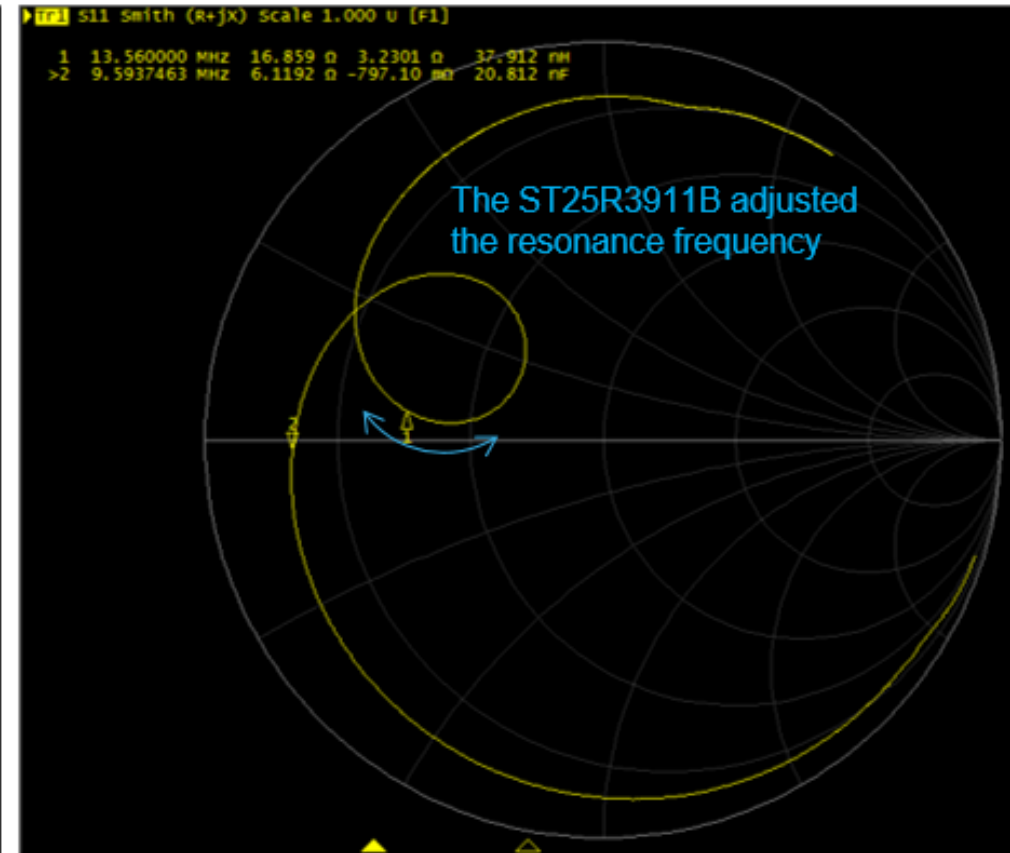
Important to turn off output drivers

- Measurement of how AAT changes the impedance of the antenna seen by the reader





ST25R3916



ST25R3911B

Simulations

ac simulation

transient simulation

S parameter simulation

AC1

TR1

SP1

Type=lin

Type=lin

Type=lin

Start=1 MHz

Start=0

Start=1 MHz

Stop=28 MHz

Stop=4 us

Stop=30 MHz

Points=1001

Points=1024

Points=1001

Noise=no

Component-Values

Equation

Eqn17

Zmatch=50

Zchip=3

Zchiphalf=1.5

AnalogSupplyVoltage=4.5

Equation

Eqn20

Lemc1=220 n

RLemc1=0

Cemc1=749 p

Equation

Eqn22

Cs1=99 p

Cp1=136 p

Rdamp=0.50

Equation

Eqn18

Cvdr1=10 p

Cvdr2=150 p

Equation

Eqn23

Cant1=7.88 p

Lant1=1114 n

Rant1=3262

AC Equations

Equation

Eqn7

magZin=mag((V_in_ac.v)/Pr13.i)

Equation

Eqn3

mag_V_out=mag((V_out_ac.v))

Equation

Eqn5

phaseZin=phase((V_in_ac.v)/Pr9.i)

phaseCapDiff=phase((V_rf_ac.v)/Pr13.i)

phaseDiff=phaseCapDiff - phaseZin+180

phaseZemc=phase((V_emc_ac.v)/Pr9.i)

phaseZout=phase((V_out_ac.v)/Pr9.i)

Antenna - Trim

Equation

Eqn10

trim3=56 p

trim2=27 p

trim1=12 p

trim0=5.6 p

Equation

Eqn9

Ctrimpara3=1.5 p

Ctrimpara2=1.5 p

Ctrimpara1=1.5 p

Ctrimpara0=1.5 p

Equation

Eqn8

Rontrim3=5e5

Rontrim2=5e5

Rontrim1=5e5

Rontrim0=5e5

on = 14; off = 5e5

on = 25; off = 5e5

on = 50; off = 5e5

on = 100; off = 5e5

Capacitive Voltage Divider

Equation

Eqn2

V_rf_in=V_rf.Vt + 1.5

Impedance Calculation

Equation

Eqn1

Zrtot=yvalue(rtot(S[1,1],P1,Z),13500000)

S-Parameter Equations

Equation

Eqn4

dBs11=dB(S[3,3])

dBs21=dB(S[4,3])

Equation

Eqn24

myphase=phaseDiff

mymag=mag((V_rf_ac.v))

Equation

Eqn16

Q=xvalue(dBS21,max(dBS21))/(abs(xvalue(dBS21,(max(dBS21)-3))-(xvalue(dBS21,max(dBS21)))))*2

Antenna - Trim

Equation

Eqn10

trim3=56 p

trim2=27 p

trim1=12 p

trim0=5.6 p

Equation

Eqn9

Ctrimpara3=1.5 p

Ctrimpara2=1.5 p

Ctrimpara1=1.5 p

Ctrimpara0=1.5 p

Equation

Eqn8

Rontrim3=5e5

Rontrim2=5e5

Rontrim1=5e5

Rontrim0=5e5

on = 14; off = 5e5

on = 25; off = 5e5

on = 50; off = 5e5

on = 100; off = 5e5

S-Parameter [ZMatch]

Source

EMC Filter

Match

P1

Num=1

Z=Zmatch

P=27 dBm

C57

C=Cemc1

R87

R=RLemc1

L23

L=Lemc1

C8

C=C

L22

L=Lemc1

R88

R=RLemc1

C56

C=Cemc1

C9

C=C

C74

C=Cp1

C18

C=Cvdr2

Component-Values

Equation

Eqn17

Zmatch=50

Zchip=3

Zchiphalf=1.5

AnalogSupplyVoltage=4.5

Equation

Eqn20

Lemc1=220 n

RLemc1=0.3

Cemc1=749 p

Equation

Eqn22

Cs1=106 p

Cp1=157 p

Rdamp=0.45

Equation

Eqn18

Cvdr1=10 p

Cvdr2=150 p

Equation

Eqn23

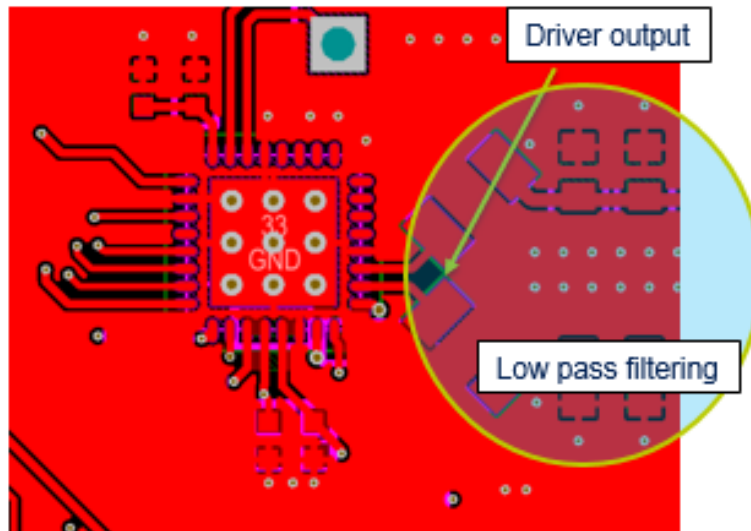
Cant1=9.02 p

Lant1=1000 n

Rant1=2863

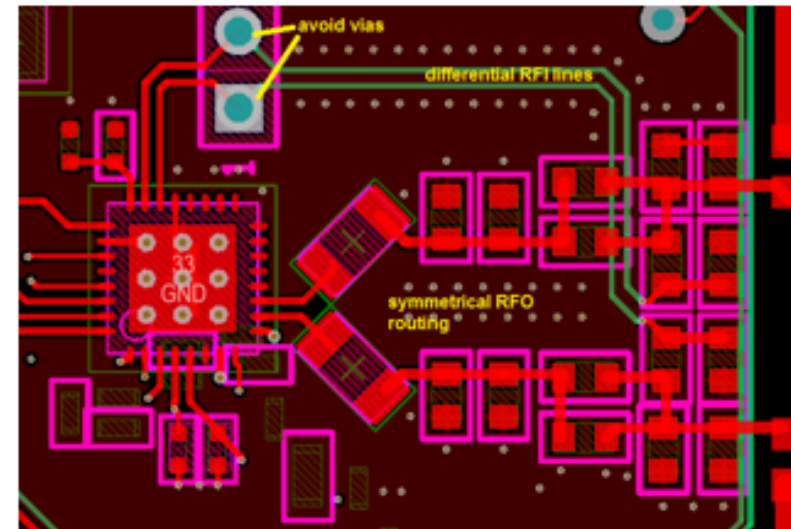
- 4 layer board if possible (Sig/GND/PWR/Sig)
- Make RFO paths symmetrical
- Keep traces short
- EMC filter as close as possible to RFO pins
- Layout extra pads for Cs and Cp for fine tuning
- Layout pads for AAT (just in case)

EMC filter



- Filter must be positioned as close as possible to the output stages

RFO & RFI routing

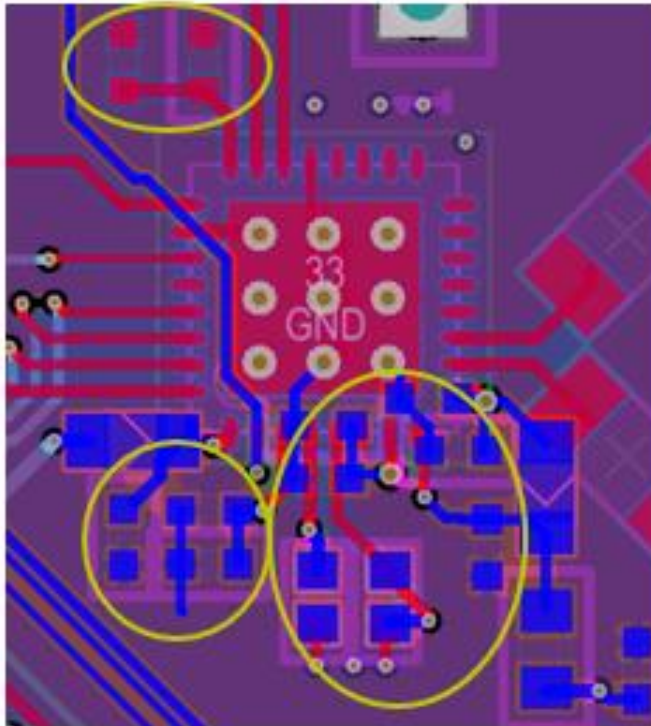


- The inductors after the RFO are placed in 90 degree direction
- The RFI lines are routed symmetrically, but in a fair distance to the RFO lines
- No long signal traces between LC filter and the remaining matching components
- The vias in the RFI lines should be avoided in a final design

Layout Suggestions

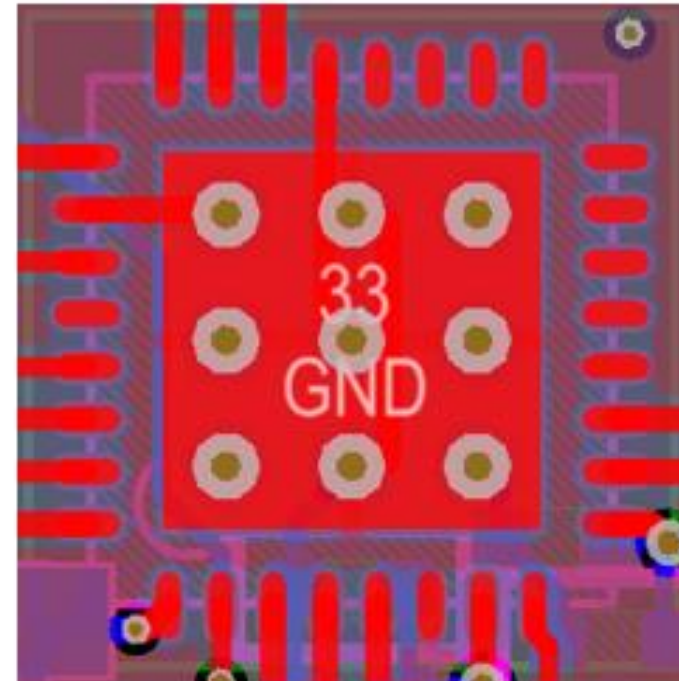
40

Decoupling



- Capacitors as close as possible to the chip
- Parallel capacitors 2.2 μF and 10 nF

Thermal pad



- Ground plane & thermal heatsink
- Multiple through vias must be used

Questions?

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