How to Design a NFC Reader Application

A Step by Step Approach

Dan Merino

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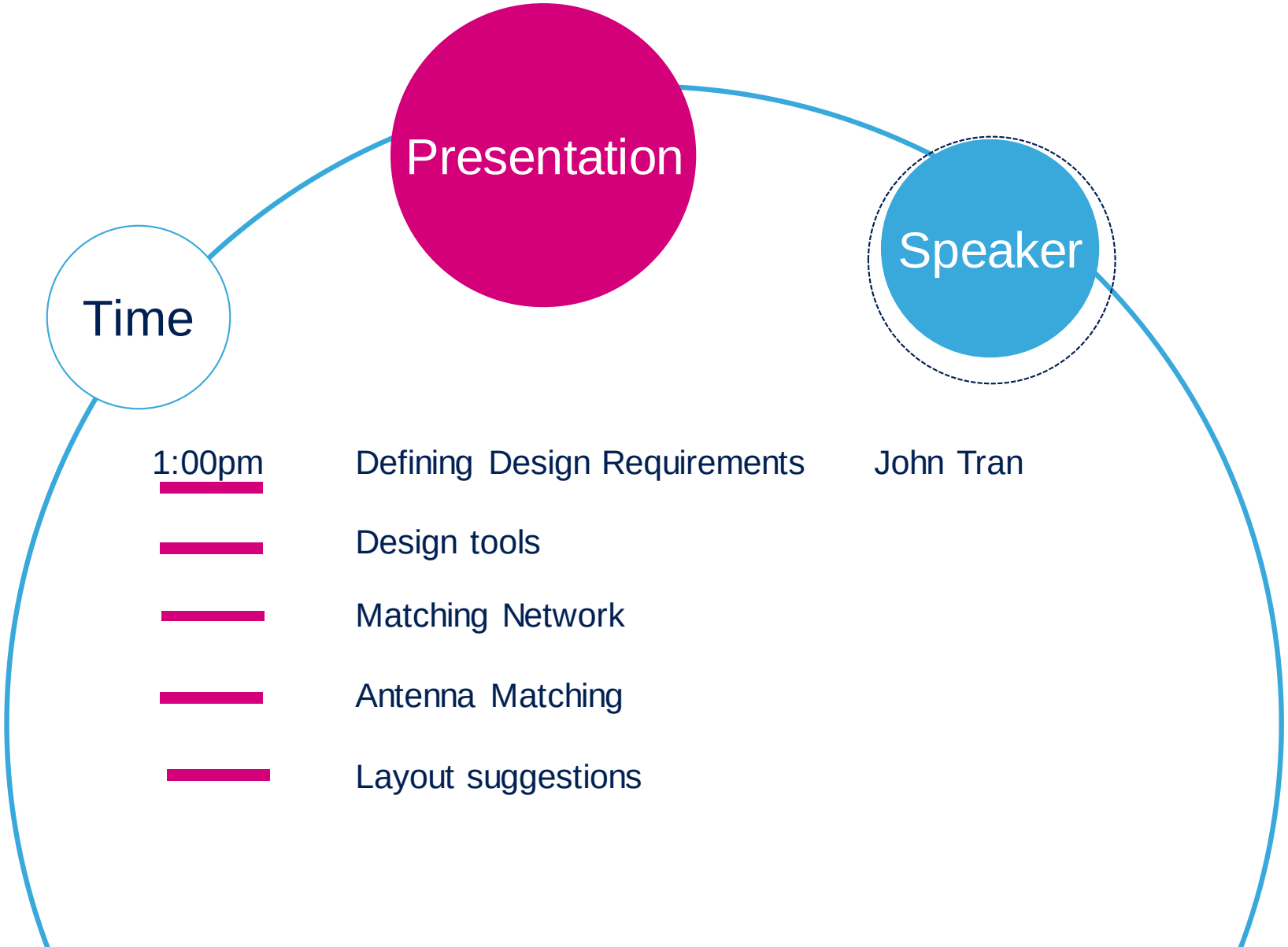
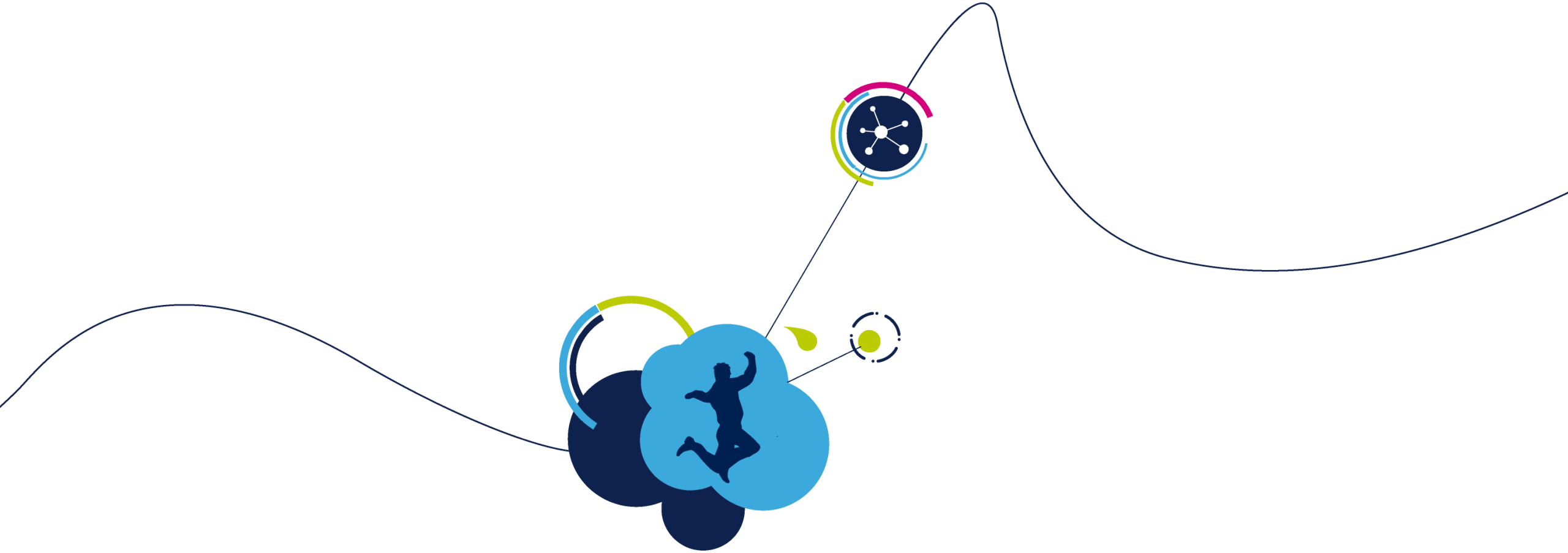
Technology Tour 2019

Dallas-Richardson, TX | March 7

Agenda





Defining Design Requirements

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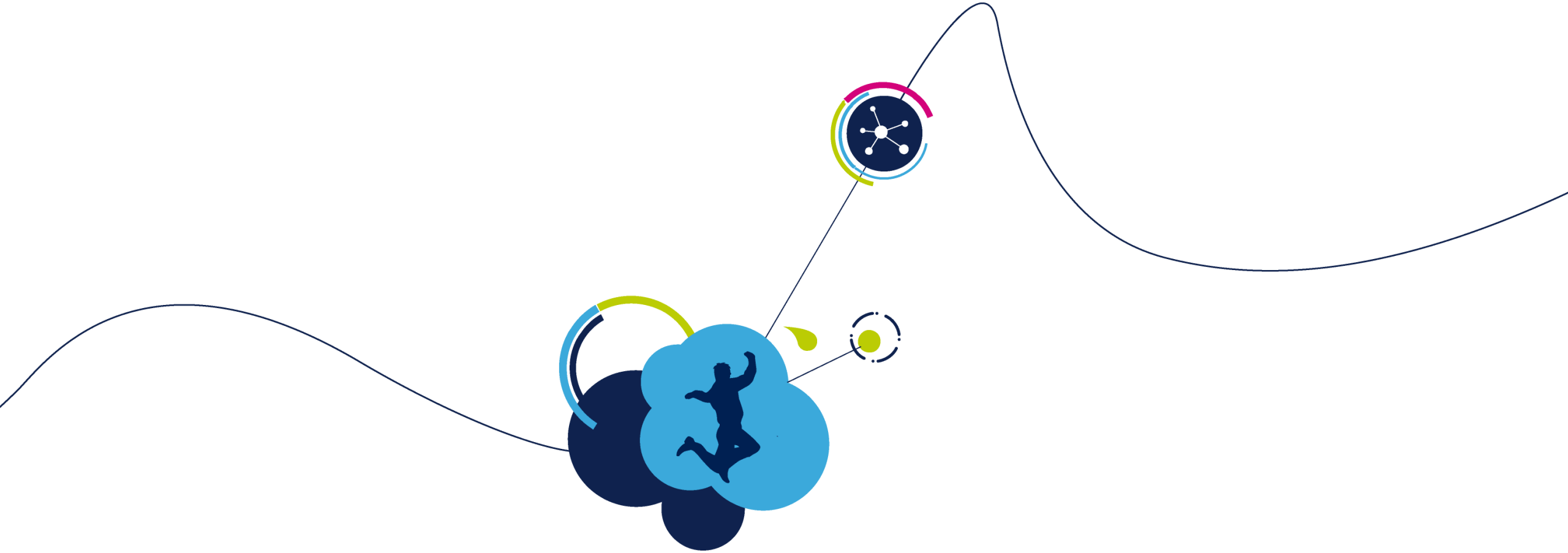
Defining Design Requirements

- End Product
  - Payment
  - General Purpose
- Communication Protocol
  - ISO 14443 A/B
  - ISO 15693
  - Felica
  - AP2P.

Defining Design Requirements

- System constraints
  - Antenna Size
  - Environmental Conditions
    - Metal
    - LCD screen
    - Antenna placement
- Design Trade-offs
  - Antenna size
  - Read Range
  - Current Consumption



System Block Diagram

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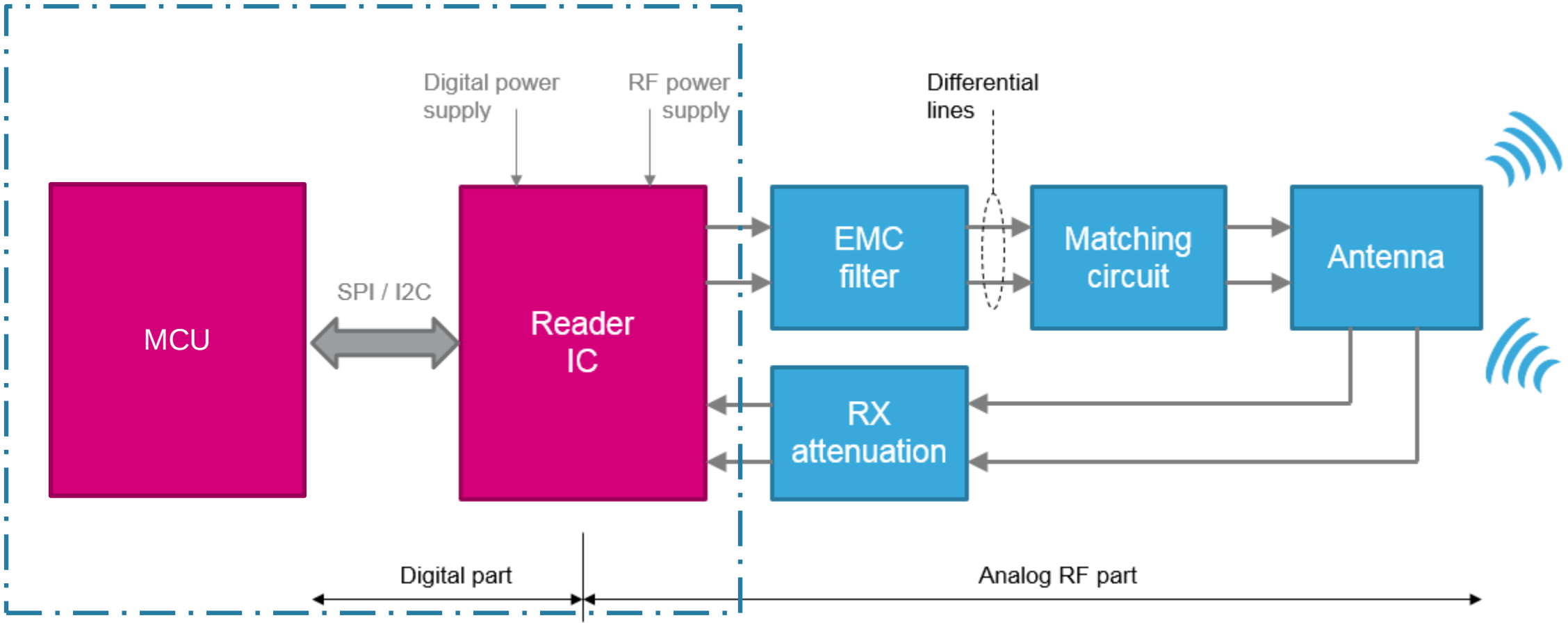
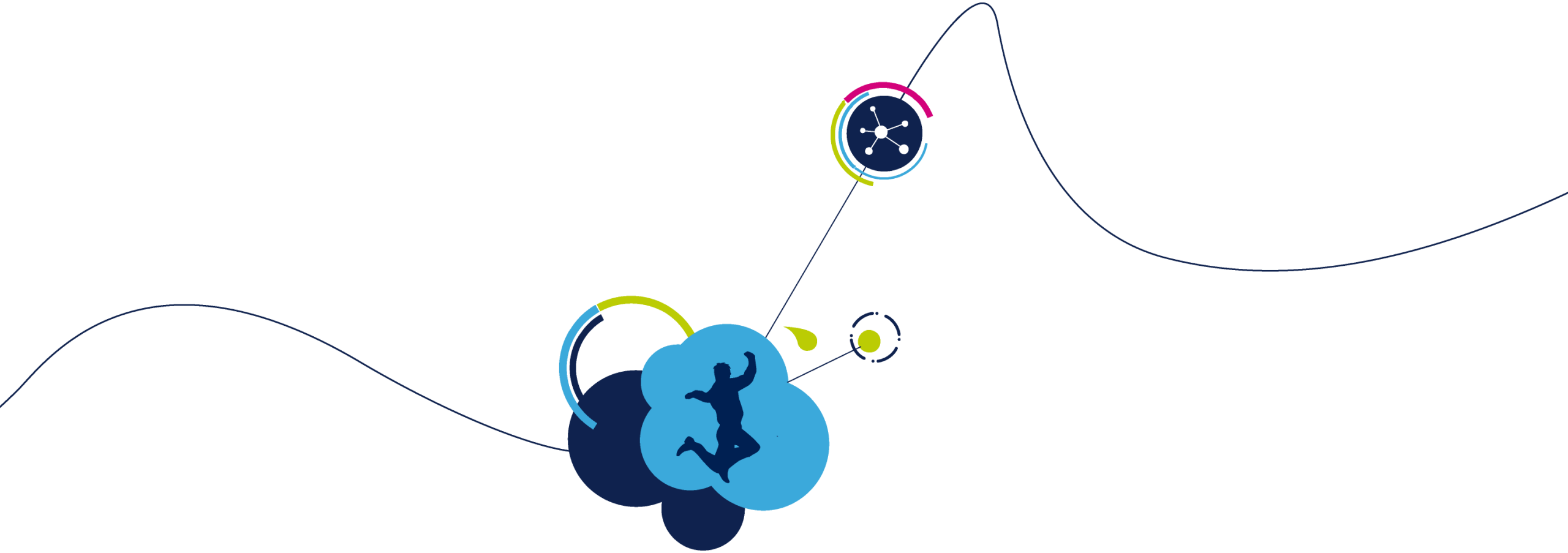
System Block Diagram





Design Tools

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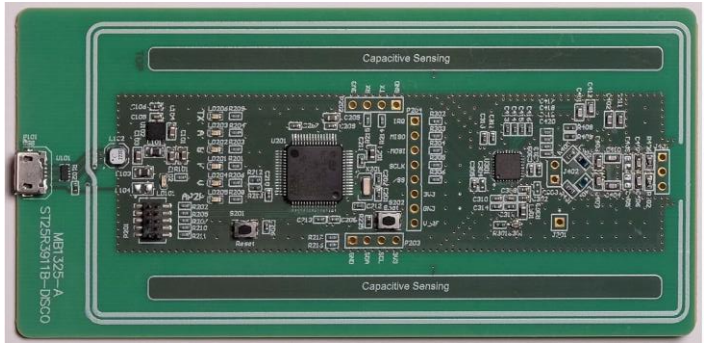
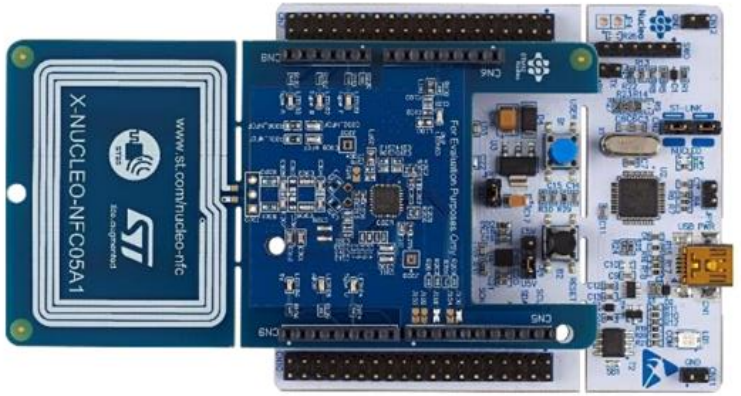
Design Tools

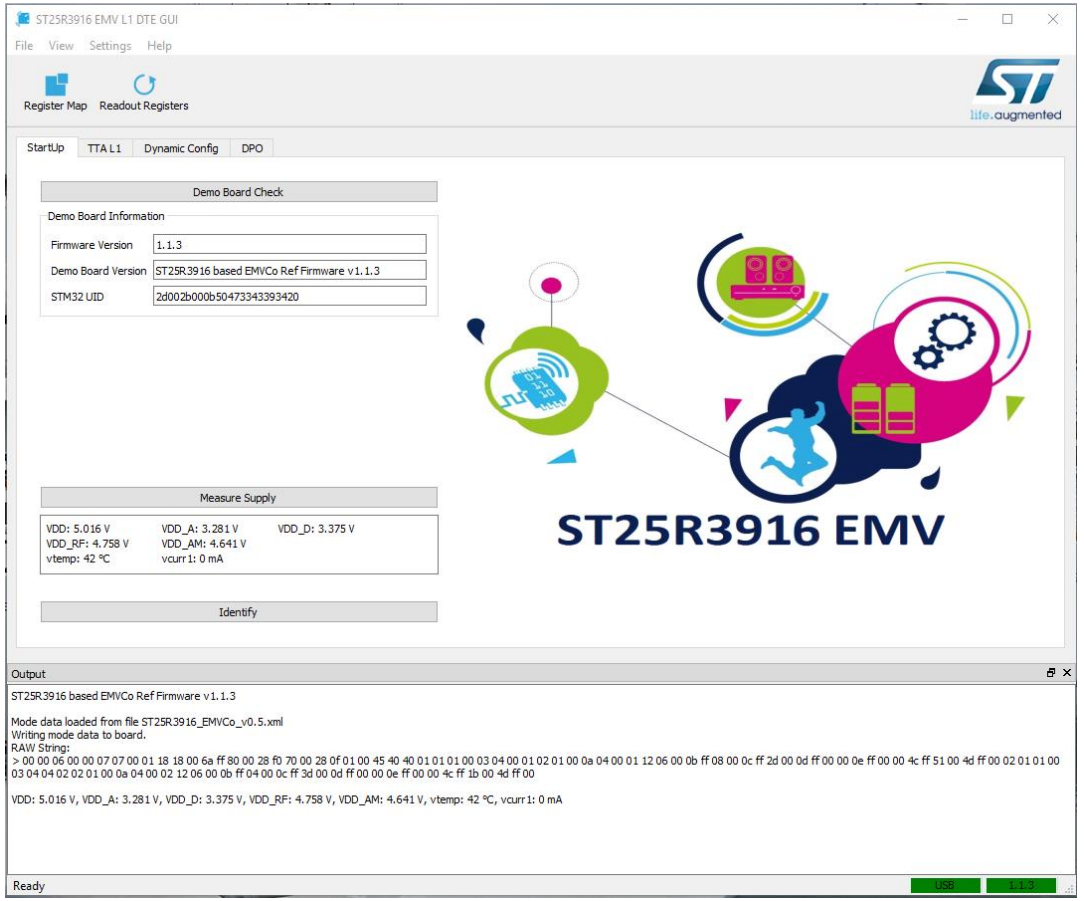
- ST25R3911B Discovery
  - Software GUI
  - Source code downloadable
  - Design files downloadable
- ST25R3911B Nucleo Shield
  - Firmware available
  - Design files downloadable
- ST25R3916 Discovery
  - Software GUI
  - Source code downloadable
  - Design files downloadable





Design Tools

- EMVCo Reference design
  - Hardware eval board
  - Software GUI
  - L1 Stack
  - Available only by Request



*ST25R3916 recommended for EMVCo 3.0 and above

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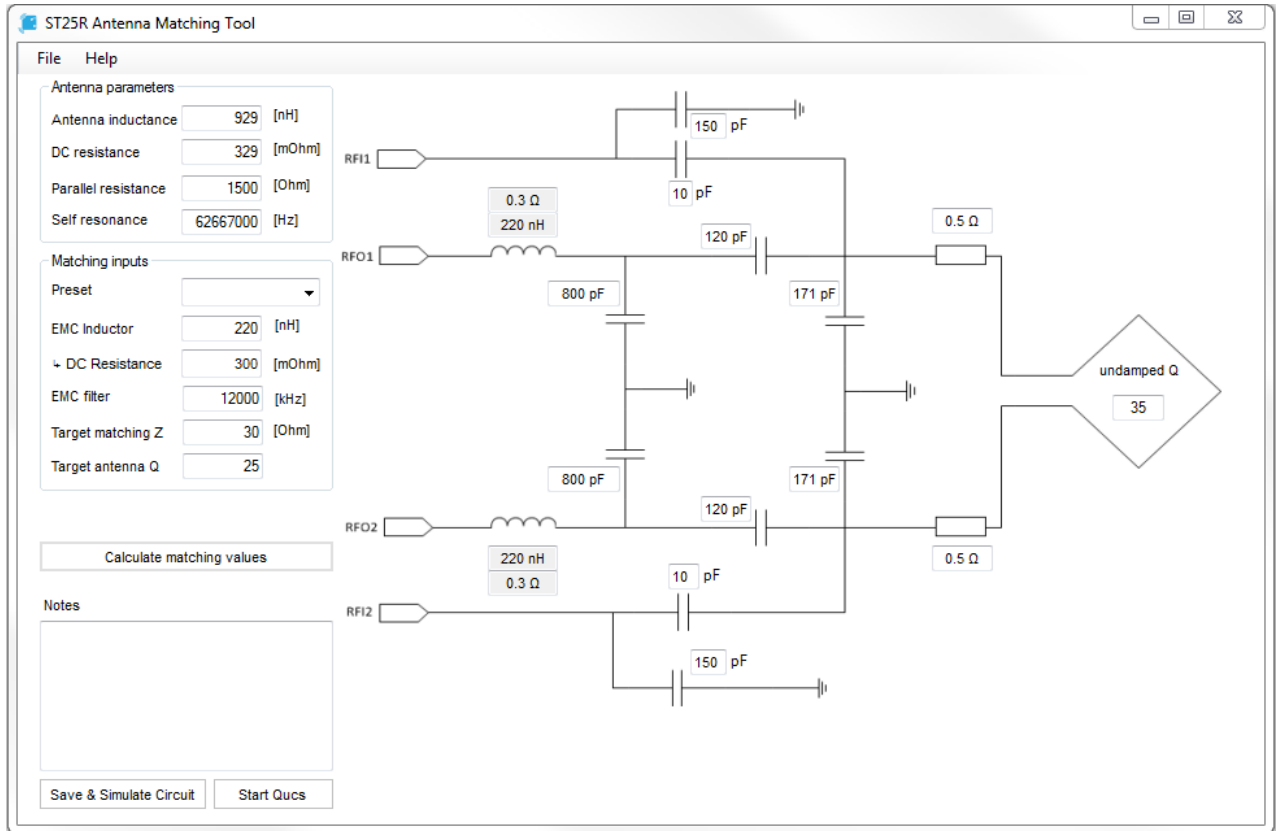
Design Tools

- Antenna Design Matching tool
  - Calculates matching components
  - Includes simulation program
  - Available on ST25R3911B landing page



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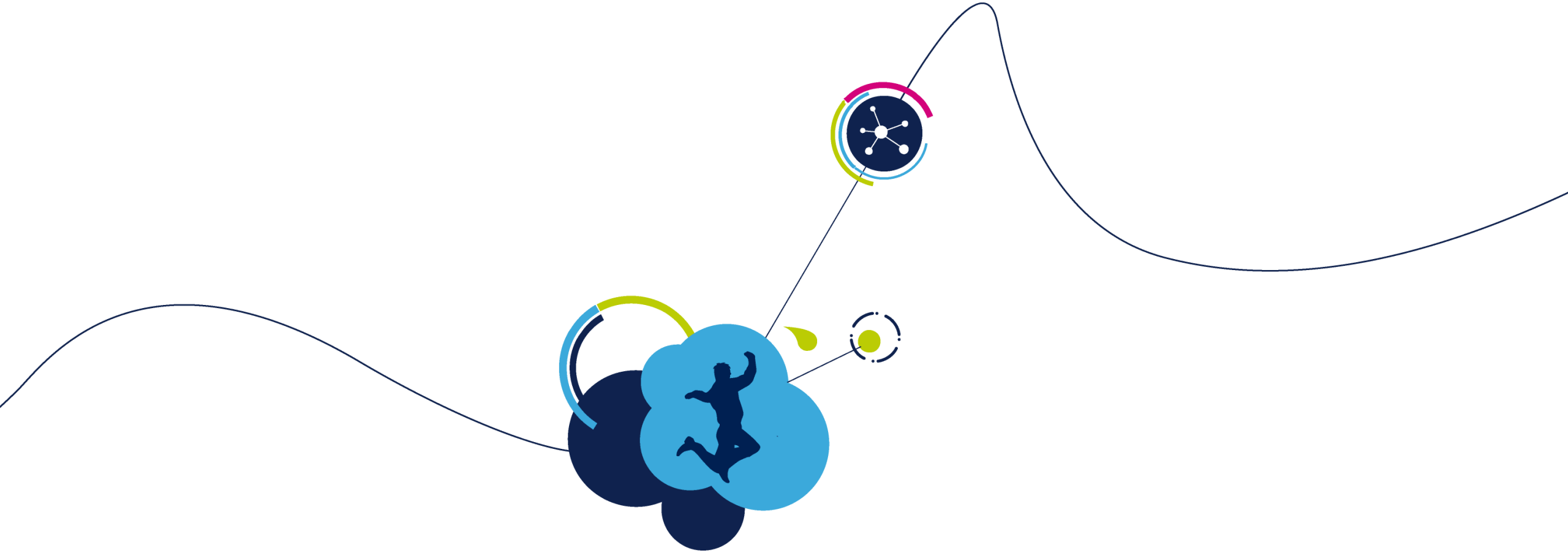

Matching network

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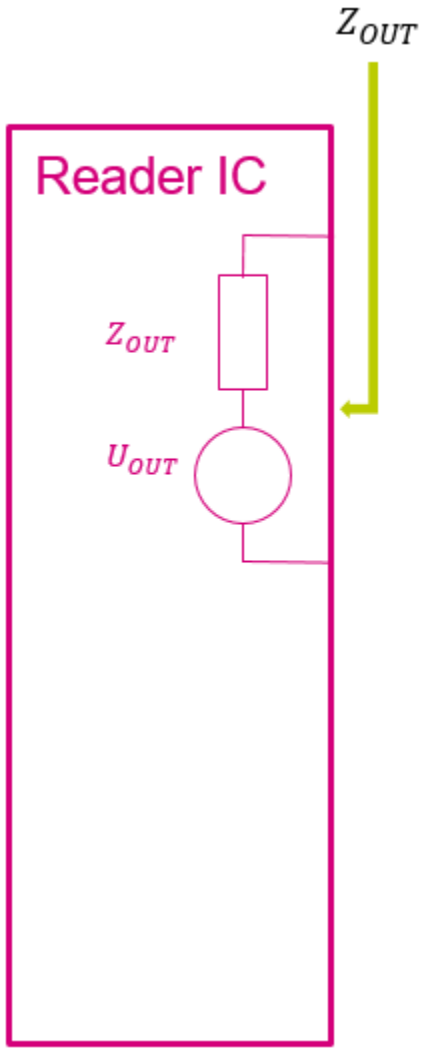
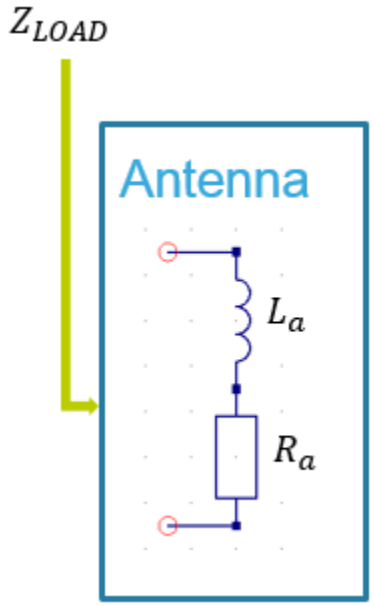
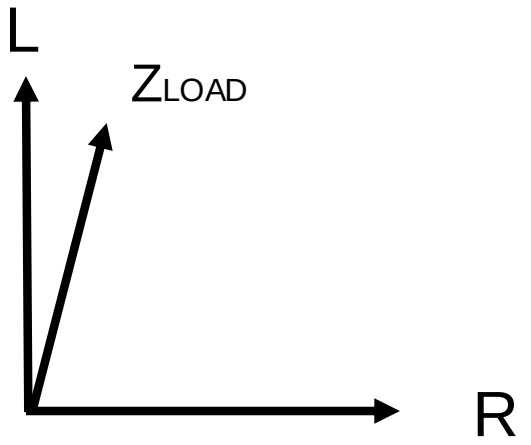
Matching Circuit

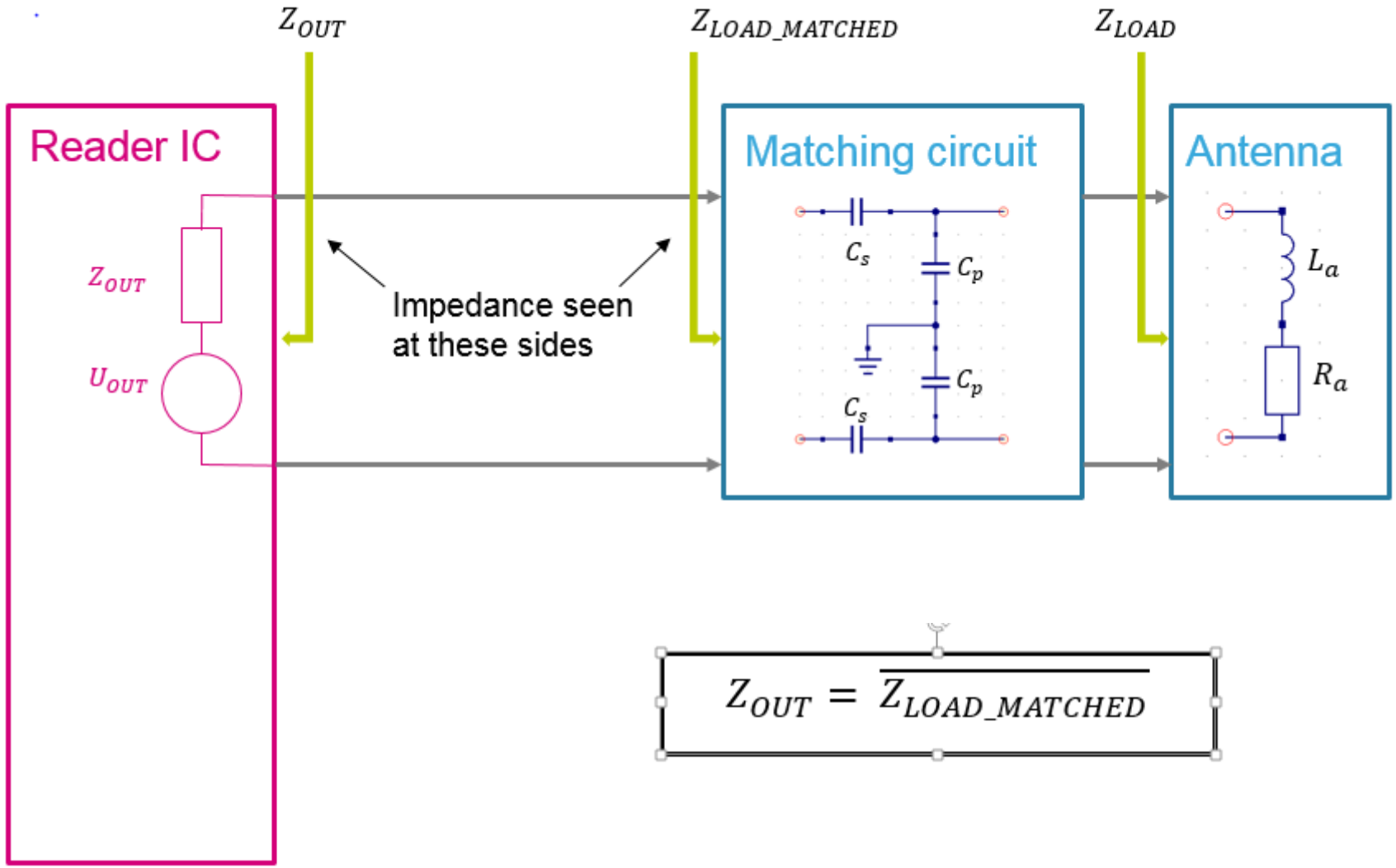


$$Z_{out} = \overline{Z_{LOAD}}$$



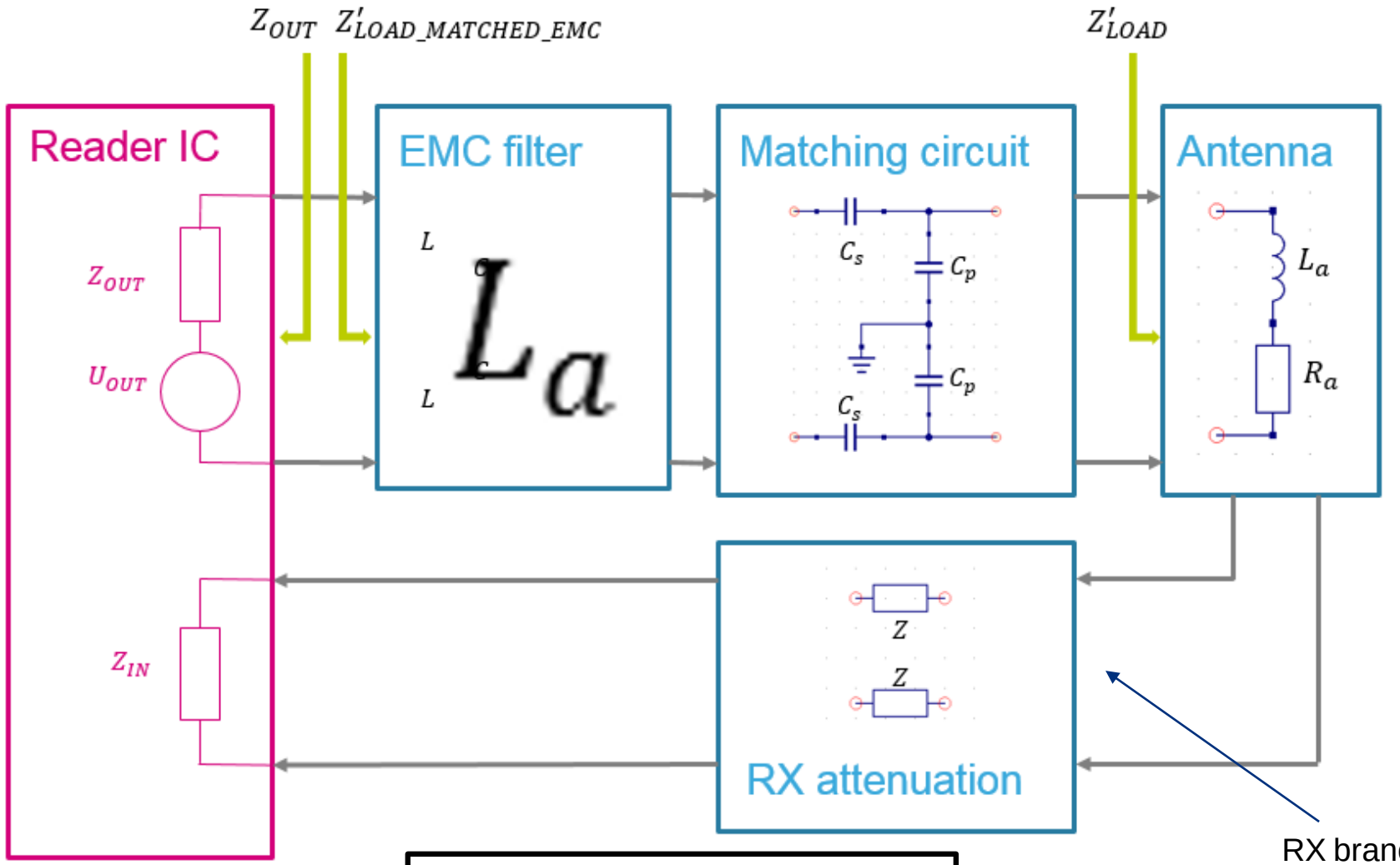


Matching Circuit



$$Z_{OUT} = \overline{Z_{LOAD\_MATCHED}}$$

Matching Circuit



$$Z_{OUT} = \overline{Z'_{LOAD\_MATCHED}}$$

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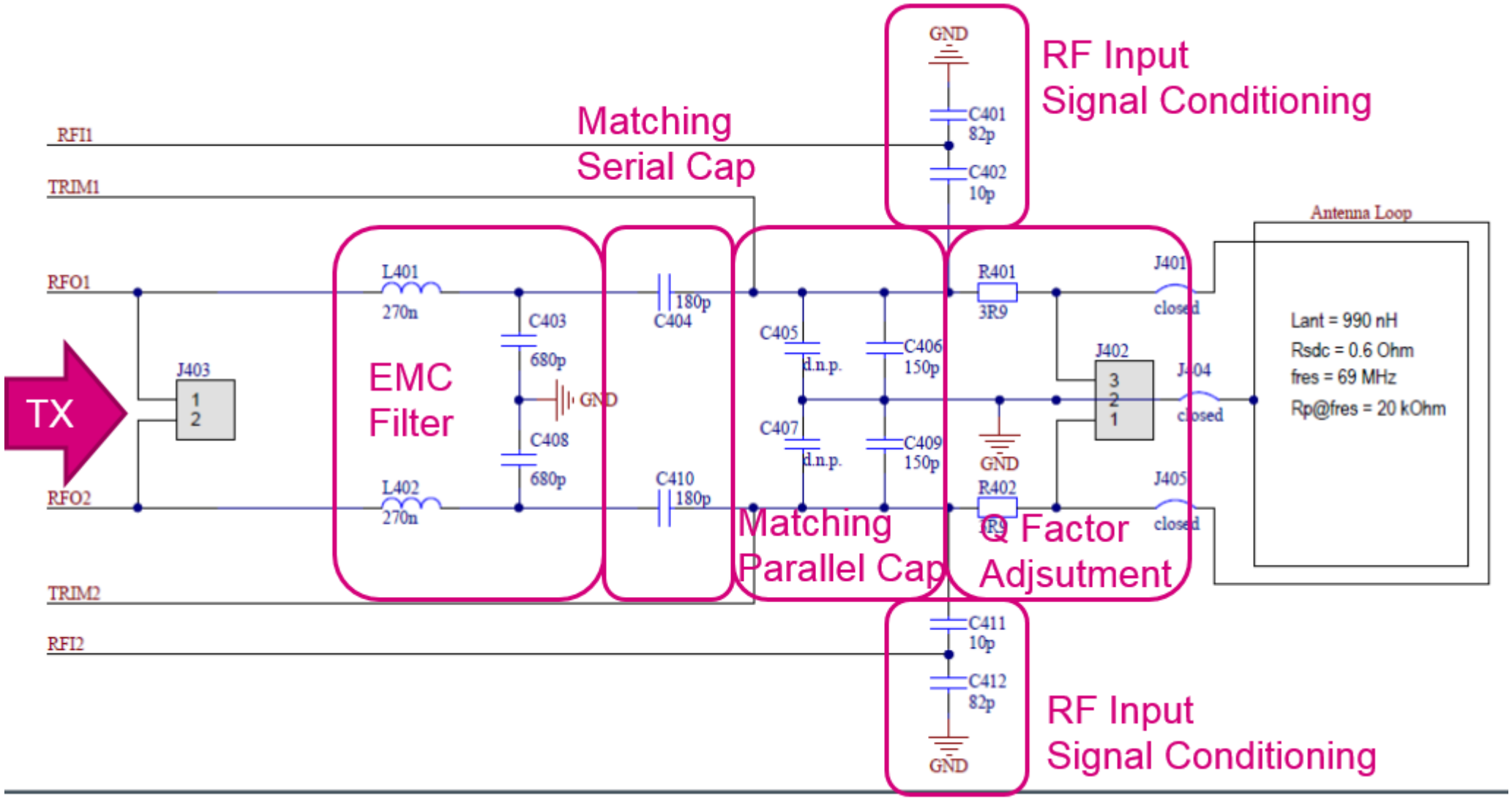
Matching Circuit



Matching Circuit

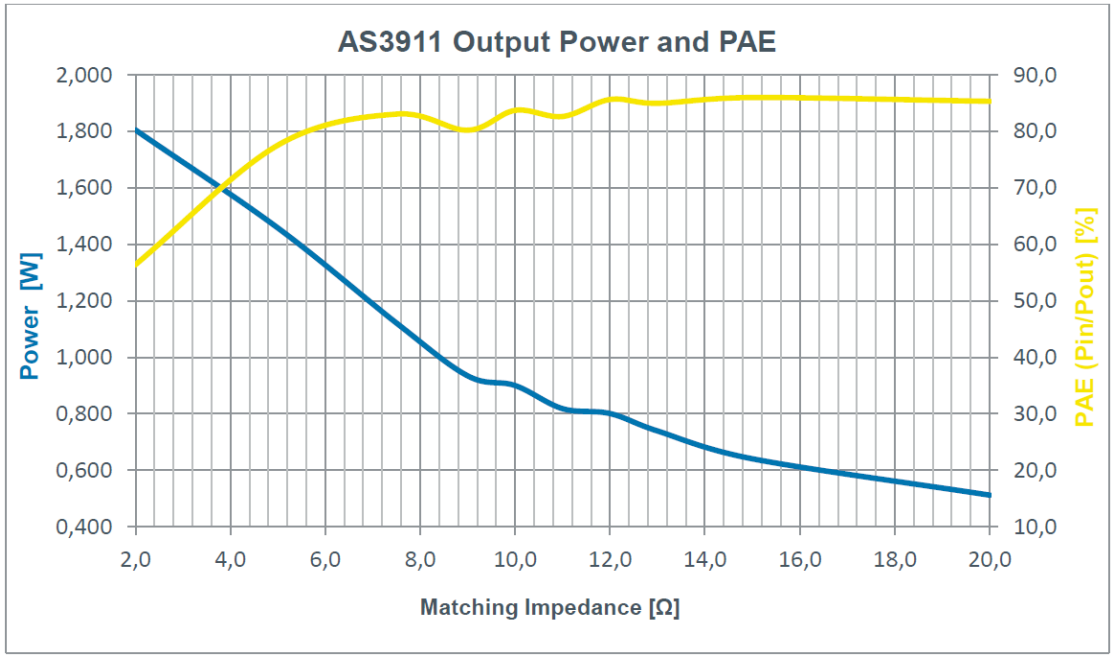
- Antenna
  - Two Turn
  - Typical Inductance 200nH – 2uH
- EMC Filter
  - Reduces harmonics of the RFO output stage
  - Target Cutoff Frequency about 13.56Mhz
- Matching Serial Cap
  - Impedance match from EMC filter to antenna resonator circuit
  - Cuts DC path from RFO1 to RFO2

Matching Circuit

- Q Factor adjustment
  - Sets System Q (antenna Q should always be higher than System Q)
  - Higher Q > More Field Strength > Lower Datarate
  - Lower Q > Faster rise/fall times > Higher Datarate
  - Target Values
    - Up to 106kbps – 25
    - Up to 848kbps – 12-16
    - Up to 3.4Mbps - 8
- RFI Input Conditioning
  - Reduces Antenna Voltage to < 3.0Vpp for RFI input

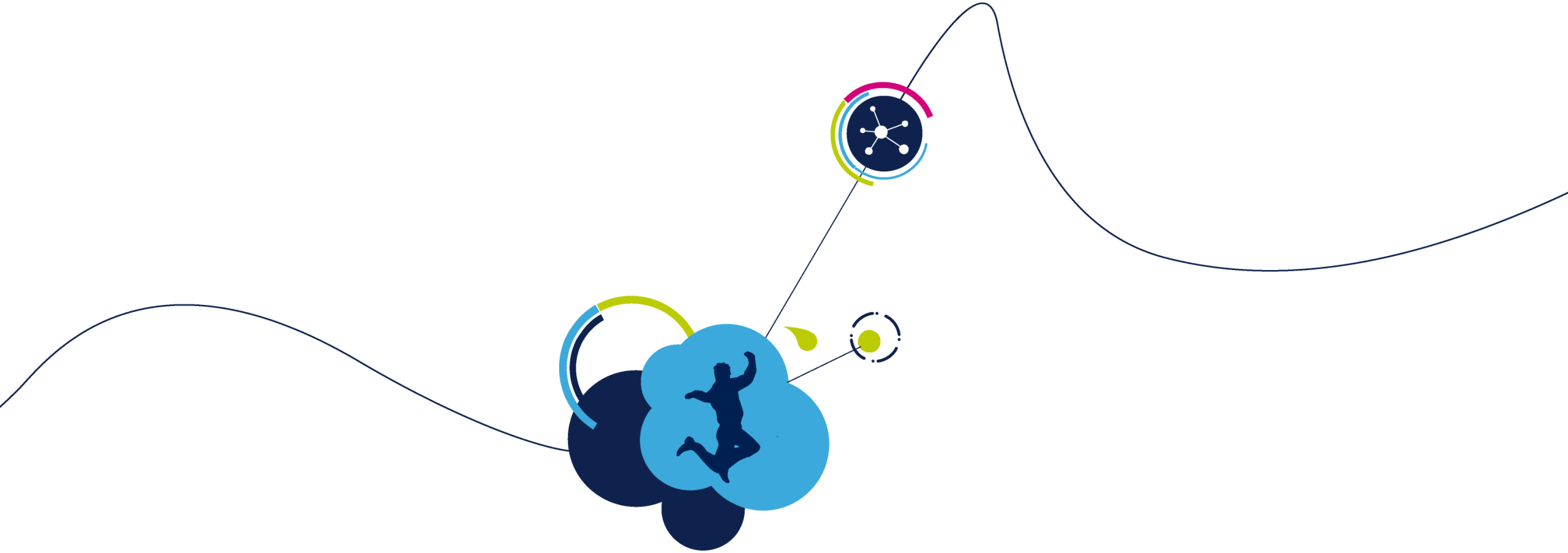
Matching Circuit

- Target Matching impedance
  - Higher > less field strength > less power consumption > higher efficiency
  - Lower > higher field strength > higher power consumption > less efficiency
  - Range 8 – 120 ohms
  - Typically between 10 – 30 ohms



Antenna Parameters

Parameter	Action	Effect on parameter	Q factor
Q factor	Increase trace width	-	Increases
	Increase gap width		
Inductance	Larger antenna	Increases	Decreases
	Decrease trace width		
	Decrease gap width		
Series DC resistance	Larger antenna	Increases	Decreases
	Decrease trace width		
	Decrease gap width		
Parallel resistance	Decrease trace width	Increases	Increases
	Increase gap width		
Resonance frequency	Smaller antenna	Increases	Increases
	increase gap width		



Antenna Matching

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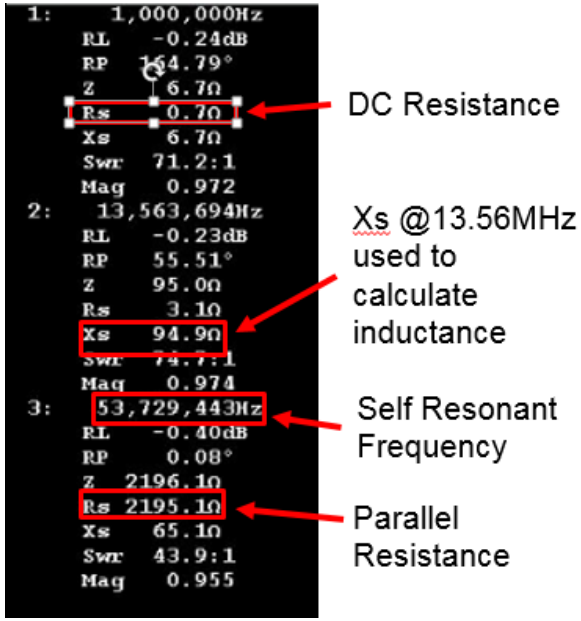
Antenna Measurements

- Measure the following Parameters with a VNA
  - DC resistance
  - Inductance
  - Self resonance frequency
  - Parallel R @ F_{SR}



DC Resistance

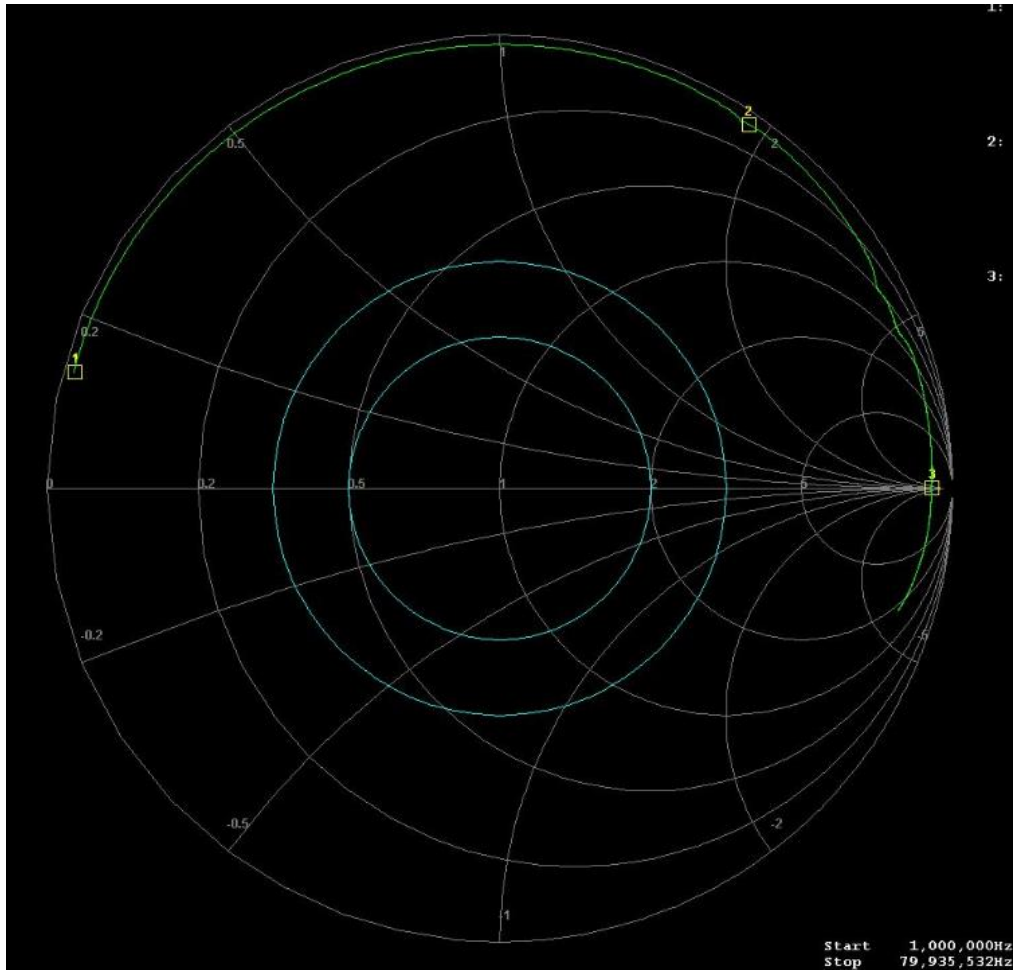
Xs @13.56MHz used to calculate inductance

Self Resonant Frequency

Parallel Resistance

$$Xs = j\omega L$$

$$L = \frac{Xs}{j\omega}$$



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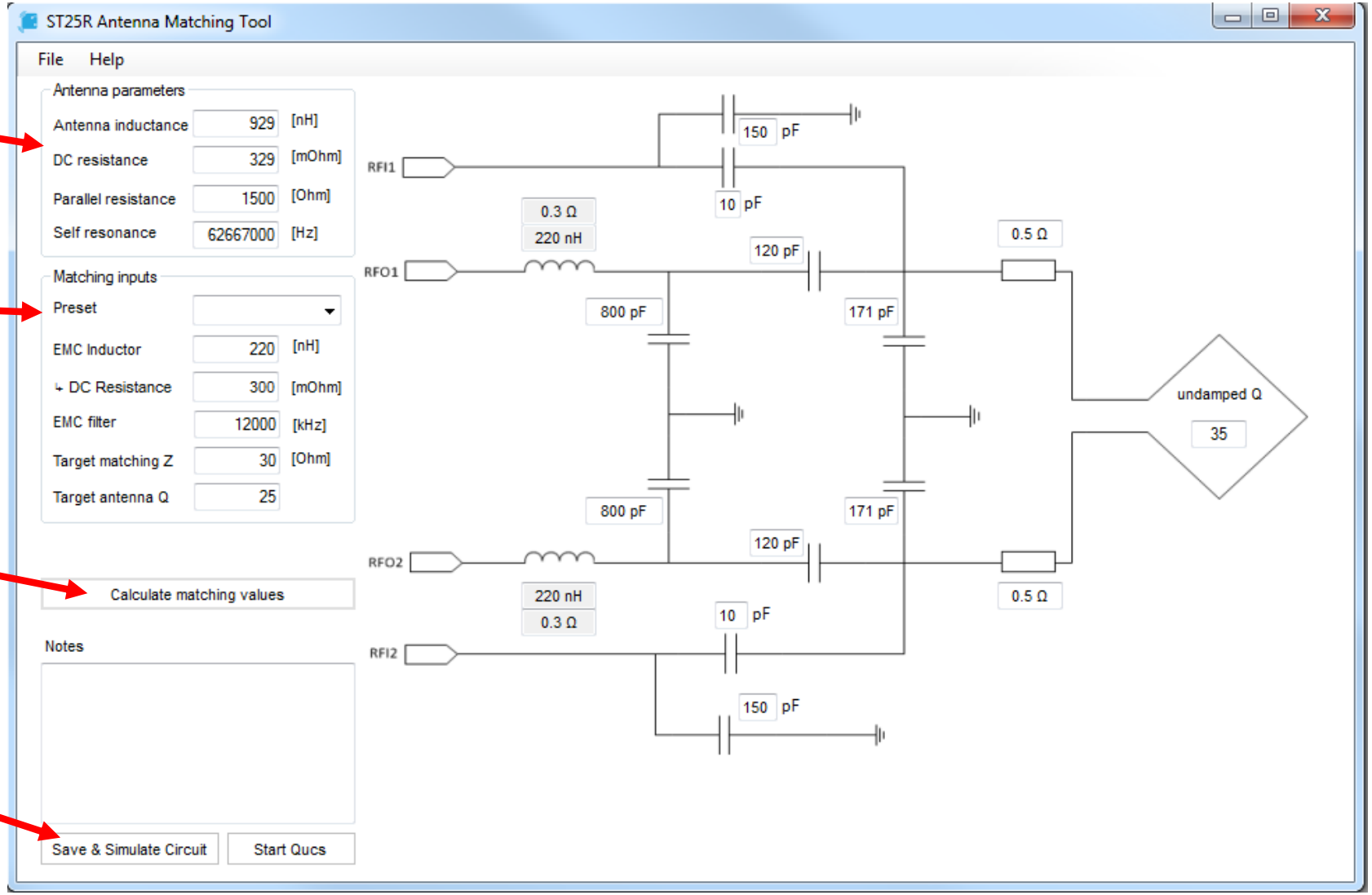
Antenna Measurements

Input antenna parameters

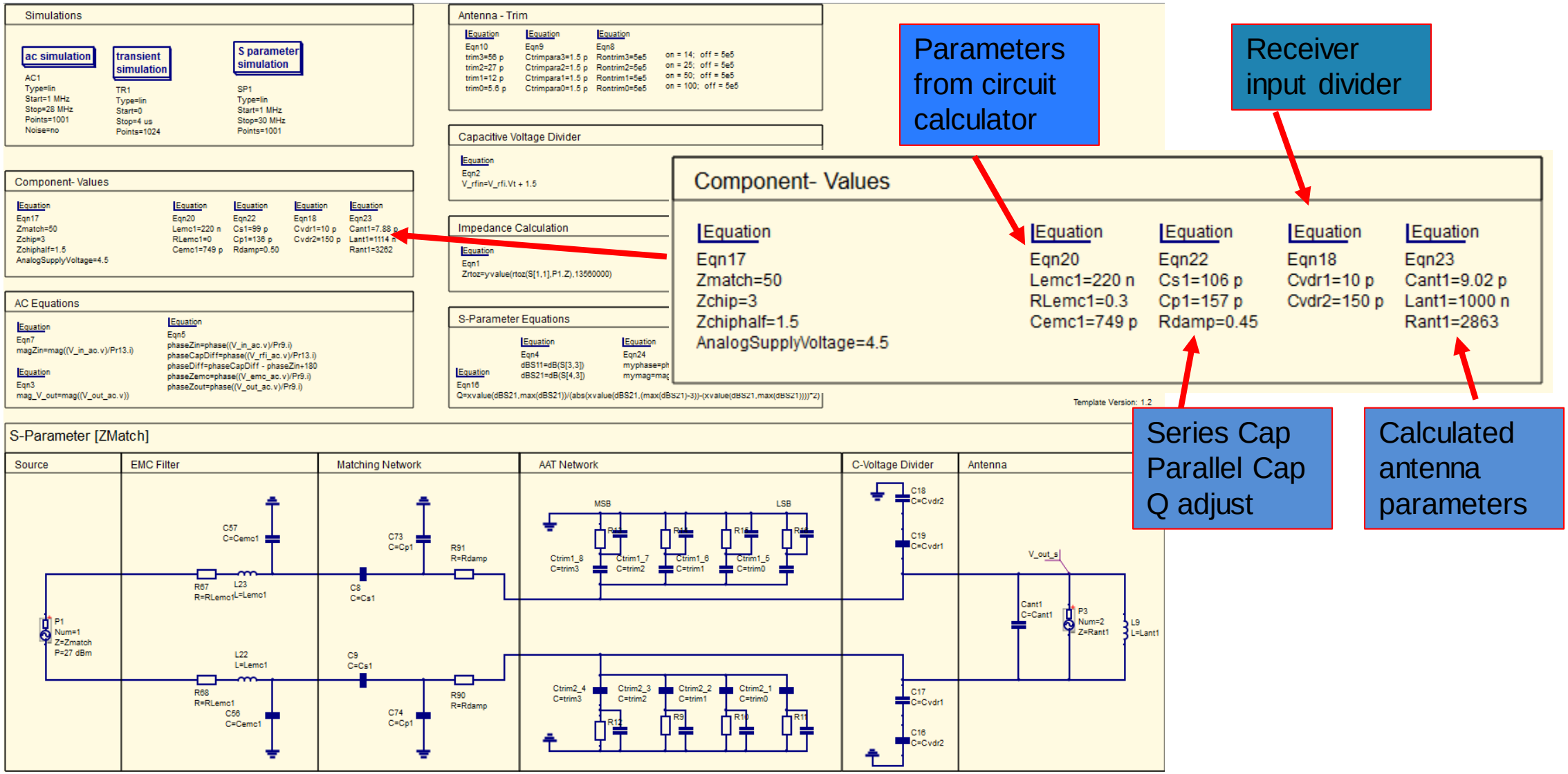
Set pre-conditions
- EMVCo
- General Pupose
- VHBR

Calculate matching values

Simulate (opens QUCs)



Antenna Simulation



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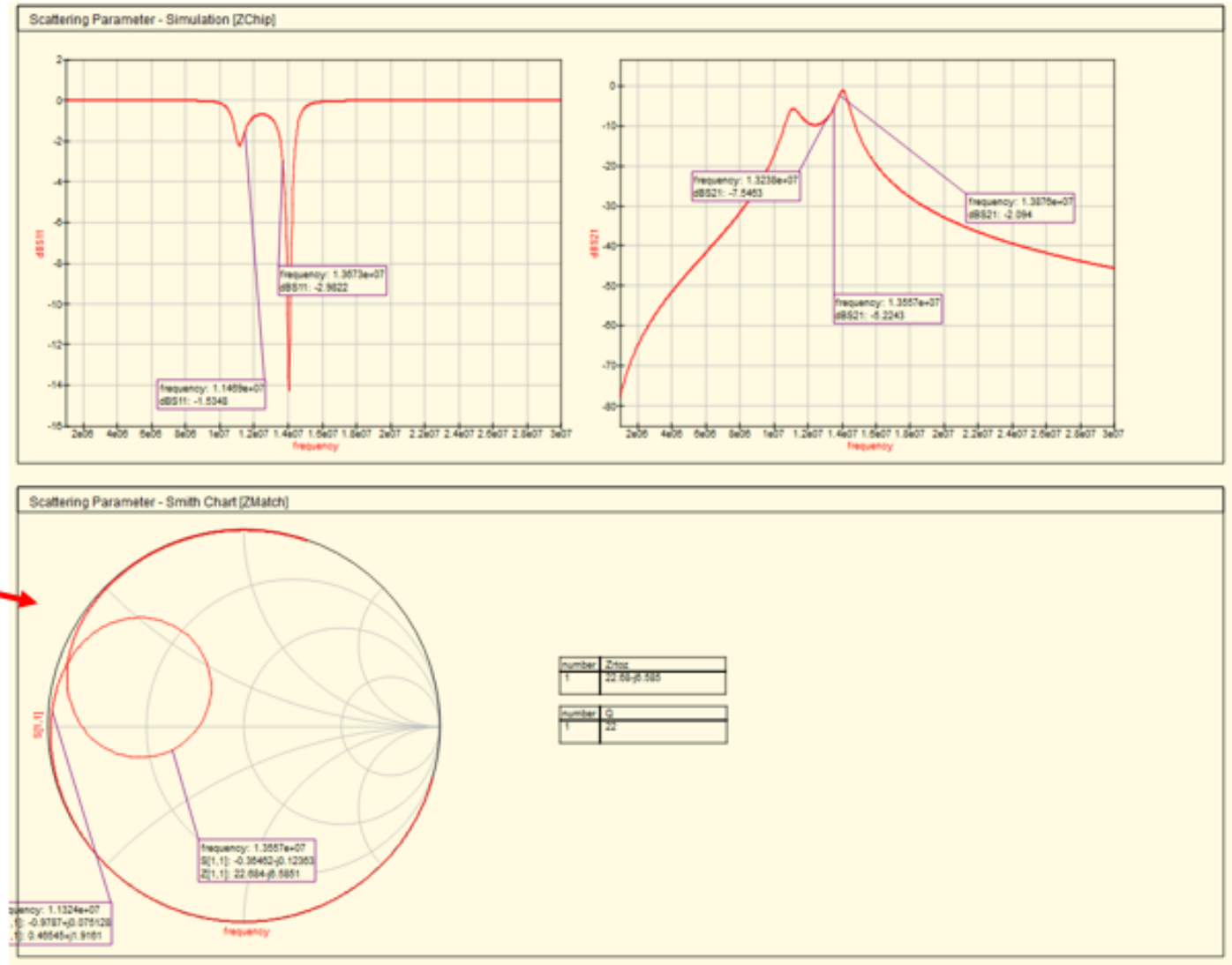
Antenna Simulation

Impedance match info



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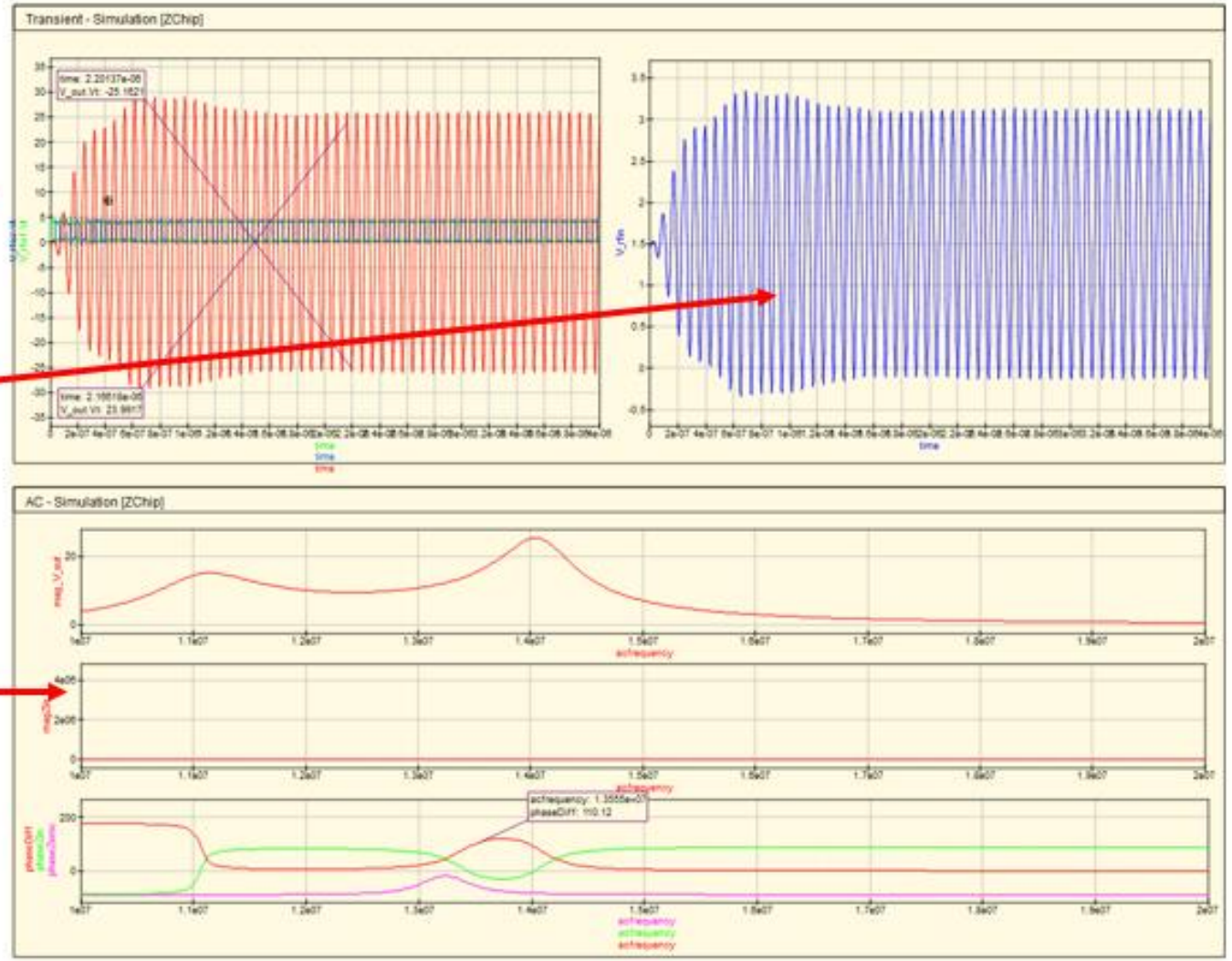
Antenna Simulation

Antenna voltage

Receiver input

Phase and Amplitude info



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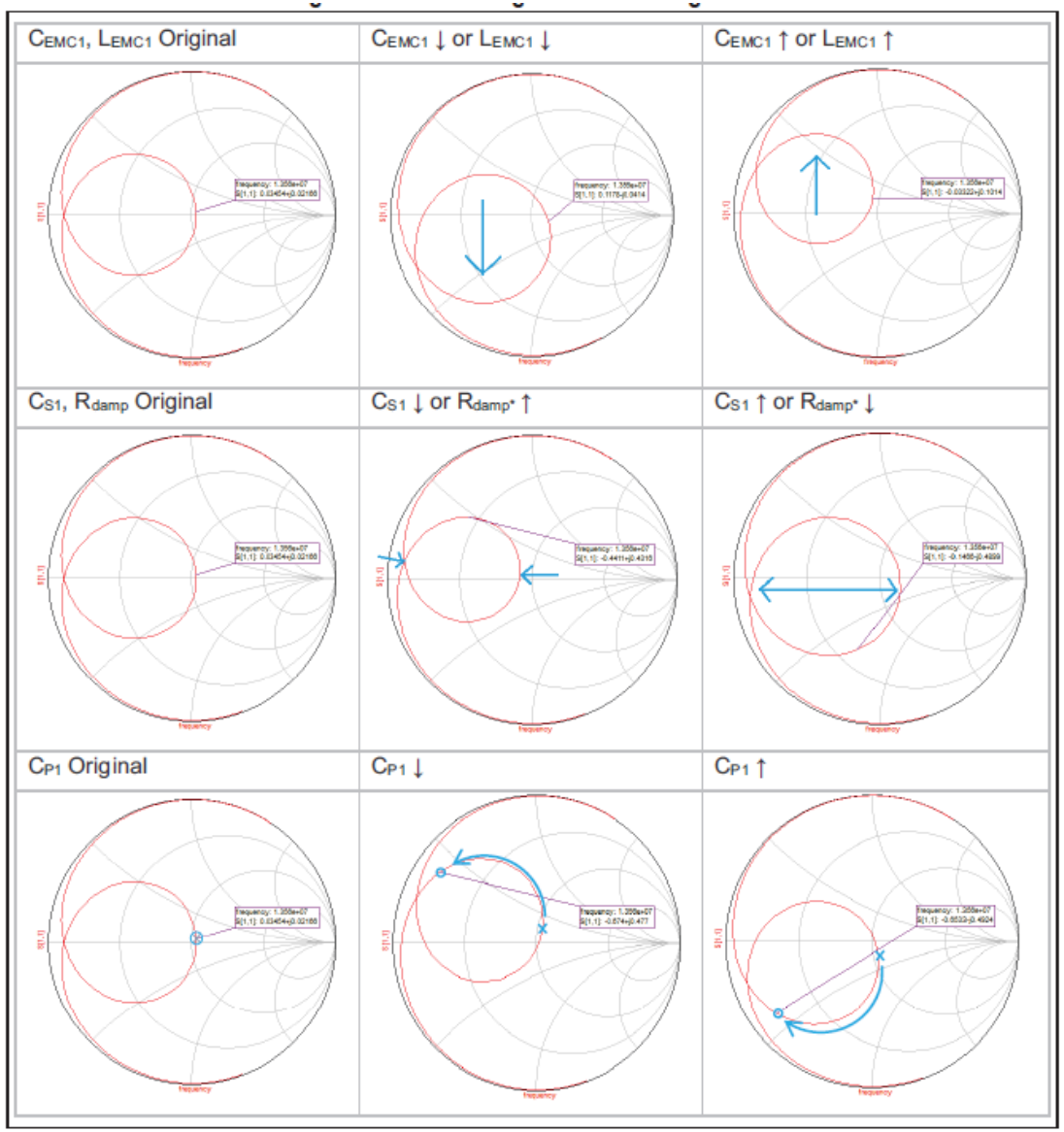
Fine Tuning



EMC Components

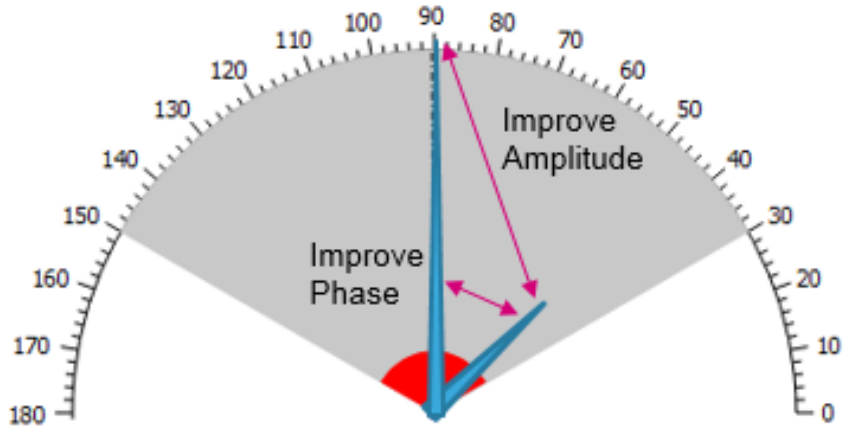
- Serial Cap
- Damping Resistor

Parallel Cap

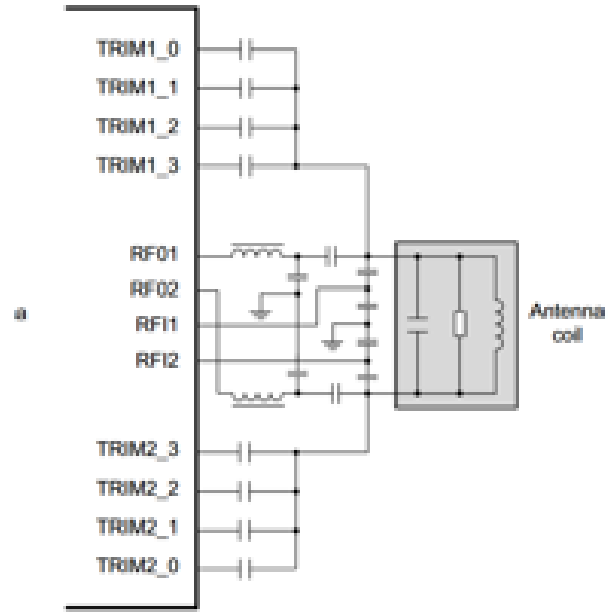
Next Steps

- Populate values on circuit board
- Measure match on RFO pins with VNA
- Re-adjust values as required
- Test
- Optimize read range vs current consumption

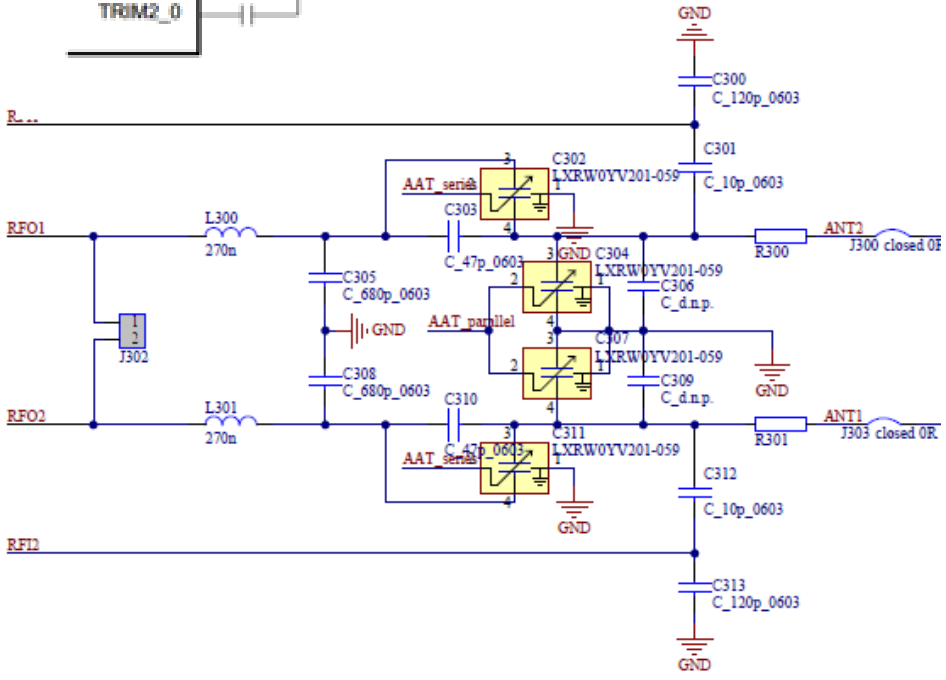
- Automatic Antenna Tuning
  - Allows the matching circuit to be adjusted on the fly
  - Adjustment range dependent on values used
  - Larger Values > Larger range > less granularity
  - Smaller Values > Smaller ranger > more granularity
  - Must be compensated for in the matching circuit



- ST25R3911B
  - 8 External Binary weighted capacitors (4 per RFO)
  - Switches internal to reader



- ST25R3916
  - Uses variable capacitors
  - Internal DAC's use to control variable capacitors
  - Can be used to control both Serial and Parallel Caps



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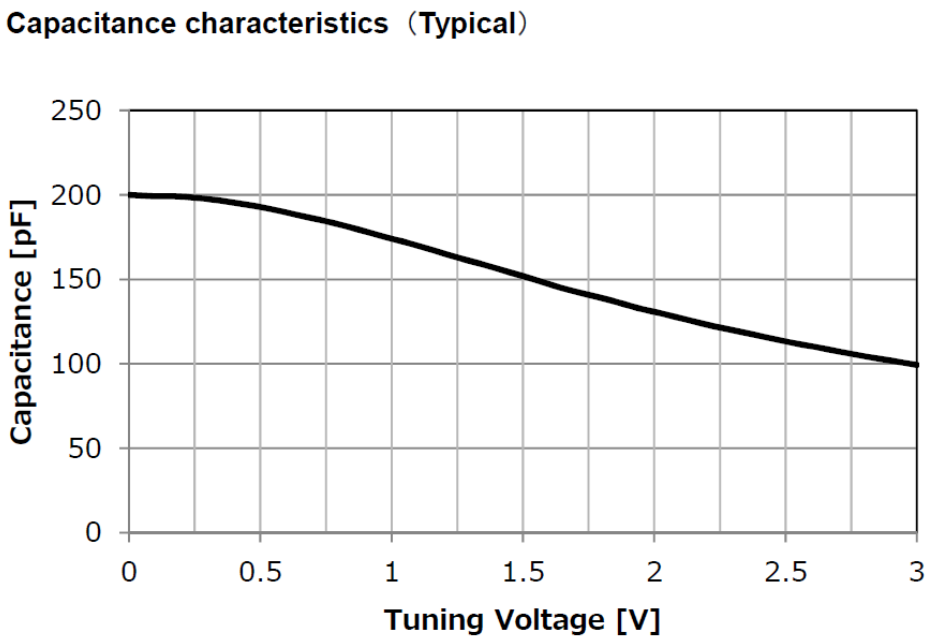
AAT Compensation

- Match antenna as before
- Determine serial/parallel capacitors
- ST25R3916
  - Subtract ¾ Variable cap value from Cp
  - This becomes new parallel capacitor
- ST25R3911B
  - Subtract Highest trim value cap from Cp
  - This becomes new parallel capacitor

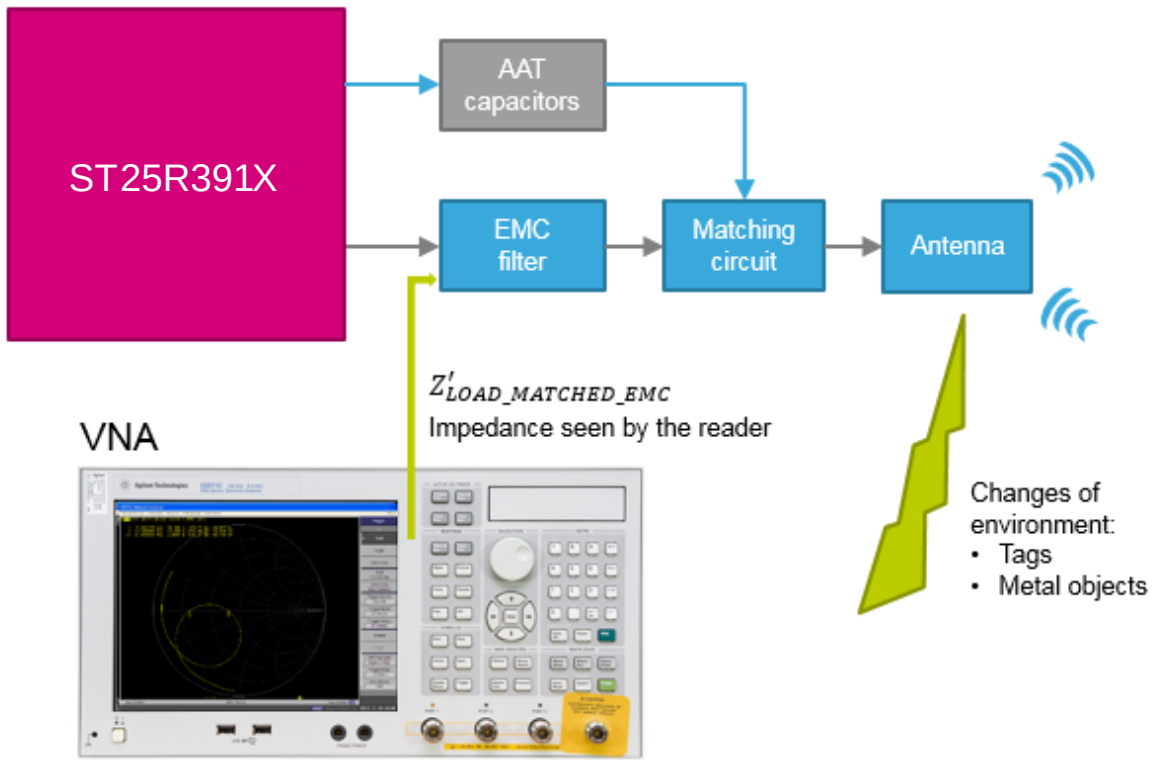


Testing AAT

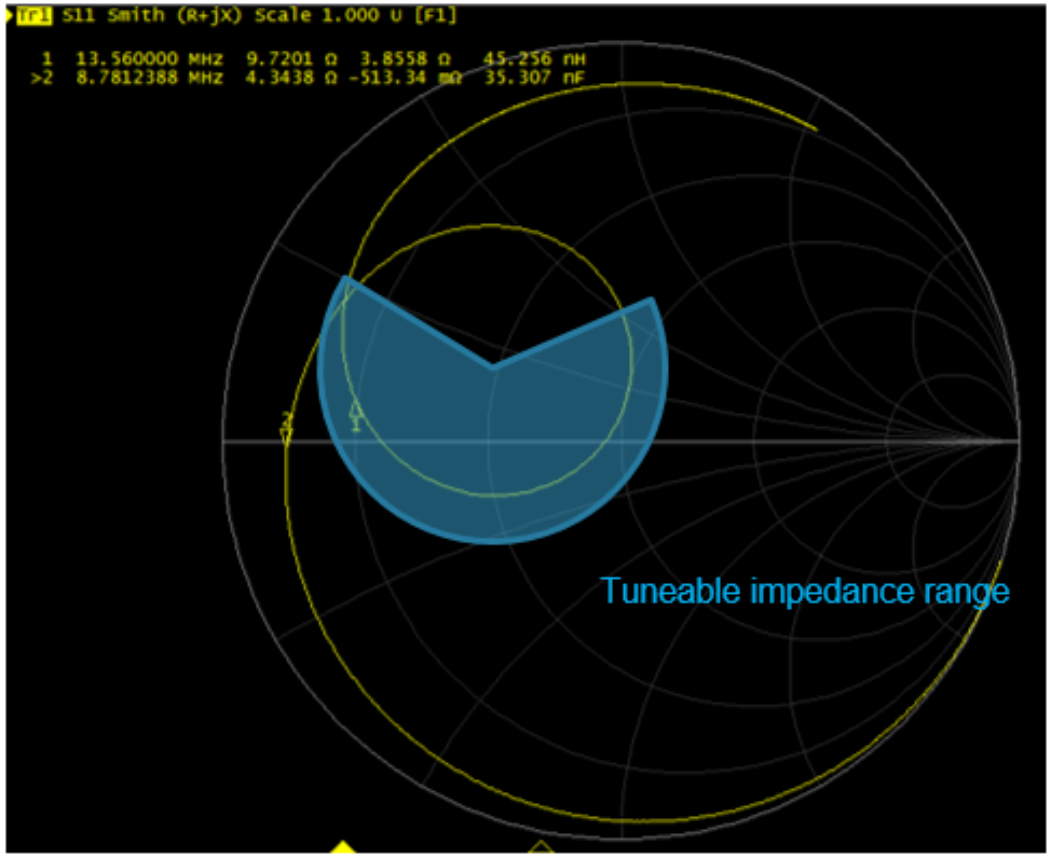
- ST25R3911B
  - Set reg 27 to 0xff (double check that no field is being generated
  - Adjust AAT trim to 8 (Antenna Tab in GUI)
  - Match should be in center of range
- ST25R3916
  - Set reg 28 to 0x7f (double check that no field is being generated
  - Adjust AAT trim mid (Antenna Tab in GUI)
  - Match should be in center of range

Important to turn off output drivers

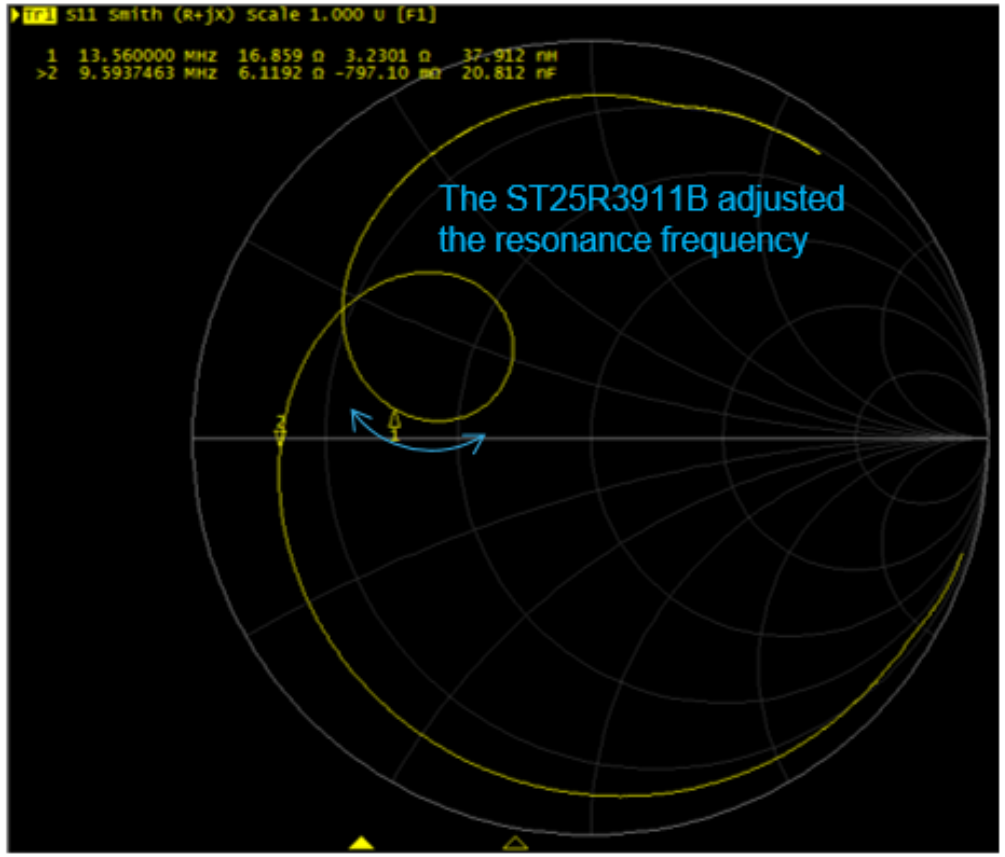
- Measurement of how AAT changes the impedance of the antenna seen by the reader



AAT Range



ST25R3916



ST25R3911B

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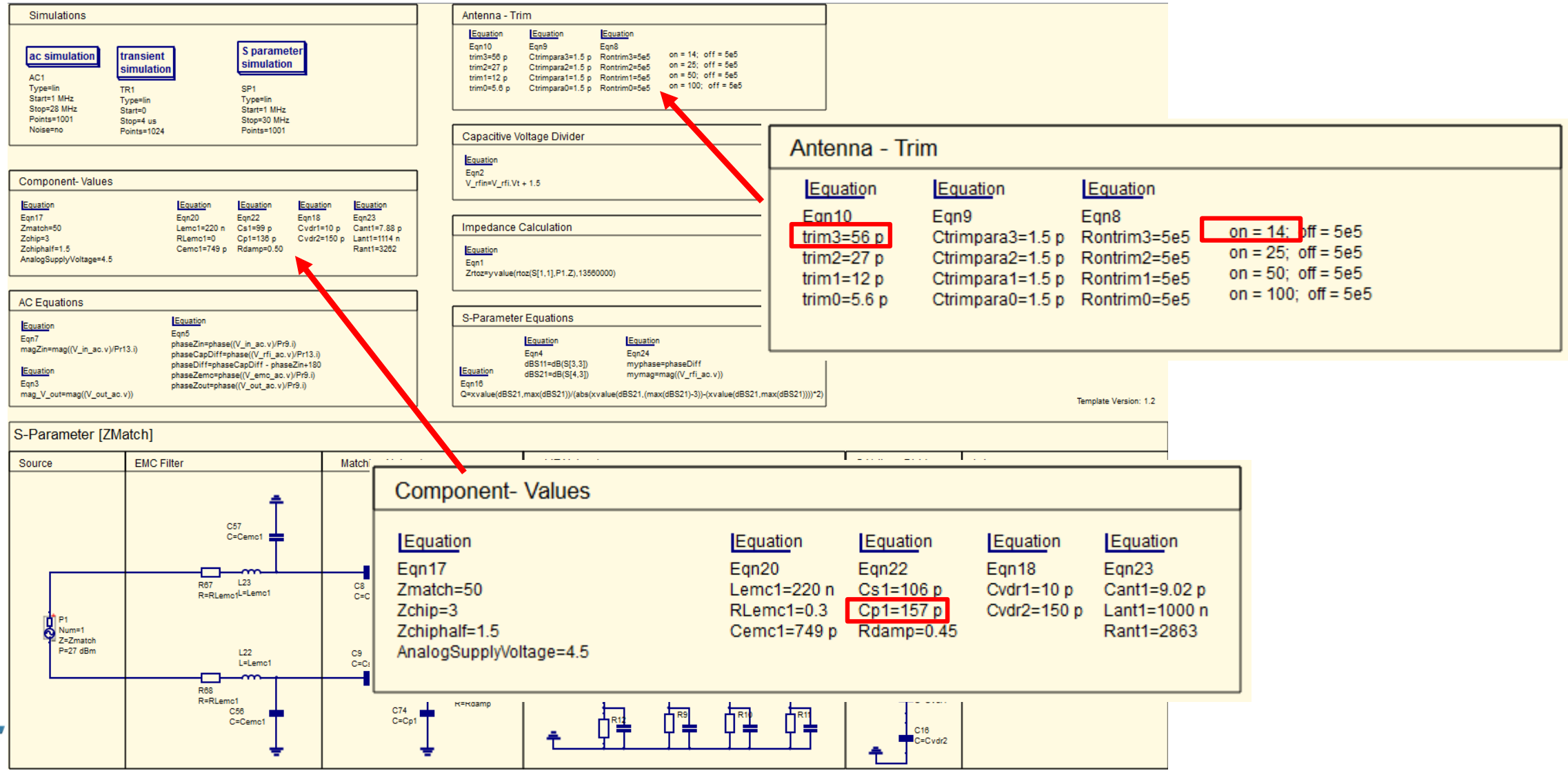
AAT Simulation

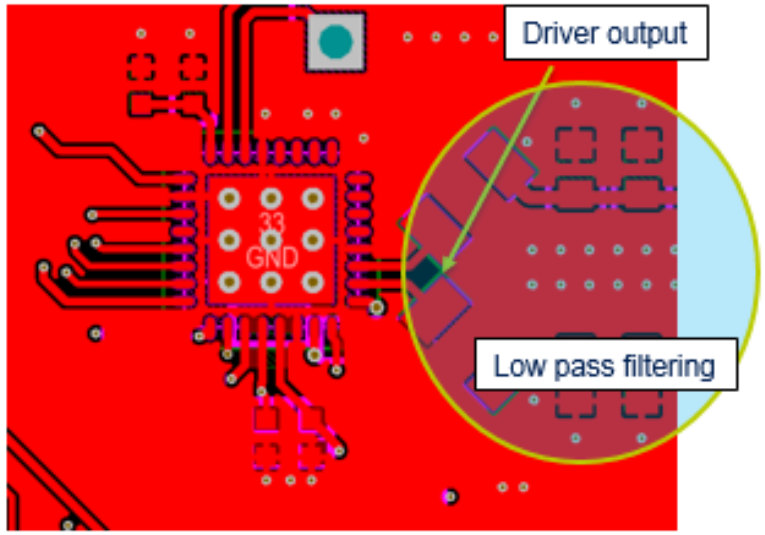


Layout Suggestions

- 4 layer board if possible (Sig/GND/PWR/Sig)
- Make RFO paths symmetrical
- Keep traces short
- EMC filter as close as possible to RFO pins
- Layout extra pads for Cs and Cp for fine tuning
- Layout pads for AAT (just in case)

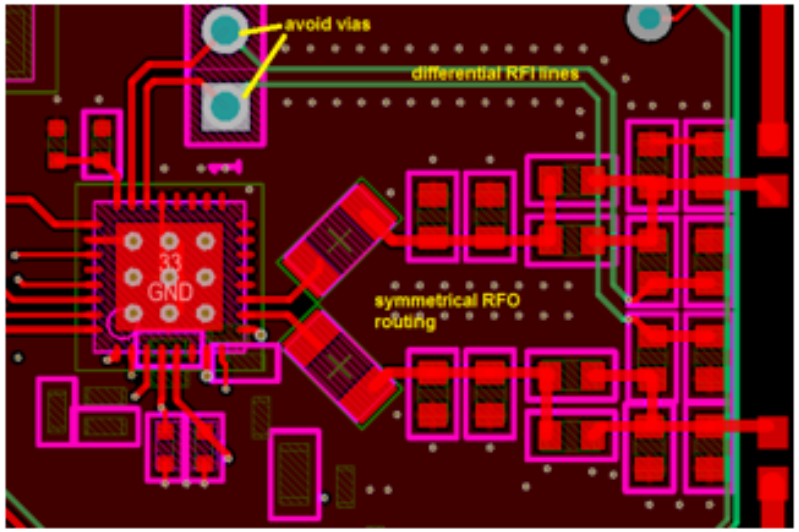
Layout Suggestions

EMC filter



- Filter must be positioned as close as possible to the output stages

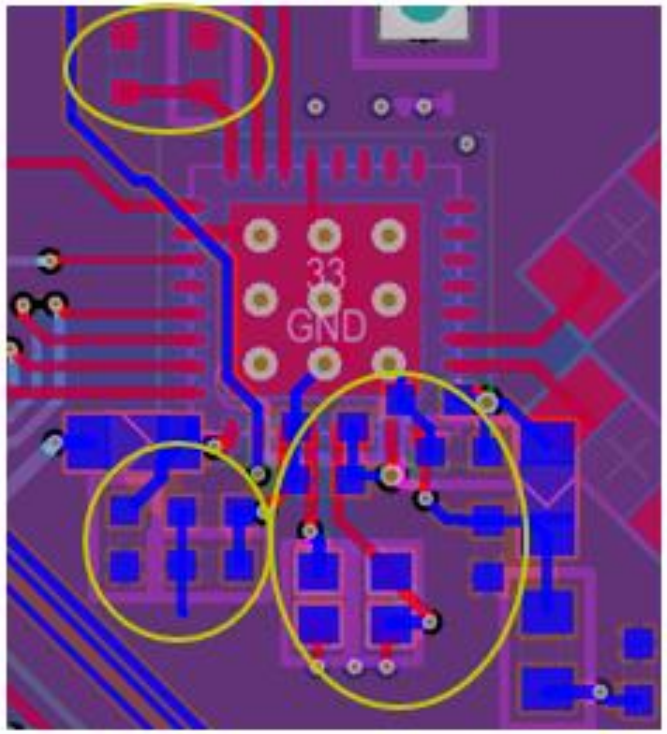
RFO & RFI routing



- The inductors after the RFO are placed in 90 degree direction
- The RFI lines are routed symmetrically, but in a fair distance to the RFO lines
- No long signal traces between LC filter and the remaining matching components
- The vias in the RFI lines should be avoided in a final design

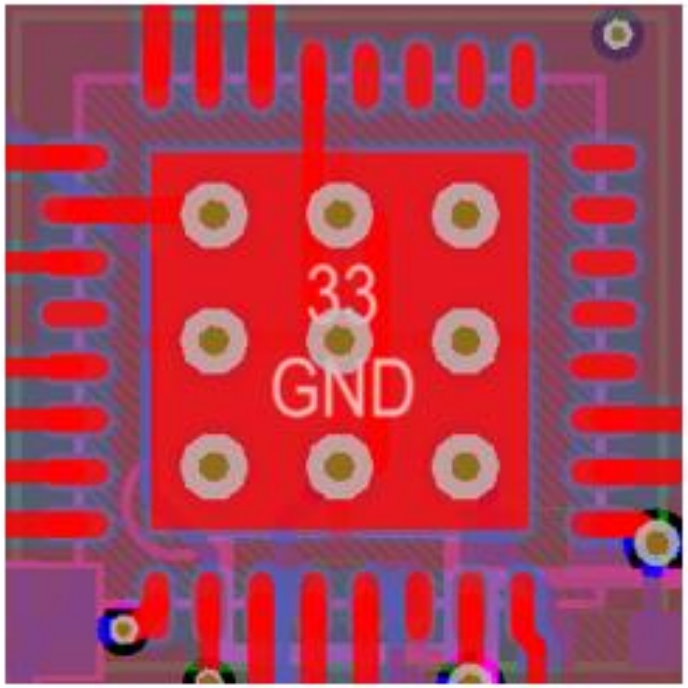
Layout Suggestions

Decoupling

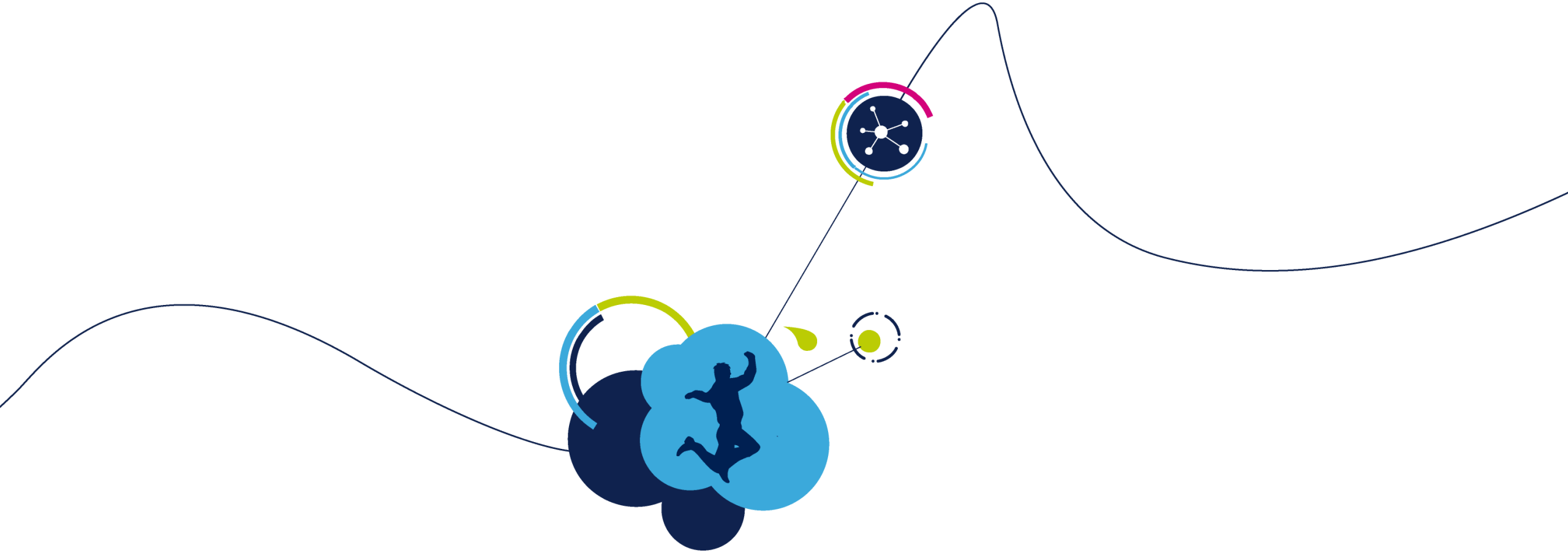


- Capacitors as close as possible to the chip
- Parallel capacitors 2.2 µF and 10 nF

Thermal pad



- Ground plane & thermal heatsink
- Multiple through vias must be used



Questions?

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