

How to Design a NFC Reader Application

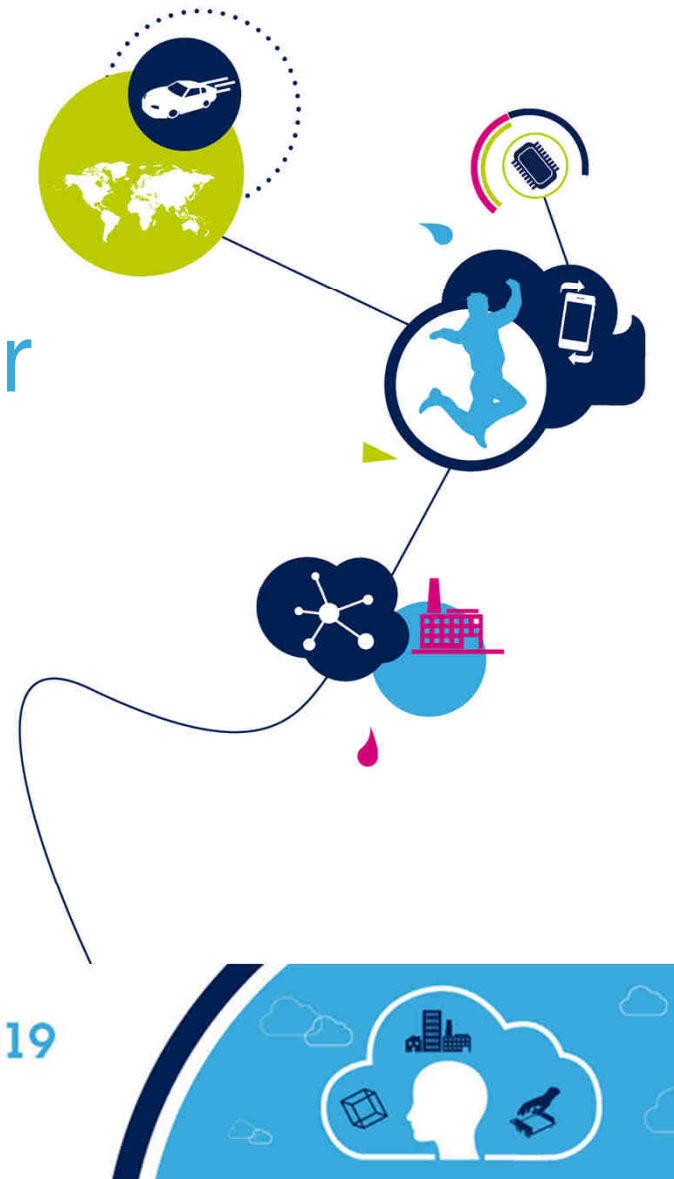
A Step-by-Step Approach

Daniel Merino



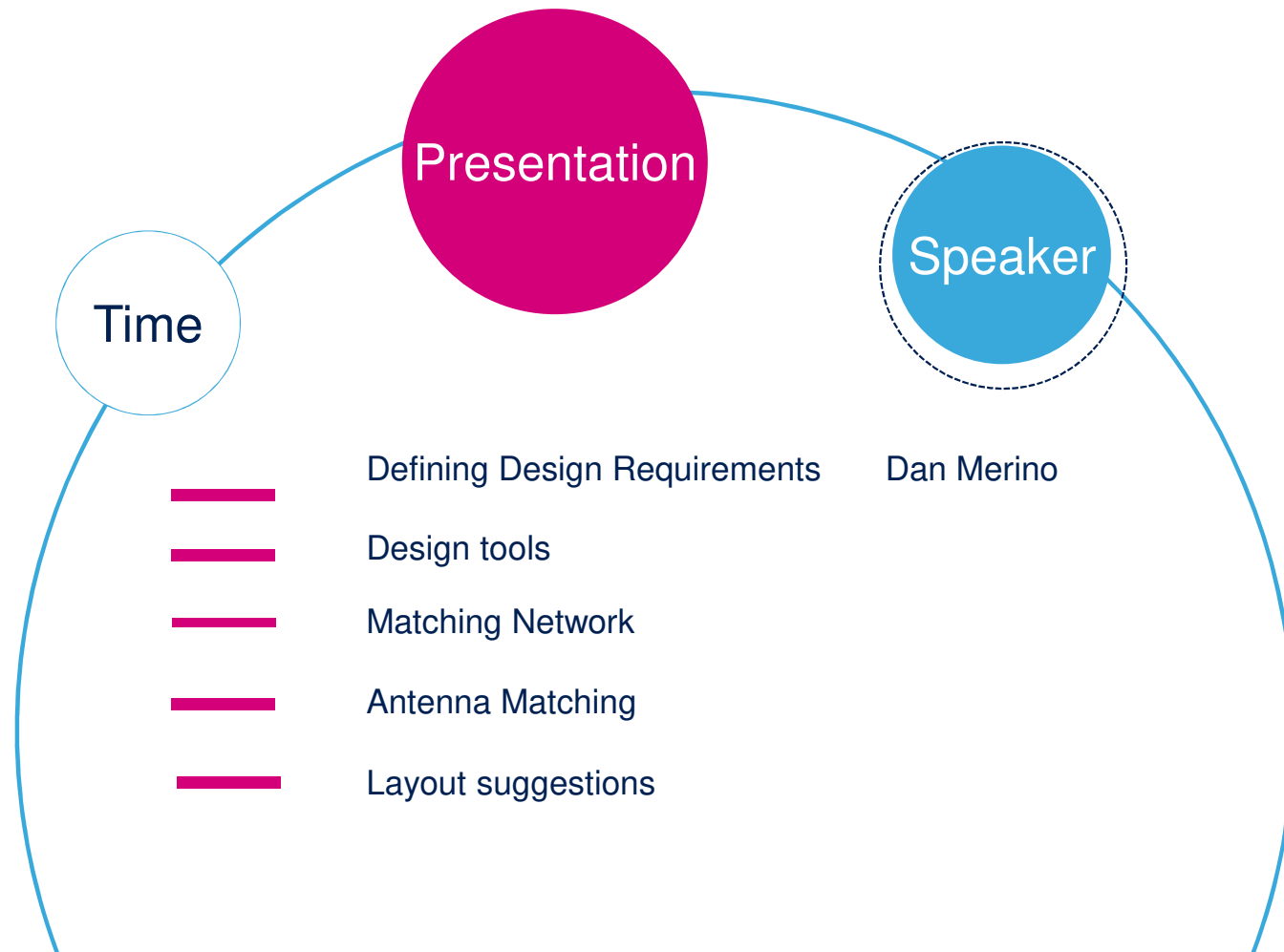
Technology Tour 2019

Vancouver, BC | September 24



Agenda

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Defining Design Requirements

Defining Design Requirements

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- End Product
 - Payment
 - General Purpose
- Communication Protocol
 - ISO 14443 A/B
 - ISO 15693
 - Felica
 - AP2P.

Defining Design Requirements

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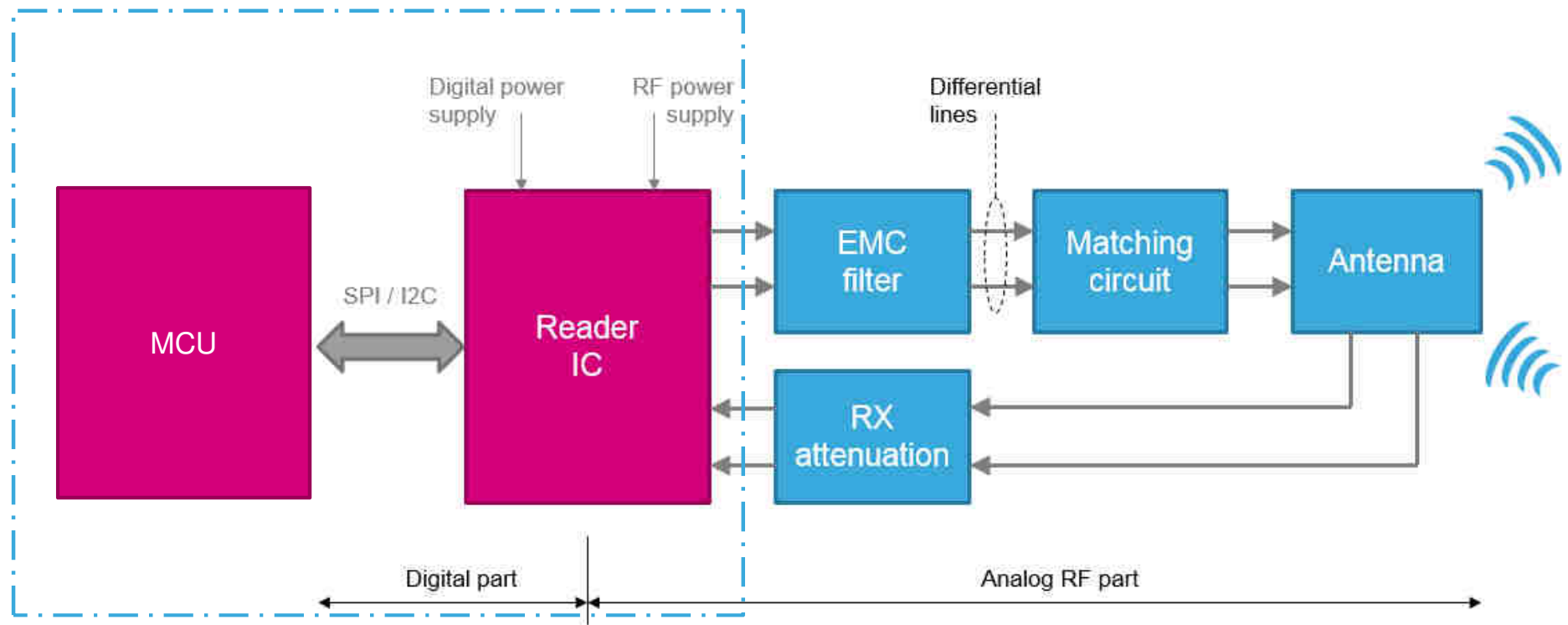
- System constraints
 - Antenna Size
 - Environmental Conditions
 - Metal
 - LCD screen
 - Antenna placement
- Design Trade-offs
 - Antenna size
 - Read Range
 - Current Consumption



System Block Diagram

System Block Diagram

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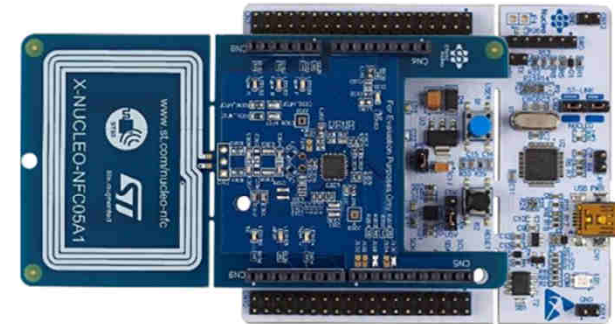


Design Tools

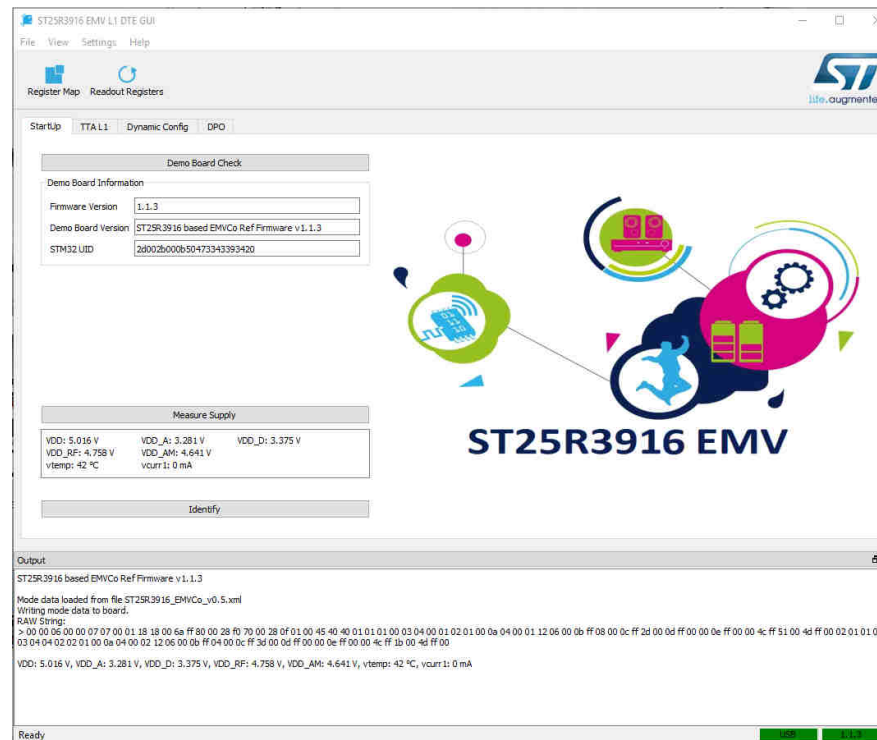
Design Tools

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- ST25R3911B Discovery
 - Software GUI
 - Source code downloadable
 - Design files downloadable
- ST25R3911B Nucleo Shield
 - Firmware available
 - Design files downloadable
- ST25R3916 Discovery
 - Software GUI
 - Source code downloadable
 - Design files downloadable



- EMVCo Reference design
 - Hardware eval board
 - Software GUI
 - L1 Stack
 - Available only by Request

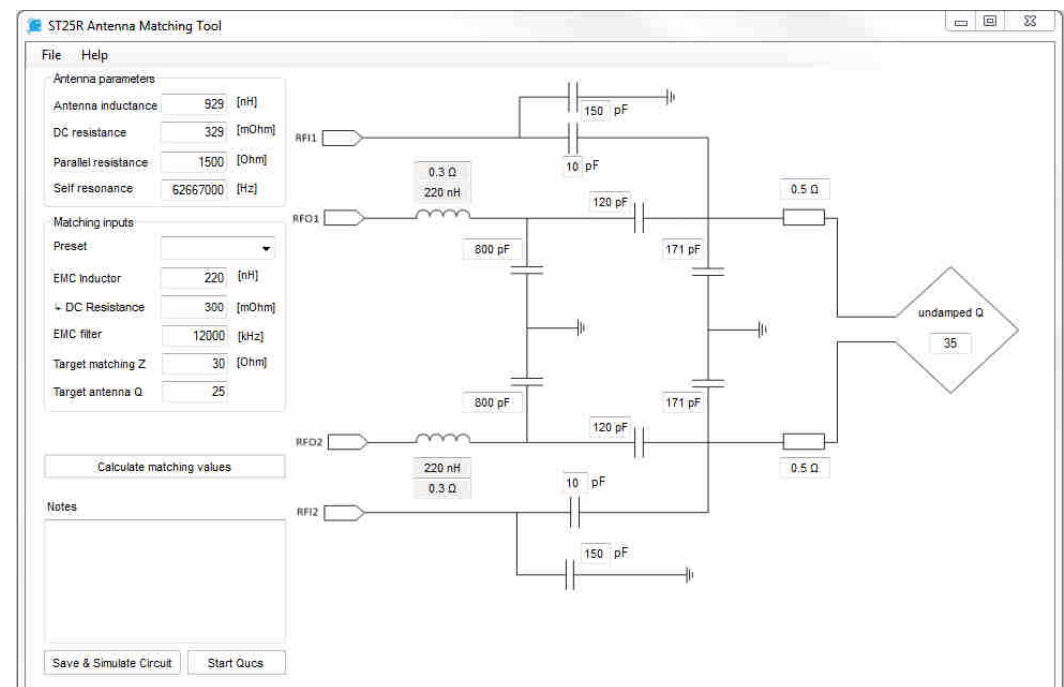


*ST25R3916 recommended for EMVCo 3.0 and above

Design Tools

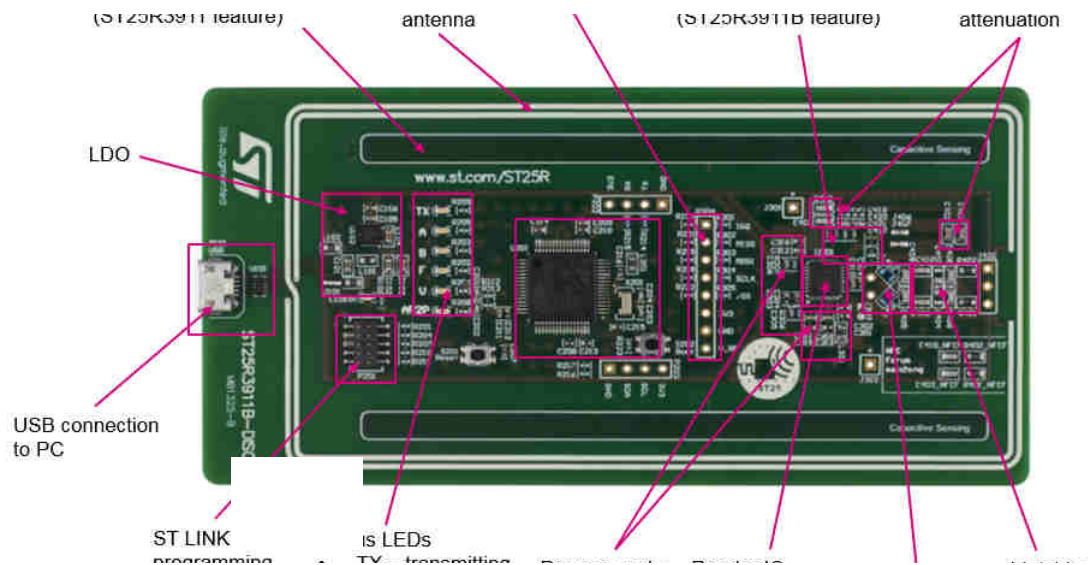
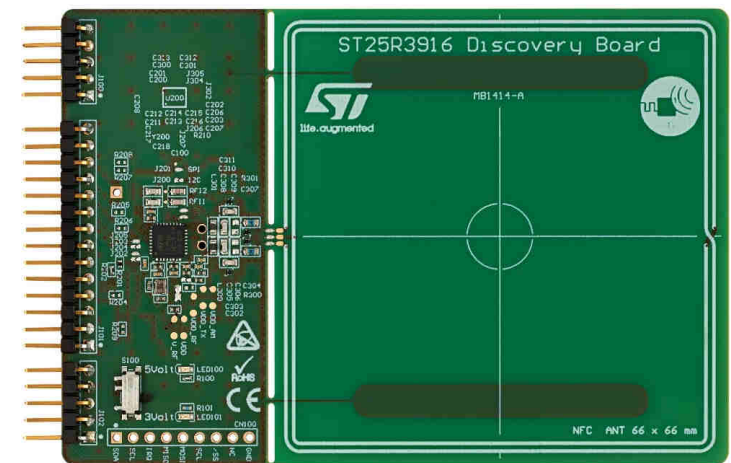
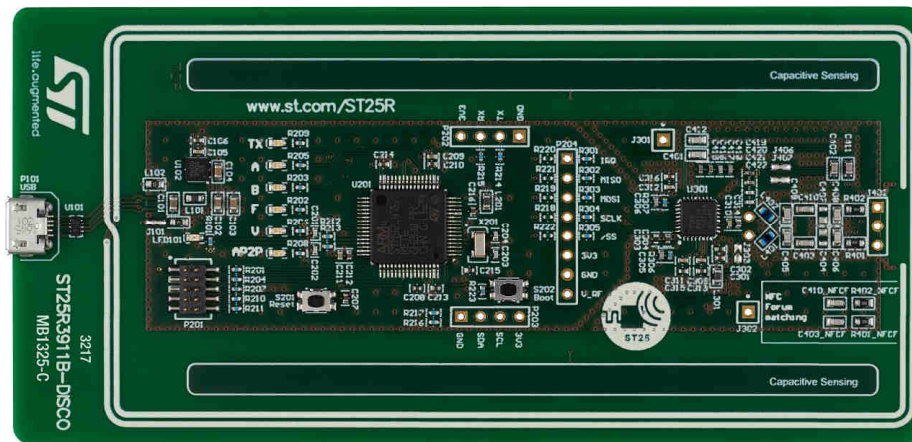
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- Antenna Design Matching tool
 - Calculates matching components
 - Includes simulation program
 - Available on ST25R3911B landing page



Design Tools

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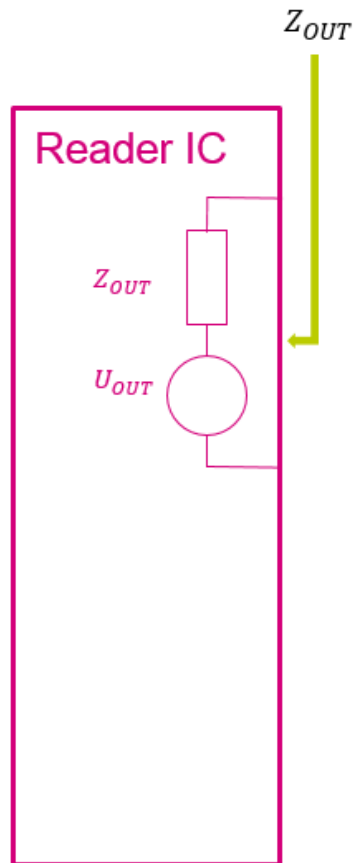




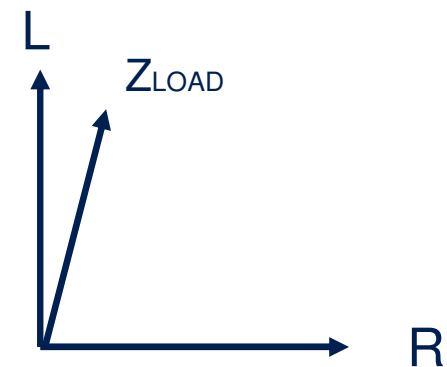
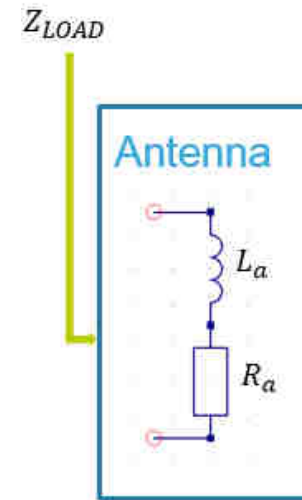
Matching Network

Matching Circuit

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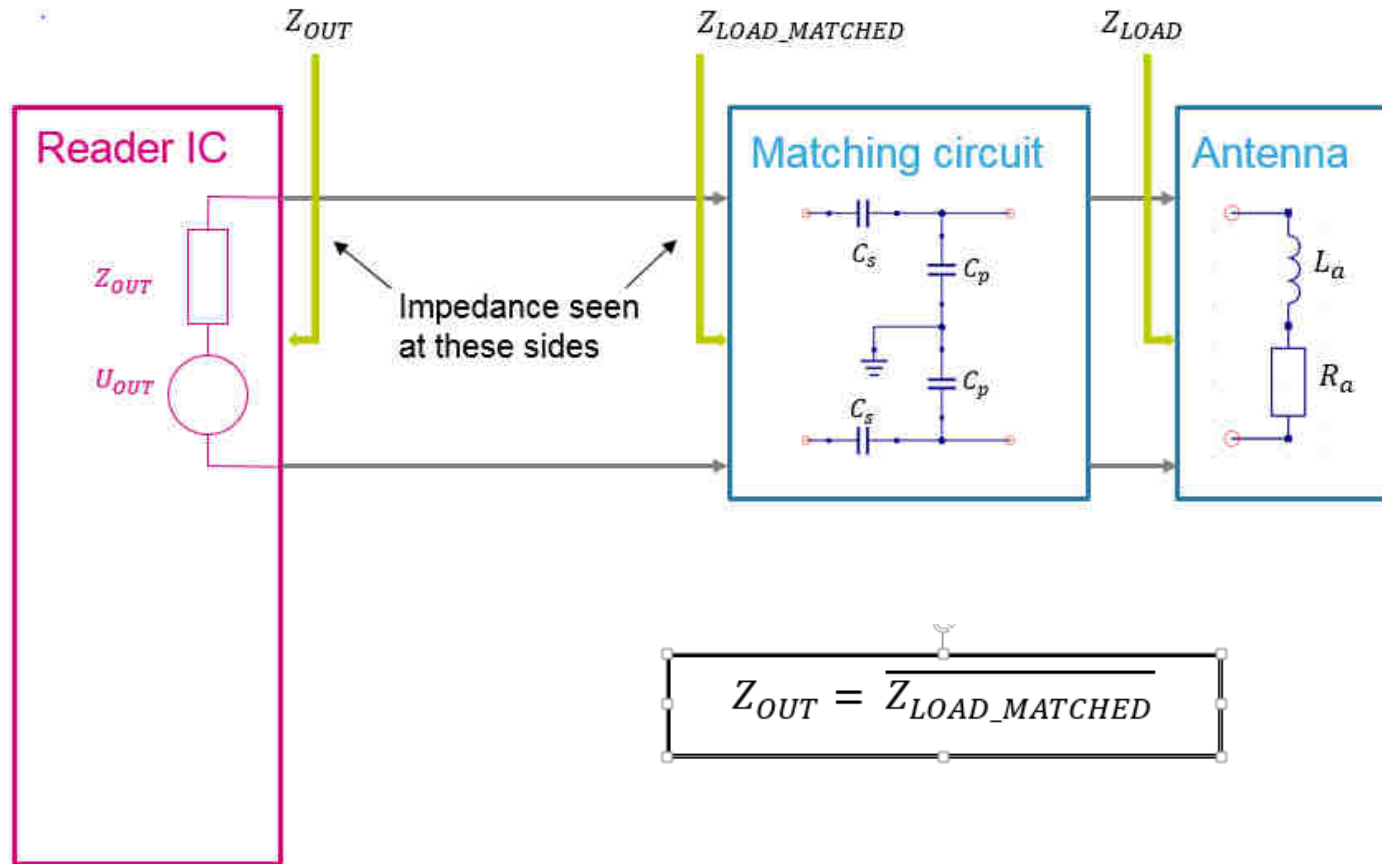


$$Z_{out} = \overline{Z_{LOAD}}$$



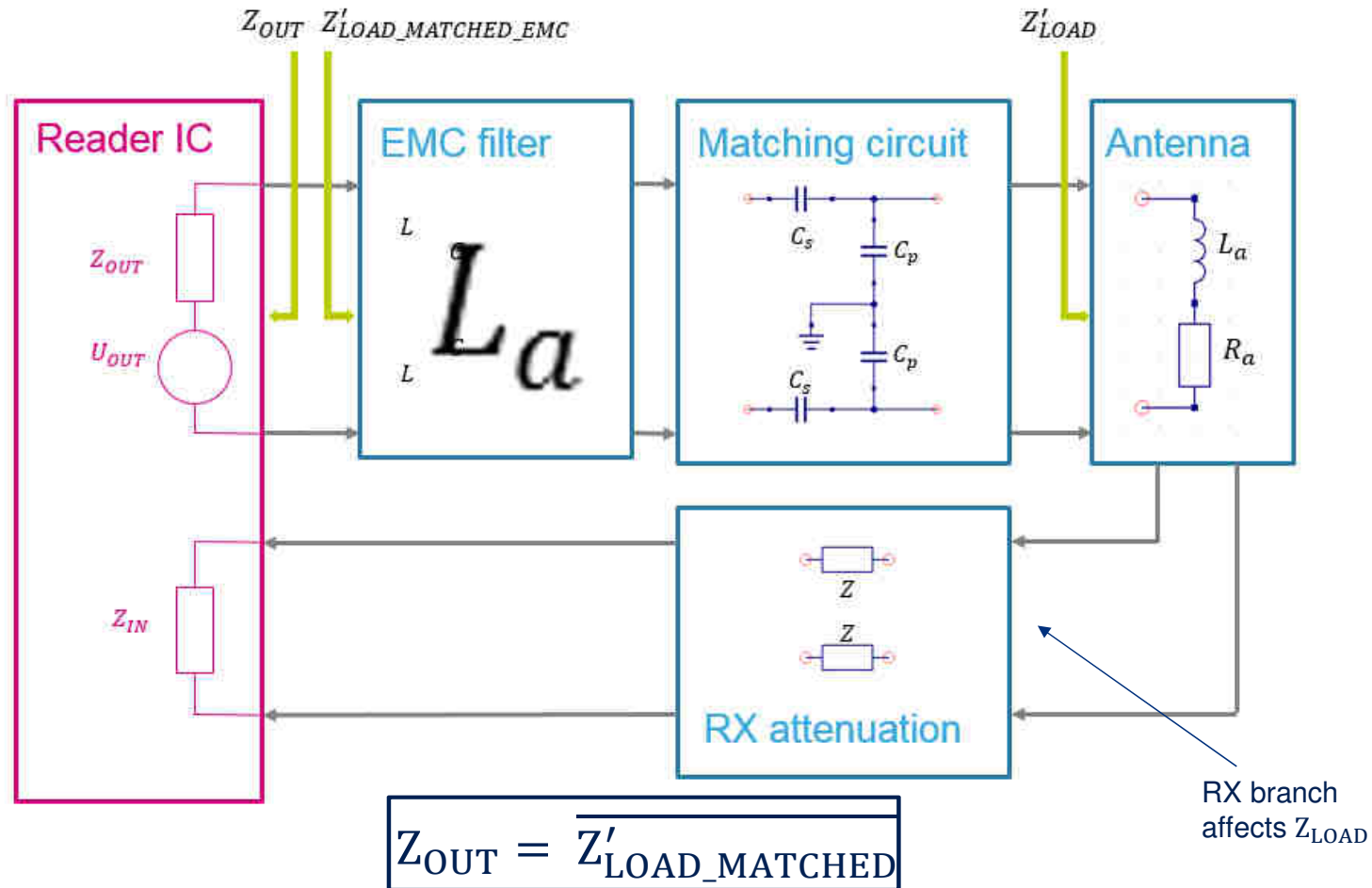
Matching Circuit

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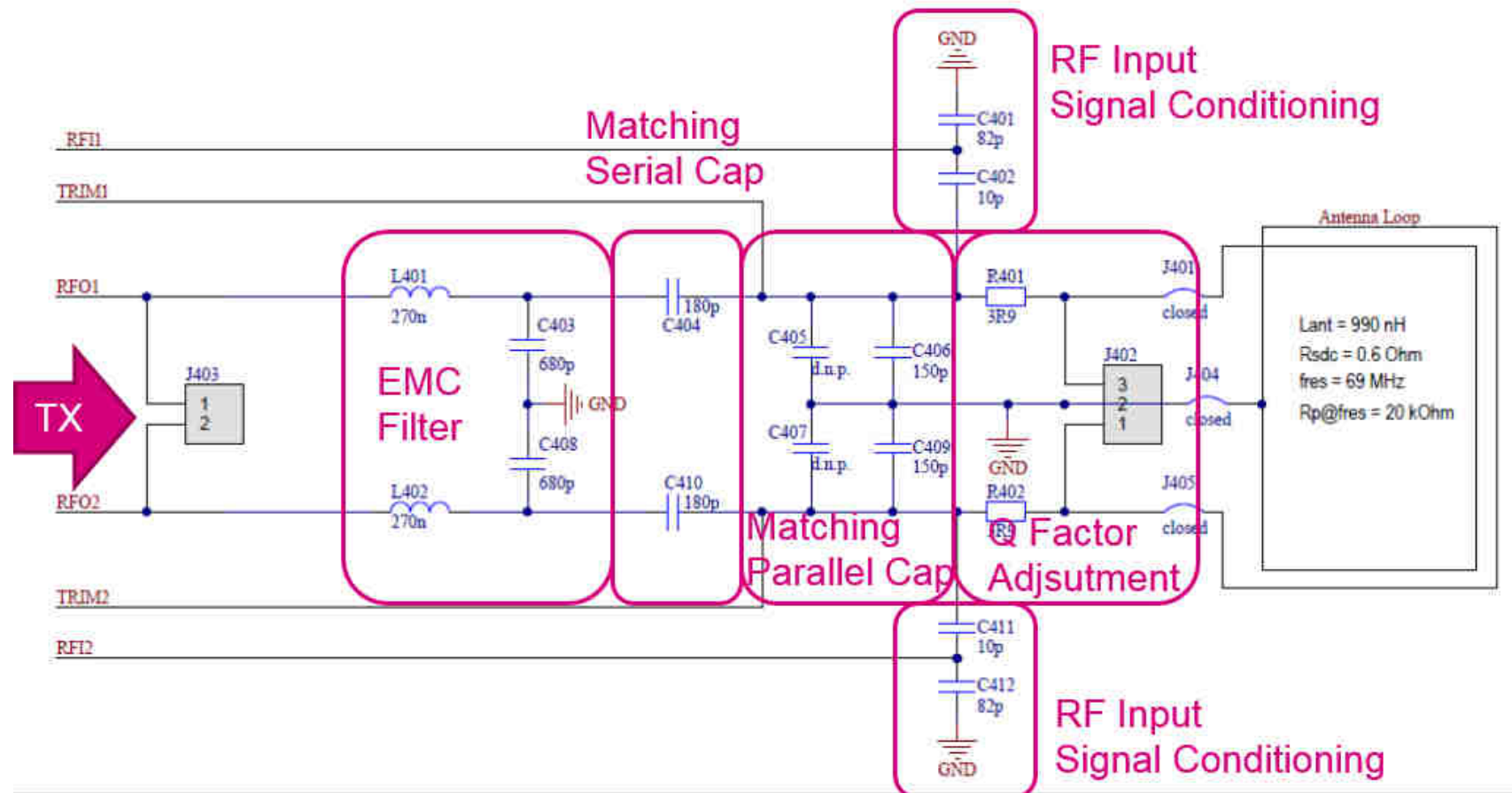
Matching Circuit

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Matching Circuit

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Matching Circuit

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- Antenna
 - Two Turn
 - Typical Inductance 200nH – 2uH
- EMC Filter
 - Reduces harmonics of the RFO output stage
 - Target Cutoff Frequency about 13.56Mhz
- Matching Serial Cap
 - Impedance match from EMC filter to antenna resonator circuit
 - Cuts DC path from RFO1 to RFO2

Matching Circuit

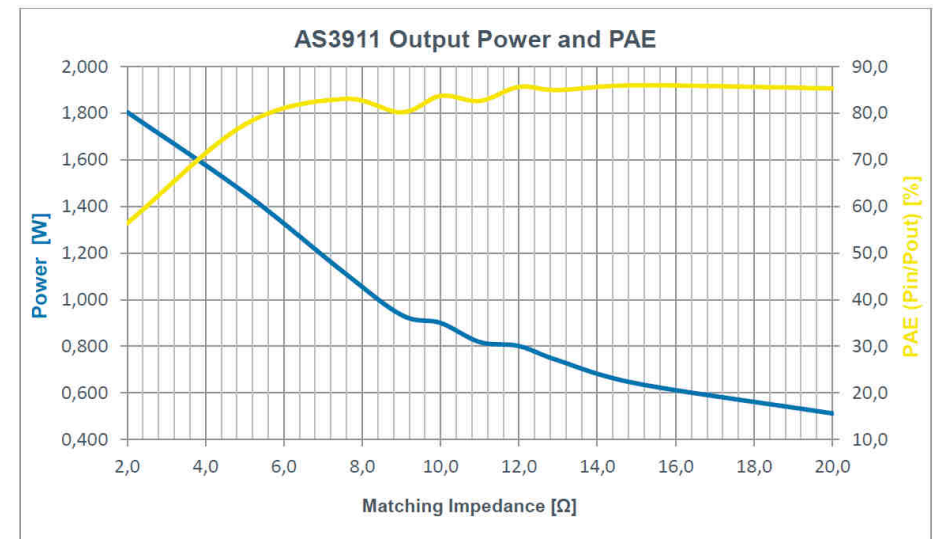
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- Q Factor adjustment
 - Sets System Q (antenna Q should always be higher than System Q)
 - Higher Q > More Field Strength > Lower Datarate
 - Lower Q > Faster rise/fall times > Higher Datarate
 - Target Values
 - Up to 106kbps – 25
 - Up to 848kbps – 12-16
 - Up to 3.4Mbps - 8
- RFI Input Conditioning
 - Reduces Antenna Voltage to < 3.0Vpp for RFI input

Matching Circuit

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- Target Matching impedance
 - Higher > less field strength > less power consumption > higher efficiency
 - Lower > higher field strength > higher power consumption > less efficiency
 - Range 8 – 120 ohms
 - Typically between 10 – 30 ohms



Antenna Parameters

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Parameter	Action	Effect on parameter	Q factor
Q factor	Increase trace width	-	Increases
	Increase gap width		
Inductance	Larger antenna	Increases	Decreases
	Decrease trace width		
	Decrease gap width		
Series DC resistance	Larger antenna	Increases	Decreases
	Decrease trace width		
	Decrease gap width		
Parallel resistance	Decrease trace width	Increases	Increases
	Increase gap width		
Resonance frequency	Smaller antenna	Increases	Increases
	increase gap width		



Antenna Matching

Antenna Measurements

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- Measure the following Parameters with a VNA

- DC resistance
- Inductance
- Self resonance frequency
- Parallel R @ F_{SR}

1:	1,000,000Hz
RL	-0.24dB
RP	164.79°
Z	6.7Ω
Rs	0.7Ω
Xs	6.7Ω
Swr	71.2:1
Mag	0.972
2:	13,563,694Hz
RL	-0.23dB
RP	55.51°
Z	95.0Ω
Rs	3.1Ω
Xs	94.9Ω
Swr	74.7:1
Mag	0.974
3:	53,729,443Hz
RL	-0.40dB
RP	0.08°
Z	2196.1Ω
Rs	2195.1Ω
Xs	65.1Ω
Swr	43.9:1
Mag	0.955

DC Resistance

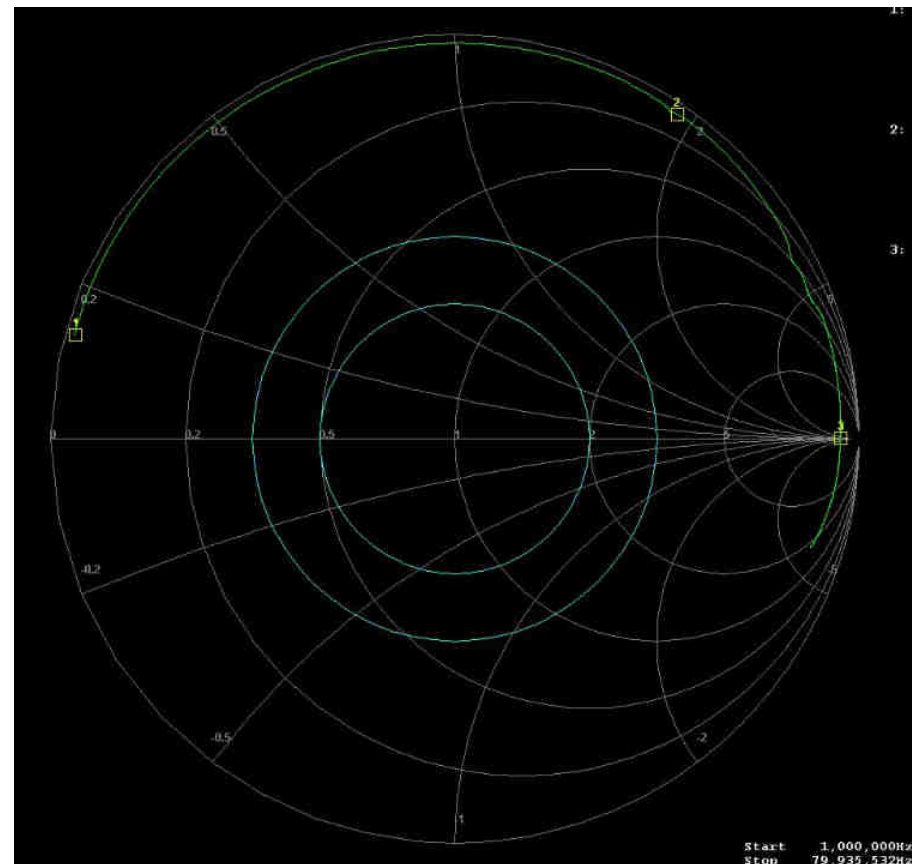
Xs @13.56MHz
used to
calculate
inductance

Self Resonant
Frequency

Parallel
Resistance

$$Xs = j\omega L$$

$$L = \frac{Xs}{j\omega}$$



Antenna Measurements

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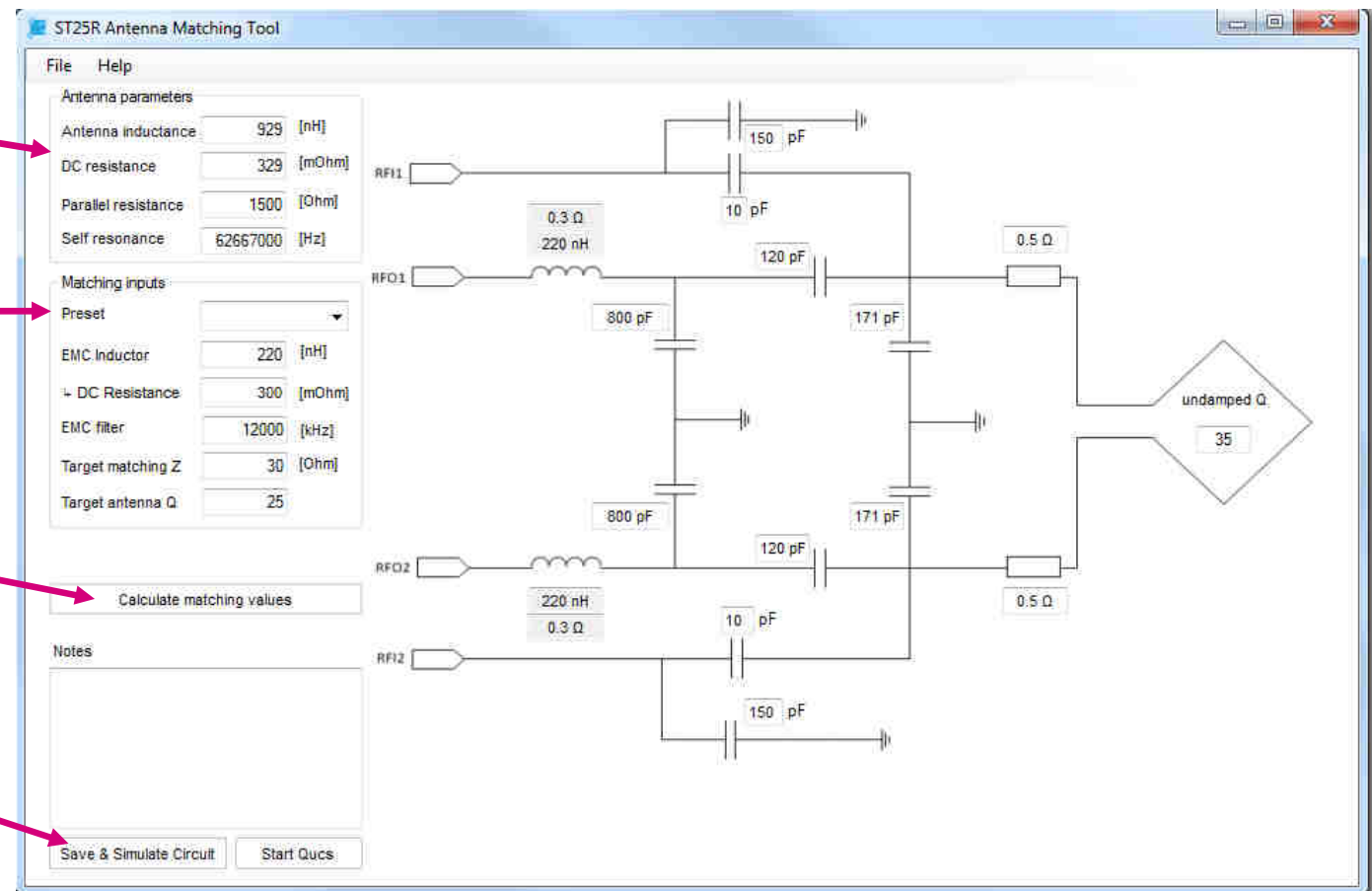
Input antenna parameters

Set pre-conditions

- EMVCo
- General Purpose
- VHBR

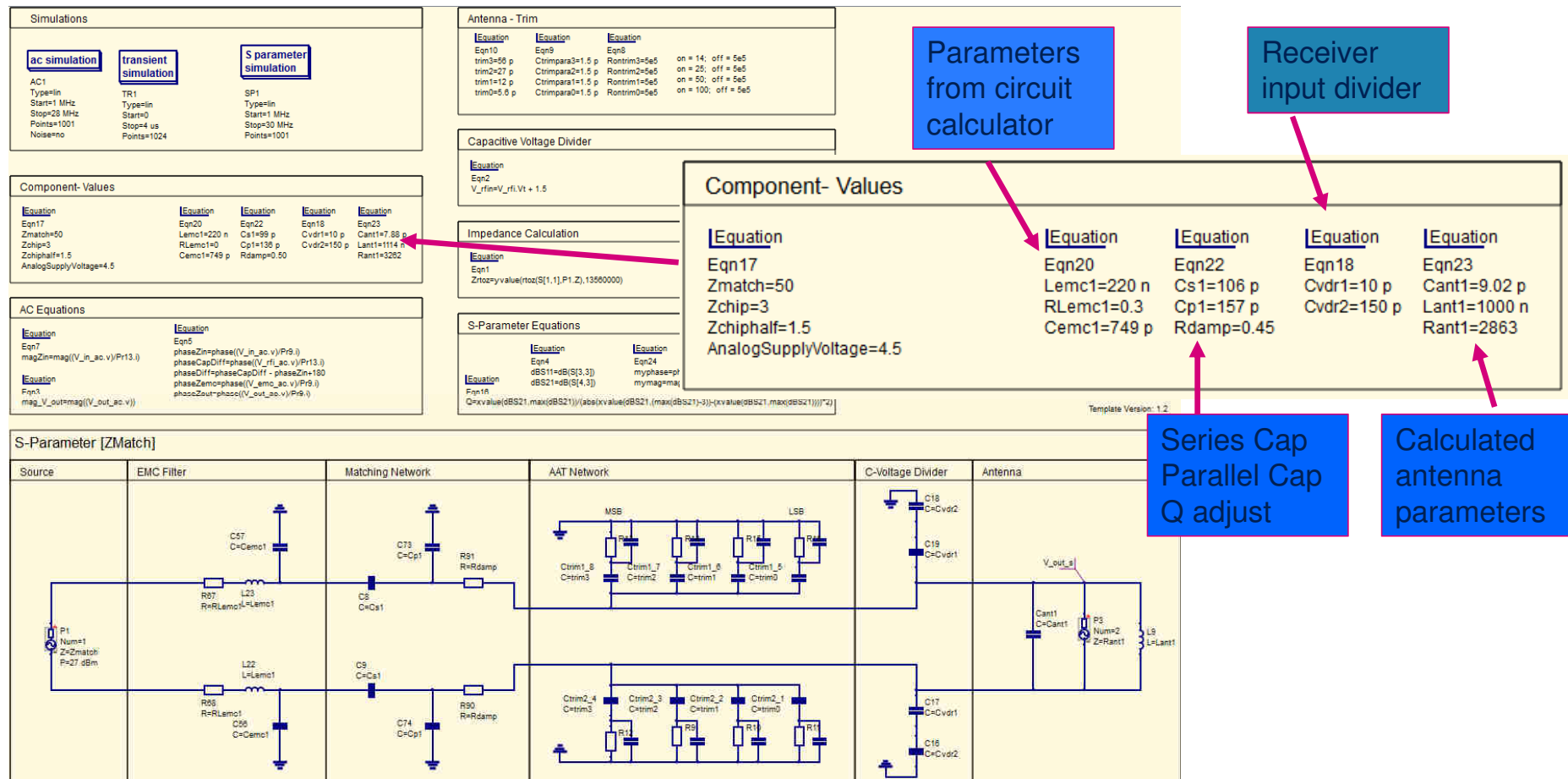
Calculate matching values

Simulate (opens QUCs)



Antenna Simulation

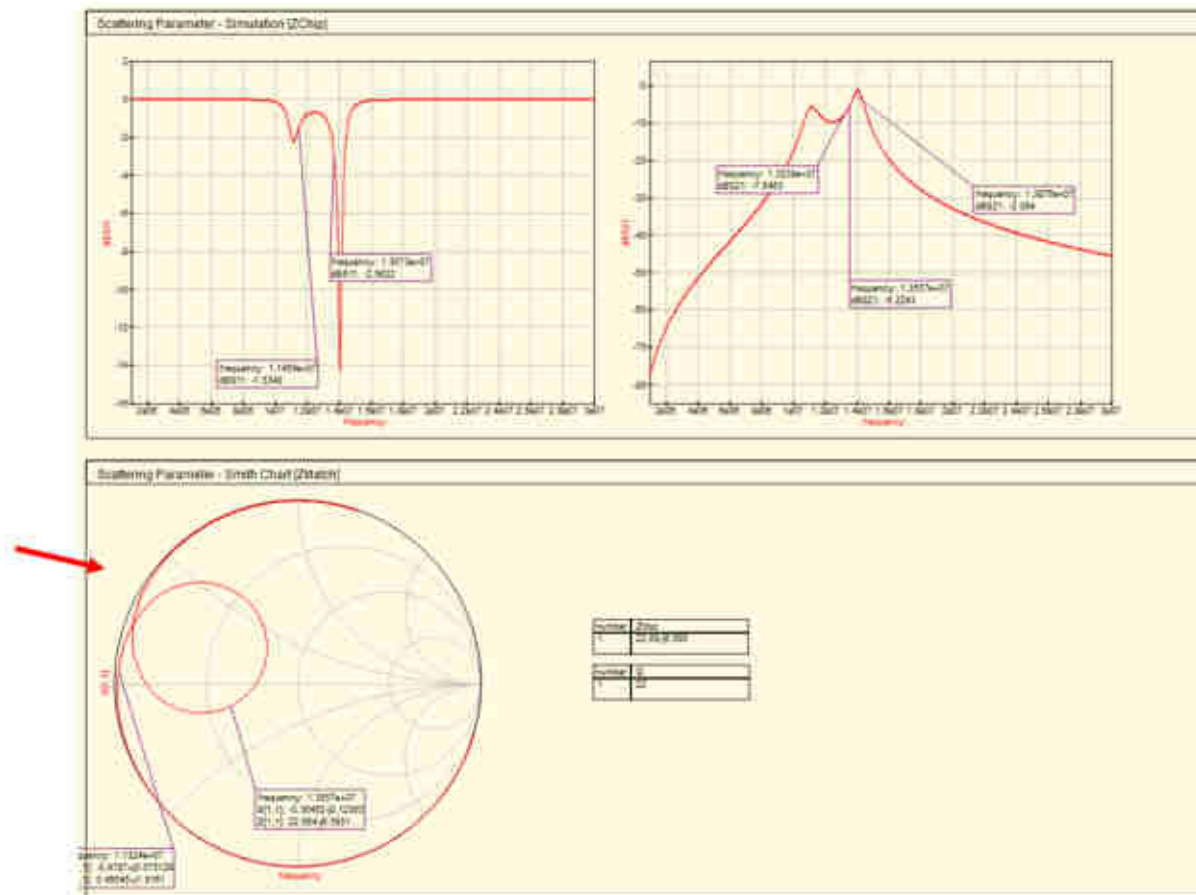
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Antenna Simulation

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Impedance
match info



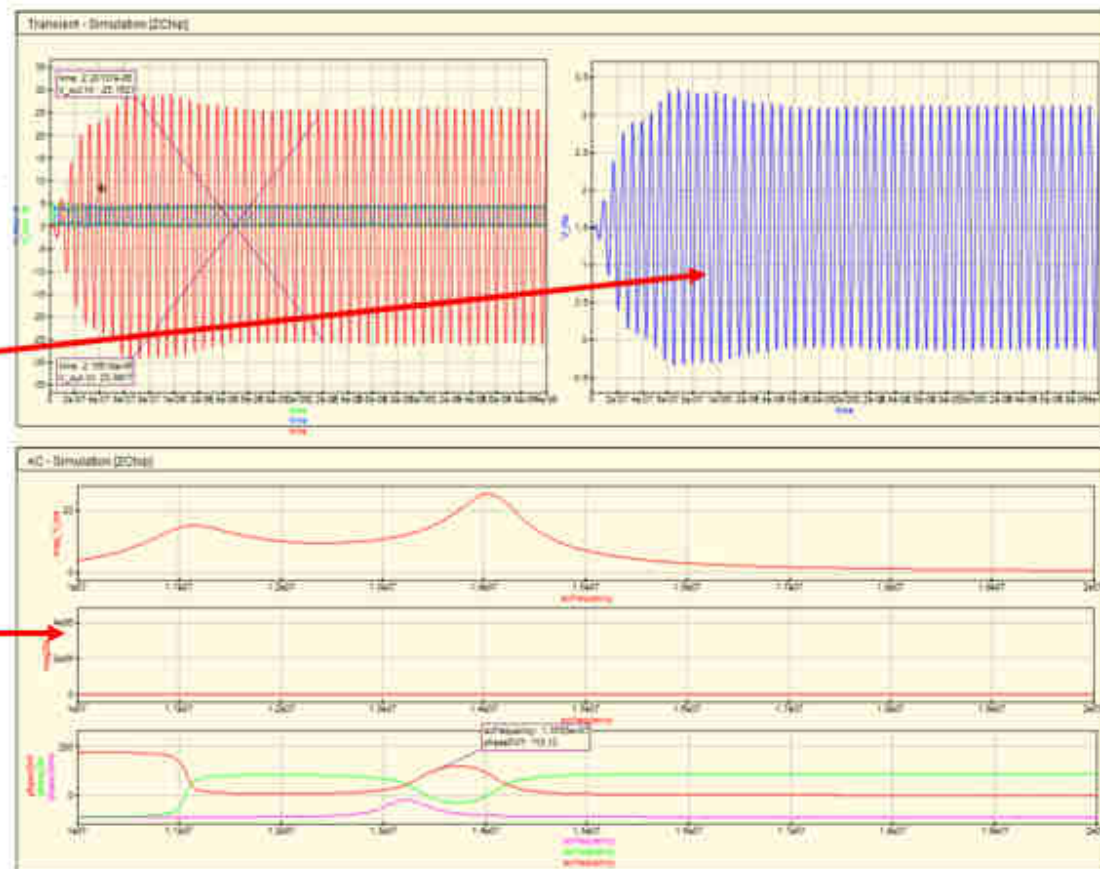
Antenna Simulation

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Antenna
voltage

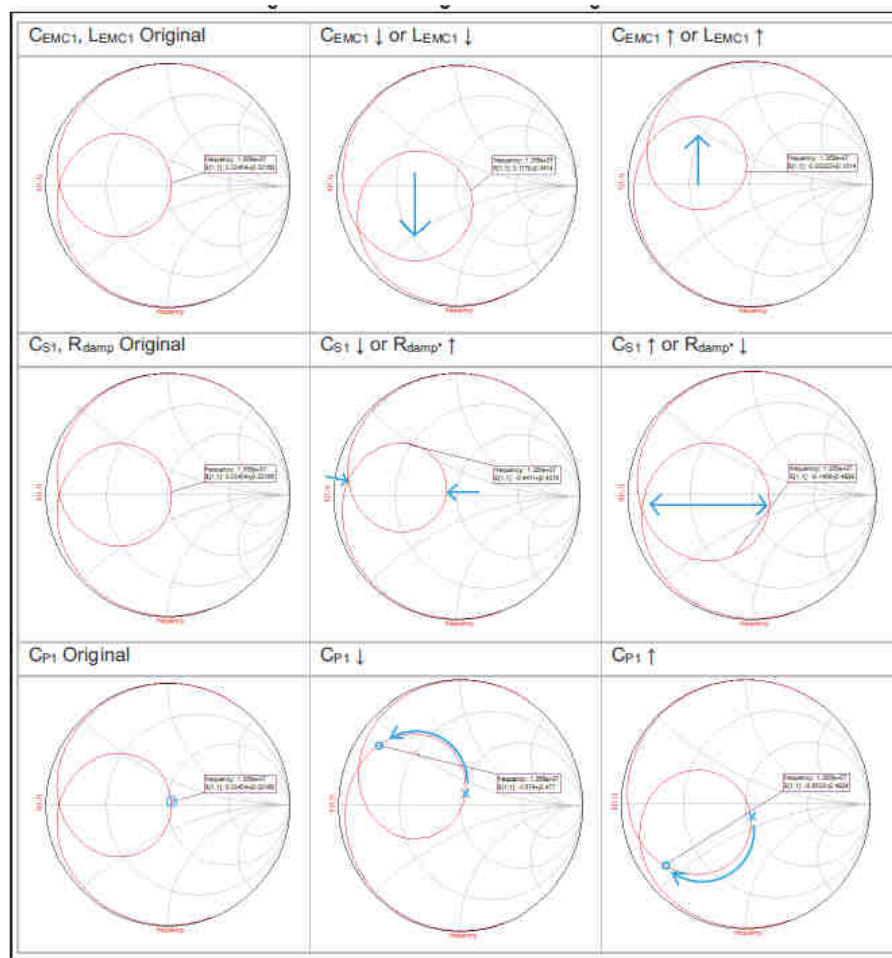
Receiver input

Phase and
Amplitude info



Fine Tuning

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EMC
Components

- Serial Cap
- Damping Resistor

Parallel Cap

Next Steps

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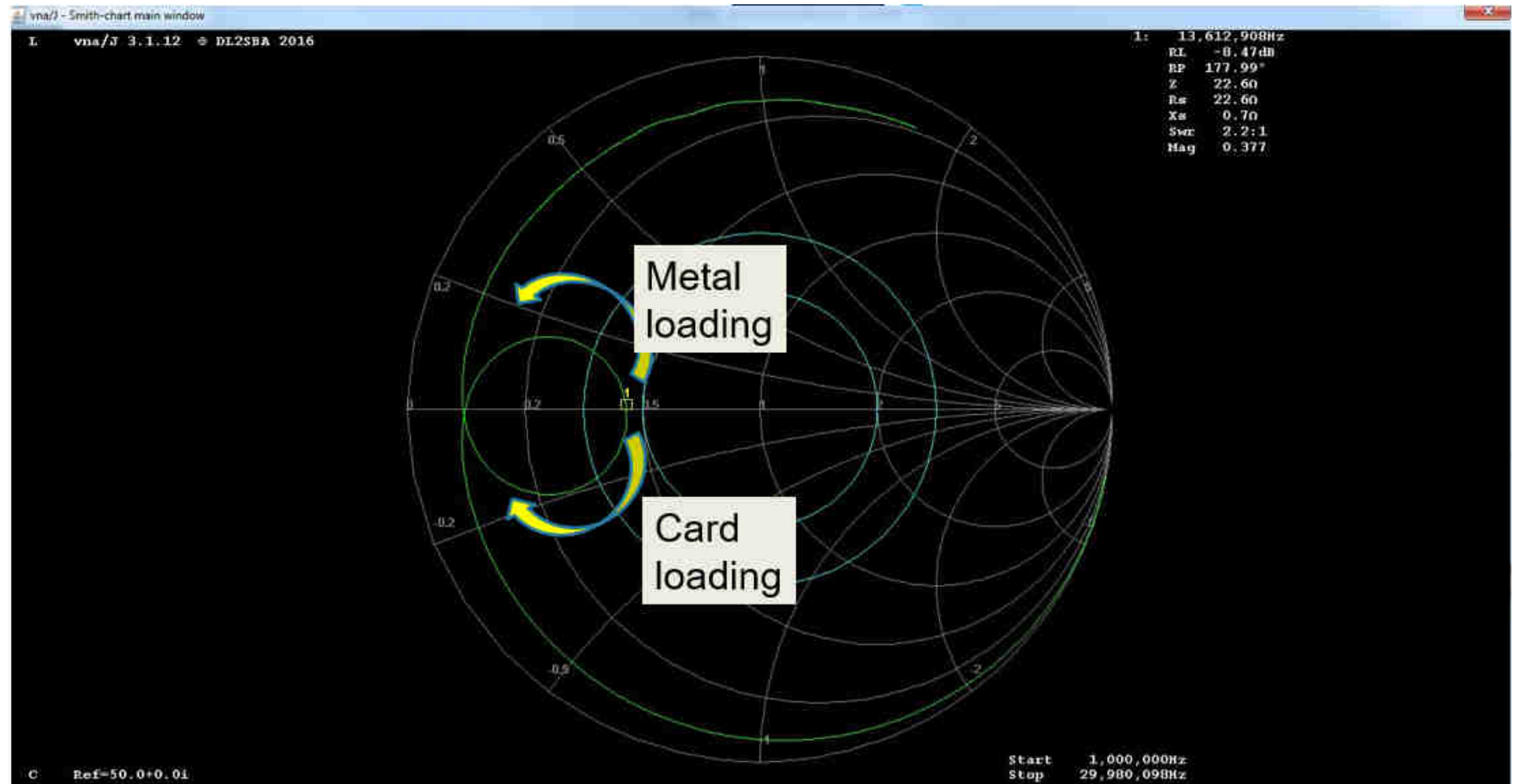
- Populate values on circuit board
- Measure match on RFO pins with VNA
- Re-adjust values as required
- Test
- Optimize read range vs current consumption

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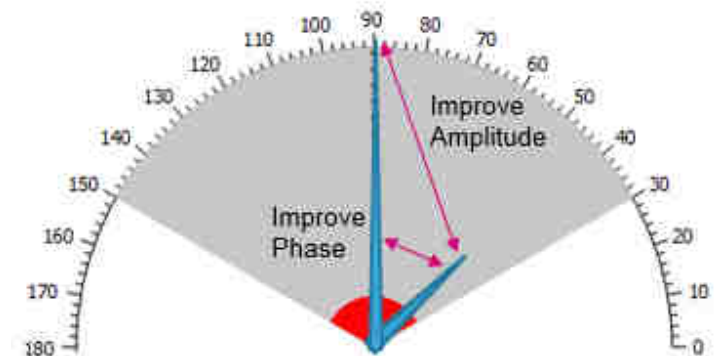


Antenna Loading

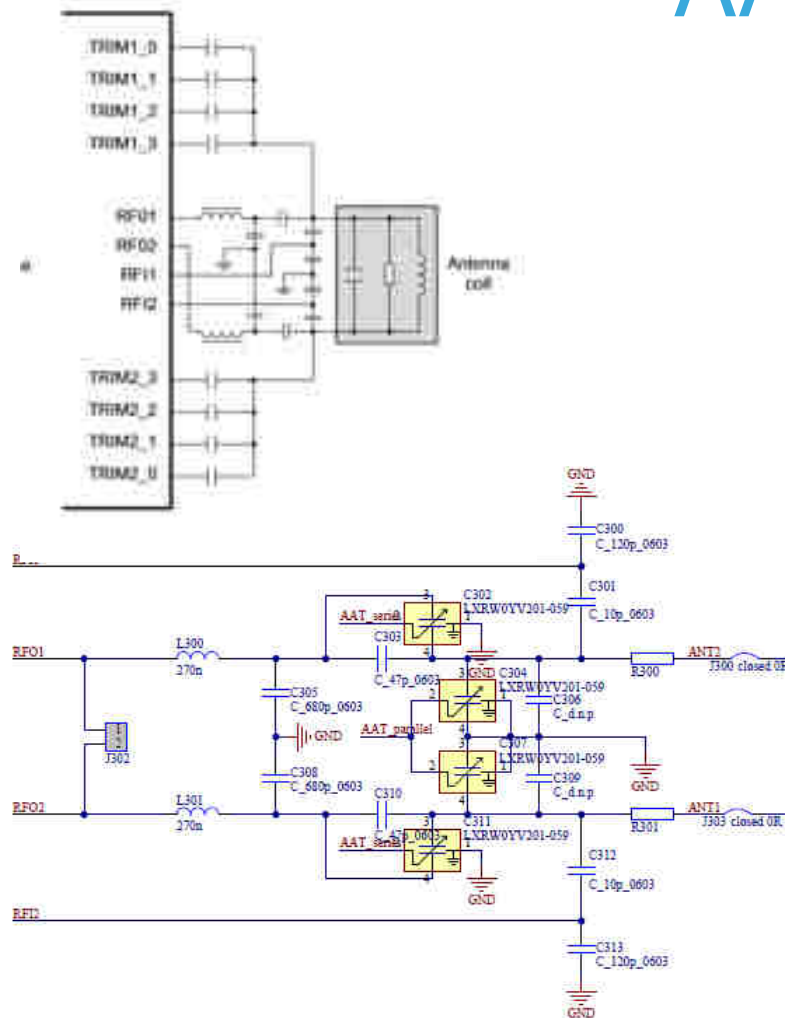
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- Automatic Antenna Tuning
 - Allows the matching circuit to be adjusted on the fly
 - Adjustment range dependent on values used
 - Larger Values > Larger range > less granularity
 - Smaller Values > Smaller range > more granularity
 - Must be compensated for in the matching circuit



- ST25R3911B
 - 8 External Binary weighted capacitors (4 per RFO)
 - Switches internal to reader
- ST25R3916
 - Uses variable capacitors
 - Internal DAC's use to control variable capacitors
 - Can be used to control both Serial and Parallel Caps



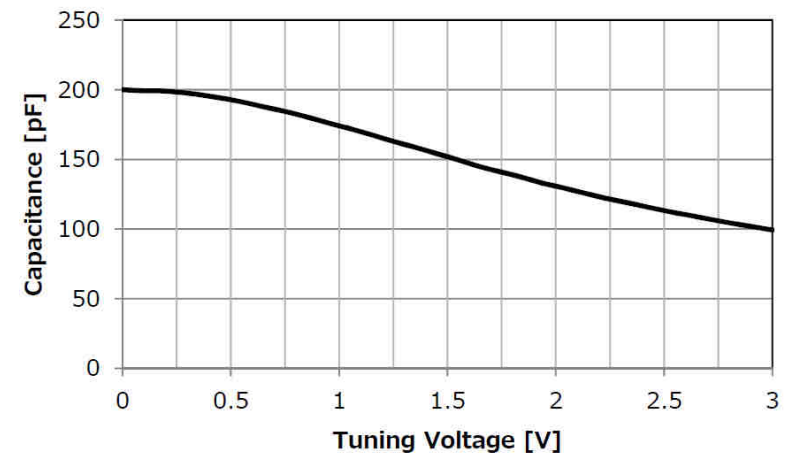
AAT Compensation

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- Match antenna as before
- Determine serial/parallel capacitors
- ST25R3916
 - Subtract $\frac{3}{4}$ Variable cap value from C_p
 - This becomes new parallel capacitor
- ST25R3911B
 - Subtract Highest trim value cap from C_p
 - This becomes new parallel capacitor



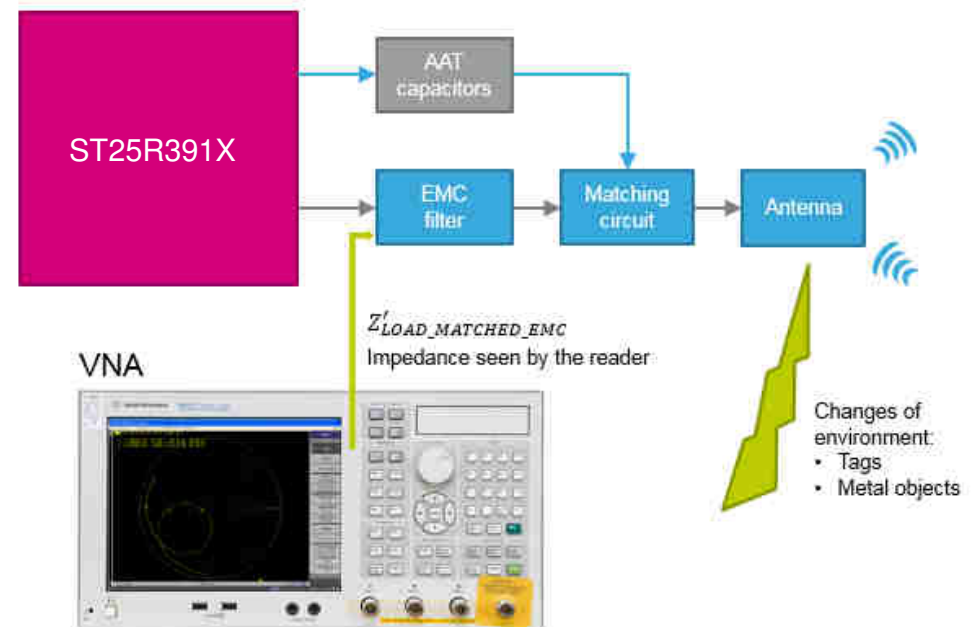
Capacitance characteristics (Typical)



- ST25R3911B
 - Set reg 27 to 0xff (double check that no field is being generated)
 - Adjust AAT trim to 8 (Antenna Tab in GUI)
 - Match should be in center of range
- ST25R3916
 - Set reg 28 to 0x7f (double check that no field is being generated)
 - Adjust AAT trim mid (Antenna Tab in GUI)
 - Match should be in center of range

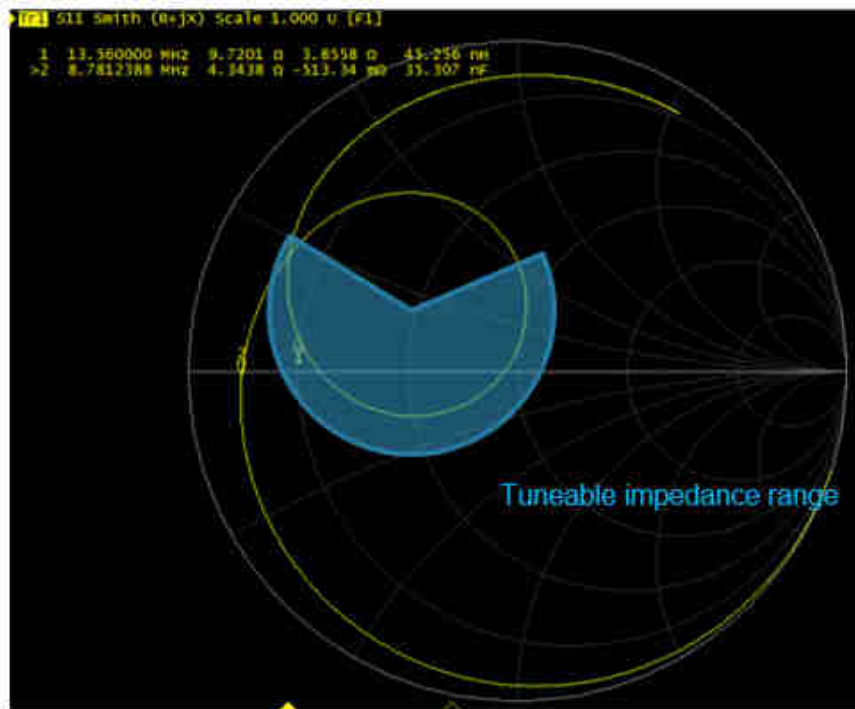
Important to turn off output drivers

- Measurement of how AAT changes the impedance of the antenna seen by the reader

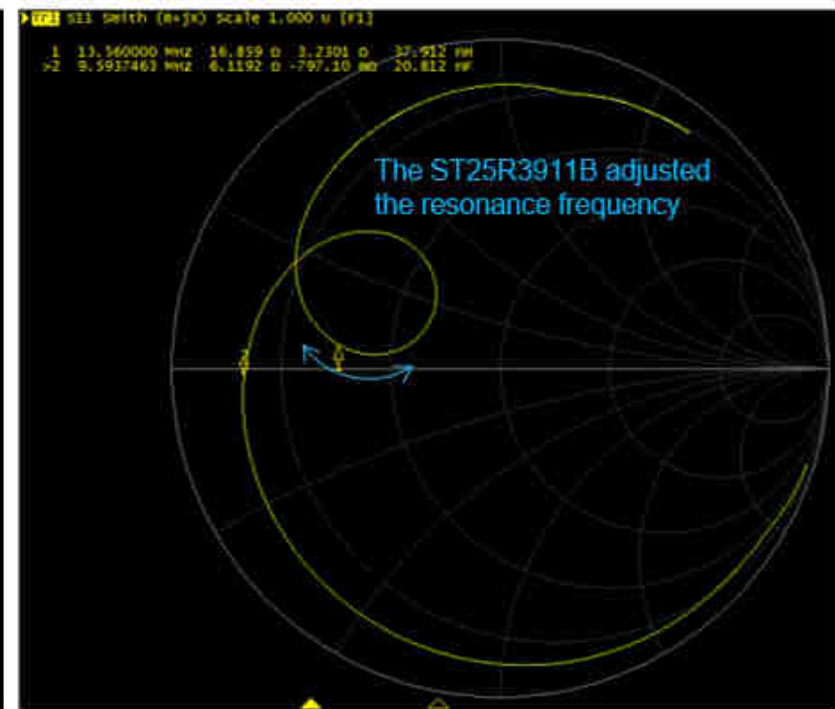


AAT Range

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ST25R3916



ST25R3911B

AAT Simulation 37

Simulations

ac simulation
 AC1
 Type=lin
 Start=1 MHz
 Stop=28 MHz
 Points=1001
 Noise=no

transient simulation
 TR1
 Type=lin
 Start=0
 Stop=4 us
 Points=1024

S parameter simulation
 SP1
 Type=lin
 Start=1 MHz
 Stop=30 MHz
 Points=1001

Antenna - Trim

Equation	Equation	Equation
Eqn10 trim3=56 p	Eqn9 Ctrimp3=1.5 p	Eqn8 Rontrim3=5e5
trim2=27 p	Ctrimp2=1.5 p	on = 14; off = 5e5
trim1=12 p	Ctrimp1=1.5 p	on = 25; off = 5e5
trim0=5.6 p	Ctrimp0=1.5 p	on = 50; off = 5e5
		on = 100; off = 5e5

Capacitive Voltage Divider

Equation
Eqn2
 $V_{rf} = V_{rf} \cdot V_t + 1.5$

Impedance Calculation

Equation
Eqn1
 $Z_{tocs} = \text{value}(\text{tocs}(S(1,1), P1, Z), 13500000)$

S-Parameter Equations

Equation	Equation
Eqn4 dBS11=dB(S(3,3))	Eqn24 myphase=phaseDiff
Eqn18 Cvxvalue(dBS21,max(dBS21))/(abs(xvalue(dBS21,3))-xvalue(dBS21,max(dBS21))))*(2)	

Antenna - Trim

Equation	Equation	Equation
Eqn10 trim3=56 p	Eqn9 Ctrimp3=1.5 p	Eqn8 Rontrim3=5e5
trim2=27 p	Ctrimp2=1.5 p	on = 14; off = 5e5
trim1=12 p	Ctrimp1=1.5 p	on = 25; off = 5e5
trim0=5.6 p	Ctrimp0=1.5 p	on = 50; off = 5e5
		on = 100; off = 5e5

Component-Values

Equation	Equation	Equation	Equation	Equation
Eqn17 Zmatch=50	Eqn20 Lemc1=220 n	Eqn22 Cs1=106 p	Eqn18 Cvdr1=10 p	Eqn23 Cant1=9.02 p
Zchip=3	RLemc1=0.3	Cp1=157 p	Cvdr2=150 p	Lant1=1000 n
Zchiphalf=1.5	Cemc1=749 p	Rdamp=0.45		Rant1=2863
AnalogSupplyVoltage=4.5				

S-Parameter [ZMatch]

Source: P1, Num=1, P=27 dBm

EMC Filter: C57 C=Cemc1, R87 R=RLemc1, L23 L=Lemc1, C8 C=C, C9 C=C, R88 R=RLemc1, L22 L=Lemc1, C56 C=Cemc1

Match: C74 C=Cp1, C16 C=Cvdr2, R1, R9, R10, R11

Layout Suggestions

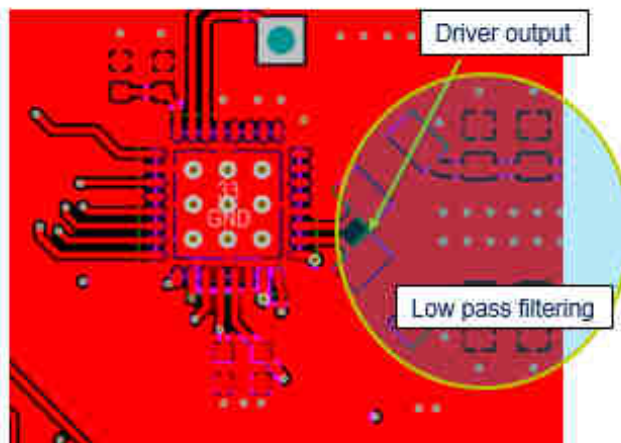
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- 4 layer board if possible (Sig/GND/PWR/Sig)
- Make RFO paths symmetrical
- Keep traces short
- EMC filter as close as possible to RFO pins
- Layout extra pads for Cs and Cp for fine tuning
- Layout pads for AAT (just in case)

Layout Suggestions

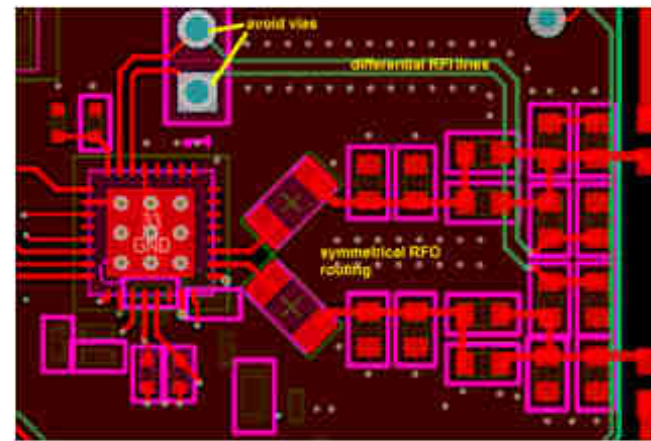
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EMC filter



- Filter must be positioned as close as possible to the output stages

RFO & RFI routing

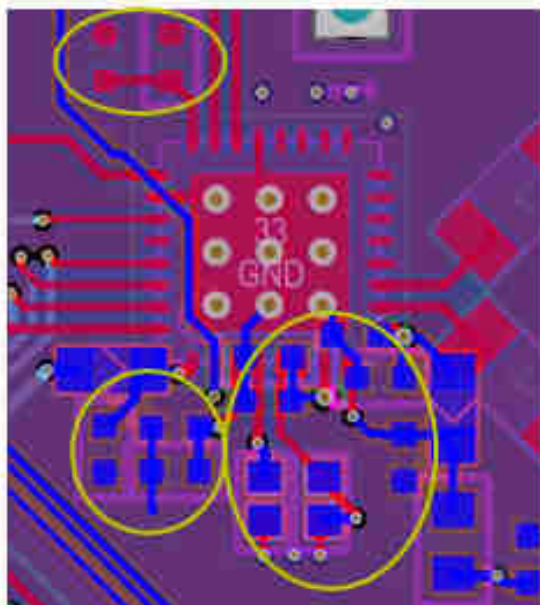


- The inductors after the RFO are placed in 90 degree direction
- The RFI lines are routed symmetrically, but in a fair distance to the RFO lines
- No long signal traces between LC filter and the remaining matching components
- The vias in the RFI lines should be avoided in a final design

Layout Suggestions

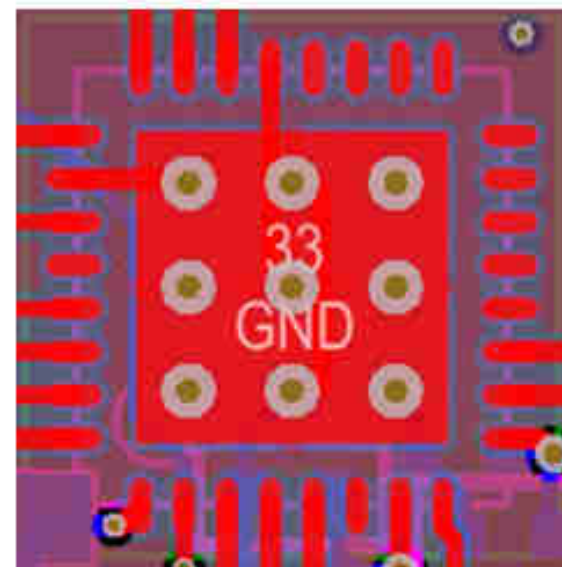
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Decoupling



- Capacitors as close as possible to the chip
- Parallel capacitors 2.2 μ F and 10 nF

Thermal pad



- Ground plane & thermal heatsink
- Multiple through vias must be used

Questions?

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