Digital power control with STNRG011

Digital Combo PFC+LLC Controller

High Integration for Efficient Digital SMPS Design

Complete Evaluation Ecosystem

Advanced Power Supply Control Topics
STNRG Provides a Complete Offline Digital Controller Solution

**Highlights**

- On chip HV Half Bridge and PFC drivers
- Complete set of PFC and LLC protections
- UART interface for monitoring functions and black box recording
Highly integrated digital SMPS controller

STNRG011 KEY FEATURES:

• 800V start-up circuit, line sense and Xcap discharge integration
• On chip HV Half Bridge and PFC drivers
• FTP memory for parameters customization
• Complete set of PFC and LLC protections
• UART interface for monitoring functions and black box recording
• Very low no load consumption (<100 mW)
• Ramp Enhanced Constant-On-Time (RECOT) multimode PFC and Time Shift LLC controllers
• Enhanced burst mode

KEY BENEFITS:

• Flexible, ROM based solutions
• Smooth transition from analog to digital SMPS
• High efficiency, low BOM count
• Excellent no load consumption (<100 mW)
High integration for efficient digital SMPS design

Integrated Digital Combo Controller Ideal for 90W to 300W SMPSs

Highlights

- Integrated digital control of HV AC/DC converter
- Low distortion front-end PFC controller
- Efficient LLC converter controller
On Chip HV&LV Drivers with 1A Peak Current
- Embedded 8-bit Core with 60MHz Clock
- 10 bit ADC with 15MHz clock, 1.5us Sampling Time
- Programmable State Machine for PWM Generation
- NVM Memory to Program Application Parameters
- UART&I2C Communication Interface

Digital COMBO PFC + LLC Control

Integrated digital control of HV AC/DC converter
Power Factor Correction Controller

- Digitally managed
  - Vout is converted through the ADC
  - Digital PI for voltage regulation
  - 2 coupled SMEDs generate the PWM signal

- Ramp Enhanced Constant On Time with 2 speed loop
  - Allows achieving very good PF & THD and dynamics
  - Ramp compensates input capacitive currents for high PF

- Multi mode operation
  - TM @ medium / high loads
  - TM, Valley skipping & skipping area @ low load
  - Burst mode @ very low load

PFC Control Structure
Efficient LLC converter controller

Resonant Controller

• LLC Control managed in Mixed Mode
  • Compensation done on secondary side
  • ADC samples opto feedback
  • 2 coupled SMEDs generate the PWM signal
  • The internal core calculates the Time Shift

• Time Shift control
  • Improved dynamic performance
  • Easy compensation
  • Great input voltage ripple rejection (> 50dB)

• Advanced features & protections
  • Safe start
  • Anti Capacitive Protection
  • Over Current management
  • Burst Mode Operation driven by LLC
available with a complete evaluation platform

Complete hardware and software solution

Highlights

• Hardware evaluation platform
• Comprehensive software tools
• Compliance through innovative digital control
A Complete set of tools is available to ease design and test

150W-12V adapter based on STNRG011 and SRK2001

GUI interface for easier configurability

STNRG011 Samples available Board prototype available

Maximum efficiency: state of the art algorithms for PCF & LLC
Communication: programmability and data monitoring
Fully Integrated solution: HV start-up & drivers

Industrial PSU
Alinco-Cone
High power adaptors
A complete development ecosystem

• INTERFACE board
  • Connect the STNRG011 board communication connector with the PC USB port
    • Converts the UART and I2C of STNRG011 to USB protocol
    • Provides electrical insulation between PC and board under test
    • Provides Vcc to STNRG011 to enable ATE mode and to program E2PROM chip

• PC GUI
  • Manages NVM reading and programming (ATE mode)
    • To manage E2PROM read & write
    • Read back real-time performance data
    • To communicate with the IC during operation
Adjust parameters with digital control

- **PROTECTIONS**
  - Protections behavior (latch / auto restart)
  - Protections levels & timings
- **COMPARATORS** filtering & hysteresis
- **PFC**
  - PFC soft start
  - PFC loop compensation
  - PFC light load behavior
  - PFC RECOT parameters (on the fly THD adjustment)
  - PFC maximum frequency
  - PFC nominal, minimum (UVP) and maximum (OVP) output voltages
- **LLC**
  - LLC dead-time
  - LLC safe start & soft start parameters
- **BURST mode operation**
  - in/out thresholds
  - Burst pulses definition
150W-12V SMPS schematic
150W platform meets global efficiency standards

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Advanced digital control topics

High efficiency through high performance control algorithms

Highlights

• High level system architecture
• Power factor correction details
• LLC converter technical details
STNRG011 architecture and pinout
## Power Factor Correction overview

<table>
<thead>
<tr>
<th>KEY features</th>
<th>Algorithms &amp; Operations</th>
</tr>
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</table>
| - PFC LV LS driver integrated  
  - Up to 20V  
  - 1A Peak Current Drive Capability  
- Integrated HV start up & HV sense for AC line sense  
- AC disconnection detection & Xcap discharge  
- Brown out detection  
- Surge detection  | - Ramp Enhanced Constant On Time (ST patented) with 2 speed loop  
  - Very good PF, THD and dynamic performance  
  - New “Ramp” compensation (patented): compensate input capacitive loads to achieve highest PF  
- Multi mode operation  
  - TM at medium / high loads  
  - TM, Valley skipping & Skipping Area at low load  
  - Burst Mode at very low load |
• **PFC control loop** is managed **digitally**
  
  - Vout is converted through the ADC
  - Compensation is done with a PI filter (calculation made by the core)
  - 2 coupled SMEDs generates the PWM signal

\[
i_m(t) \approx I = \frac{v_{AC} \times t_{ON}}{2L} \tag{1}
\]
Power Factor Correction details: eCOT

- Considerable reduction of the cross-over distortion with enhanced COT:
  - Current level ($I_{TH}$) defines the start of the Ton period
  - Compensation of the energy lost in MOS charging
  - More effective energy transfer when the instantaneous line voltage is very low.
  - Using eCOT is it possible to join the benefit of COT and TM:
    - Easy implementation
    - Low switching losses
    - High PF & THD

\[ I_{in} \approx V_{inpk} \cdot \sin \theta \cdot \frac{T_{ON}}{2} \cdot L - I_{neg} \] (2)

\[ I_{in} = V_{inpk} \cdot \sin \theta \cdot \frac{T_{ON}}{2L} + V_{inpk} \cdot \sin \theta \cdot \sqrt{\frac{\text{Coss}}{L}} - V_{o} \sqrt{\text{Coss}} \] (3)

\[ I_{TH} = V_{o} \cdot \sqrt{\frac{\text{Coss}}{L}} \] (4)

\[ I_{in} \approx V_{inpk} \cdot \sin \theta \cdot \frac{T_{ON}}{2} \cdot L - I_{neg} + I_{TH} \] (5)

\[ I_{in} \approx V_{inpk} \cdot \sin \theta \cdot \frac{T_{ON}}{2} \cdot L - I_{neg} + V_{inpk} \cdot \sin \theta \cdot \sqrt{\frac{\text{Coss}}{L}} \] (6)

\[ I_{in} \approx K \cdot V_{inpk} \cdot \sin \theta \] (7)
Ramp eCOT allows compensating reactive energy (current) generated by big input filtering capacitor.

All PFCs have one or more capacitors to filter current ripple.

Capacitor current is 90° out of phase.
  - Power factor and distortion are impacted.

PFC details: recot 1/2
ReCOT implementation concept.
PFC details: multimode operation

- PFC uses valley skipping to switch between TM, valley skipping & skipping area and DCM

Max load ➔ TM

Mid load ➔ valley skipping

Low load ➔ Skipping area
### LLC resonant converter features

<table>
<thead>
<tr>
<th>KEY features</th>
<th>Algorithms &amp; Operations</th>
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<tbody>
<tr>
<td>LLC HV Half Bridge drivers integrated</td>
<td></td>
</tr>
<tr>
<td>* Up to 600 V</td>
<td></td>
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<tr>
<td>* 1 A Peak current drive capability</td>
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<tr>
<td>Matched propagation delays between both channels</td>
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<tr>
<td>dV/dt immunity ± 50 V/ns</td>
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</tr>
<tr>
<td>Advanced features &amp; protections</td>
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</tr>
<tr>
<td>* Safe start</td>
<td></td>
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<tr>
<td>* Anti Capacitive Protection</td>
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<tr>
<td>* Over Current management</td>
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<tr>
<td>Time-shift control (ST patented)</td>
<td></td>
</tr>
<tr>
<td>* Improved dynamic performance</td>
<td></td>
</tr>
<tr>
<td>* Easy compensation</td>
<td></td>
</tr>
<tr>
<td>* Great input voltage ripple rejection (&gt; 50 dB)</td>
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<tr>
<td>Burst Mode operation</td>
<td></td>
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<tr>
<td>* LLC drives burst mode operation</td>
<td></td>
</tr>
<tr>
<td>* Fixed burst packet with soft start / stop for reduced acoustic noise</td>
<td></td>
</tr>
<tr>
<td>* Most of the circuitry is turned off during no switching periods, I_{cc} = 500 , \mu A</td>
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LLC details: time shift algorithm

- Time-shift $T_D$ is defined as **time elapsing from zero-crossing of tank current to next half-bridge toggling**
- A relationship exists between $T_D$ and tank current phase-shift $\Phi_Y$: $\Phi_Y = 180°\left(1 - 2\frac{T_D}{T_{SW}}\right)$
- PWM is toggled after $T_D$ has elapsed from tank current zero crossing
- $T_D$ is calculated by $\mu$C based on ADC reading from FB
• **LLC control loop is managed in mixed mode**
  • Compensation is done at secondary side with standard analog circuitry
  • The information from the optocoupler is sampled with the ADC
  • The core calculates the time shift and the SMEDs generates the HS & LS PWM
LLC details: time shift benefits vs DFC

- TSC makes LLC resonant converter dynamics very close to that of a first-order system
- Frequency compensation is much easier
- Response to perturbations is overdamped
- TSC improves load transient response
- Overshoots and undershoots are nearly halved
- Settling time is reduced 3-4 times
- TSC improves input ripple rejection
- 100 Hz gain can be increased considerably
- Rejection ratio increases by more than 15 dB
- TSC prevents hard switching at start-up
- Converter reliability is improved
- Moreover STNRG011 implements the safe start: before the soft start the LVG is turned on for about 10 us order to discharge the resonant capacitor
LLC operation

- Safe start
- Full load start-up
- Full load steady state
- Min load steady state
LLC dynamic performance

Step load (min ↔ max) on main output

Mains freq ripple rejection ≈ 50dB