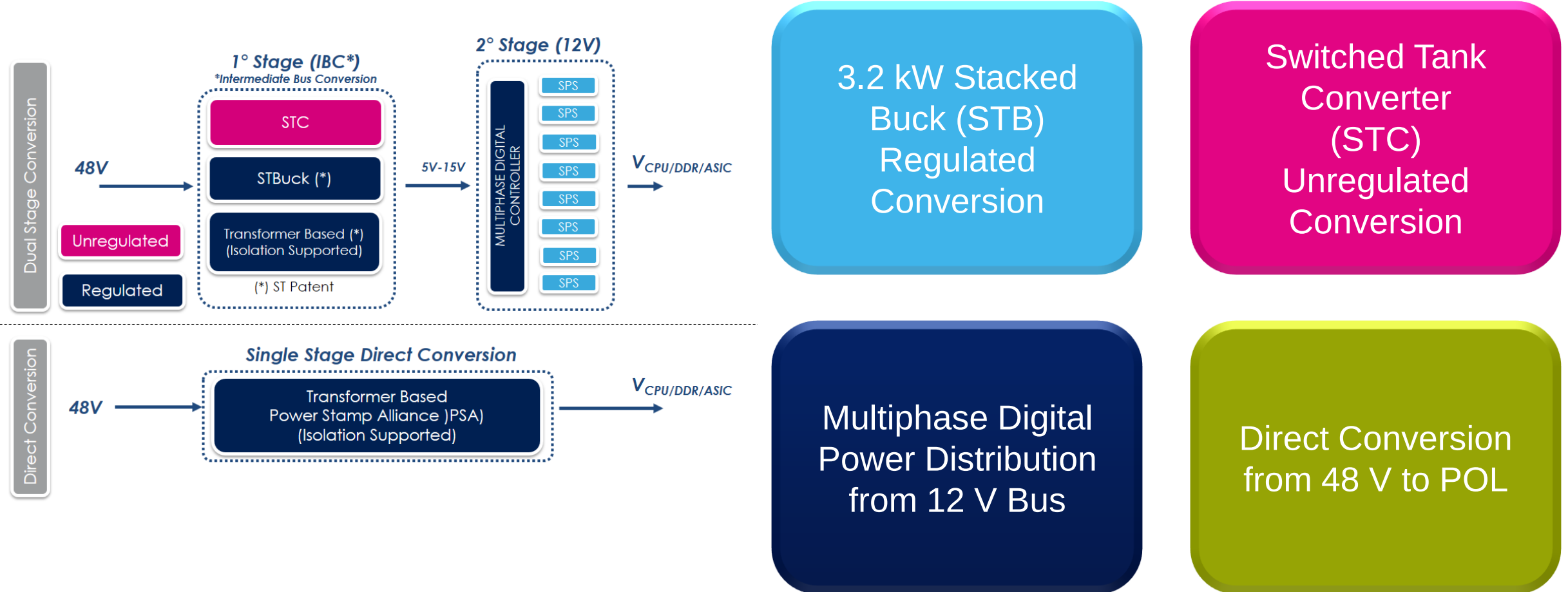
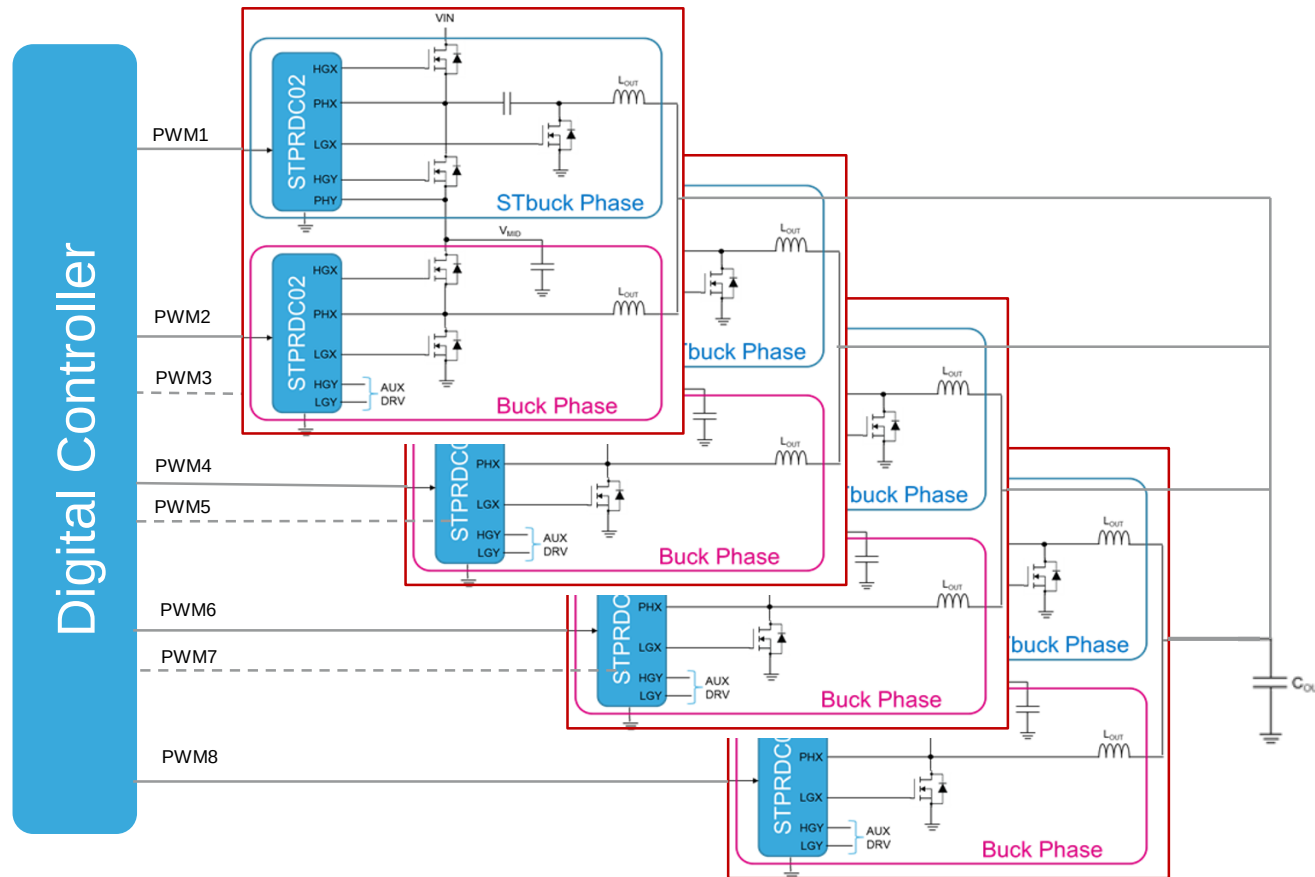


Power Delivery for Modern Data Center



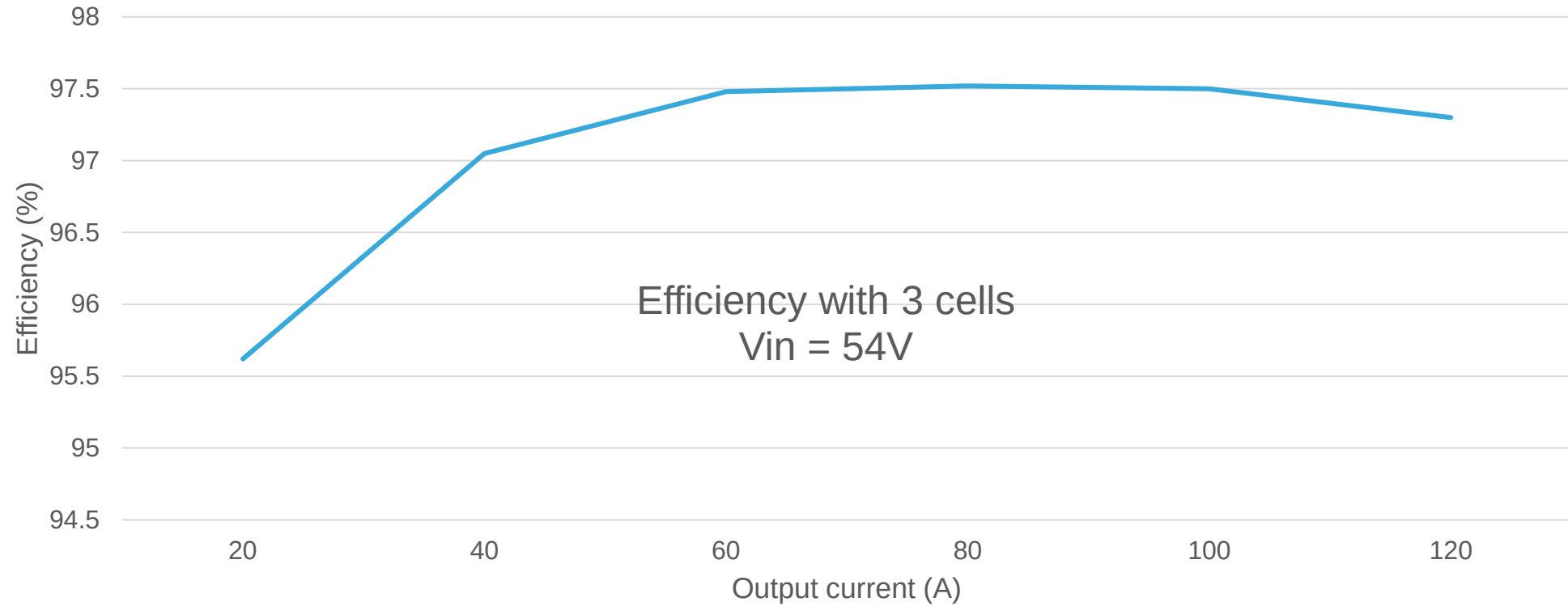
3.2KW Stacked Buck (STB) Regulated Conversion

Regulated Intermediate Bus Scalable Architecture up to 3.2 kW



- Input Voltage Range: 36 V-60 V
- 12V V_{OUT} Adjustable by PMBus
- 3.2 kW Regulated Power Delivery
- Four 800 W 1/8 Brick Form Factor Interleaved Cells
- Scalable Solution for Efficiency Optimization
- Off-the-Shelf Components
- PMBus Commands Compliant to Intel VR14
- Layout dedicated for Heat sink
- High Power Density:
 - 3 cells Size (3x4x1) Inches
 - 4 cells Size (3x5.3x1)Inches

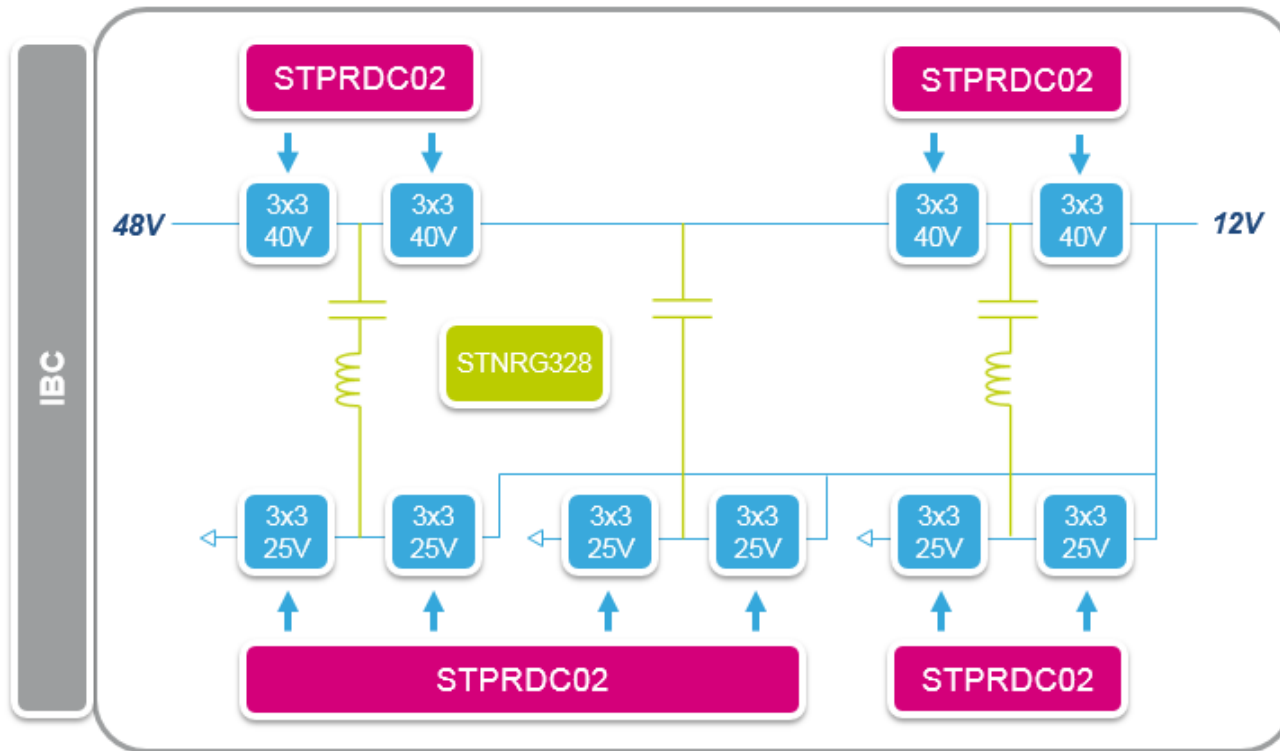
STB Efficiency Results



Switched Tank Converter (STC)

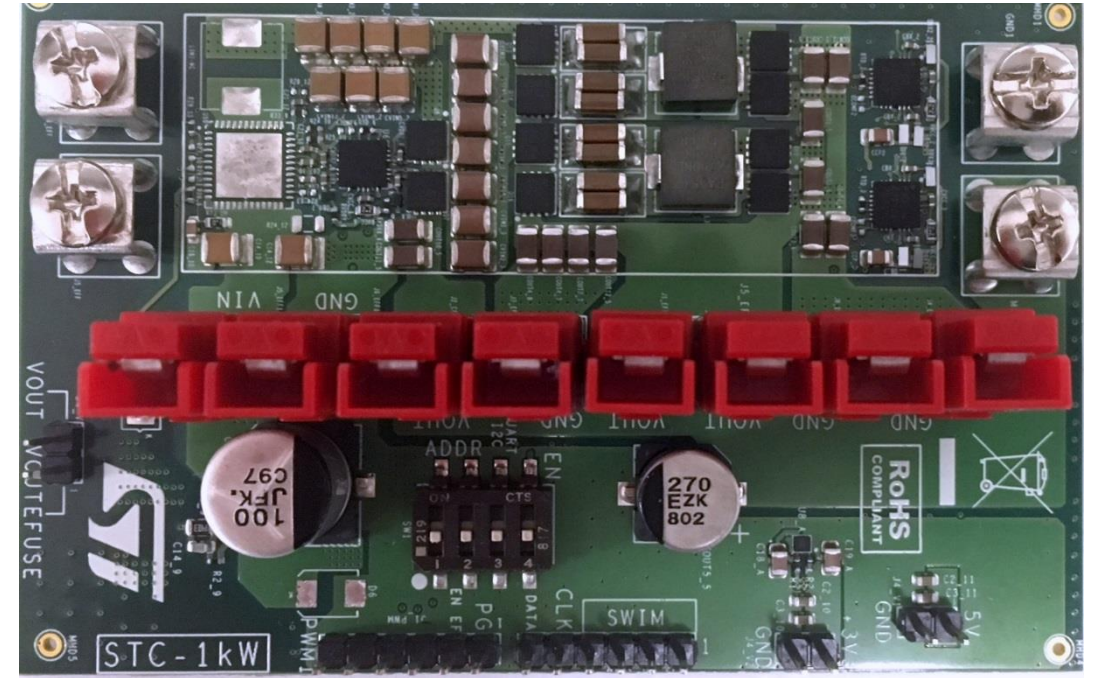
Unregulated Conversion

Un-Regulated Intermediate Bus Architecture up to 1 kW



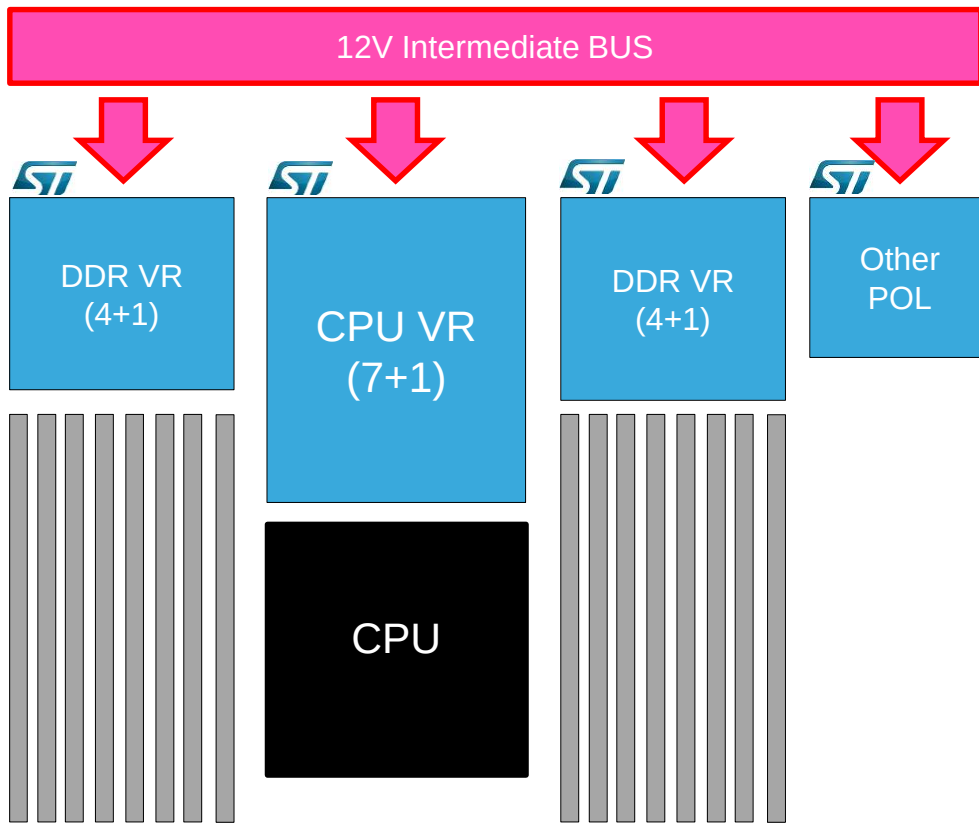
- Input Voltage Range: 40 V-60 V
- 4:1 Conversion Ratio
- Up to 1 kW Thermal Design Power (TDP)
- High Power Density
- Maximizes Conversion Efficiency
- Low Profile Solution (< 5 mm)
- ZCS Operation for all MOSFET
- Off-the-Shelf Components (X7R)

1 kW STC Efficiency Results



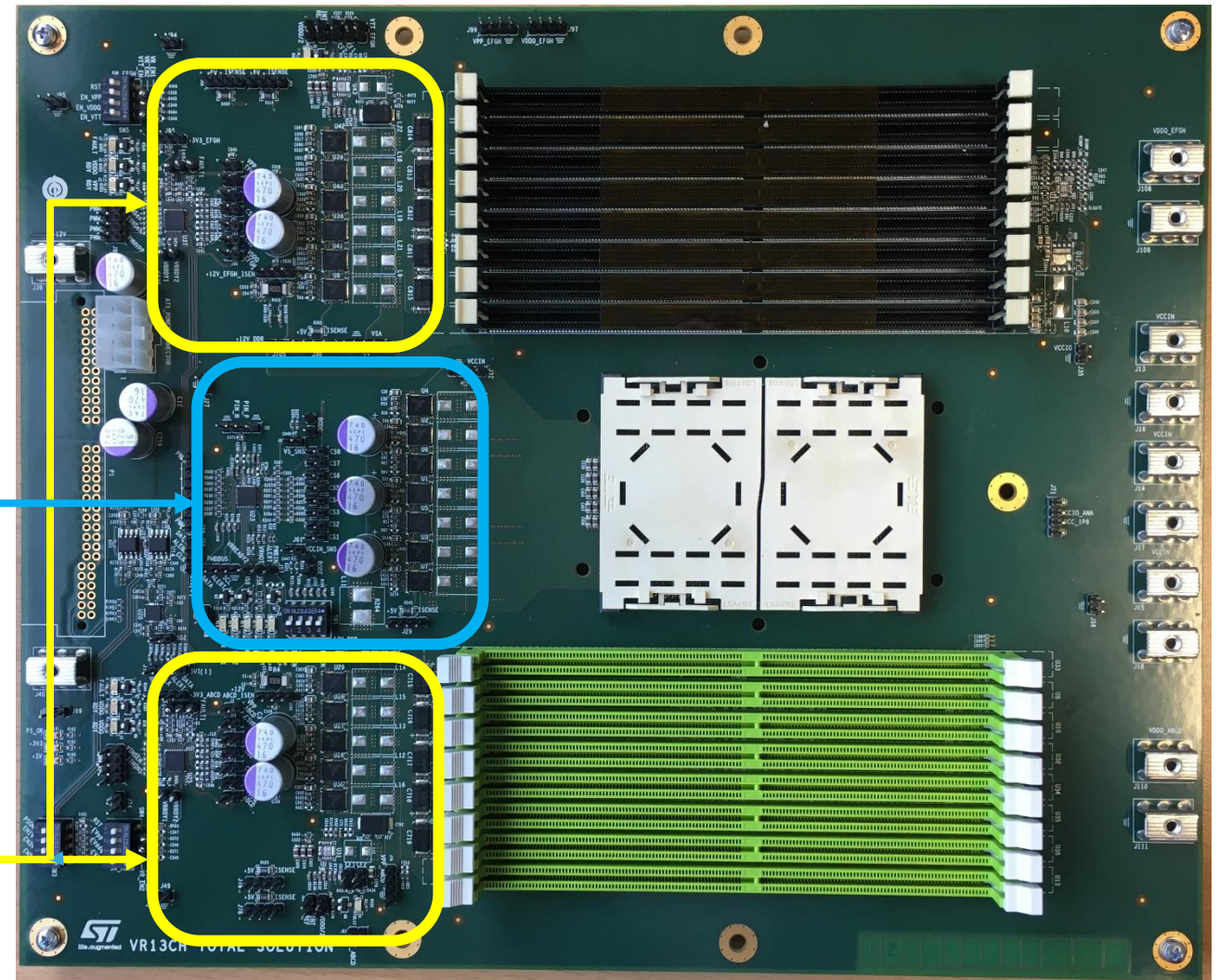
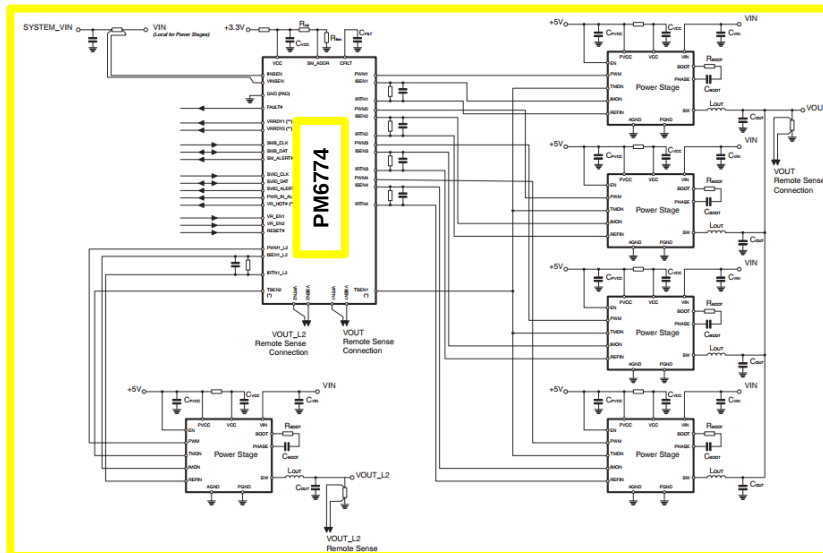
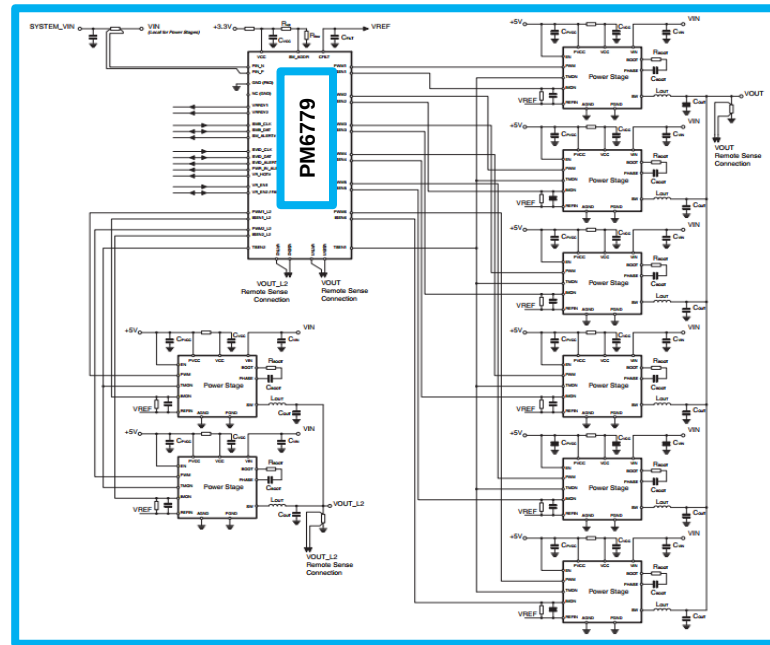
Multiphase Digital Power from 12 V Bus

Complete Multiphase Digital Solution for CPU and DDR



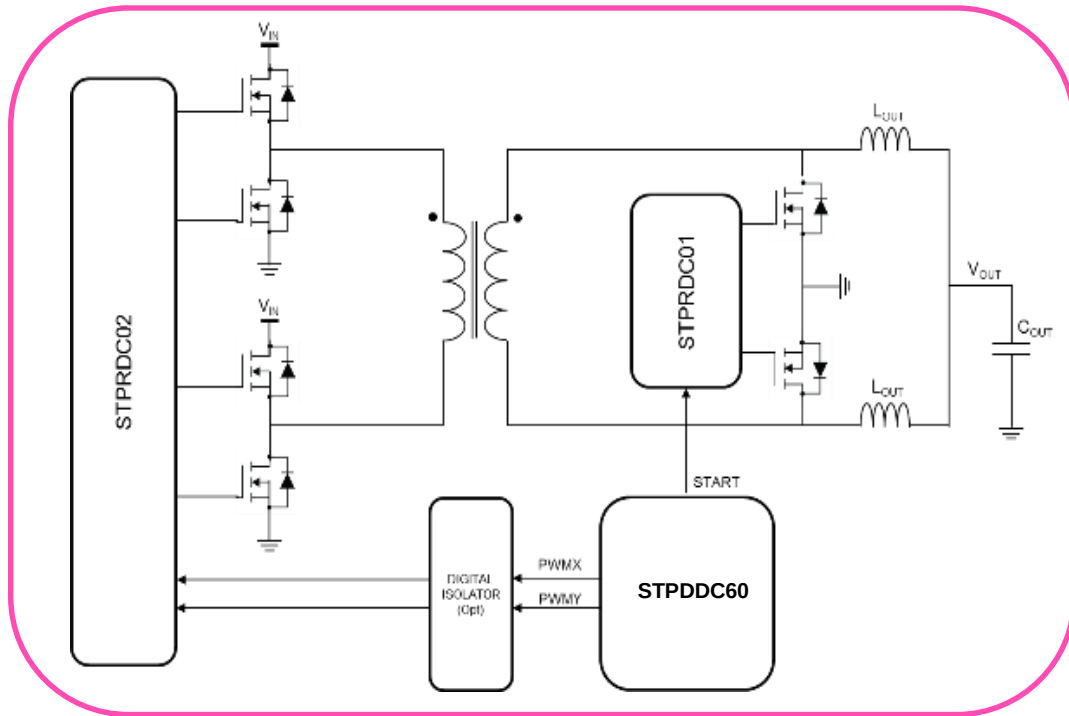
- 12 V Input Voltage, Vout range: 0.5 to 2.5 V
- CPU and DDR Power Distribution
- PMBus Rev1.2 at 400 kHz
- High-Performance Digital Control Loop (Digital STVCOT)
- Autonomous Dynamic Phase Shedding
- Remote Sense with $<0.5\%$ V_{OUT} Accuracy
- Current monitor signal with calibration
- Programmable Voltage Positioning
- OV, UV and FB Disconnection Protection

Intel VR13HC Complete Solution



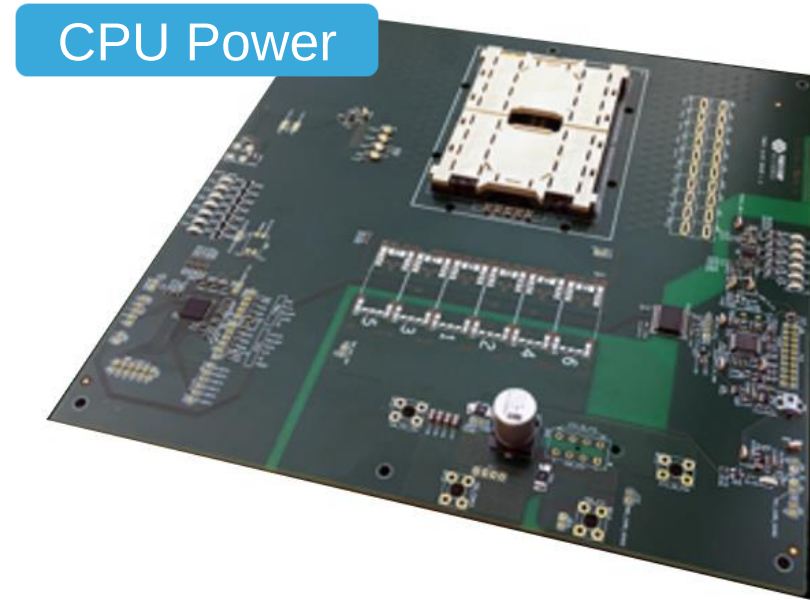
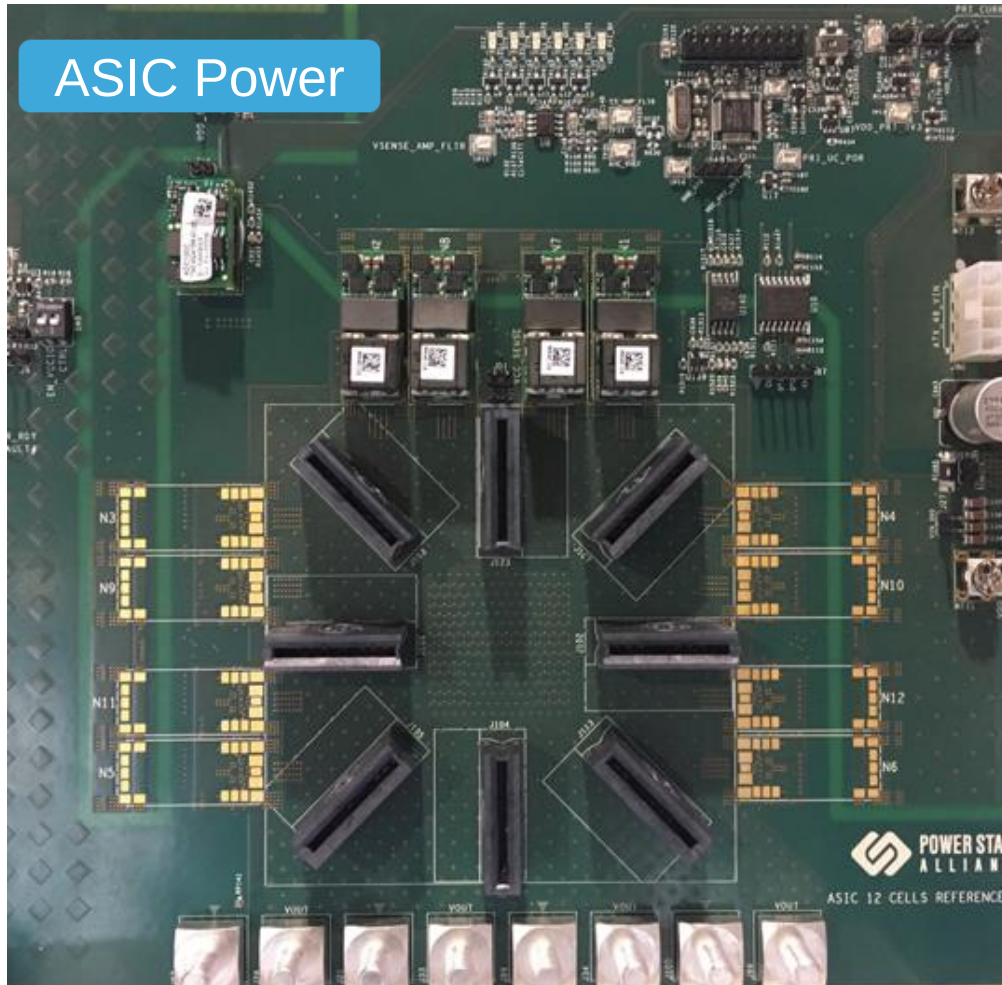
Direct Conversion from 48V to POL

Scalable, Flat Efficiency, High Density, Isolated or Non-Isolated Direct Conversion



- Input Voltage Range: 40 V-60 V
- Vout: Intel VR13HC (1.8 V_{Typ})
- Full Compliance to Intel Test Plan
- Vout Load Line: 0.9 mOhm
- 205 W TDP, 413 W Max
- Iout Max: 228 A
- Switching Frequency: 570 kHz
- Power Density: 100 W/inch²
- Solution Size: 1.6" x 2.60"

Multi-Cells Reference Designs



- 6 Cells Intel VR13 and VR13HC Compliant
- Up to 12 Interleaved Cells for ASIC (1200A Peak)
- 100 A/cell in (12.9 x 29 x 18)mm (W, L, H)
- Scalable Solution for Optimal Design
- Cell Shedding from Maximized Efficiency