Techday

Taiwan | 2023

OUR TECHNOLOGY STARTS WITH YOU

Sub-track II –
Power & Energy Presentation

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Digital power approach with STM32G4 in unidirectional/bidirectional totem pole PFC

Benson CHU
Power and Energy Competence Center, APeC & China
STMicroelectronics

Power & Energy
Competence
Center

Agenda

1 Unidirectional totem pole PFC solution

2 Bidirectional totem pole PFC solution

3 ST key products on solution

4 Takeaways

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Uni-directional totem pole PFC solution

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3 kW CCM totem pole PFC solution

Key features

- Input AC voltage: **90–264 VAC**
- DC output voltage: **400 VDC**
- Switching frequency: 70 70 kHz
- Operation mode: CCM
- Peak efficiency: **98.5%** @ 230 VAC
- Power Factor: **>0.98** @ 100% load
- iTHD: **<5%** @ 100% load
- Peak inrush current: **<30 A**

Key components

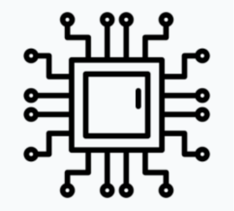
- STM32G474RBT (32-bit MCU)
- SCTW35N65G2V (SiC Gen2) → SGT40R65ALD (SiC Gen3)
- STGAP2D (gate driver)
- STW70N65DM6-4 (DM6 SJ MOS)
- VIPER26HD (Aux. SMPS)

Target application

Telecom & 5G PSU

Datacenter & Server PSU

Design material **Demo video**



(Key words on ST.COM STDES-3KWTPFC)

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PFC digital platform - STM32G474

Configurations of MCU key functions on digital PFC

Arm® Cortex® -M4 up to 170 MHz

Floating-point unit (FPU)

- Control loop computation (reserved for future use)

32-Kbyte **CCM-SRAM**

- Zero wait-state for critical code execution

CORDIC for trigonometric functions acceleration

- Software phase-locked loop (reserved for future use)

FMAC filter mathematical accelerator

- Hardware digital filter (CPU off-load) for loop computation

Hi-Resolution PWM Timer (184 ps)

- Mainly for high frequency (HF) MOSFET control at 70 kHz

Multiple **ADCs (4 Msps)** up to 5

- AC voltage, PFC voltage/current, and hotspot temperature sensing

Comparators and **DACs** up to 7

- PFC OVP and critical current protection

UART, **SPI**, **CAN** and **USB**

- UART for internal/external communication

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Totem pole PFC operation

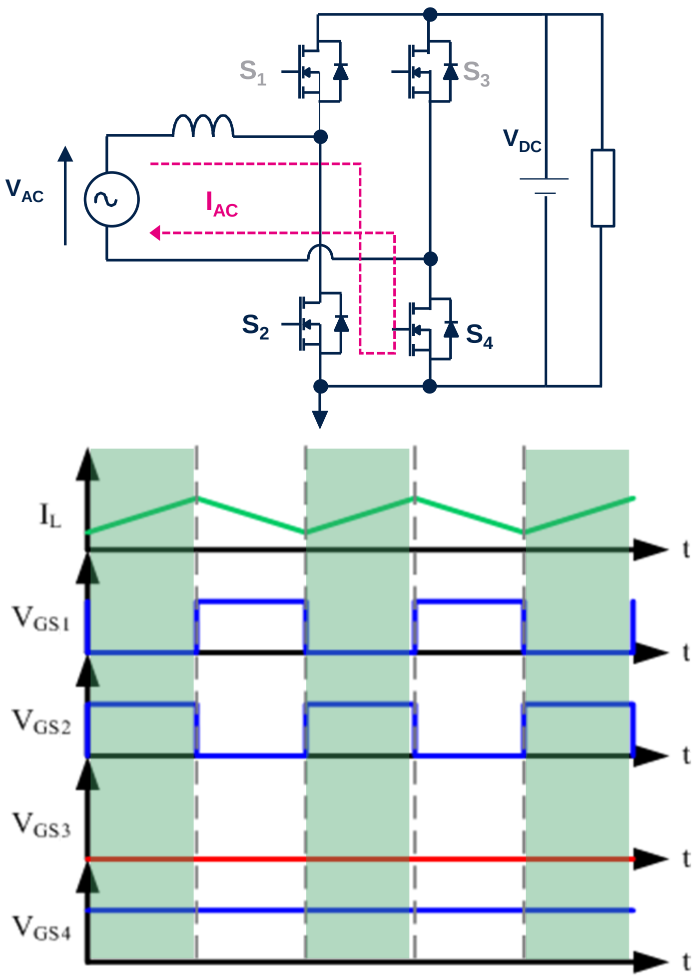
AC positive cycle (VAC > 0)

Major behavior

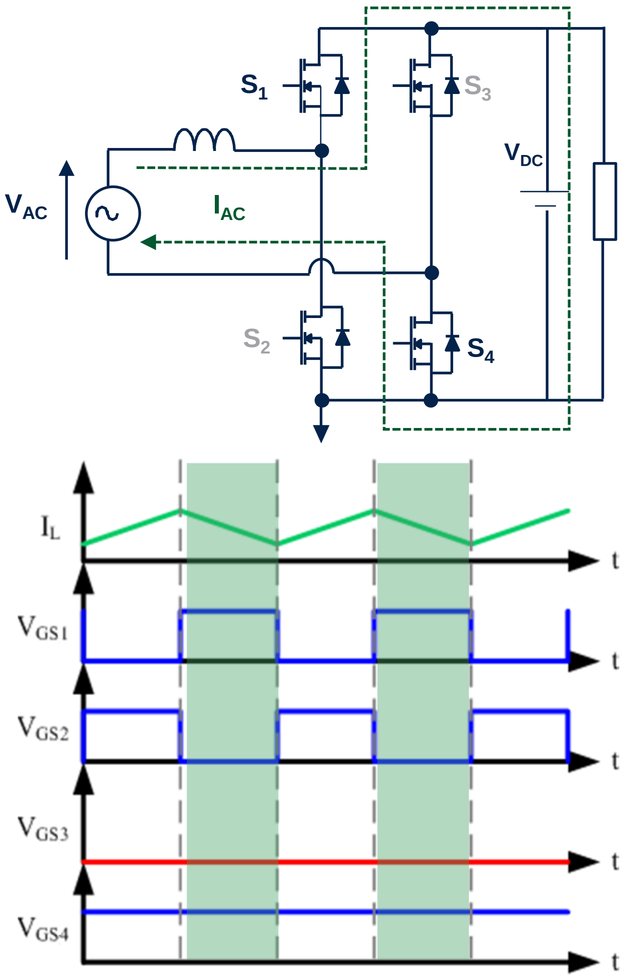
- **Active switch: S2** controls the input current to charge to PFC choke for making a sinusoidal waveform
- **Synchronous switch: S1** is the complementary switch that provides a path to discharge inductor current
- **Always-on switch: S4**
- **Always-off switch: S3**

- *S1, S2: High switching frequency*
- *S3, S4: Low switching frequency*

S2 on, inductor current charging



S2 off, inductor current discharging



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Totem pole PFC operation

AC positive cycle (VAC < 0)

Major behavior

- **Active switch: S1** controls the input current to charge to PFC choke for making a sinusoidal waveform
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- **Always-off switch: S4**

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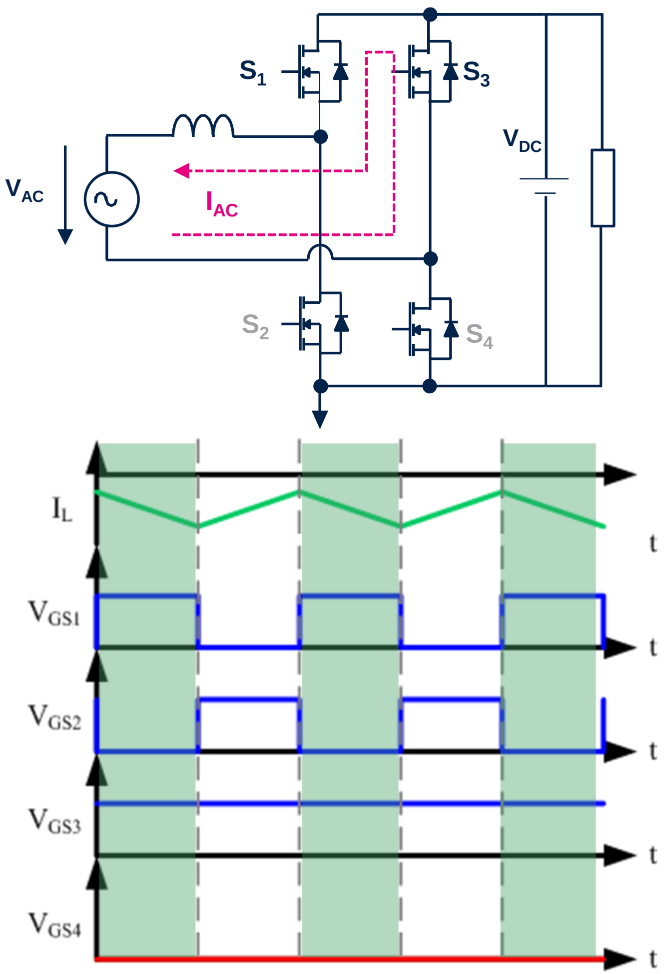
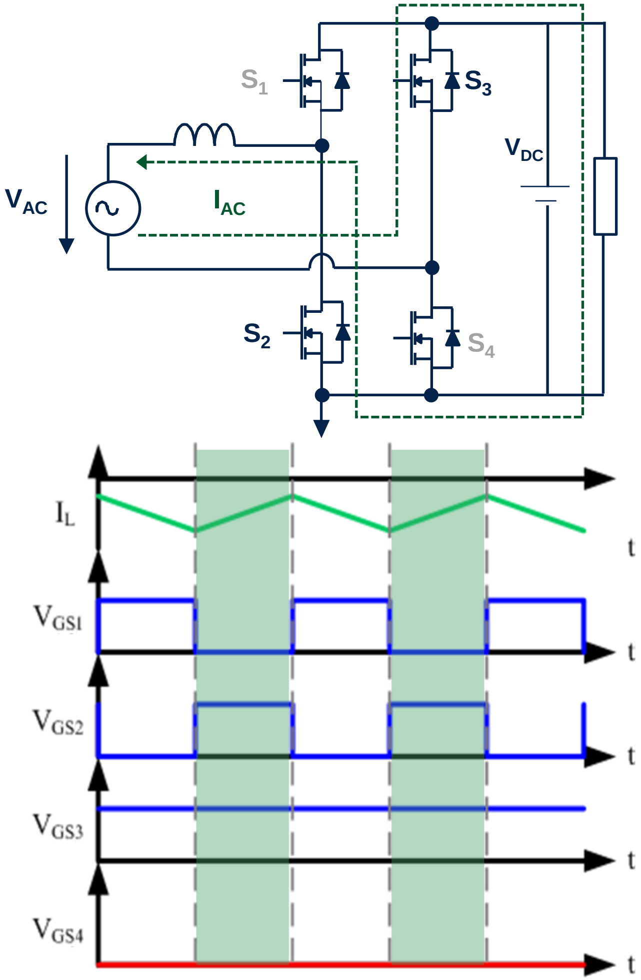
- *S3, S4: Low switching frequency*

S1 on, inductor current charging



S1 off, inductor current discharging



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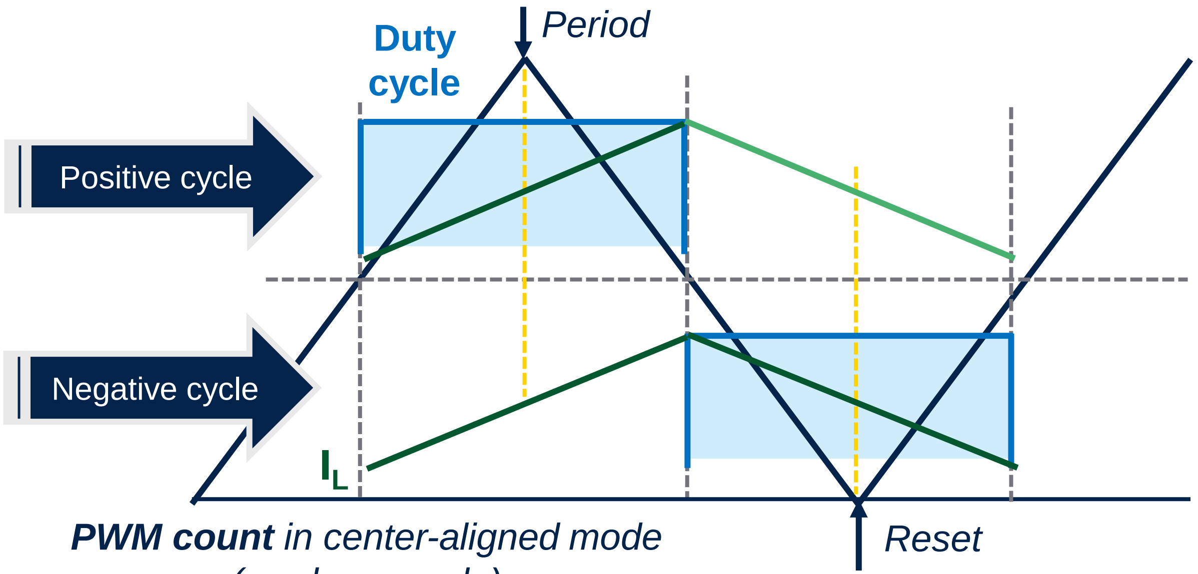
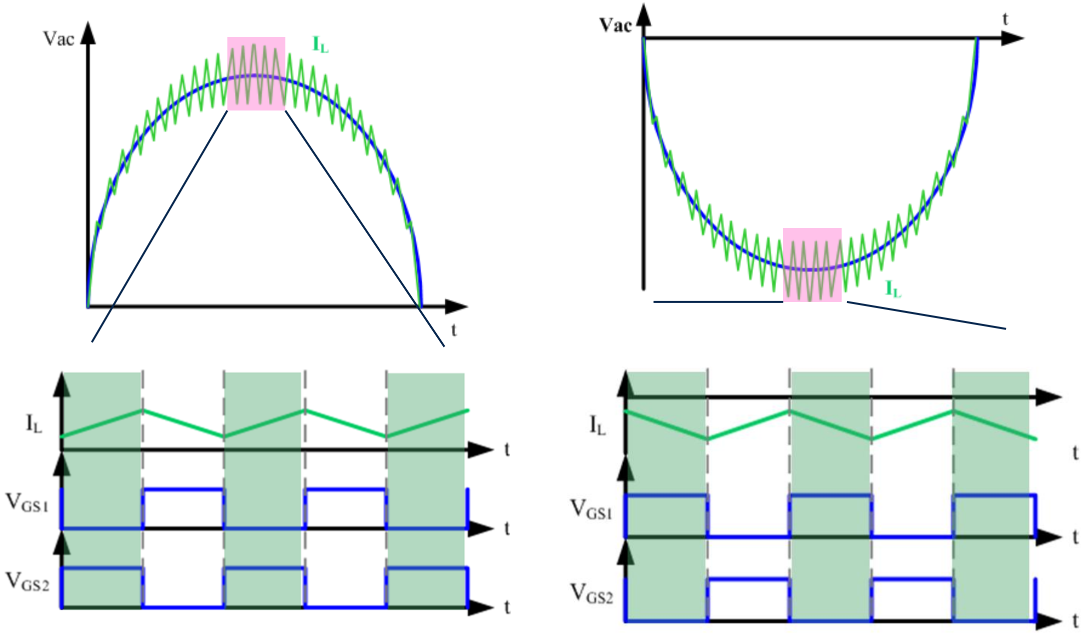
Current sampling strategy in TTP

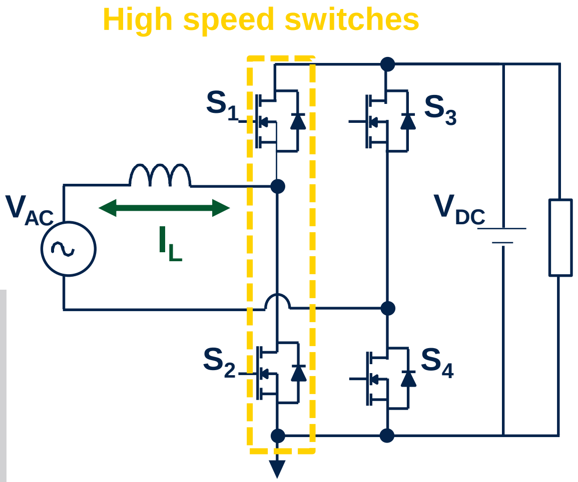
Sampling consideration and configuration

- ✓ Active switch is swapped according to AC polarity
- ✓ Inductor current is sampled at middle duty of active switch
- ✓ Sampling at both of period and reset of PWM count for software filtering (interrupt is double to switch frequency)



***PWM count** in center-aligned mode (up-down mode)*





- Positive cycle: current sampling at PWM count **period** and then doing PI computation
- Negative cycle: current sampling at PWM count **reset and** then doing PI computation

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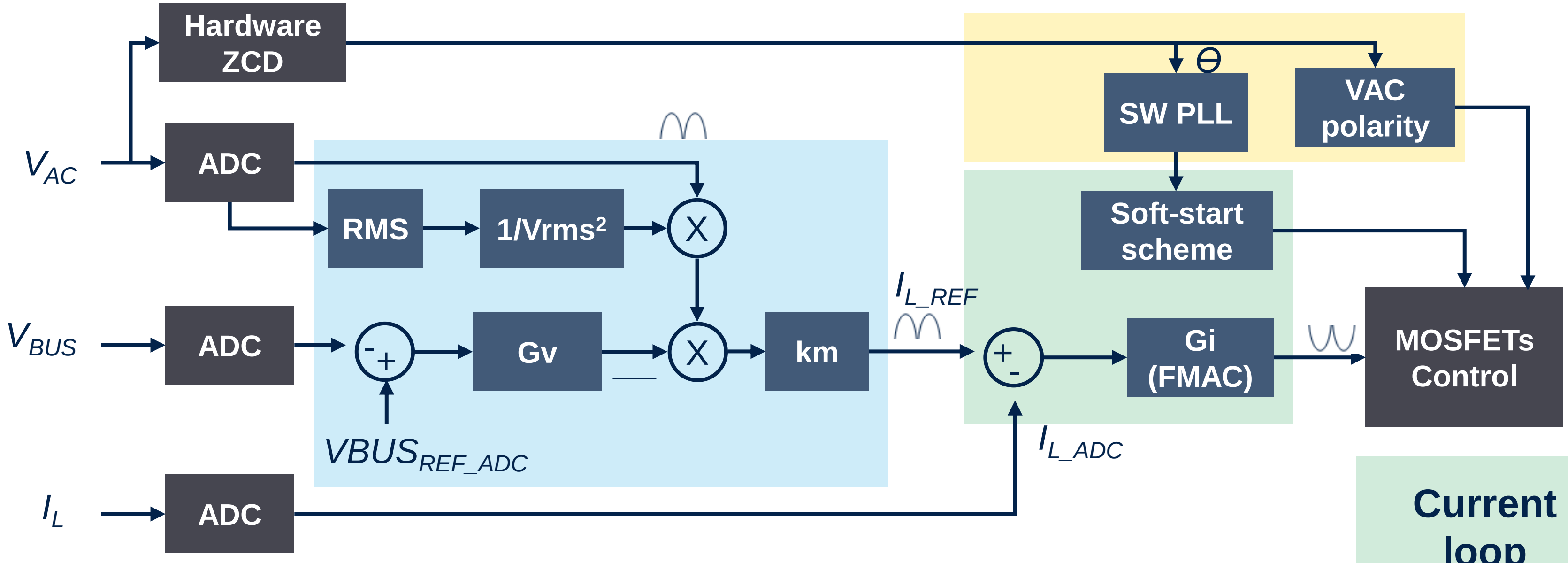
PFC control block diagram

Dual loops with SW phase locked loop

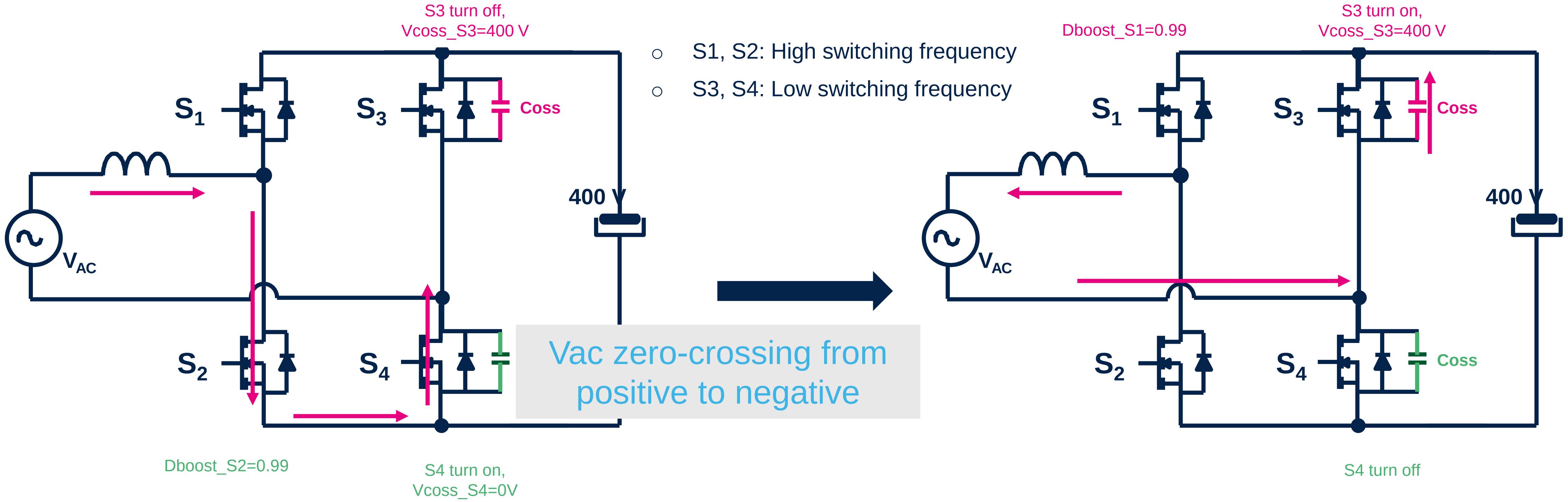


Current loop	Inner loop for shaping AC current that is executed by built-in hardware filter (FMAC)
Voltage loop	Outer loop for bulk voltage regulation and with input voltage feedforward compensation
SW loop	SW PLL (frequency + phase tracking) to synchronize AC phase to achieve blanking time and soft-start scheme

- ✓ *Voltage loop: performed at 10 kHz*
- ✓ *Current loop: performed at 70 kHz*
- ✓ *SW loop: performed at 10 kHz*

Design challenge: current spike at AC zero-crossing

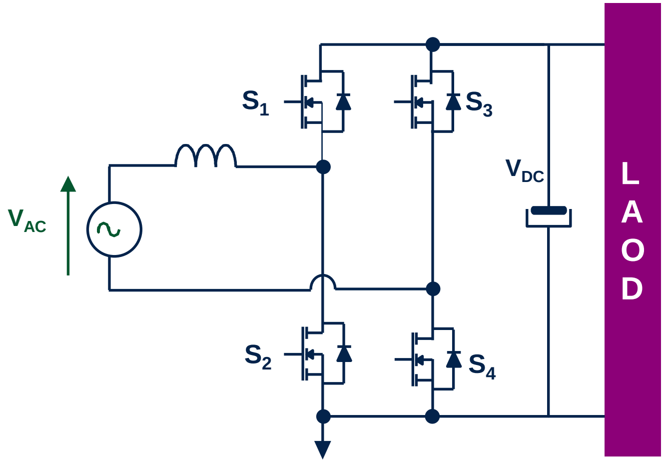
- S1, S2: High switching frequency
- S3, S4: Low switching frequency

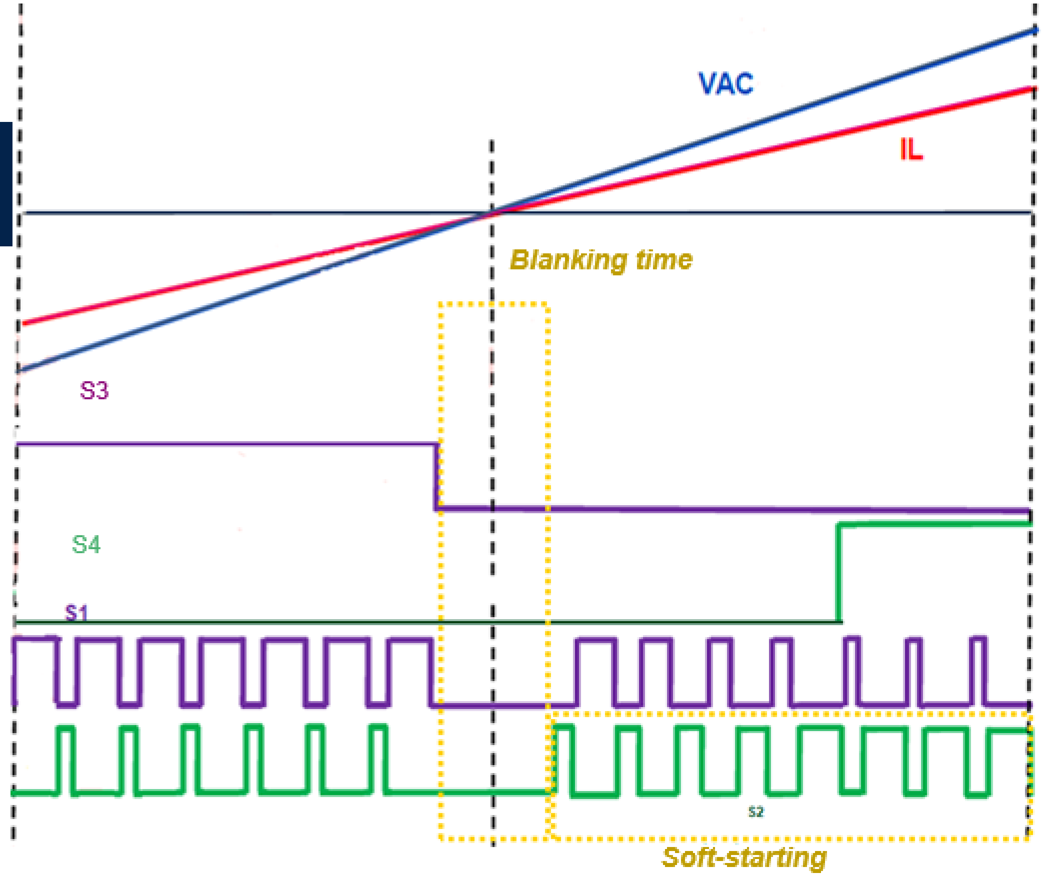


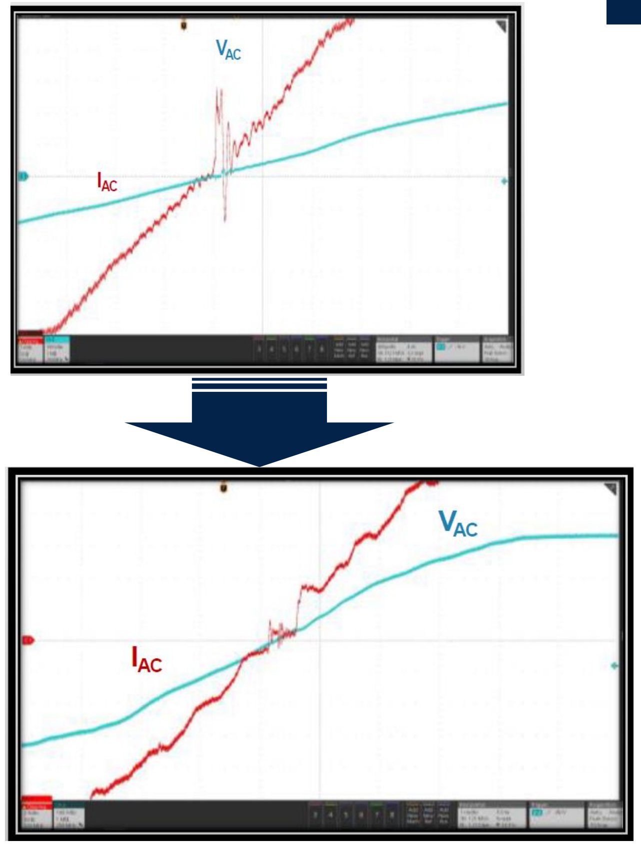
- At a zero-crossing when the AC input is going from positive to negative.
  - Before zero-crossing, Vcoss_S3=400 V, Dboost=0.99 to S2, (1-Dboost)=0.01 to S1
  - After zero-crossing, Vcoss_S4=400 V, Dboost=0.99 to S1, (1-Dboost)=0.01 to S2
- Right at zero-crossing, if Dboost changes abruptly, the Vcoss_S3 will cause a current spike.

Solution for eliminating current spike

Blanking time and soft-start duty control scheme







All MOSFETs are turned OFF to ensure a safe permutation of the power switches control and to avoid to short-circuit of the output DC capacitor.

S1 or S2 active switches are controlled with a soft duty cycle.

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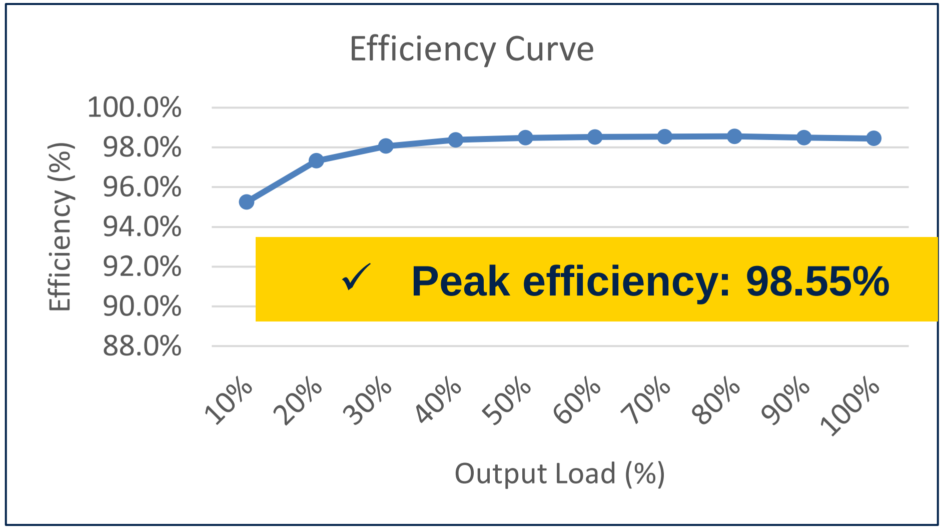
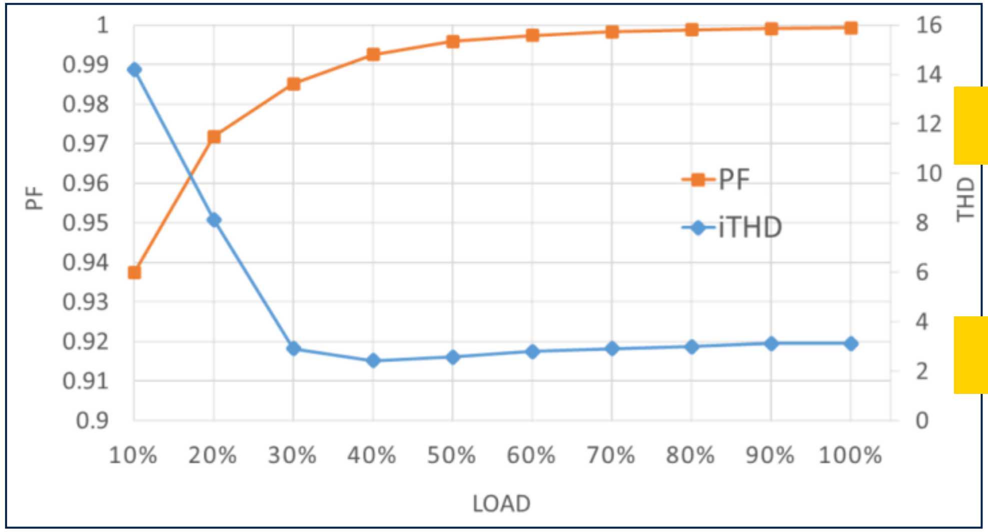
Experimental results @230 Vac



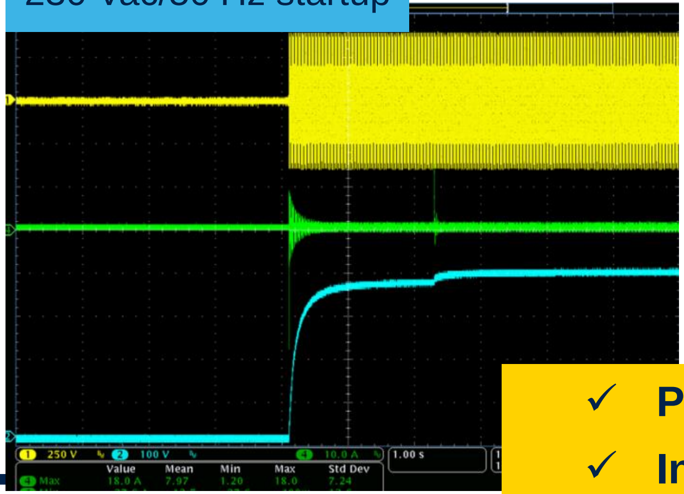
✓ **Peak efficiency: 98.55%**



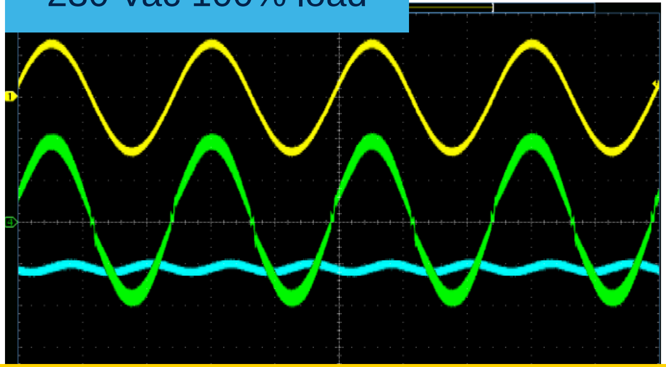
✓ **PF ≥ 0.99**

✓ **iTHD ≤ 5**

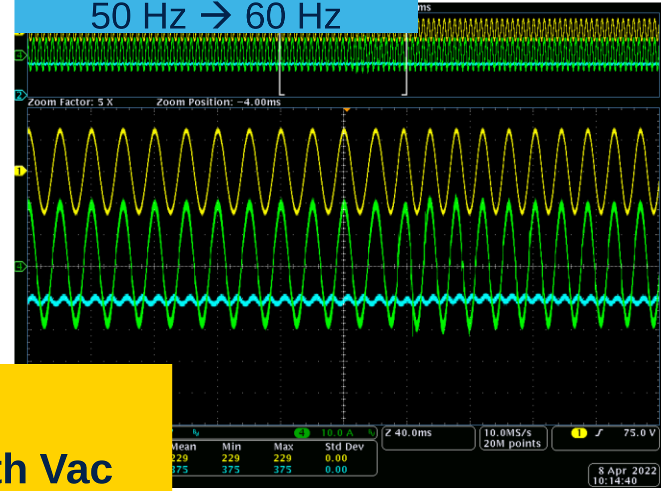
230 Vac/50 Hz startup



230 Vac 100% load



230 Vac 100% load
50 Hz → 60 Hz



- ✓ **Peak inrush current < 18A**
- ✓ **Input current is smooth & aligned with Vac**
- ✓ **Unit operates without protection triggered**

- *CH1 (yellow): Input voltage*
- *CH2 (blue): DC bus voltage*
- *CH4 (green): Input current*

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Bidirectional totem pole PFC solution

6.6 kW bidirectional totem pole PFC solution

Key features

- Grid voltage: **180-265 VAC**
- DC bus voltage: **380-580 VDC**
- Switching frequency: **100 kHz**
- Operation mode: CCM
- Peak efficiency: **98.5%** @230VAC
- Power factor: **>0.99** @100% load
- iTHD: **<5%** @ 50%-100% load

Key components

- STM32G474VBT (32-bit MCU)
- SCTWA60N120G2-4 (SiC Gen2)
  → SCT040W120G3-4AG (Gen3)
- STGAP2SICS (gate driver)
- STP75NF20 (N-ch power MOS)
- VIPer 319HD (Aux. SMPS)

STPOWER STGAP STM32

Target application

Energy storage system (ESS)

Power conditioning system (PCS)

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PFC digital platform–STM32G474

Configurations of MCU key functions on digital PFC

Arm® Cortex® -M4 up to 170 MHz

Floating-point unit (FPU)

- Control loop computation (reserved for future use)

32-Kbyte **CCM-SRAM**

- Zero wait-state for critical code execution

CORDIC for trigonometric functions acceleration

- Software phase-locked loop (EPLL)

FMAC filter mathematical accelerator

- Hardware digital filter (CPU off-load) for loop computation (reserved)

Hi-Resolution PWM Timer (184 ps)

- Mainly for high frequency (HF) MOSFET control at 67 kHz

Multiple **ADCs (4 Msps)** up to 5

- Grid voltage, inductor current, DC bus voltage/current and hotspot

Comparators and **DACs** up to 7

- PFC OVP / OCP

UART, **SPI**, **CAN** and **USB**

- CAN for internal/external communication

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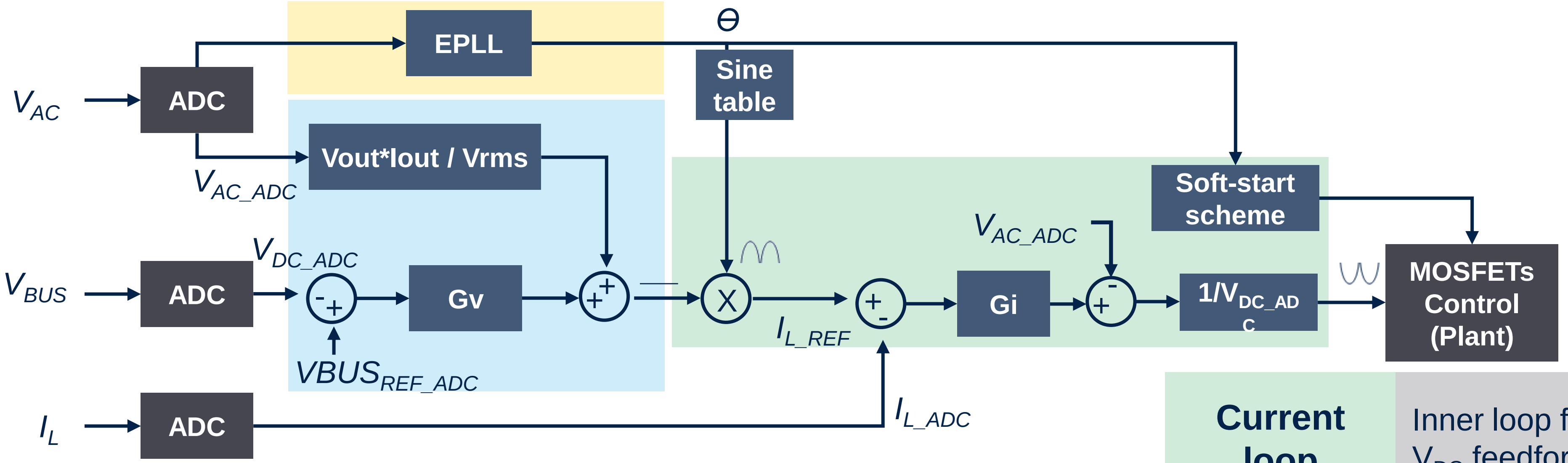
Control block diagram: rectifier mode (charging)

Dual loops with enhanced phase locked loop



- ✓ *Voltage loop: performed at 10 kHz*
- ✓ *Current loop: performed at 100 kHz*
- ✓ *EPLL loop: performed at 100 kHz*

Current loop	Inner loop for shaping AC current with V_{AC} and V_{DC} feedforward compensation
Voltage loop	Outer loop for bulk voltage regulation and with current feedforward compensation
EPLL loop	Enhanced PLL to synchronize AC phase to achieve blanking time and soft-start scheme

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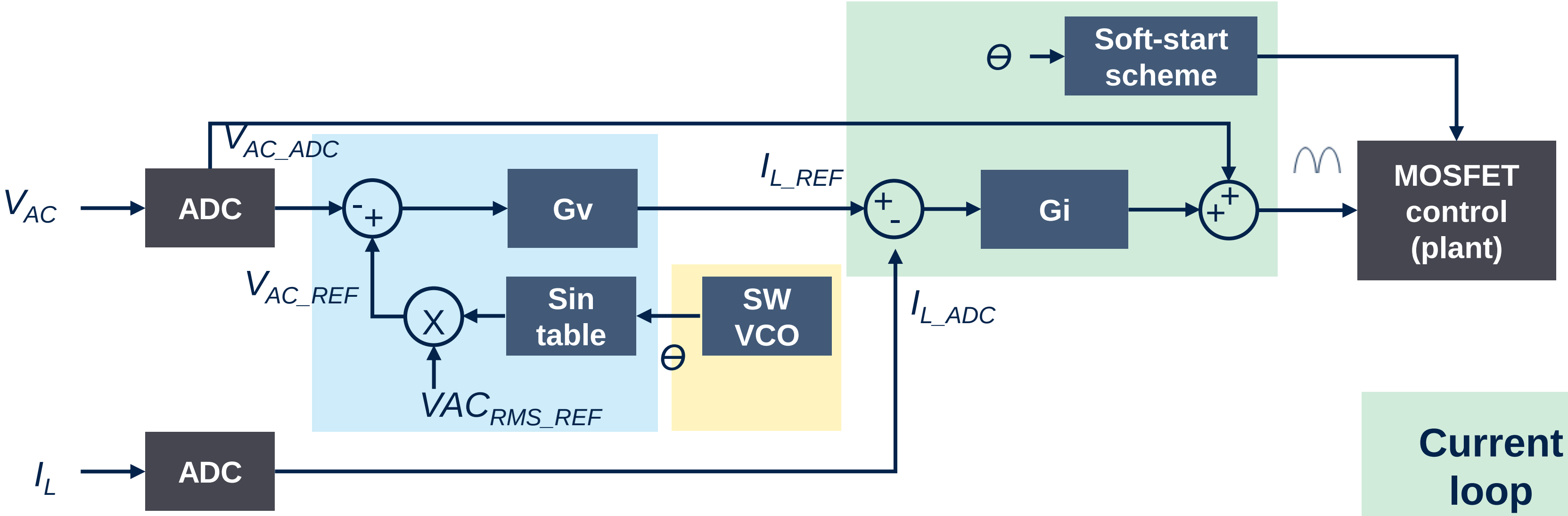
Control block diagram: inverter mode (off-grid)

Dual loops with SW VCO for sine generation



- ✓ *Voltage loop: performed at 100 kHz*
- ✓ *Current loop: performed at 100 kHz*
- ✓ *SW VCO: performed at 100 kHz*

Current loop	Inner loop for controlling AC current and with V_{AC} feedforward compensation
Voltage loop	Outer loop for shaping AC voltage and the reference is from SW sine table basically
Theta Ѳ generation	Simple software VCO for AC phase (Ѳ) generation

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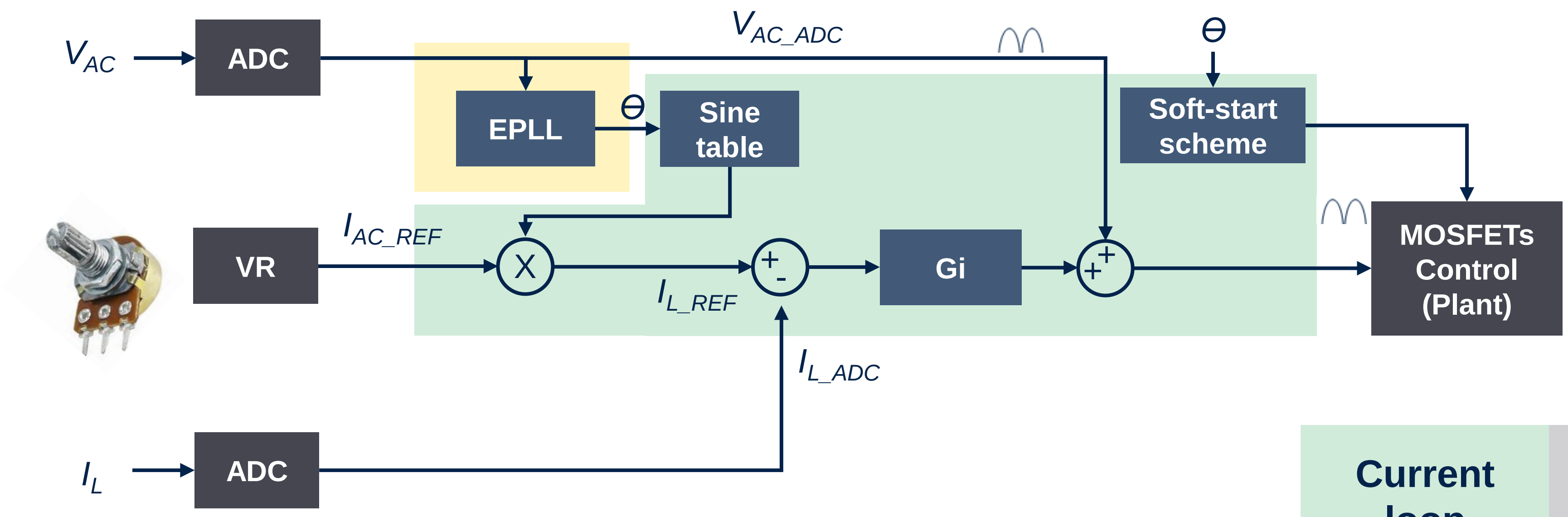
Control block diagram: inverter mode (on-grid)

Current loop only for grid-tied feature

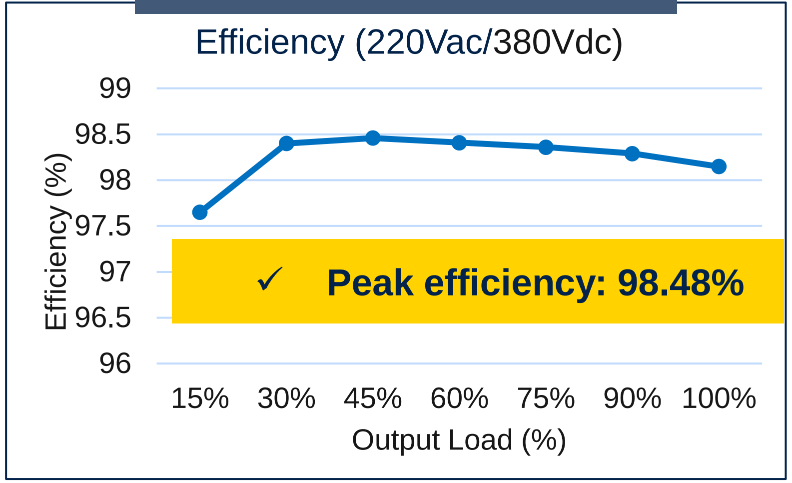


- ✓ *Current loop: performed at 100 kHz*
- ✓ *EPLL loop: performed at 100 kHz*

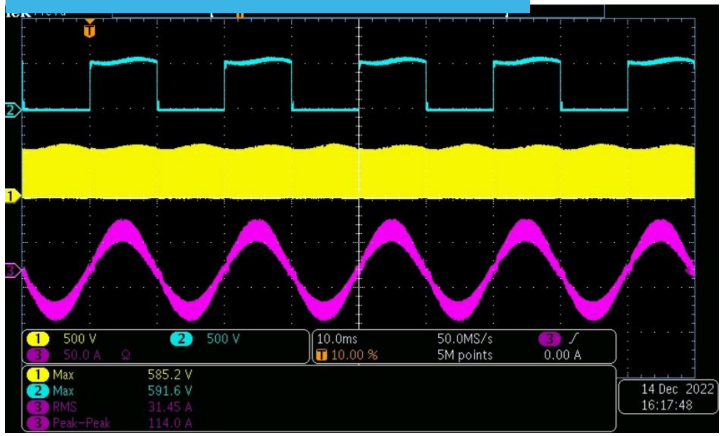
Current loop	Inner loop for with V_{AC} feedforward compensation, and AC current reference is from VR (due to no DCDC section)
EPLL loop	Enhanced PLL to synchronize AC phase to achieve grid connection and phase control

Experimental results

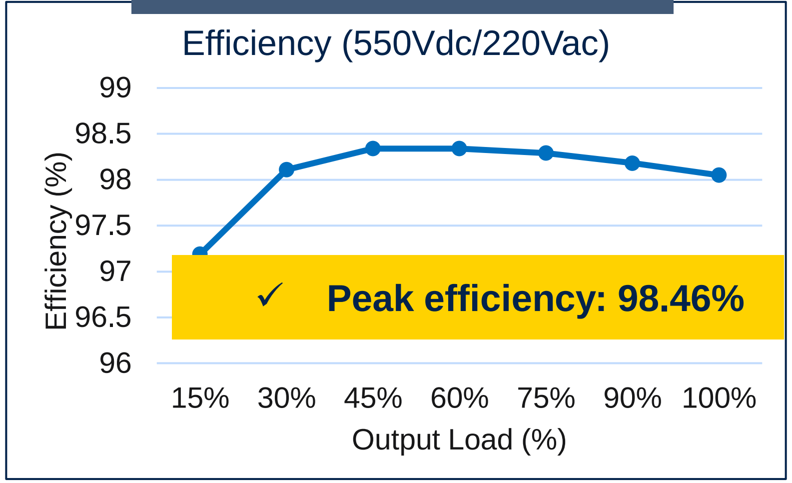
Rectifier mode



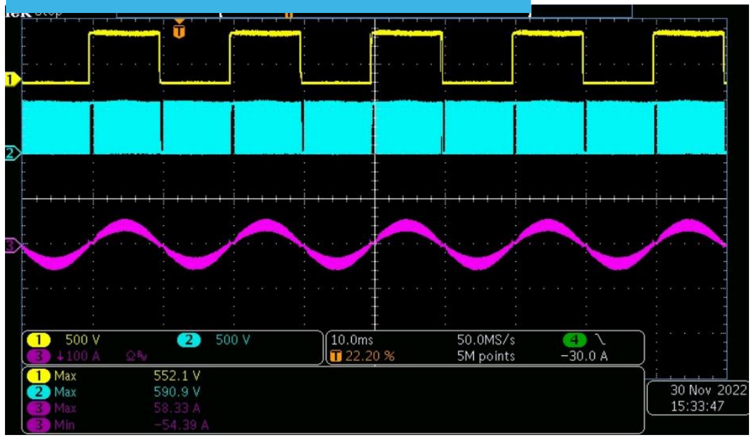
230Vac/50Hz, 550 Vdc with 6600 W load



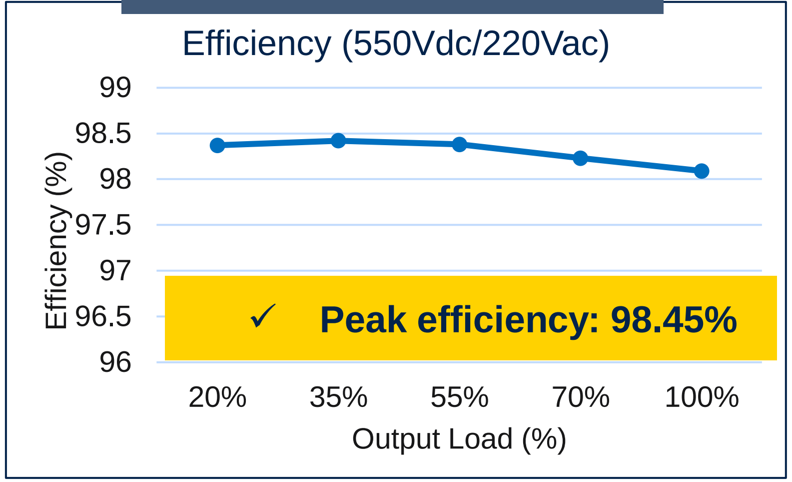
Inverter mode (off-gird)



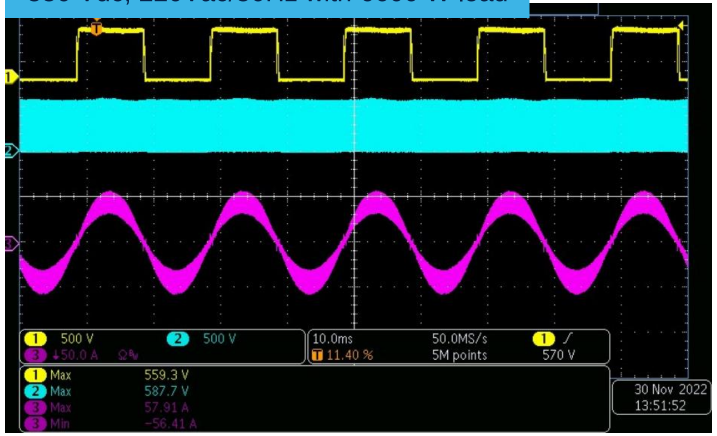
550 Vdc, 220Vac/50Hz with 6600 W R load



Inverter mode (gird-tied)



550 Vdc, 220Vac/50Hz with 6600 W load



- *CH1 (yellow): Vds of upper high-speed MOSFET*
- *CH2 (blue): Vds of upper low-speed MOSFET*
- *CH3 (purple): Inductor current*

- *CH1 (yellow): Vds of upper low-speed MOSFET*
- *CH2 (blue): Vds of upper high-speed MOSFET*
- *CH3 (purple): Inductor current*

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ST key product on solution

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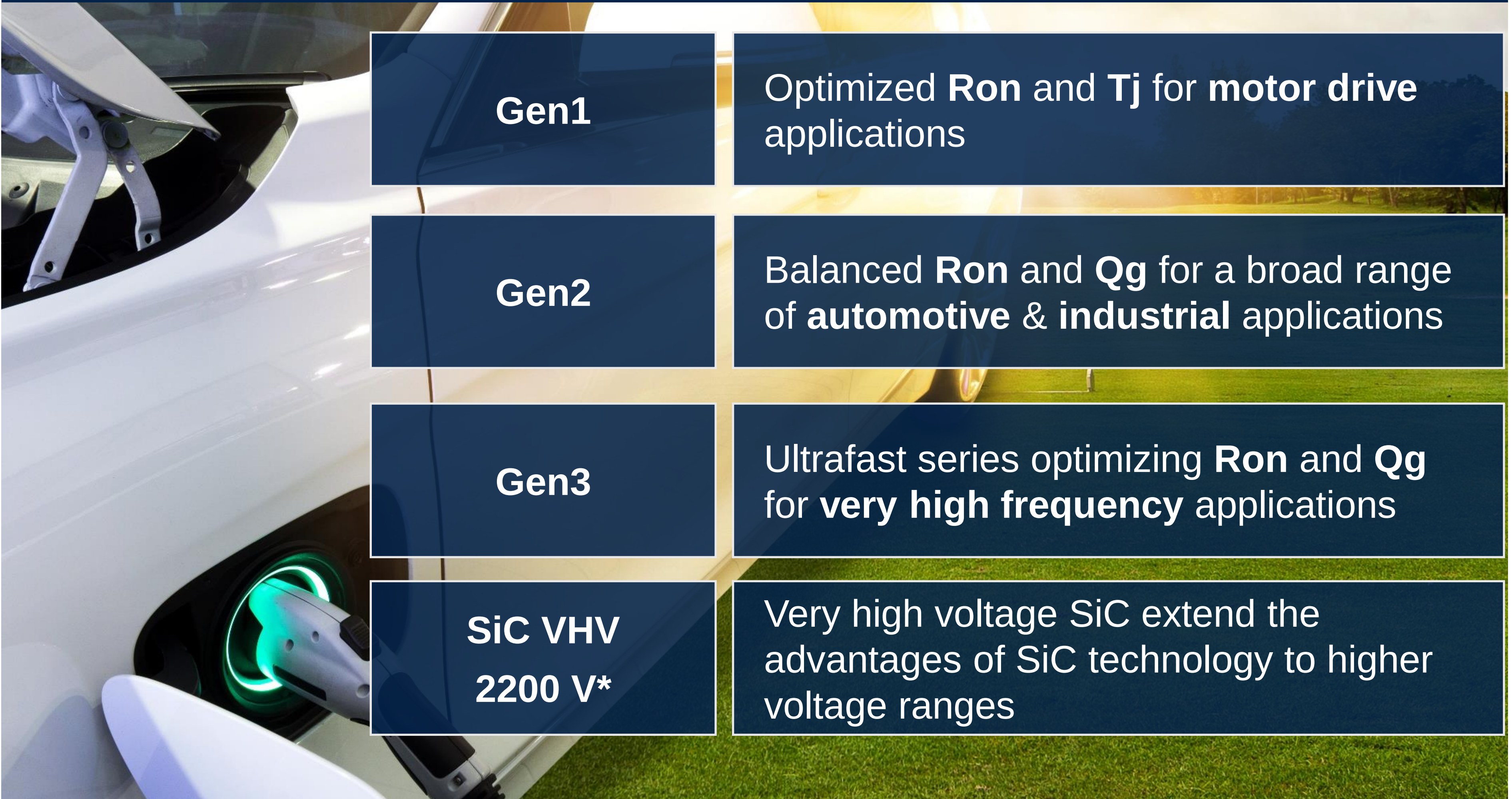
SiC MOSFET range

High voltage and fast switching for high density applications

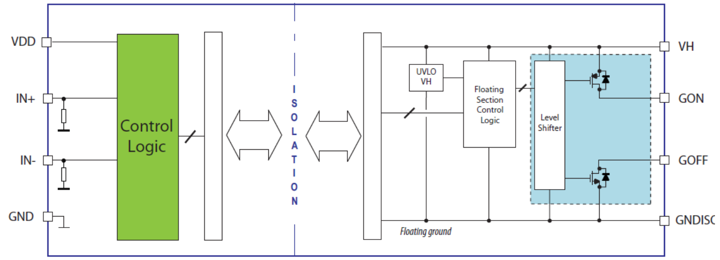


Gen1	Optimized **Ron** and **Tj** for **motor drive** applications	**1200–1700 V**
Gen2	Balanced **Ron** and **Qg** for a broad range of **automotive** & **industrial** applications	**650 V, 1200 V, 2200 V**
Gen3	Ultrafast series optimizing **Ron** and **Qg** for **very high frequency** applications	**650 V, 750 V, 900 V, 1200 V**
SiC VHV 2200 V*	Very high voltage SiC extend the advantages of SiC technology to higher voltage ranges	**2200 V**

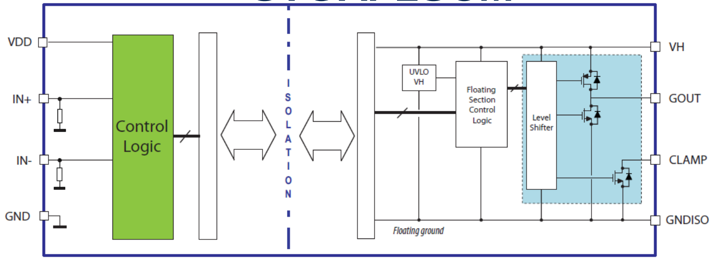
*** industrial grade**

STGAP gate driver
1700V/6kV galvanic isolated single- & dual-channel

STGAP2SM

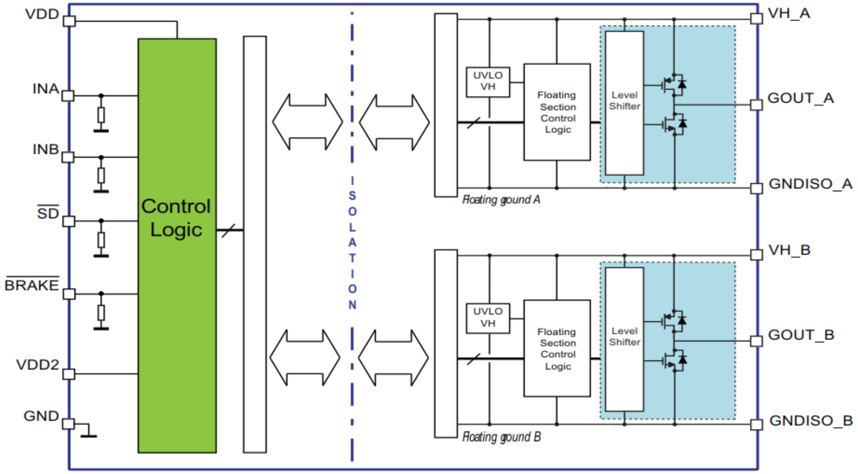


STGAP2SCM



- 3V3 / 5 V logic inputs
- **Up to 26 V supply voltage**
- **4A sink / source driver current capability**
- 100 V / ns CMTI
- Propagation delay 80 ns
- Standby function
- High-voltage rail up to 1700 V
- Temperature shut down protection

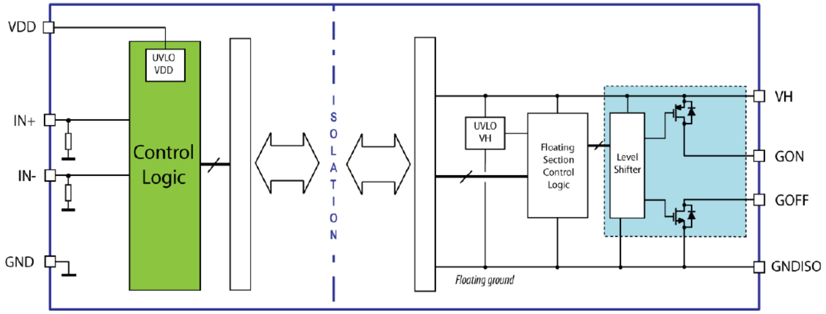
STGAP2D (3 kW PFC)



High performance
- Galvanic isolated up to1700V

Robustness
- Interlocking
- Negative gate drive ability

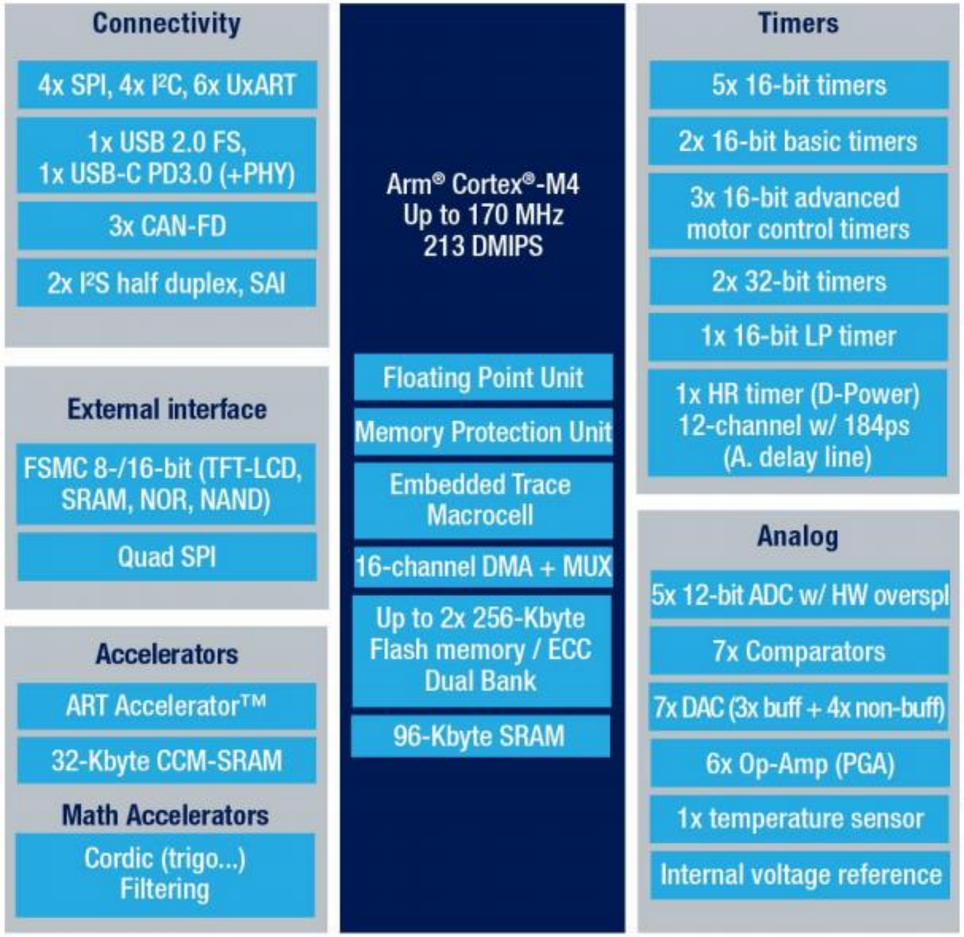
STGAP2SICS (6.6 kW PFC)



High performance
- Galvanic isolated up to 6 kV optimized for SiC MOSFET

STM32G474 MCU

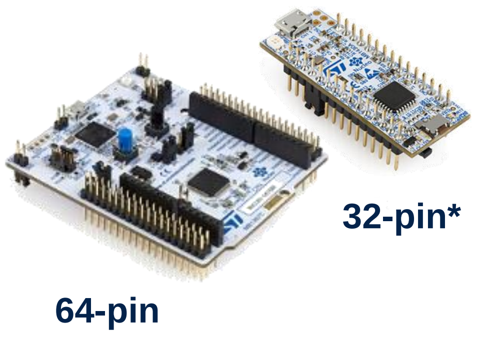
Hi-resolution PWM and comprehensive set of analog peripherals for digital control

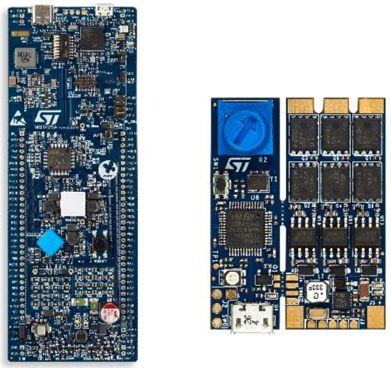


- 170 MHz 32-bit Arm® Cortex®-M4 core with FPU
- Routine booster of CCM-SRAM up to 32 KB
- Mathematic hardware accelerators (CORDIC / FMAC)
- High-resolution timer (184 ps) for precise PWM control
- Rich advanced analog
- USB Type-C® Power Delivery (PD)
- ±1% internal clock

STM32G4 hardware solutions

Accelerate evaluation, prototyping, and design





STM32 Nucleo

Flexible prototyping

- NUCLEO-G431RB
- NUCLEO-G474RE
- NUCLEO-G431KB

Evaluation boards

Full feature STM32G4 evaluation

- STM32G484E-EVAL
- STM32G474-EVAL

Motor control Pack

Full feature for motor control and analog

- P-NUCLEO-IHM03

Discovery kits

Key feature prototyping

- B-G474E-DPOW1
- B-G431B-ESC1

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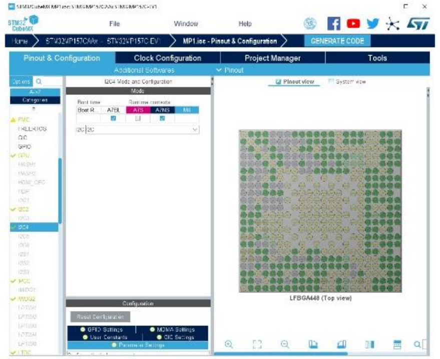
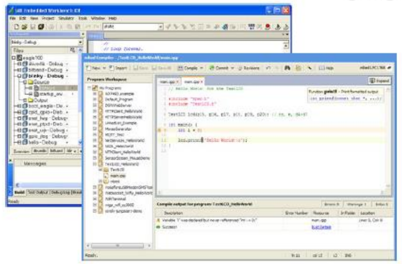
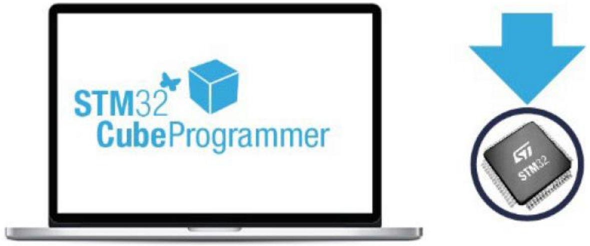
STM32G4 software tools

Complete support of Arm® Cortex®-M ecosystem





All-in-one STM32 programming tool
Multi-mode, user-friendly



STM32CubeMX

STM32CubeMX

- Configure and generate code
- Conflicts solver

IEDs compile and debug

Flexible solutions

- Partners IDE, like IAR and Keil
- Free IDE based on Eclipse, like STM32CubeIDE

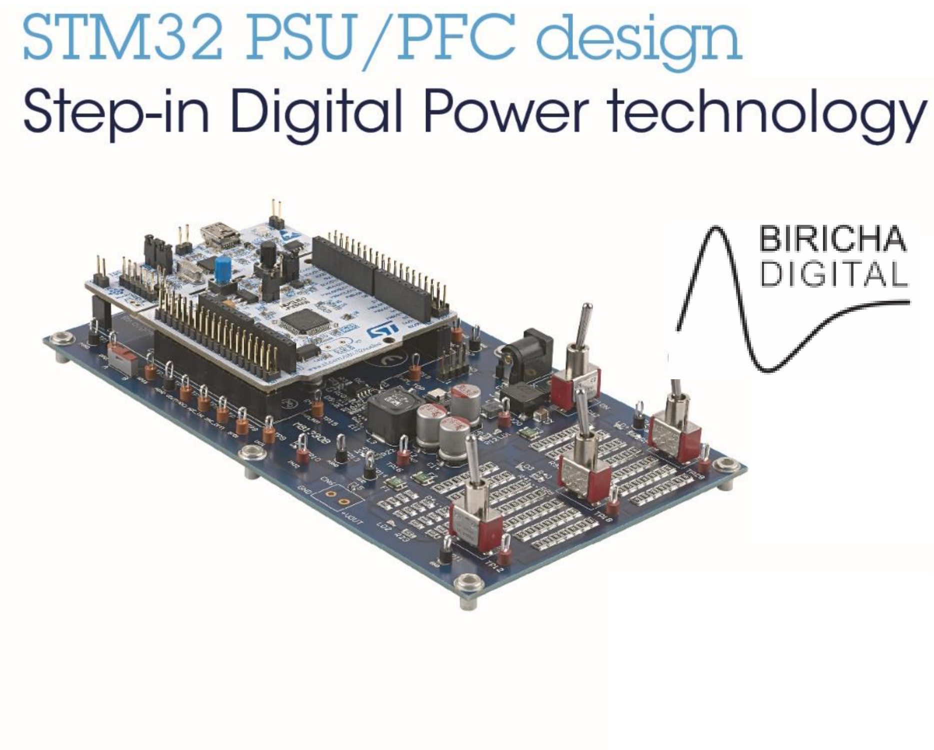
STM32 programming tool

STM32CubeProgrammer

- Flash and/or system memory
- GUI or command-line interface

Digital power workshops with Biricha

Combining industry leading ST MCUs with Biricha's tools and training



Biricha digital power:

- World leading expertise and training in digital power
- Workshop based on STM32F334/G474 Nucleo and dedicated digital power expansion board
- Learn how to implement digital power supplies and power factor correction

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Takeaways

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Takeaways

Digital control with STM32G4 allows unidirectional/bidirectional solutions based on bridgeless totem pole topology

Totem pole PFC offers inherent bidirectional power flow control and can be used for various applications

ST 3 kW reference design for telecom rectifier application demonstrates a conventional unidirectional solution

6.6 kW reference design demonstrates bidirectional capability, including rectifier, off-grid, and on-grid

STM32 ecosystem provides a complete design environment and rewarding development experience

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Our technology starts with You

Find out more at www.st.com

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