Sub-track II –
Power & Energy Presentation
48 V power management solution for AI servers

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Technical Marketing
STMicroelectronics
Complete solution for direct/dual-stage power delivery in 48 V systems

Powering datacenters with highest efficiency solution

Dual-stage conversion

48 V $\rightarrow$ 1st stage

Intermediate bus conversion

Unregulated $\rightarrow$ 12 V $\rightarrow$ Regulated

Or

2nd stage

Multiphase digital controller

SPS

SPS

SPS

SPS

SPS

SPS

CPU

DDR

ASIC

Direct conversion

48 V $\rightarrow$ Resonant solution with isolation support

CPU

DDR

ASIC

Driving the evolution of power in server & communications infrastructure
Dual stage conversion intermediate bus: 48 V to 12 V

3 topologies available based on customer needs for server and telecom 12 V bus distributions

**STC**: switched tank converter
- Low profile solution (5 mm)
- High density 1 KW in 1/8 brick
- High efficiency

**STB**: stacked buck converter
- Scalable solution
- High power capability above 3 kW
- ST patent

**HSTC**: hybrid switched tank converter
- Flexible conversion ratio
- High power and high-density solution
- Minimized BOM count for any ratio
- ST patent

Intel VR13.HC
Reference design

Intel VR13.HC
Intel VR14
Reference design

Unregulated
98.2% Efficiency

Regulated
98.4% Efficiency

Unregulated
98.5% Efficiency
**Main features**

- Regulated output, nonisolated
- Server and telecom 12 V bus distribution
- Input voltage: 38–60 V
- Output voltage: 12 V regulated (adjustable by PMBus)
- Thermal design power (TDP): 1000 W
- Coupled inductor for higher density and efficiency
- Digital controller PM6779/PM6780, STPRDC02/A drivers
- Total area: 58x37 mm (quarter brick)

### STB-UCL-1kW

<table>
<thead>
<tr>
<th>ST PN used</th>
<th>Controller: PM6779/80 Driver: STPRDC02/A</th>
</tr>
</thead>
<tbody>
<tr>
<td>TDP (W) (*)</td>
<td>1000</td>
</tr>
<tr>
<td>Peak power (W)</td>
<td>1100</td>
</tr>
<tr>
<td>Input voltage (V)</td>
<td>38–60</td>
</tr>
<tr>
<td>Output voltage (V)</td>
<td>12 V</td>
</tr>
<tr>
<td>Regulated or nonregulated</td>
<td>Regulated</td>
</tr>
<tr>
<td>Efficiency at 54 V (20%-60%-100%) (**</td>
<td>98.0%-98.1%-97.3</td>
</tr>
<tr>
<td>Peak efficiency (%) At Vin=54 V</td>
<td>98.3</td>
</tr>
<tr>
<td>PCB size (X, Y, Z) mm</td>
<td>58 x 37 x 15</td>
</tr>
<tr>
<td>Normalized BOM cost</td>
<td>0.6</td>
</tr>
</tbody>
</table>

Whitepaper available–board available
STB-UCL status

• STB-UCL on-board solution is stable and validated:
  • Topology already in production since 2Y in one customer
  • Solution in qualification at >10 customers, completed at 2 customers
  • Extensive bench validation (EBV) completed successfully
  • Chamber tests 3 batches (8 boards each) completed successfully

• 2 inductors qualified:
  • Vendor I: max. 14.3 mm height
  • Vendor T: max. 14 mm height

• Keep working with 2 more inductors vendors:
  • Vendor A: max. 16 mm height
  • Vendor P: max. 14 mm height

• 2 MOSFET vendors qualified
**HSTC 750**

**Main features**
- Fixed conversion ratio
- Nonregulated output (4:1), nonisolated
- High-efficiency and low profile (5 mm)
- Input voltage: 40–60 V
- Thermal design power (TDP): **1000 W (1200 W peak)**
- Digital controller STNRG328, STPRDC02/A drivers
- Total area: 65 x 55 mm (or 65 x 25 if dual-side PCB)

**HSTC 750**

<table>
<thead>
<tr>
<th>ST PN used</th>
<th>Controller: PM6779/80 Driver: STPRDC02A</th>
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</thead>
<tbody>
<tr>
<td>TDP (W) (*)</td>
<td>750</td>
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<tr>
<td>Peak power (W)</td>
<td>900</td>
</tr>
<tr>
<td>Input voltage (V)</td>
<td>38-60</td>
</tr>
<tr>
<td>Output voltage (V)</td>
<td>5:1</td>
</tr>
<tr>
<td>Regulated or nonregulated</td>
<td>Non-Regulated</td>
</tr>
<tr>
<td>Efficiency at 54 V (20%-60%-100%) (**)</td>
<td>98.4%-98%-96.6%</td>
</tr>
<tr>
<td>Peak efficiency (%) At Vin=54 V</td>
<td>98.5</td>
</tr>
<tr>
<td>PCB size (X, Y, Z) mm</td>
<td>60x25x12.5</td>
</tr>
<tr>
<td>Normalized BOM cost</td>
<td>0.6</td>
</tr>
</tbody>
</table>

*98.5% Efficiency*
Main features

- Fixed conversion ratio
- Nonregulated output (4:1), nonisolated
- High-efficiency and low profile (5 mm)
- Input voltage: 40V-60V
- Thermal design power (TDP): 1000 W (1200 W peak)
- Digital controller STNRG328, STPRDC02/A drivers
- Total area: 65x55 mm (or 65x25 if dual side PCB)

<table>
<thead>
<tr>
<th>STC U2J 1KW</th>
<th>Controller: STNRG328</th>
</tr>
</thead>
<tbody>
<tr>
<td>ST PN used</td>
<td>Driver: STPRDC02</td>
</tr>
<tr>
<td>TDP (W) (*)</td>
<td>1000</td>
</tr>
<tr>
<td>Peak power (W)</td>
<td>1200</td>
</tr>
<tr>
<td>Input voltage (V)</td>
<td>40-60</td>
</tr>
<tr>
<td>Output voltage (V)</td>
<td>4:1</td>
</tr>
<tr>
<td>Regulated or nonregulated</td>
<td>Non-Regulated</td>
</tr>
<tr>
<td>Efficiency at 54 V (20%-60%-100%) (**)</td>
<td>97.35%-97.6%-96.4%</td>
</tr>
<tr>
<td>Peak efficiency (%) At Vin=54 V</td>
<td>97.9</td>
</tr>
<tr>
<td>PCB size (X, Y, Z mm)</td>
<td>65x55x6</td>
</tr>
<tr>
<td>Normalized BOM cost</td>
<td>1.2</td>
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</tbody>
</table>

(*) PCB area equivalent moving from "double side" to "single side" component mounting

Efficiency

98.3%

STC 1kW ⅛ Brick Efficiency

Total efficiency with bias

- 58Vin
- 54Vin
- 40Vin
54 V solutions: BOM cost roadmap

Unregulated solution

STC 600 W U2J
STC 600 W X7R

Regulated solution

STB 850 W
STB-UCL 850 W

ST is committed to reducing total BOM cost
And increasing the overall system performance
Dual stage conversion
second stage: 12 V to CPU/DDR/ASIC

Major experience in 12 V solutions for INTEL/AMD CPU/DDR and SoC

The ST logo is a registered trademark of STMicroelectronics. All other names and logos are the property of their respective owners.
Example of 48 V → 12 V → load ST Total solution

48 V → 12 V conversion

ST components on bottom side: controller, driver, MOSFET; eFuse coming

12 V → load conversion

ST components: Controller, SPS, eFuse
Our technology starts with You

Find out more at www.st.com