How to optimize SiC MOSFET gate driving in applications

Kimi Lu

Field Application Engineering team

Power & Discrete Marketing and Application

ST Taiwan , APeC Region

Agenda

1 Composition of SiC Driving Application Circuit

2 Potential Risk - Parasitic Turn On (PTO)

3 Techniques to reduce Gate Voltage glitch effect

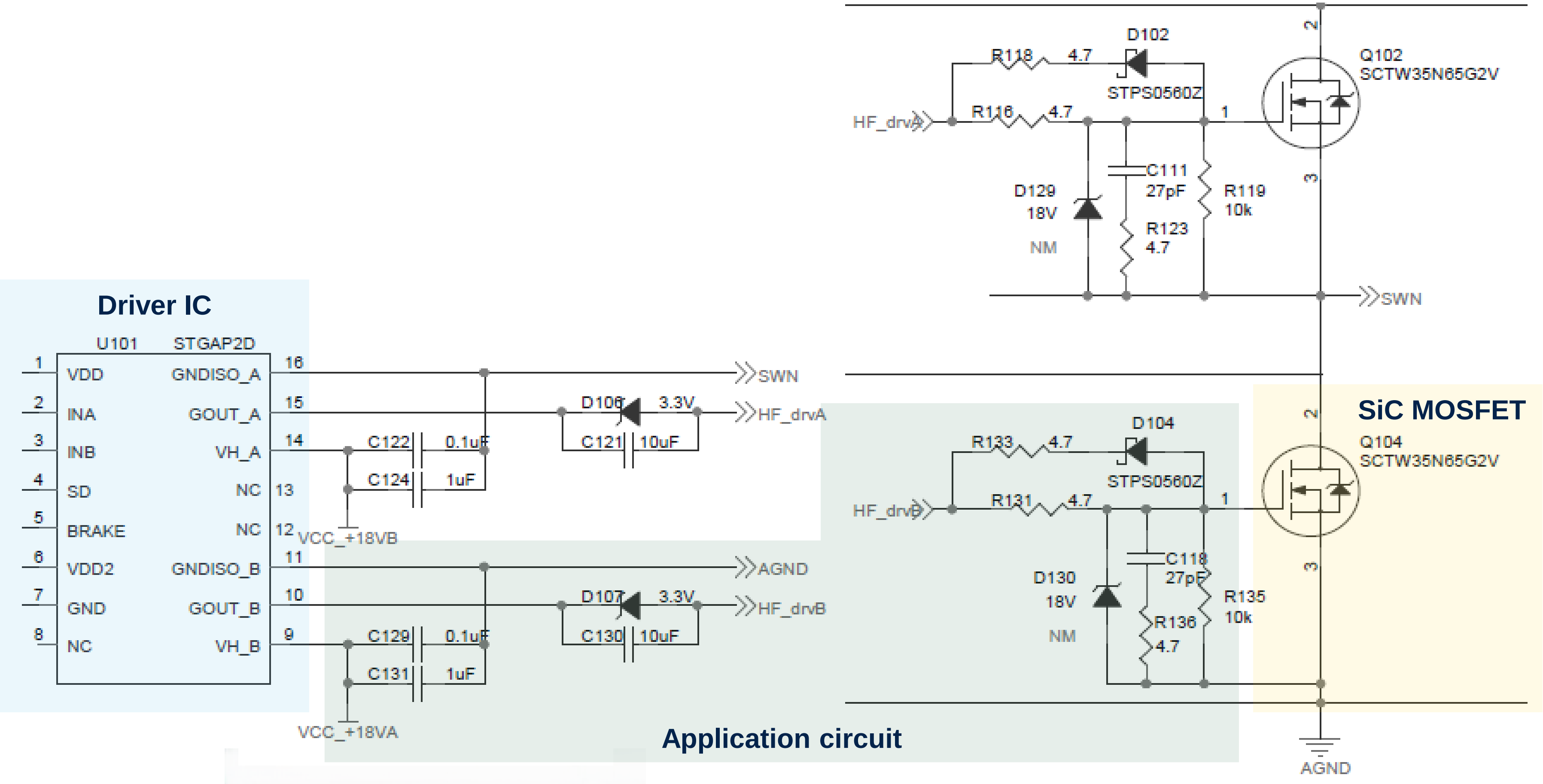
4 How to measure V_{GS} on SiC applications

5 Key SiC MOSFET parameters to consider

Composition of SiC Driving Application Circuit

Driver IC, components, and SiC MOSFET constitute the driving circuit

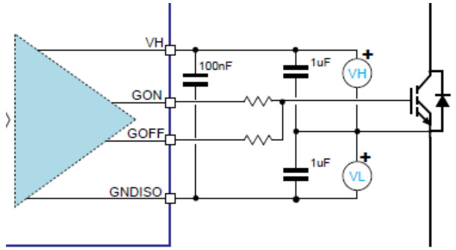
How to optimize SiC MOS gate driving in applications
How to fine tune SiC MOS gate driving to minimize losses



Application circuit consideration

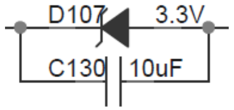
Negative voltage driving.

- Not mandatory, further reduce losses and increase robustness.



Negative voltage clamping circuit.

- To produce negative voltage driving.

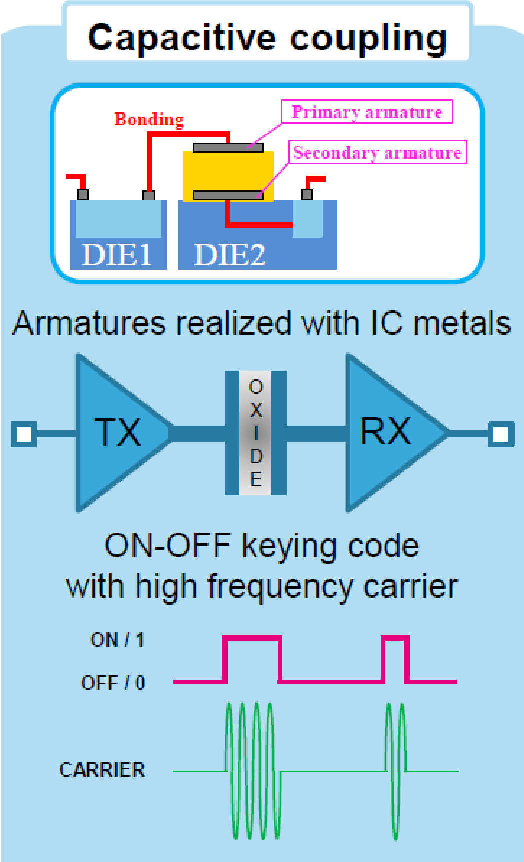


R_{gon}, R_{goff}, C_{GS}, Zerner diodes.

- To optimize efficiency, EMI and glitch.

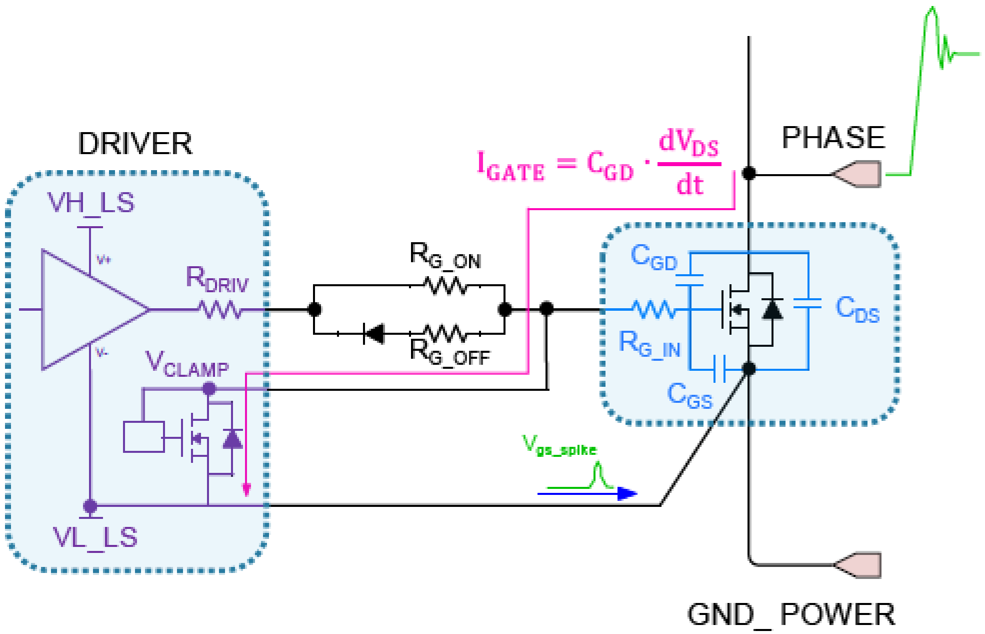
Driving IC consideration

Isolation is needed from SiC IC to avoid noise interference
Protection: Millar Clamp function to prevent gate voltage spike



Armatures realized with IC metals

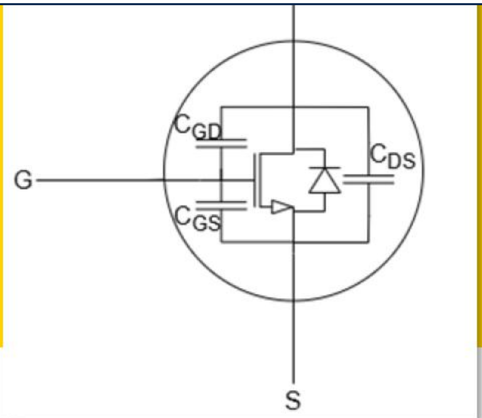
ON-OFF keying code with high frequency carrier



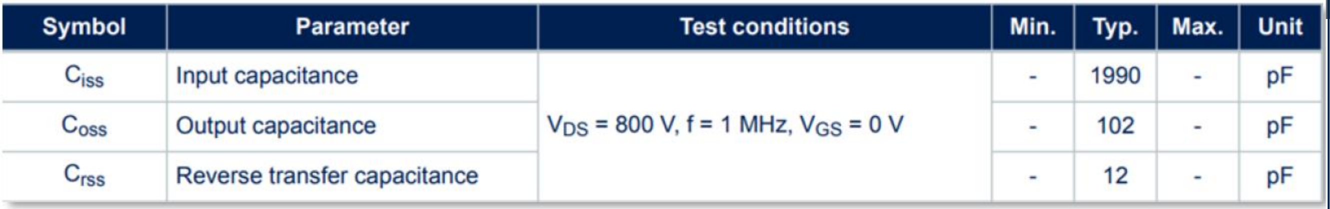
SiC MOSFET consideration

A lower capacitance ratio (Crss/CGS) in a device can reduce susceptibility to false turn-on or parasitic turn on (PTO)

To improve device performance and reliability, it is crucial to manage parasitic capacitance carefully. It’s directly related to Miller effect.



$$Ratio = \frac{C_{GD}}{C_{GS}} = \frac{Crss}{Ciss - Crss} << 1$$



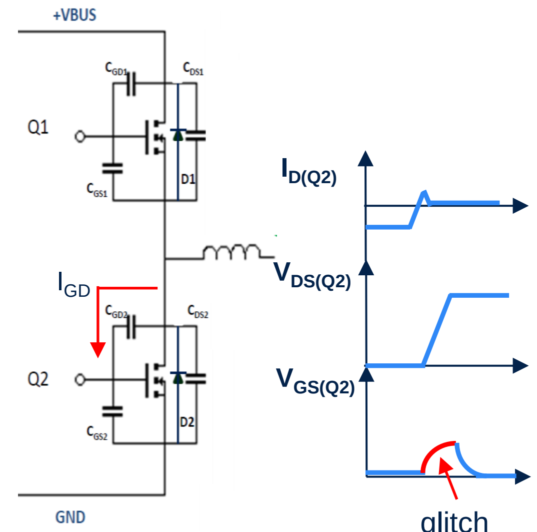
Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 800 V, f = 1 MHz, V_{GS} = 0 V	-	1990	-	pF
C_{oss}	Output capacitance		-	102	-	pF
C_{rss}	Reverse transfer capacitance		-	12	-	pF

Potential Risk - Parasitic Turn On (PTO)

Parasitic turn-on effect

SiC MOSFETs technology improves performance by providing faster switching solutions than traditional power semiconductors – CGD

Parasitic turn-on (PTO) caused by the Miller capacitance is considered a weakness of SiC MOSFETs. Gate spikes sometime happen in SiC applications – glitch.



$I_{GD} = C_{GD} * dV_{DS(Q2)}/dt$

Parasitic Turn-On: Parasitic turn-on refers to the phenomenon that occurs when a fast dv/dt causes a power transistor to conduct in a command-off state.
It's typically the capacitive feedback via the Miller capacitance which is considered.

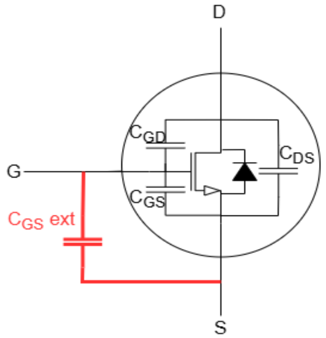
Risk: If a glitch occurs with substantially higher than $V_{GS(th)\_min}$, it can lead to a shoot-through failure state.

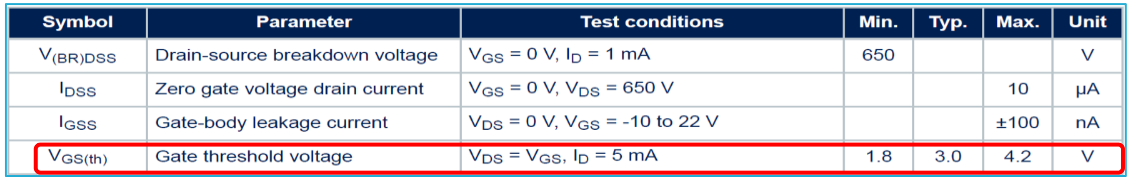
Key factor of PTO:
Fast dV_{DS}/dt.

To avoid Parasitic Turn On, gate-drive designs for high dv/dt applications are typically implemented with negative turn-off gate voltages. But is that really needed with SiC MOSFETs?

K elements in Miller turn on Phenomenon

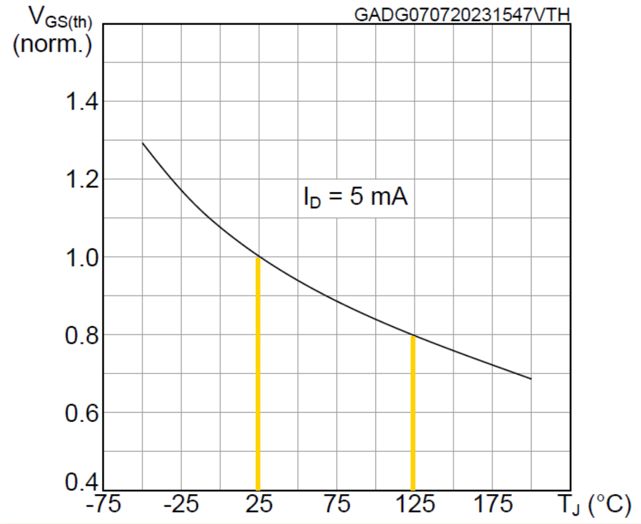
SiC $V_{GS(th)}$ threshold voltage is the minimum gate-to-source voltage to create a conducting path between MOSFET source & drain terminals





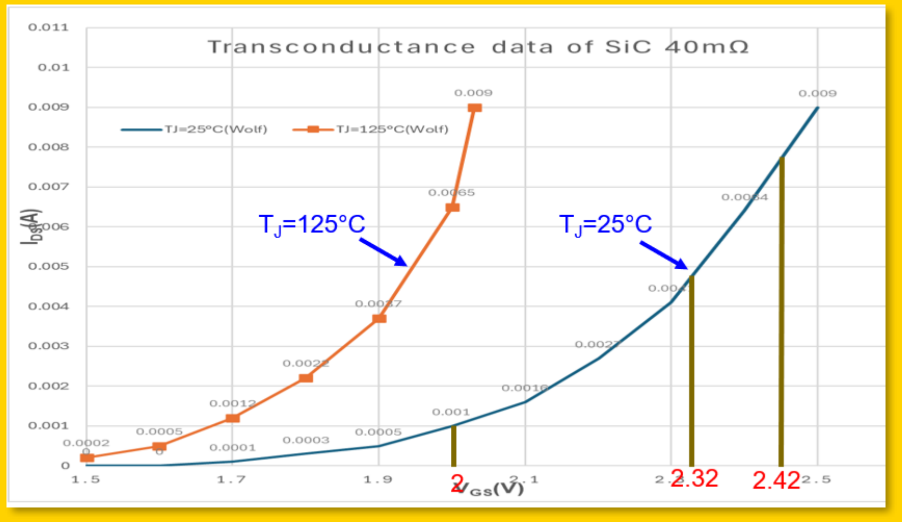
Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V, I_D = 1 mA	650			V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0 V, V_{DS} = 650 V			10	µA
I_{GSS}	Gate-body leakage current	V_{DS} = 0 V, V_{GS} = -10 to 22 V			±100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 5 mA	1.8	3.0	4.2	V

Normalized gate threshold voltage vs. temperature



Temperature effects:
$V_{GS(th)}$ tends to decrease at higher temperatures, This behavior must be considered in applications where devices operate at elevated temperatures.

$V_{GS(th)}$ comparison at T_J=25°C vs. T_J=25°C

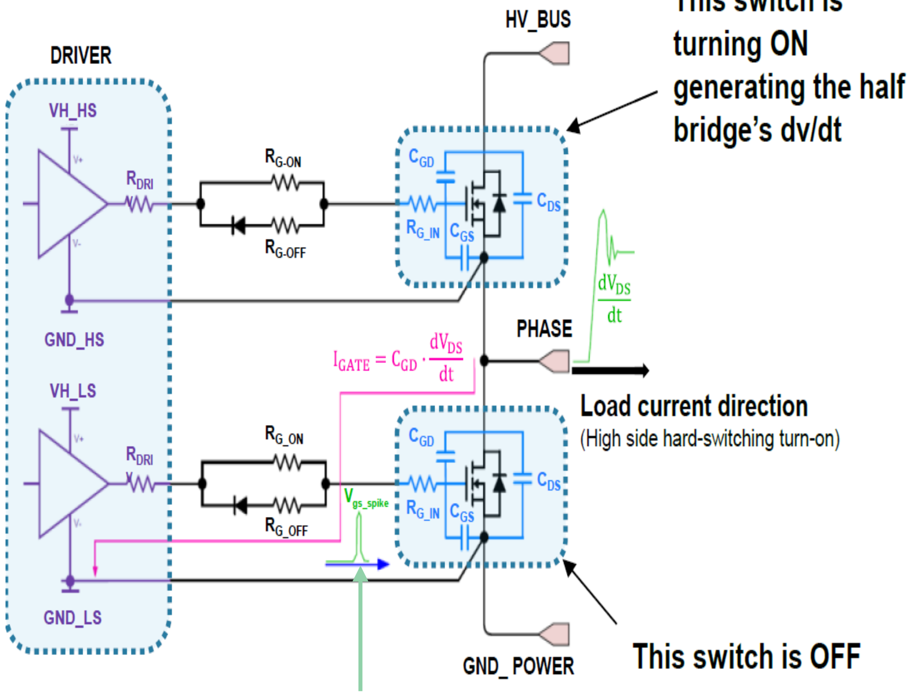


Techniques to reduce Gate Voltage glitch effect

Fine tuning RG

- **Gate resistance:**
  -- In Initial status, R_{G_ON}, R_{G_OFF} select a gate resistance such that the ratio is $R_{G\_ON}/R_{G\_OFF} \geq 1.5$.
  -- This ensures faster turn-off compared to turn-on, reducing the risk of Miller turn-on.
  -- V_{gs_spike}(glitch) vs R_G do not have a definite positive or negative relationship.

Reference topology



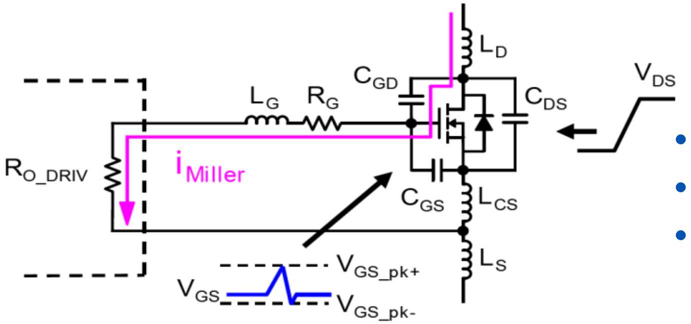
This switch is turning ON generating the half bridge's dv/dt

Load current direction
(High side hard-switching turn-on)

This switch is OFF

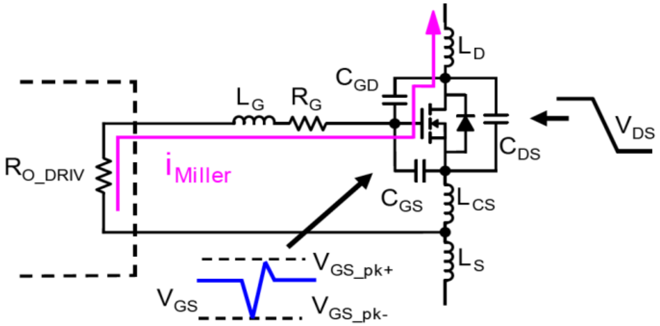
V_{gs_spike}(glitch) = I_{GATE}*R_G = $\mathbf{C_{GD}}$*$dV_{DS(S2)}/dt$* R_G

Miller current generation with positive dv/dt



- V_{gs_spike}=I_{GATE}*R_G=$\mathbf{C_{GD}}$*$dV_{DS(S2)}/dt$*R_G
- Higher dV_{DS}/dt happens suddenly.
- $V_{gs\_spike}\downarrow$ = I_{GATE} * $R_G \downarrow$

Miller current generation with negative dv/dt



- V_{gs_spike}=I_{GATE}*R_G=$\mathbf{C_{GD}}$*$dV_{DS(S2)}/dt$*R_G
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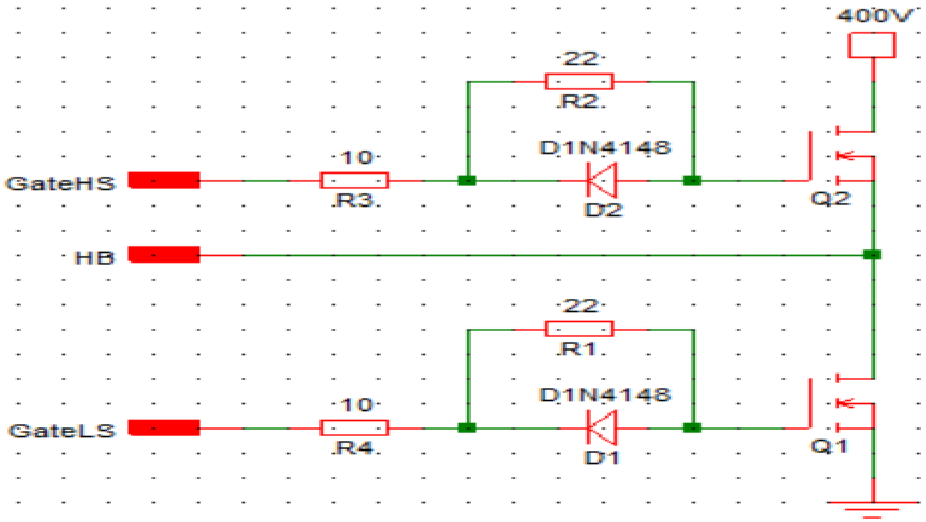
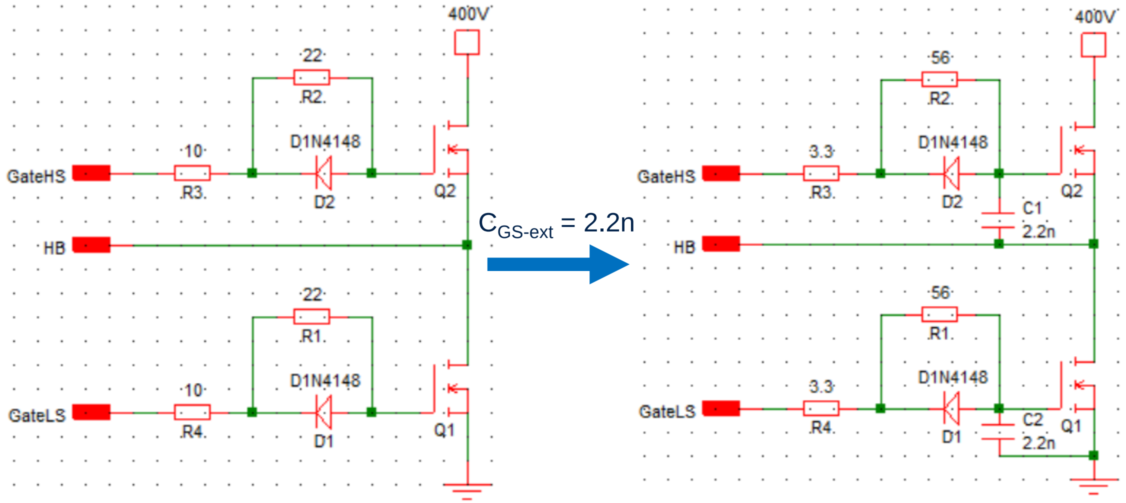
CGS-ext

LLC topology and driver circuit



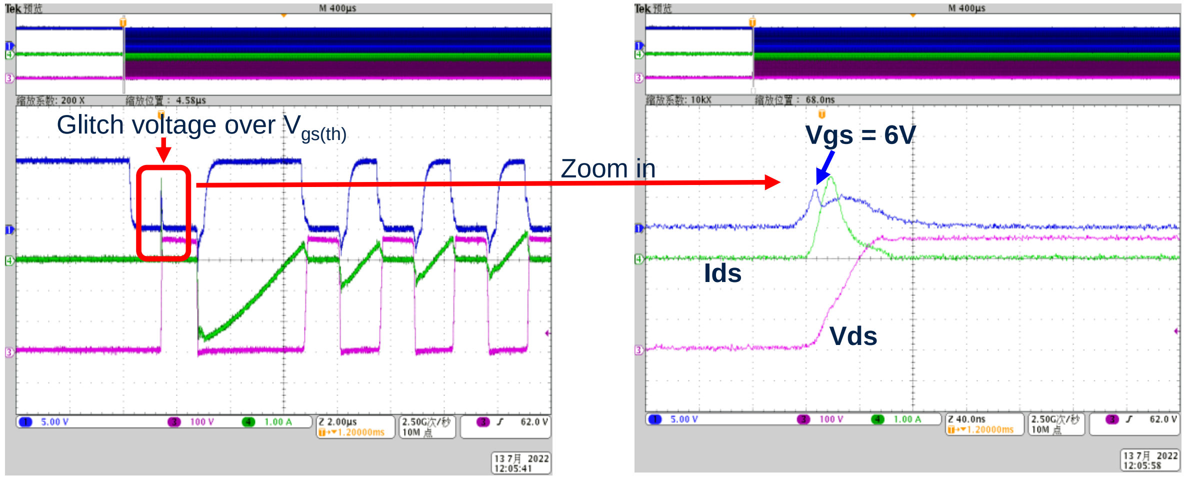
Add 2.2nF to $C_{GS\text{-}ext}$



Initial waveforms and Vgs_spike

Test condition: LLC start-up

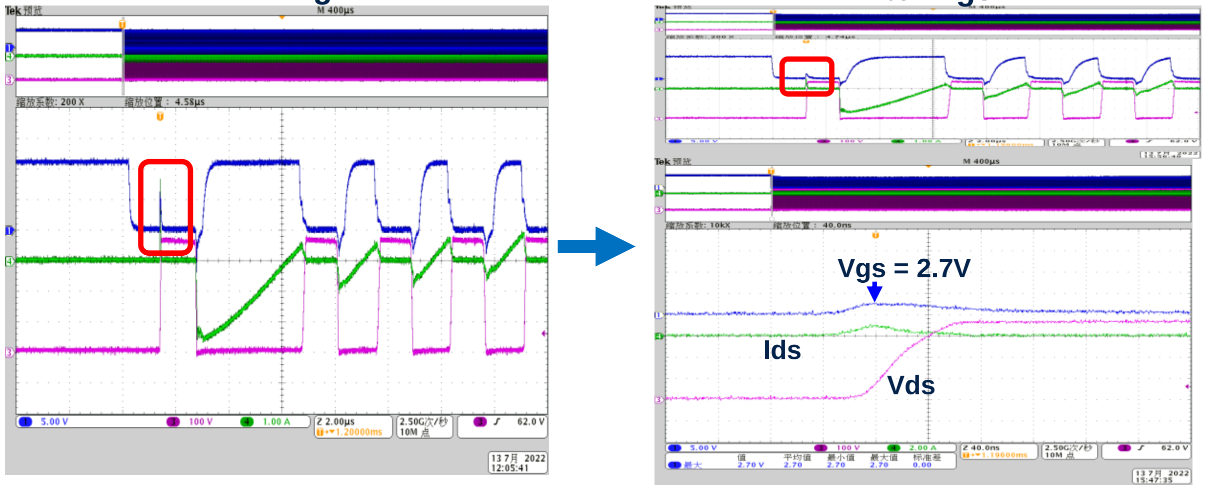
Test condition: LLC start-up



Add Cgs 2.2nF waveforms and Vgs_spike

Before Vgs=6V

After Vgs=2.7V



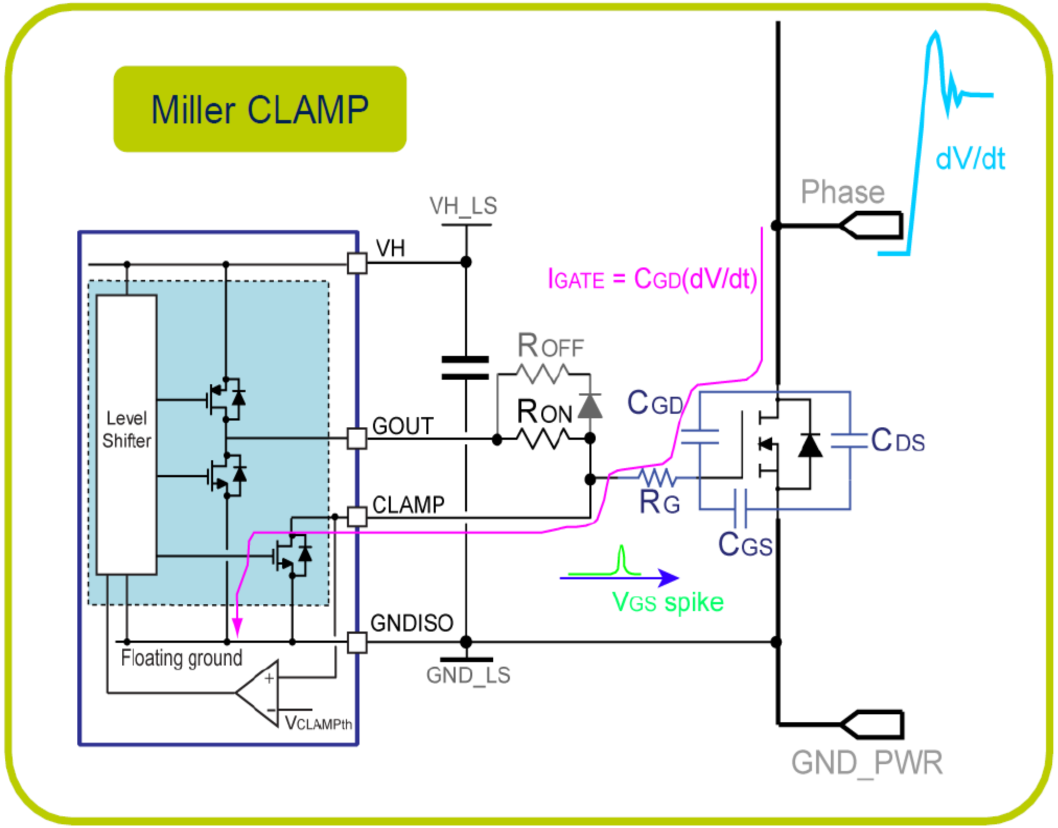
Active Miller Clamp

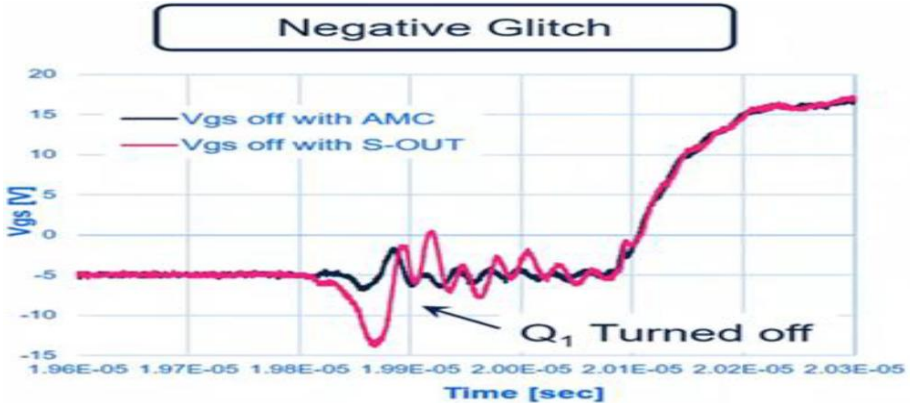
Active Miller Clamp:

-- use a gate driver with an active Miller clamp to prevent the gate voltage from rising due to the Miller effect during switching.

-- Negative Vgs bias can improve SiC Mosfet staying at turn-off conditions.

-- The Miller clamp function is effective during SiC Mosfet turn-off and does not affect SiC turn-on.

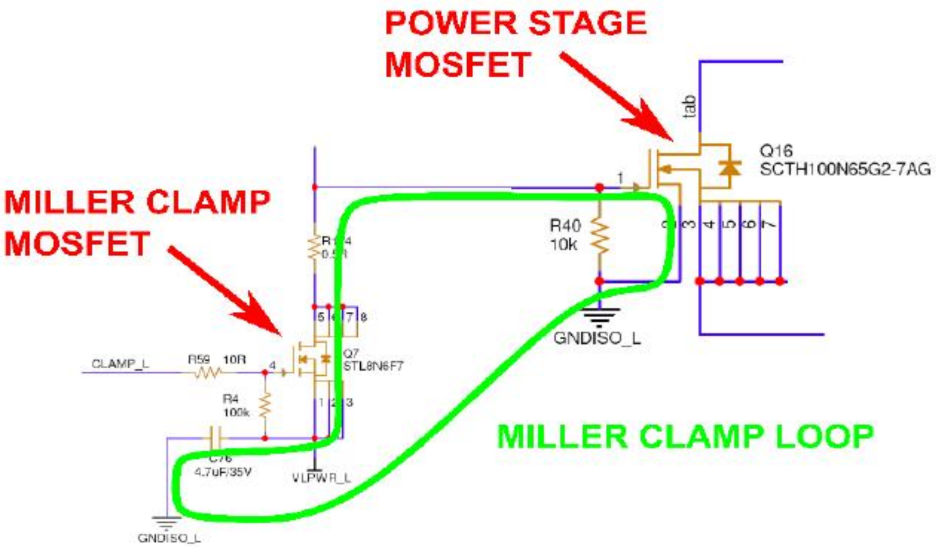


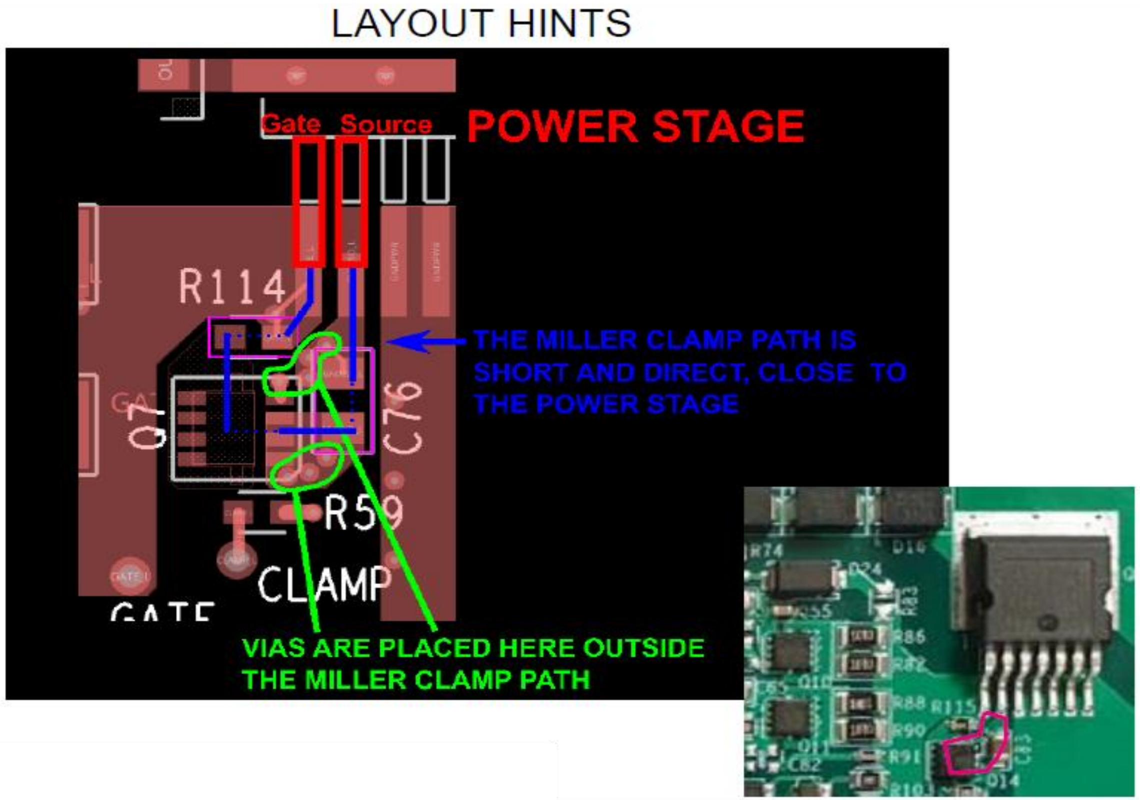


Layout

SiC driver layout guide:

-- Prefer SiC MOSFET with Kelvin source pin.
-- Keep Miller clamp loop closest as possible to power stage.
-- Keep the routing short as possible.
-- Keep the clamp loop with the small area as possible.
-- Avoid vias in the path.



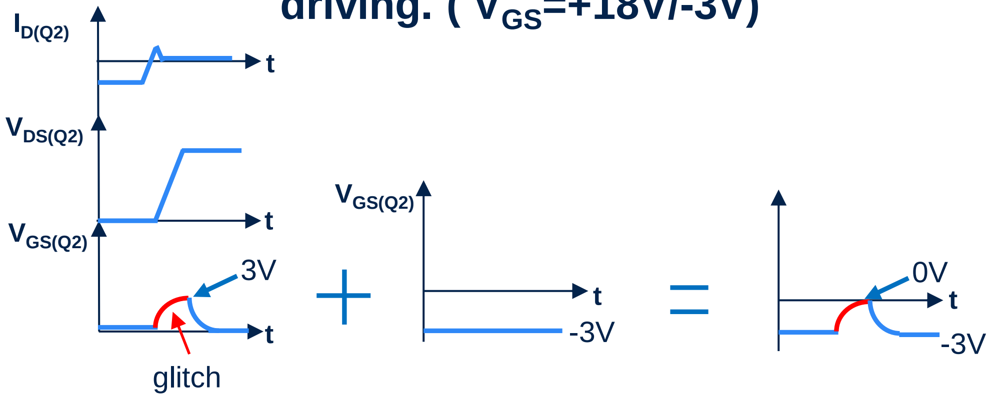


THE MILLER CLAMP PATH IS SHORT AND DIRECT, CLOSE TO THE POWER STAGE

VIAS ARE PLACED HERE OUTSIDE THE MILLER CLAMP PATH

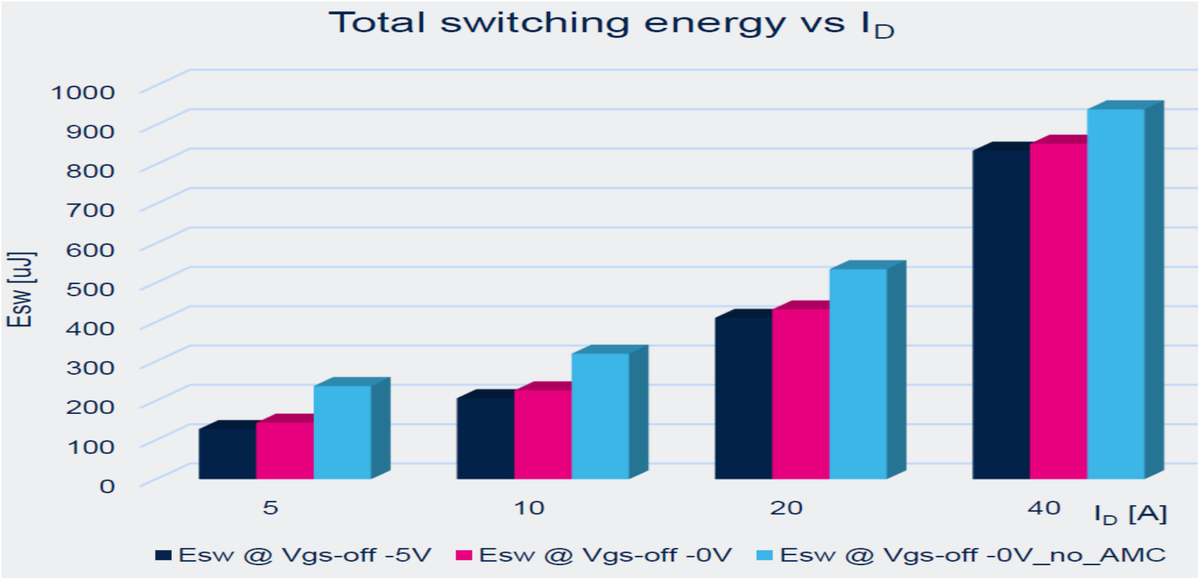
Negative gate driving

The more effective way to reduce glitch is negative gate driving. (V_{GS}=+18V/-3V)



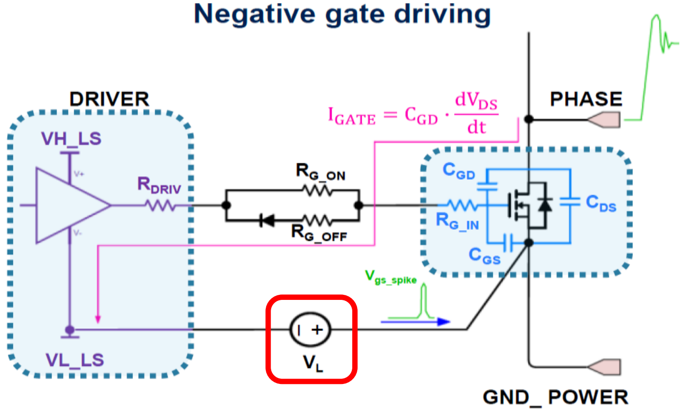
Energy comparison bipolar vs unipolar driving

Experimental data on 650V, SiC MOSFET Gen3, 29mΩ



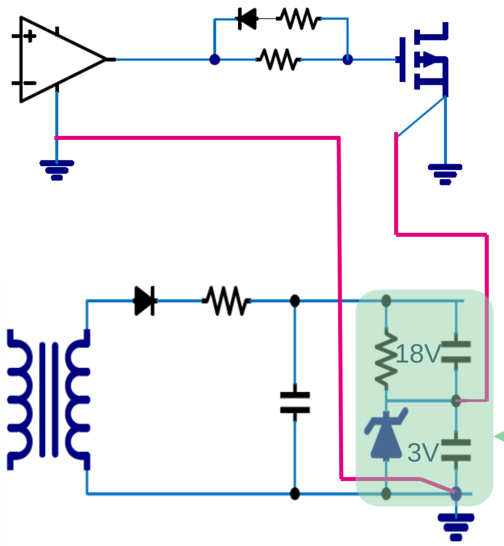
Optimize negative gate driving circuit

Negative gate driving

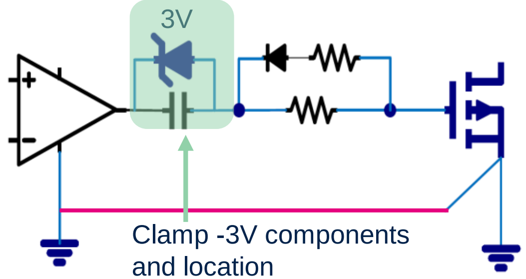


Traditional negative gate driving
→Create G, S long routing trace(pink).

Optimize negative gate driving
→G, S very short routing trace.



Clamp -3V components and location



Clamp -3V components and location

How to measurement V_{GS} in SiC applications

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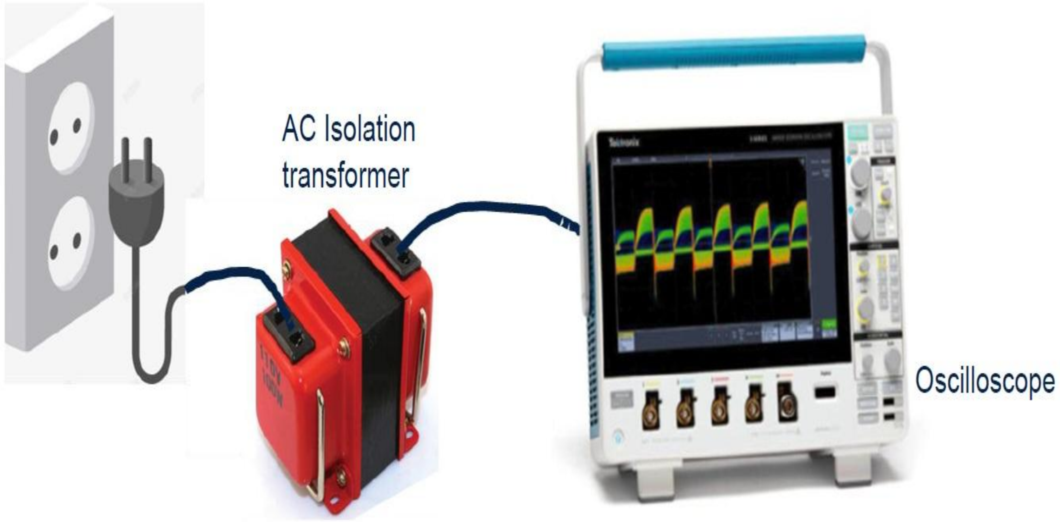
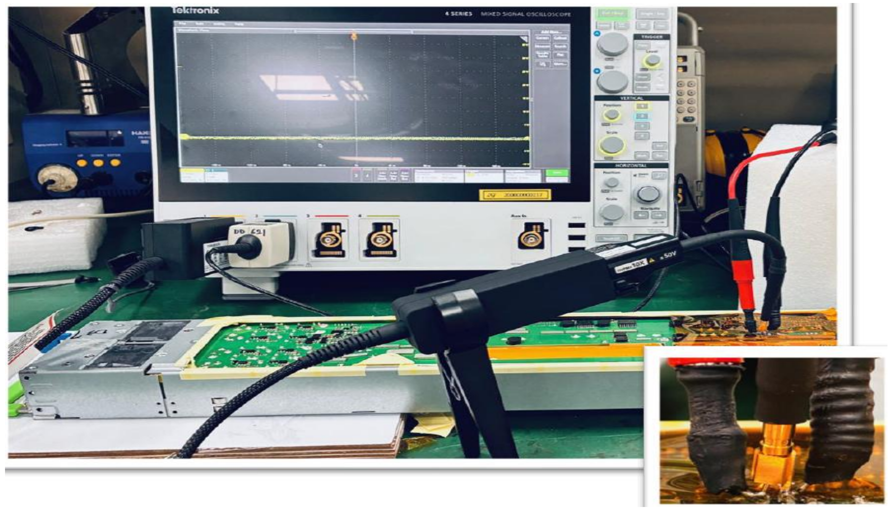
Measurement environment setting



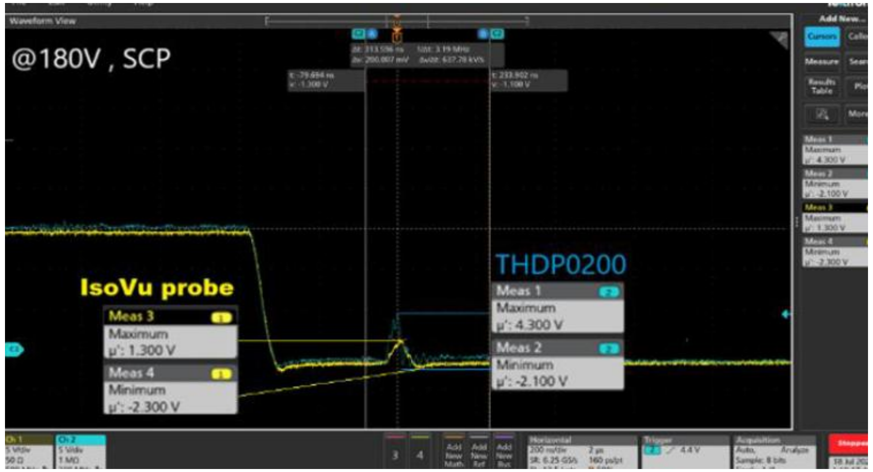

THDP0200


IsoVu probe

Compare waveforms between Iso Vu and differential Probes



Test result: Iso Vu probe= 1.3V, Different probe= 4.3V


@180V , SCP

IsoVu probe

Meas 3
Maximum
μ': 1.300 V

Meas 4
Minimum
μ': -2.300 V

THDP0200

Meas 1
Maximum
μ': 4.300 V

Meas 2
Minimum
μ': -2.100 V

Key SiC MOSFET parameters to consider

Kelvin Source

Inductively loaded switching clamp circuit

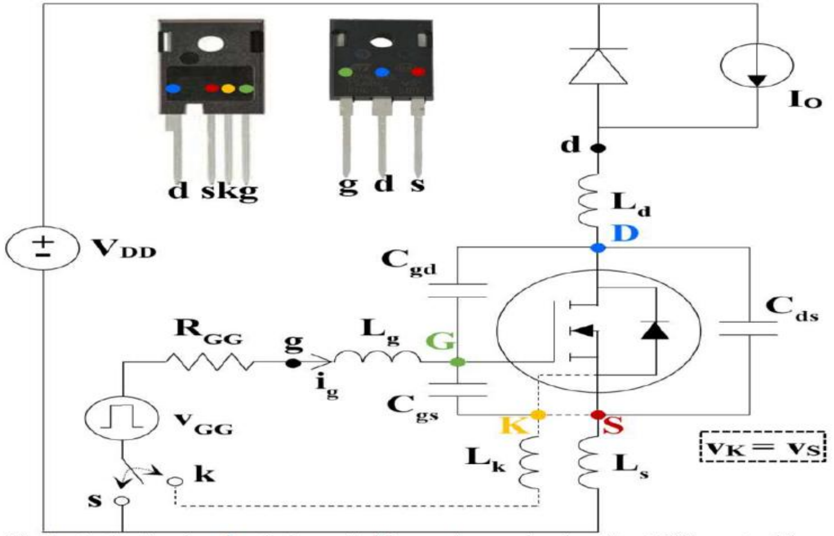


Fig.1 Inductively loaded switching clamped circuit. Different driver connection in case of 3-pin and 4-pin device. Ideal case: only parasitic inductances of the device are considered.

Test vehicle used for comparing TO-247-3L and TO-247-4L

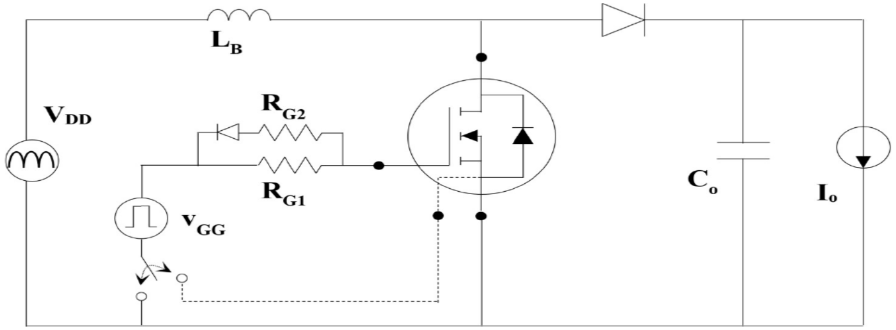


Fig.3 Test vehicle used for comparing the TO-247-3L and the TO-247-4L MOSFET: boost converter operated in continuous-conduction-mode.

TO-247-4L efficiency and temperature are better than TO-247-3L.

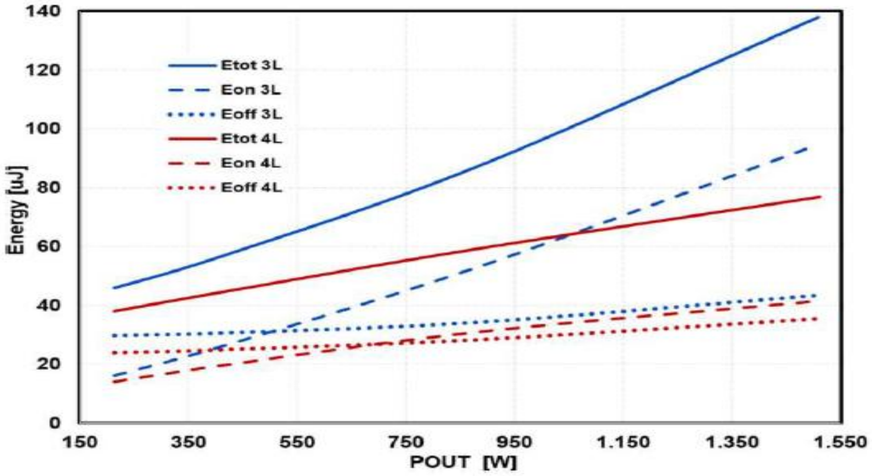
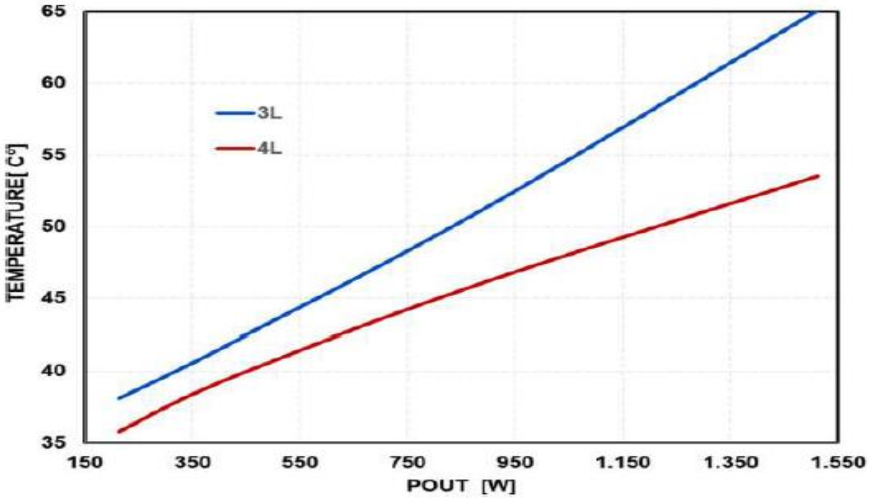
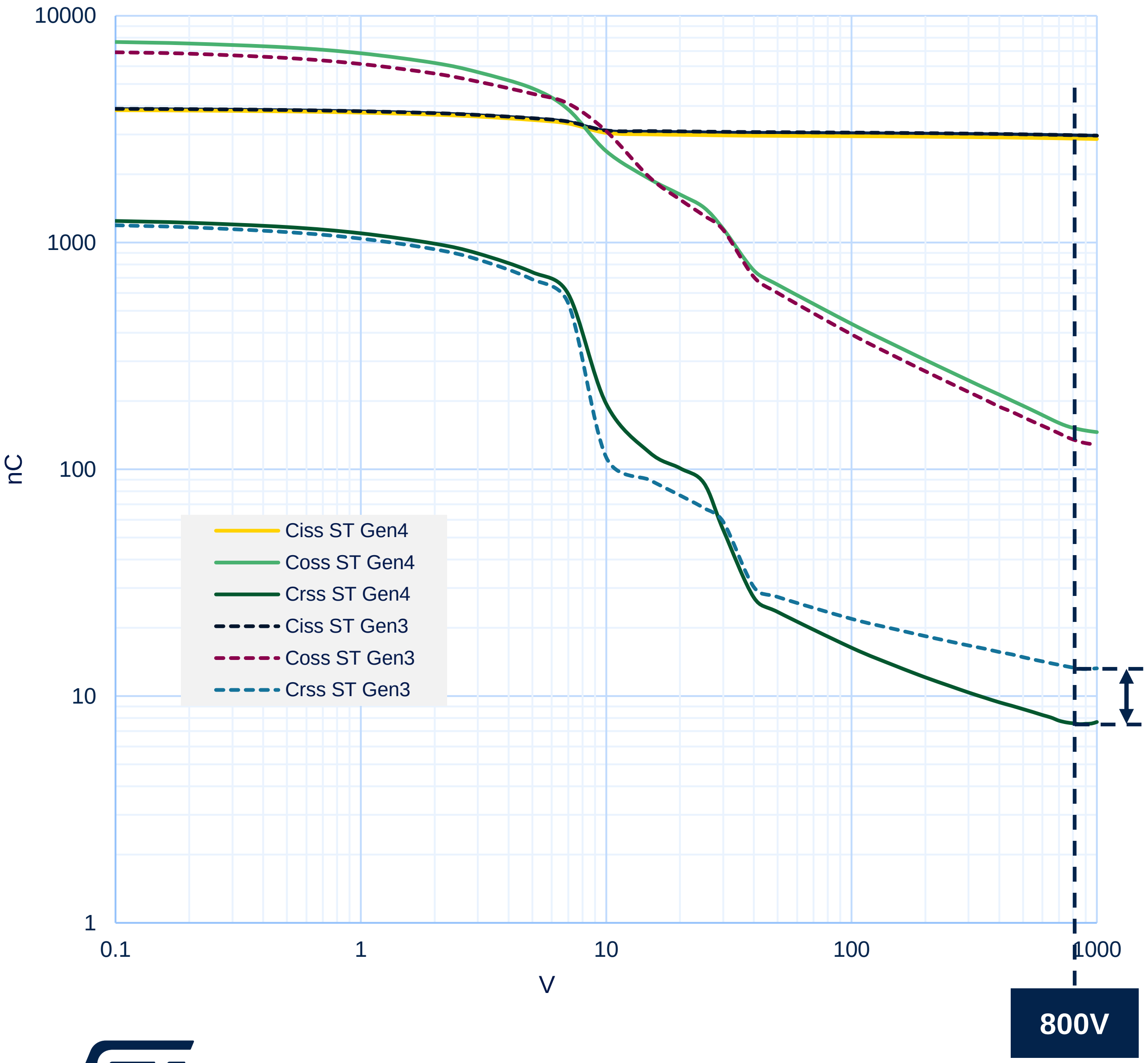


Fig.6 Experimental evaluation of the switching energy losses vs. different load conditions.



Crss

Capacitance variation



Gen4 vs. Gen3 capacitance variations

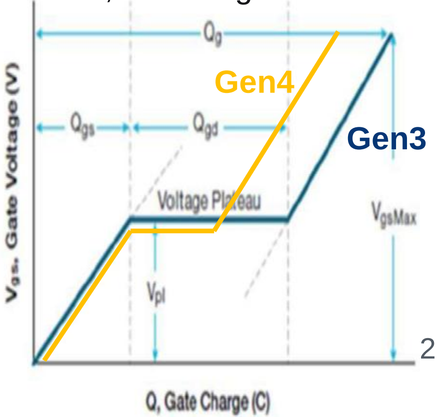
		Values [pf] (VDS=800 V)	
Parameter	**Symbol**	**ST Gen4**	**ST Gen3**
Input Capacitance	Ciss	2875.3	2976.5
Output Capacitance	Coss	152.3	135.3
Reverse Transfer Capacitance	**Crss**	**7.6**	13.3

-43%

Crss reduces 43%, Miller plateau reduces, switching loss reduces.

ST MOSFET Gen4 technology introduces **a significant reduction in reverse transfer capacitance,** enabling**:**

- Improved Miller ratio **Qgd/Qgs**
- Lower switching losses
- Reduce Parasitic Turn On.
  → $V_{gs\_spike} = \mathbf{C_{rss}} * dV_{DS(S2)}/dt * R_G$



Takeaways

Key takeaways

R_{gon} and R_{goff} (and the driving circuit in general) **can be tuned to optimize performance, minimizing spikes** and switching losses with negative and with zero-volt Vgs-off.

The comparison between -5 V and 0V shows negligible differences in case of typical threshold voltage ($V_{TH(typ)}$).

For design robustness, system and driving circuit design should consider **worst case V_{TH} and temperature**, factoring the additional energy loss in comparison with the case at typical V_{TH}.

Our technology
starts with You