Modeling and Experimental Verification of the Impact of Noise Sources on Projection Accuracy of Mems Linear Micromirrors for Raster Scanning Applications

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ABSTRACT

The architecture used for driving linear micromirrors in raster scanning systems is typically composed of digital circuits, responsible for generating a sawtooth-like reference signal synchronized to the fast axis, and analog circuits responsible of driving the device. Bridging the two domains is the D/A converter, typically clocked in the MHz range, whose noise sources and distortion affect the accuracy of the scan line. With typical refresh rates in the order of 60 Hz, simulating transistor-level implementations requires up to days for a few operating cycles (i.e. 1.7 cycles/day). This drives the need for accurate models of the dominant noise sources and their impact on scan accuracy, able to achieve verification times compatible with typical design flow timelines. The architecture of this work is composed of a sigma-delta based current-steering D/A converter, which is modelled analytically and behaviorally with its white and flicker noise sources and non-idealities. Each current generator is modelled independently to capture time-variant effects. The developed model can accurately predict noise both from Cadence simulations and experimental measurements, while also reducing simulation times by three orders of magnitude (i.e. 5.7 cycles/minute). The model thus allows to optimize the design and quickly verify the possibility to achieve a tilt-angle rms noise within 1 m° in open-loop driving conditions. Experimental results also show a significant distortion, which is not predicted by the model: as hypotheses on its root causes are formulated, the model will enable their investigation within reasonable times.

Keywords: MEMS, micromirror, projectors, linear, open-loop, model, noise

1. INTRODUCTION

Linear micromirrors are used to implement the vertical scan in raster scanning applications, such as pico-projectors or retinal scanner displays.[1] Such devices are typically driven by sawtooth signals, whose period corresponds to the refresh rate of the projected image, and may range from 60 Hz to even larger values.[2] In order to maintain a good accuracy of the vertical scan, and thus of the whole image, the circuit architectures to drive such devices are typically based on a digital core, like a microcontroller, an FPGA, or a dedicated DSP, that generates the drive waveform with a sufficient degree of accuracy. This is particularly important given the necessity to compensate the fairly large quality factor (e.g. 100) shown by micromirrors although operated in air, that generates a significant distortion as the sawtooth frequency approaches the mechanical resonance frequency, which is typically very low (e.g. 500 Hz to few kHz).[3] A pre-filtering of the drive signal is thus mandatory when operating the device in open-loop conditions in order to maintain accuracies in the positioning of the image pixels within a few tens of m°,[4] and thus a digital processing core is practically unavoidable.

However, micromirrors need be actuated by very large analog signals, in order to achieve a significant field-of-view (FOV). Mirrors based on electrostatic actuation, for example, require voltages in the order of few hundreds of volt [REF], whereas devices based on piezoelectric actuation require smaller, but still quite large, voltages in the order of tens of volt [REF]. The latter, in particular, typically also offer a significant load to the driving circuits, with large piezoelectric actuators reaching even nF capacitances. Hence the digitally generated signal needs to

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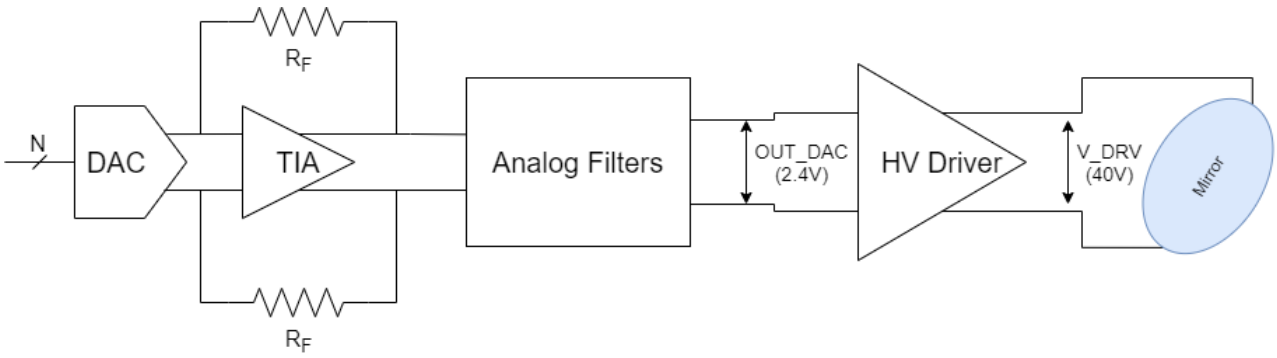

Figure 1. Linear Driver block diagram. DAC converts N-bit input word in the analog domain. The DAC output current signal is transformed in voltage, filtered and provided to the High-Voltage driver.

be processed by a digital-to-analog converter (DAC) and subsequently amplified by a power stage capable of generating the large actuation voltages while still being able to drive large capacitive loads. All the added analog circuits, especially the DAC, introduce a plethora of noise sources and non-idealities that contribute to worsening the projected image accuracy. The process of designing a custom integrated circuit must be accompanied by a careful study of the non-idealities introduced by the chosen circuit topology and their effect on the mirror tilt angle, in terms of noise and distortion, as both will worsen the perceived image quality.

In this scenario, transistor-level simulations of mixed-signal circuits, even assisted by behavioral models, become quite cumbersome and time consuming, especially considering the typical image refresh rates, resulting in simulation speeds as low as 1.7 cycles/day when simulating even a simple 60 Hz sinusoidal signal. Transient time simulations are also unavoidable for a proper validation of the design, as they allow to identify any time-variant phenomenon that may be missed by performing simpler analyses. It is thus mandatory to assist the design by a careful modeling of the system, capable of offering significantly faster simulation speeds while still retaining the capability to properly simulate noise and non-ideal effects.

This work presents a dedicated custom topology for the DAC used in the driving chain of a linear microscanner. The converter has been modeled both analytically and through behavioral modeling, resorting to MATLAB and Simulink software, with the aim to verify the circuit behavior and optimize the design. After a brief description of the circuit topology, a model of the converter is presented, following a stationary noise analysis and a time-variant one. Additional second order effects are described before comparing the results to a transient time simulation performed via Cadence software as well as experimental data obtained by fabricated test chips.

2. CIRCUIT DESCRIPTION

The digital data provided by a generic DSP engine are converted by the DAC in the analog domain and used as input for the Linear Driver block whose topology depends on the specific micro-mirror solution. Moreover, if on one side the performance in terms of bandwidth is not so challenging, on the other side the output noise requirements and the reduced power consumption lead to non-trivial designs. Linearity (such as THD, total harmonic distortion, performances) are often not critical due to control loop adjustment, nevertheless, in order to guarantee proper driving performances and to simplify the control loop implementation, at least 15 bits of equivalent absolute resolution should be realized. From an electrical standpoint, piezoelectric micromirrors behave like a simple capacitive load whose value is usually in the range of 1 nF-50 nF. In order to get an acceptable opening angle, a maximum voltage close to 40 V is required. Considering all the above-mentioned requirements, a specific driving architecture for piezoelectric micro-mirrors in presented in Figure 1. The digital samples defining the driving signal are provided to the input of a current steering DAC. Both a Nyquist and a $\Sigma\Delta$ approach can be followed for DAC design. Considering the desired resolution, $\Sigma\Delta$ implementation allows to strongly relax the design by exploiting oversampling to reduce quantization noise. The only recommendation in case of an oversampled DAC implementation is to ensure a proper quantization noise filtering. This comes almost for free since, in such kind of chain, the output load (the mirror) offers a 2nd order filter. Additional filter

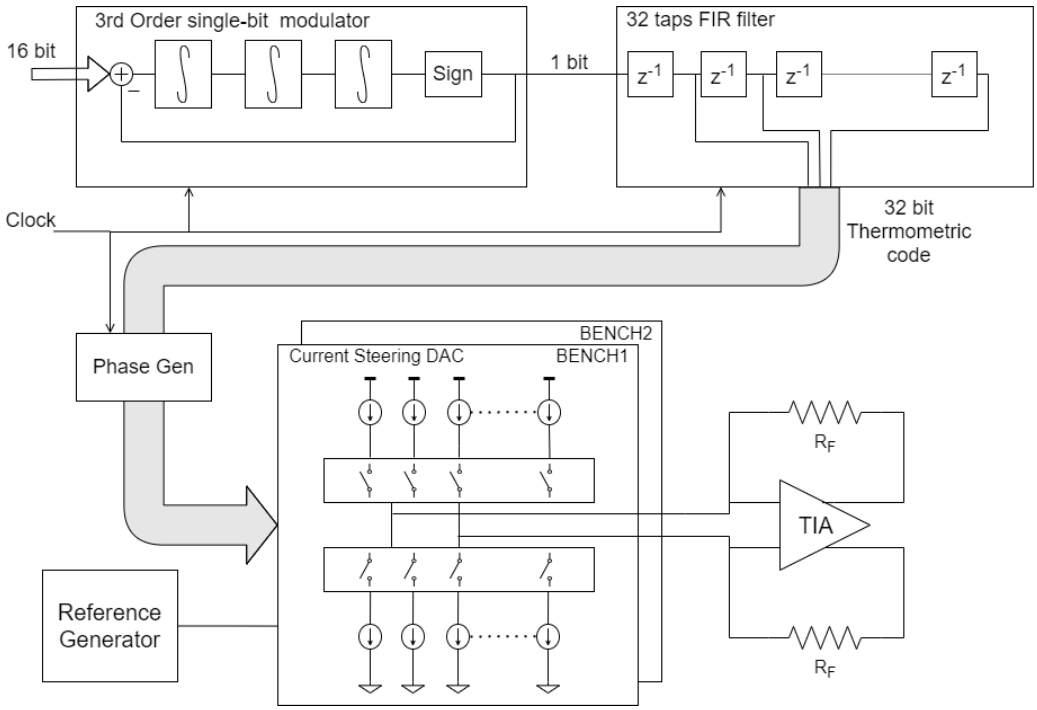

Figure 2. Single-Bit ΣΔ Steering Current DAC Architecture

orders can be implemented into the intermediated stages taking advantage of the fact that the chain itself must manage only low frequency signals, although low-frequency poles typically reduce the phase margin in view of a possible closed-loop approach.

ΣΔ DAC are generally designed with a N-bits thermometric topology that can be driven either directly through a dedicated N-bits bus or via a single-bit signal implementing well-known additional FIR filtering. Independently on the chosen DAC architecture, noise reduction (mainly low frequency) is a task that needs to be faced during the steering current generators design. On top of usual hints (low-pass filter for current seed and large area device) the use of a ΣΔ DAC implementation allows to directly integrate some approaches, such as Large-Scale Excitation (LSE) and scrambling, quite useful as additional means to contain the low frequency noise sources.

The adopted implementation, presented in this paper, is composed by a Single-Bit ΣΔ DAC whose architecture is shown in Figure 2. The single-bit digital signal is obtained from a digital 3rd order ΣΔ modulator and is applied to a 32 tap FIR filter with unitary coefficients whose outputs are processed by a local digital block that creates the phase signals for the steering of currents. The DAC is composed by a bias section that provides the voltage references to the current generators, grouped in two benches in order to perform three possible operations. The first is NRZ (Not Return to Zero) Mode, in which only one bench is used whereas the other is kept in power down. This is the worst scenario both in terms of linearity (Inter-Symbolic Interference, ISI) and in terms of noise (1/f noise of the current generators not canceled). The second is DRZ Mode (Double Return to Zero): this approach allows to reduce the ISI by alternatively switching, during a single clock period, both benches. The current generators not used are kept in power-on and connected to a reference voltage sink. The third is LSE Mode (Large Scale Excitation): This approach allows to move the 1/f noise at high frequency. The current generators benches are switched alternatively. The generators that are not used are set in power down in order to "reset" their flicker noise component thus moving the noise around the switching frequency and beyond the mirror bandwidth.

The digital information, once converted into a current, is transformed in a voltage signal by means of a Trans-Impedance Amplifier (TIA) whose gain, given by the value of a feedback resistor R_F, is properly sized to produce

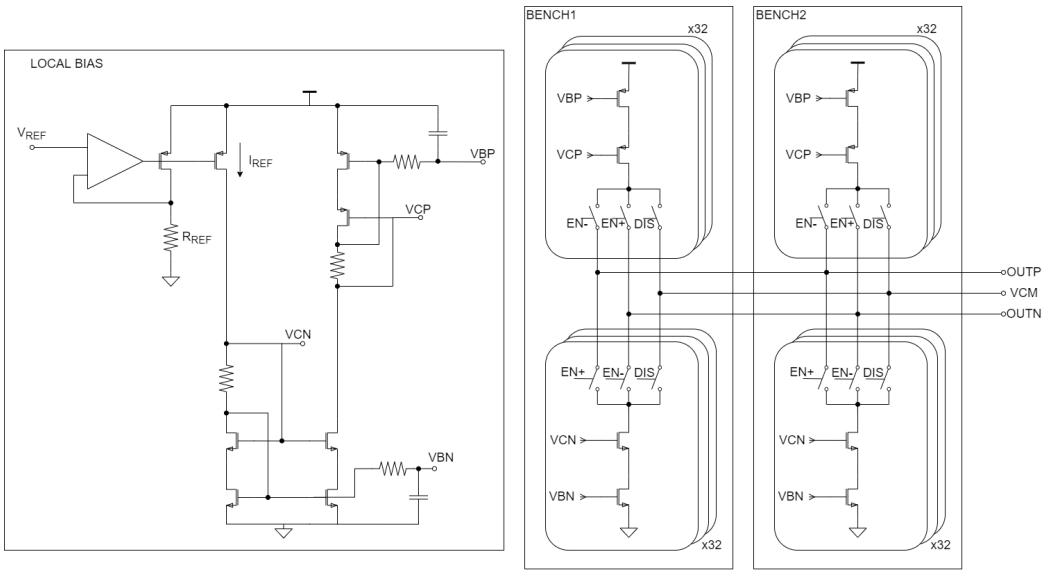

Figure 3. Reference current generator and DAC mirrors.

the maximum dynamic (set to 4.8 V peak-to-peak). The circuital core of the Steering Current Digital-to-Analog Converter is shown in Figure 3. A local bias block, starting from the reference voltage V_{REF}, generates the current I_{REF} that is replied and rescaled in order to properly produce the controlling voltages VBP and VBN for the P/N current generators (32 for each bench) and the voltages VCP, VCN for their corresponding cascode MOSFETs. Depending on the FIR filter output code and on the DAC operation modality, a group of three switches may connect each current generator either to the TIA positive input or to the TIA negative input or to the TIA input/output common voltage VCM or eventually keeping it disconnected. In this last case the generator wont produce any current. Since the reference current I_{REF} is obtained from the ratio V_{REF}/R_{REF}, being the resistors R_{REF} and RF of the same type and constructed with the same resistive modules, the converted output can be considered with good approximation independent from process variations.

3. CIRCUIT MODEL

To evaluate the expected projection accuracy it is mandatory to model the dominant circuit non-idealities. The main source of error is the noise of the analog stages, especially white and flicker noise of the transistors that implement the current generators. An additional challenge is to also account for time-variant effects related to the switching of the current generators and its effect on flicker noise. An additional contribution comes from the input referred noise sources of the operational amplifiers used for the trans-impedance amplifier (TIA) and the low-pass filters (LPF). As additional error sources, the switching delay between current generators and the finite rise and fall time of the steered currents are considered, that may generate significant ISI. These effects are modeled first of all from an analytical standpoint, and are subsequently verified by an optimized MATLAB code and a Simulink model. The developed models allowed to increase simulation speed up to 5.7 cycles/minute when simulating a 60 Hz sinusoidal signal.

3.1 Stationary Noise Analysis

The stationary noise analysis is carried out by setting the taps of the FIR filter to a fixed configuration and evaluating the output noise. In order to perform a fair comparison with Cadence AC noise simulations, the noise is first evaluated and simulated at the output of the low-pass filter stages. The technological parameters needed for modeling are extracted by Cadence simulation of the elementary blocks.s. The analytical noise power spectral densities according to the model are shown in Fig. 4. Flicker noise is the dominant contribution within the entire bandwidth, limited to about 50 kHz.

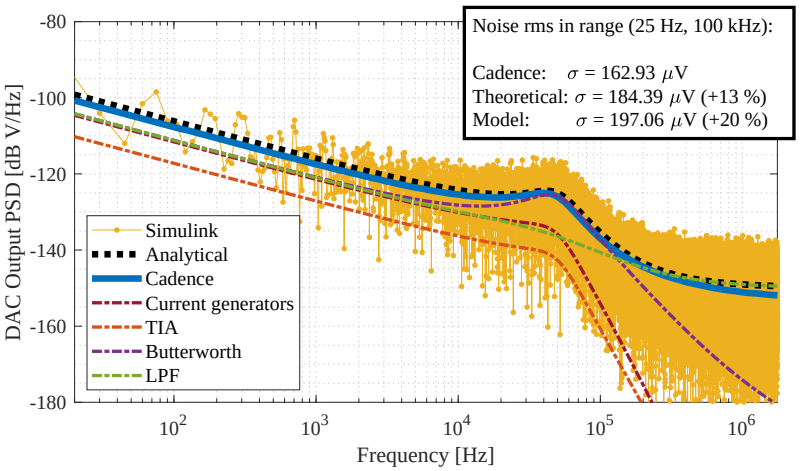

Figure 4. DAC output noise spectrum provided by the stationary noise analysis. The plot shows a comparison of the individual effect of all the noise sources. The theoretical model and the behavioral models agree within 20%, likely due to imperfect modeling of technological parameters.

The achievable angle accuracy can be derived by combining the total noise density with a model of the modulator quantization noise, and by filtering them by a model of the mirror transfer function, defined as:

$$H_m(s) = \frac{H_0}{1 + \frac{s}{\omega_0 Q} + \frac{s^2}{\omega_0^2}} \tag{1}$$

where H_0 is the DC gain relating the driving voltage amplitude to the tilt angle (in the order of 13° for the results discussed in this work), whereas ω_0 is the resonance frequency (i.e. 700 Hz), and Q is the quality factor (i.e. 100). From the corresponding power spectral densities shown in Fig. 5, shown for different analog filtering configurations, two conclusions can be drawn. First of all, the integrated noise does not depend on the analog low-pass filters. The simple TIA would be sufficient to suppress the modulator quantization noise, once the mirror transfer function is taken into account. Indeed, for a third order modulator, the cascade of moving average, single-pole TIA and two-pole mirror transfer function is enough to attenuate high frequency noise, which is then clearly dominated by low-frequency flicker noise. Secondly, the overall estimated integrated noise, resulting in 0.29 $\mathrm{m°_{RMS}}$, is actually dominated by noise amplified by the peak of the MEMS transfer function, suggesting that a closed loop operation of the device able to dampen the quality factor would provide a large

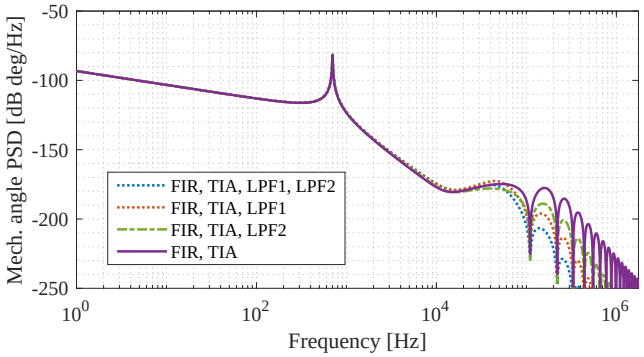

Figure 5. Angle power spectral density from the theoretical noise analysis for different filtering configurations, considering three analog filters (the 32-tap FIR, the TIA, a 2nd order Butterworth, LPF1, and a 1st order low-pass filter, LPF2).

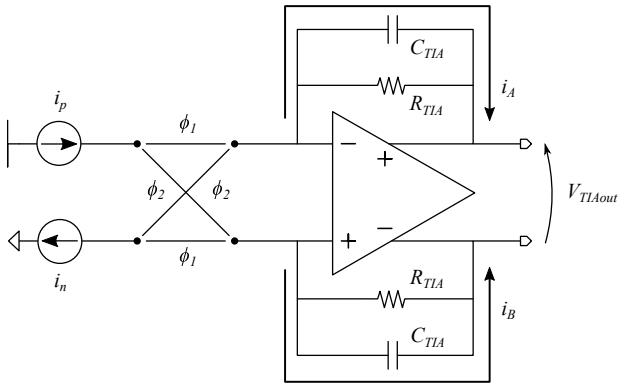

Figure 6. Simplified model for the time-variant analysis of flicker noise.

improvement on the already small integrated noise, although itself introducing additional error sources.

3.2 Current Generators Noise

As flicker noise is the dominant contribution, a more rigorous treatment is needed. Indeed due to its autocorrelation and the current steering between the input terminals of the TIA, the output noise is expected to be time-variant and dependent on the switching pattern. The following analysis applies to NRZ mode.

As represented in Fig. 6, the problem can be simplified by considering only one pair of current generators (that is, one nMOSFET and one pMOSFET). The currents flowing in the two feedback branches of the TIA are dependent on the instantaneous state of the switches, and can be written as:

$$\begin{aligned} i_A(t) &= N_k(t) i_{p,k}(t) + \overline{N}(t) i_{n,k} \\ i_B(t) &= \overline{N}_k(t) i_{p,k}(t) + N(t) i_{n,k} \end{aligned} \tag{2}$$

where the subscript k indicates the k-th pair of transistors, the subscripts p and n represent the type of transistor, and $N(t)$ represents the state of the switches. This signal assumes values of 0 and 1: if $N(t) = 1$ the pMOSFET is connected to the upper branch and the nMOSFET to the lower branch, and vice-versa if $N(t) = 0$.

Since the 32 generator pairs are driven by the 32 independent taps of the FIR filter, the total currents can be simply derived by summing all the contributions, which effectively implements the intended moving average:

$$\begin{aligned} i_A(t) &= \sum_{k=1}^{n_{tap}} N_k(t) i_{p,k}(t) + \sum_{k=1}^{n_{tap}} \overline{N}(t) i_{n,k} \\ i_B(t) &= \sum_{k=1}^{n_{tap}} \overline{N}_k(t) i_{p,k}(t) + \sum_{k=1}^{n_{tap}} N(t) i_{n,k} \end{aligned} \tag{3}$$

where $n_{tap} = 32$. In terms of noise currents, since all the individual noise sources are uncorrelated, once the output voltage spectrum is calculated for one pair, the total noise density is simply obtained by multiplying the result by a factor n_{tap}.

As briefly shown in the following, the stage effectively operates a modulation of the noise that strictly depends on the shape of the mirror driving signal. The time-variant differential current is:

$$i_k = i_A(t) - i_B(t) = (i_{pk}(t) + i_{nk}(t)) \cdot \Delta\phi_k(t) \tag{4}$$

having defined the two modulation phases $\phi_{1k}(t) = N(t)$ and $\phi_{2k}(t) = \overline{N}(t) = 1 - N(t)$ respectively, and $\Delta\phi_k = \phi_{1k} - \phi_{2k}$. Calculation of the autocorrelation function yields:

$$R_i(t, \tau) = E[i(t)i(t+\tau)] = (2N(t) - 1)(2N(t+\tau) - 1) \cdot R_{pn}(\tau) \tag{5}$$

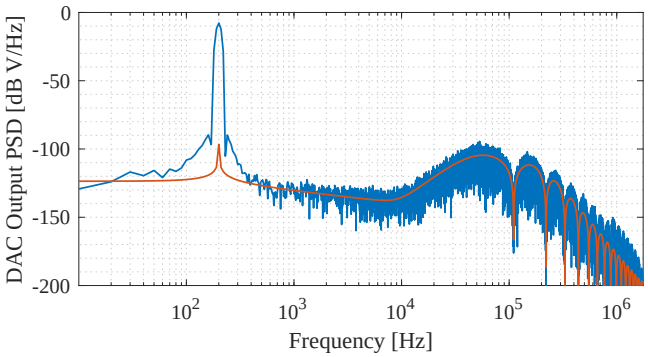

Figure 7. Power spectral density of the DAC output voltage with an applied 60-Hz sinusoidal signal, showing the contributions of the ΣΔ modulator and of the flicker noise obtained by Simulink modeling (blue line), matching the theoretical analysis (orange line).

where $R_{pn}(\tau)$ represents the autocorrelation of the sum $i_p + i_n$, and E is the expected value. Now since the TIA performs a low-pass filtering, the high frequency switching can be neglected and the final expression is much simplified. Noting that the time average of the modulation function can be expressed as a function of the input word $D(t)$:

$$\langle N(t) \rangle \approx \left\langle \frac{1}{2} + \frac{D(t)}{2} + q(t) \right\rangle \approx \left\langle \frac{1}{2} + \frac{D(t)}{2} \right\rangle \tag{6}$$

where $q(t)$ represents the zero-mean quantization noise, and taking the time average of the autocorrelation function:

$$\langle R_i(t,\tau) \rangle = (4\langle N(t)N(t+\tau) \rangle - 1) \cdot R_{pn}(\tau) = \Gamma(\tau) \cdot R_{pn}(\tau) \tag{7}$$

where $\Gamma(\tau) = \langle D(t)D(t+\tau) \rangle$, the result depends on the autocorrelation function of the input signal. Including now the contribution of all the generators, the noise spectrum at the output of the TIA due to the current generators is:

$$S_v(f) = n_{tap} \left| H_{TIA}(f) \right|^2 \cdot \mathcal{F} \left\{ \Gamma(\tau) \right\} * \sum_{j=n,p} \left(2k_B T \gamma_j g_{mj} + g_{mj}^2 \frac{K_{fj}}{W_j L_j f} \right) \tag{8}$$

where H_{TIA} is the TIA transfer function, k_B is the Boltzmann constant, $\gamma = 2/3$ for a transistor in saturation, g_m is the transconductance, K_f is the flicker noise coefficient, W and L are the transistor dimensions.

The modulation function $\Gamma(\tau)$ can be evaluated for simple driving, and in general for any periodic signal considering its Fourier series expansion. Below three examples are reported for a constant signal c, a sinusoidal signal and an ideal sawtooth both of period T:

$$\Gamma(\tau) = \begin{cases} c^2 & \text{if} \quad D(t) = c = \text{const.} \\ \dfrac{1}{8} \cos\left(\dfrac{2\pi}{T} \tau \right) & \text{if} \quad D(t) = \dfrac{1}{2} \sin\left(\dfrac{2\pi}{T} t \right) \\ \displaystyle\sum_{n=1}^{\infty} \frac{1}{8\pi^2 n^2} \cos\left(\frac{2\pi n}{T} \tau \right) & \text{if} \quad D(t) = \dfrac{1}{2} \left(\dfrac{t}{T} - \left\lfloor \dfrac{t}{T} \right\rfloor \right) \end{cases} . \tag{9}$$

As shown in Fig. 7 the implemented model correctly matches the theoretical expectation. Time domain modeling of flicker noise in both the MATLAB and Simulink models is based on works by Corsini and Saletti.[5]

3.3 Activation Delay

The activation delay between generators produces an error in the injection of current into the virtual ground of the TIA, which can be modeled as a noise in terms of image resolution. The issue arises during transitions of the state

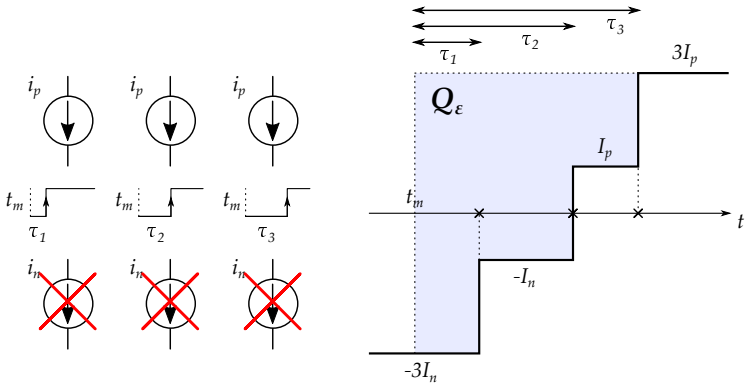

Figure 8. Schematic view of the error charge generated by activation delays.

N for any of the current generators. The first tentative model that is proposed consists in accounting for delays between different generator pairs, that may arise due to asymmetries in the traces layout. The issue is illustrated in Fig. 8 in terms of the differential current $i(t)$ considering only three generators whose state N transitions from 0 to 1 at different delays τ from the ideal onset. The error current is a sum of rectangular contributions whose amplitude depends on the transition times. As long as the fastest generator hasn't transitioned, the error is maximum and corresponds to $3I_p + 3I_n$. As the first generator transitions the error is reduced by $(I_p + I_n)$. When the slowest generator has transitioned, the final current value of $3I_p$ is set and the error becomes zero. Thus, during the transition interval, each generator contributes with an error equal to $(I_p + I_n)$. This results in the net charge error Q_ϵ represented in the figure. A similar argument can be made for the opposite transition from 1 to 0, leading to an elementary errors opposite in sign.

A generalized argument can thus be derived, with a few simplifying assumptions. The error current waveform corresponding to the m-th sampling interval of the converter is:

$$I_\varepsilon[m](t) = (I_p + I_n) \cdot \left[\sum_{k=1}^{n_\uparrow} \underset{\tau_k}{\mathrm{rect}}(t - t_m) - \sum_{k=1}^{n_\downarrow} \underset{\tau_k}{\mathrm{rect}}(t - t_m) \right] \tag{10}$$

where $n_\uparrow$ and $n_\downarrow$ represent the number of transitions $0 \to 1$ and $1 \to 0$ respectively, whereas $\mathrm{rect}(t - t_m)$ represents a rectangle function starting at the m-th sampling instant t_m with duration indicated by the underset τ_k, which represents the delay of the k-th generator. The expression is then simplified considering $\tau_k = \tau_\epsilon = \text{const.}\ \forall k$, assuming that τ_ϵ is much smaller than the sampling time, thus approximating the rectangle as a Dirac delta function, and considering that the difference between the number of transitions $n_\uparrow - n_\downarrow$ is equal to half the variation of the FIR output word between subsequent sampling intervals, that is $\Delta N[m] = N[m] - N[m-1]$. This allows to write the previous equation as:

$$I_\varepsilon[m](t) \approx \frac{(I_p + I_n)\tau_\epsilon}{2} \Delta N[m]. \tag{11}$$

Moving to the discrete domain dividing by the sampling time T_s yields the final expression:

$$I_\varepsilon[m] \approx \frac{(I_p + I_n)\tau_\epsilon}{2T_s} \Delta N[m] \tag{12}$$

which links the error to the derivative of the driving signal. To verify this result a sinusoidal driving signal can be considered. The FIR output word can be approximated as:

$$N[m] \approx \frac{n_{tap}}{2} \sin\left(\frac{2\pi m}{T} T_s\right) + q[m] * h_{FIR}[m]. \tag{13}$$

Further approximating the derivative with the cosine, knowing that the sampling frequency of a few MHz is much larger than the typical signal frequencies of about 60 Hz, and taking the Z-transform the following expression is

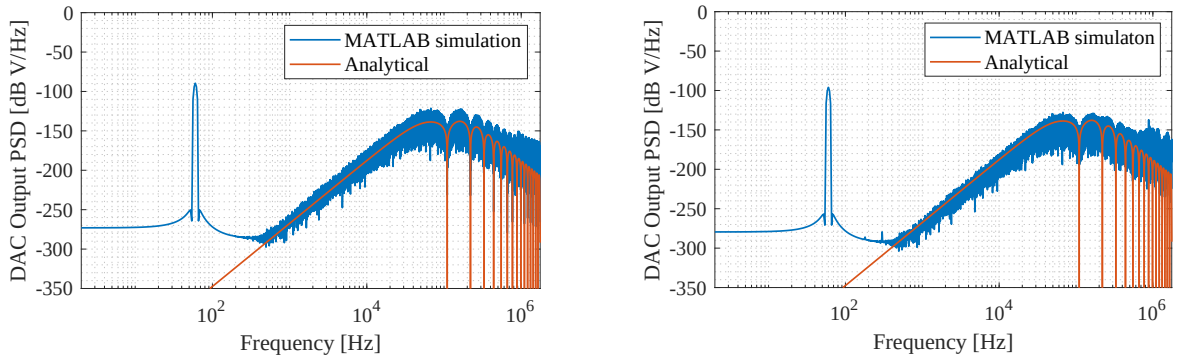

Figure 9. Comparison of the effect of activation delays between MATLAB behavioral simulation and theoretical prediction: (a) for constant delays of 200 ns, (b) for randomly distributed delays within 200 ns.

obtained:

$$I_\epsilon(z) = \frac{(I_p + I_n)\tau_\epsilon}{2T_s} \cdot \left[\frac{n_{tap}\pi T_s}{2T} \left(\frac{z}{z - e^{j2\pi T_s/T}} - \frac{z}{z - e^{-j2\pi T_s/T}} \right) + (1 - z^{-1}) q(z) H_{FIR}(z) \right] \tag{14}$$

where the first term represents the residual cosine error, and the second term is the differentiated quantization noise introduced by the modulator. The resulting error verified running two simulations with the MATLAB code with and without delay and performing subtraction of the resulting waveforms is shown in Fig. 9) for uniform and randomly distributed delays. In practice, this effect introduces no harmonic distortion, and the resulting high frequency noise is still dominated by the modulator quantization noise. Thus the effect of even significant delays up to half the sampling time (as shown in Fig. 9) should be practically negligible with the proposed DAC architecture.

4. COMPARISON BETWEEN MODEL AND CIRCUIT SIMULATIONS

Although time consuming, a comparison between model and Cadence transient simulations has been attempted. Both the model and the transistor-level circuit have been tested with a 600 Hz sinusoidal signal as the modulator input. For Cadence simulation, the output bitstream of the modulator has been first calculated using the MATLAB model, then this pattern was fed to the input of the FIR filter for proper transistor-level simulation, avoiding an even more time consuming AMS simulation adopting a behavioral model of the modulator. The result is shown in Fig. 10, where the spectrum of the output of the last LPF is shown both as an analytical expectation and as obtained by Simulink and Cadence data. Clearly the resolution of the spectrum obtained by circuit simulation is much worse, given that the CAD simulated only 5 cycles over 8 days of continuous simulation. In particular it is not possible to directly verify the low frequency trend of flicker noise in time-variant conditions. However, circuit simulations show an unexpected and quite large second harmonic distortion (about 72 dB), which was not predicted by simulating the model. This phenomenon is expected to be related to modulation of the virtual ground of the TIA, but so far it has not yet been included in the model.

5. EXPERIMENTAL RESULTS

An experimental validation was performed on an ASIC implementing the discussed DAC. Fig. 11(a) shows the DAC output spectrum with the current generators in a fixed state, corresponding to the model spectrum shown in Fig. 4. The developed model slightly overestimates the measured RMS noise value (+13%).

Fig. 11(b) shows the DAC output spectrum with an applied sinusoidal signal (1 kHz frequency), showing an even harmonic distortion that was not predicted by the model. The postulated source of such distortion is expected to be related to an overlap of the generators control phases, whose effect has not been included in the model so far, but will be the topic of future work. A circuit redesign aimed at removing any overlap between the phases has shown indeed no significant even harmonic distortion, as shown in Fig. 11(c), leaving only odd distortion that is still open to verification.

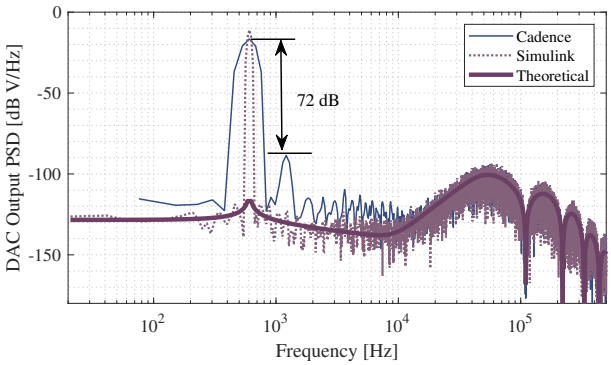

Figure 10. Comparison between the output spectrum obtained from theoretical analysis, behavioral Simulink modeling and Cadence simulations (limited by time constraints). Cadence simulations show a second harmonic distortion not correctly modeled.

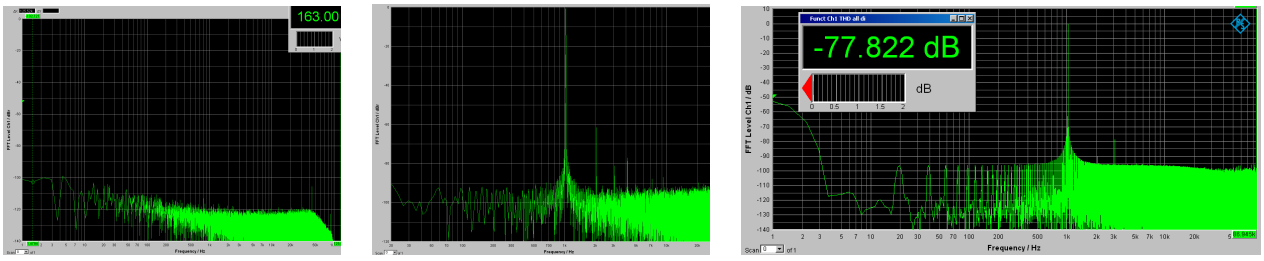

Figure 11. (a) Measured DAC output noise spectrum with the generator fixed in a single state, showing an integrated RMS value of 163 µV, matching Cadence simulations. The developed model slightly overestimates (+13%) this noise value. (b) Measured DAC output spectrum in NRZ mode with an applied 1-kHz sinusoidal signal, showing the harmonic distortion. The noise floor is limited by the driving pattern provided to the DAC. (c) Measured DAC output spectrum in NRZ mode for the re-designed chip. Even harmonic distortion is no longer appreciable.

6. CONCLUSION AND FUTURE WORK

This work presented an implementation of a digital-to-analog converter to be employed in the driving circuitry of linear micromirrors. Both analytical and behavioral models have been realized, with the aim of studying the impact of noise sources on the effective mirror tilt angle while reducing the time required for transient simulations at transistor level. While these are only able to simulate 1.7 cycles/day of a 60 Hz sinusoidal signal, due to the high frequencies involved, the developed behavioral models allowed to reduce simulation time enabling simulation speeds of to 5.7 cycles/minute, thus allowing to simulate and verify time-variant effects that can be predicted analytically. The model has also been useful to optimize the chip area by removing unnecessary analog filtering. While the model is still not able to correctly predict harmonic distortion observed by circuit simulation and experimental data acquired from a few test chips, future work will be focused on improving the model by understanding and including these effects. Additional effects that will be modeled are the non-ideal virtual ground of the TIA and the mismatch between current references to verify their effect on THD.

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