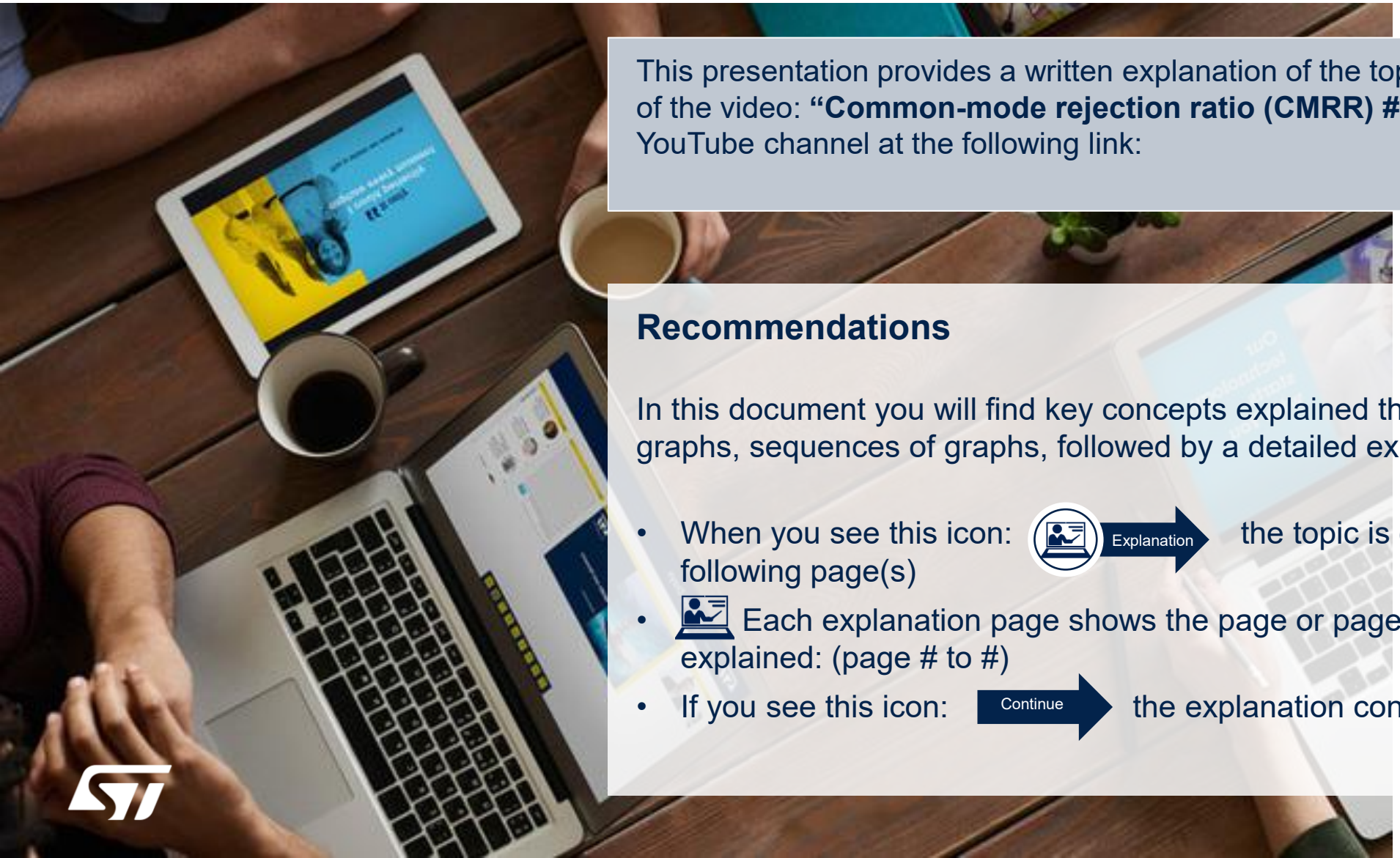
Exploring current sense amplifiers

STMicroelectronics Tech Days

Common-mode rejection ratio (CMRR)

Chapter 6

User guide



This presentation provides a written explanation of the topic covered in the fifth chapter of the video: **“Common-mode rejection ratio (CMRR) #6**”, which is available on our YouTube channel at the following link:

Video on YouTube

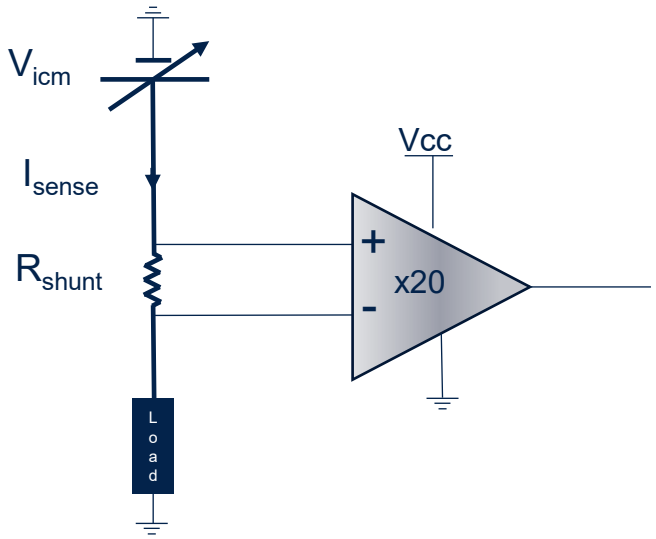
Recommendations

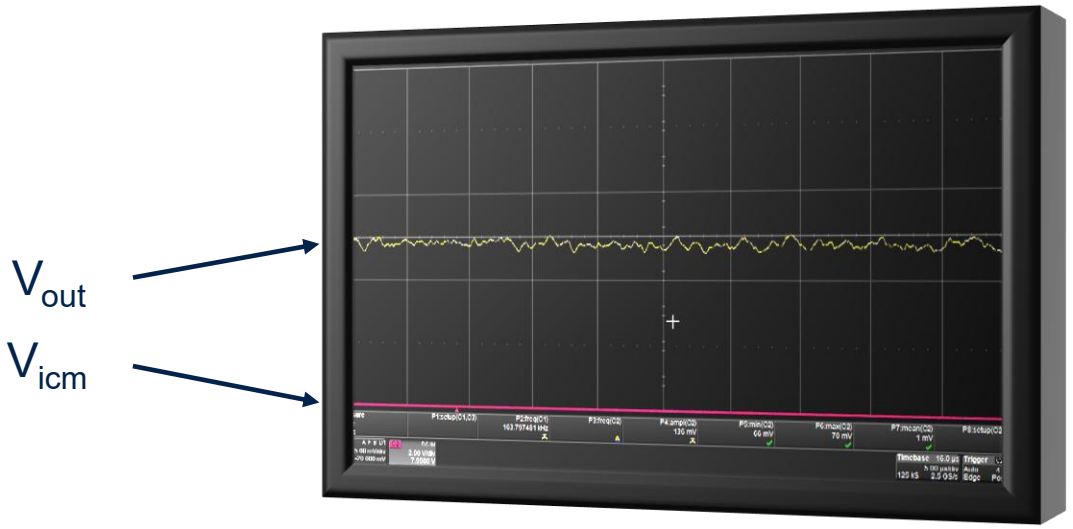
In this document you will find key concepts explained through informative tables, graphs, sequences of graphs, followed by a detailed explanation.

- When you see this icon: Explanation the topic is explained in detail on the following page(s)
- Each explanation page shows the page or page range where the topic is explained: (page # to #)
- If you see this icon: Continue the explanation continues on the next page(s)

What is the common-mode rejection ratio?

CMRR





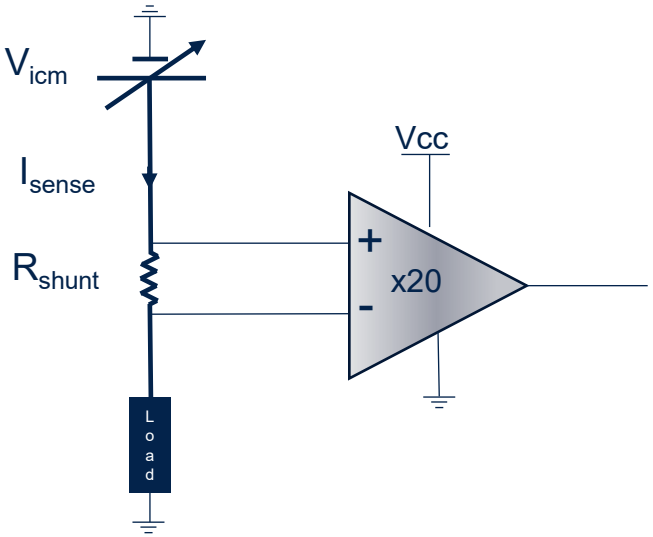
TSC2010

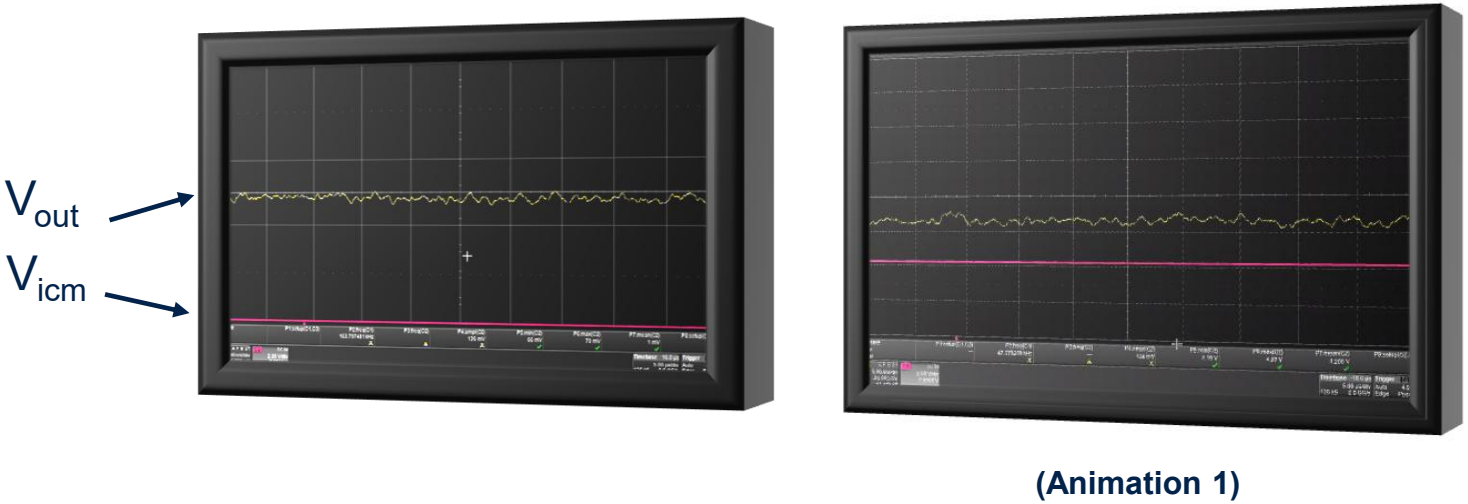
CMR	Common mode rejection	V_{icm} = -20 to 70 V, DC mode $T_{min} < T < T_{max}$	90 85	120		dB

Explanation

What is the common-mode rejection ratio?

CMRR





(Animation 1)

TSC2010

CMR	Common mode rejection	V_{icm} = -20 to 70 V, DC mode $T_{min} < T < T_{max}$	90 85	120		dB

Explanation

What is the common-mode rejection ratio?

Explanation of pages 4–5

CMRR is the ratio of **differential voltage gain** to **common-mode voltage gain**.
Practically, it is measured as the ratio between a change in **input common-mode voltage** and the resulting change in **input offset voltage**.

In datasheets, CMRR appears in the **DC** and/or **AC** parameter sections. Here we focus on **DC CMRR**. As shown in the TSC2010 current-sense amplifier datasheet, CMRR is usually given in **dB**, emphasizing that it is a ratio.

In our example:

- The shunt voltage **Vsense** is **constant**.
- The output voltage is therefore expected to be **stable**.

On the oscilloscope:

- The **yellow trace** shows the **output voltage**.
- The **red trace** shows the **common-mode voltage**, varied from **0 V to 70 V**.

What is the common-mode rejection ratio?

Explanation of pages 4–5

Animation explanation:

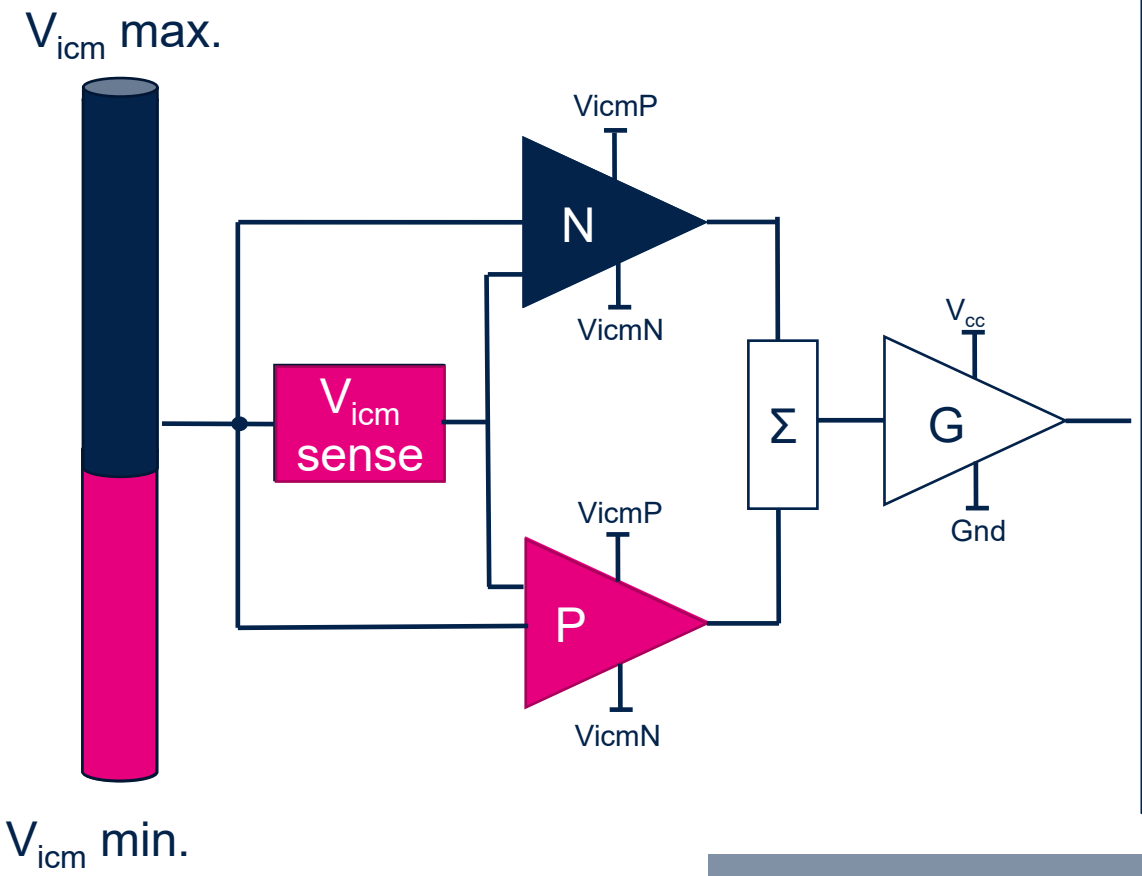
During the test, only the **common-mode voltage** is swept, while **Vsense remains constant**.

- The **yellow curve** shows that the **output voltage changes** with the common-mode voltage.
- Since **V_{sense} does not change**, this comes from the amplifier's **input-offset voltage** V_{IO} ,which depends on the common-mode voltage.

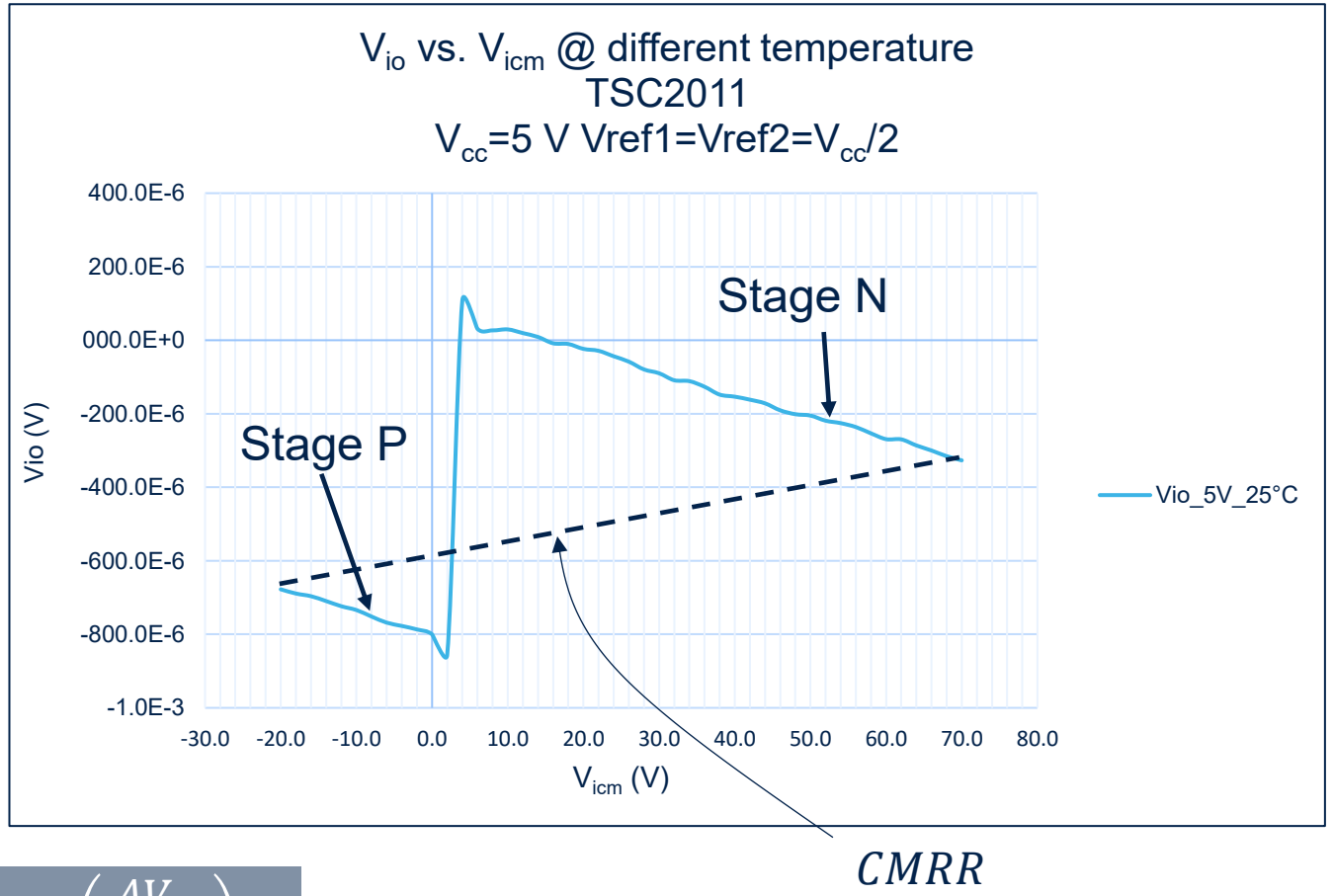
CMRR expresses how V_{IO} varies with common-mode voltage.
Because it is expressed in **dB**, a **lower CMRR value** means **worse common-mode rejection** and thus a **larger equivalent input voltage variation** for a given change in common-mode voltage.

Common-mode rejection ratio origin 1

Input stage of current sensing



TSC2011

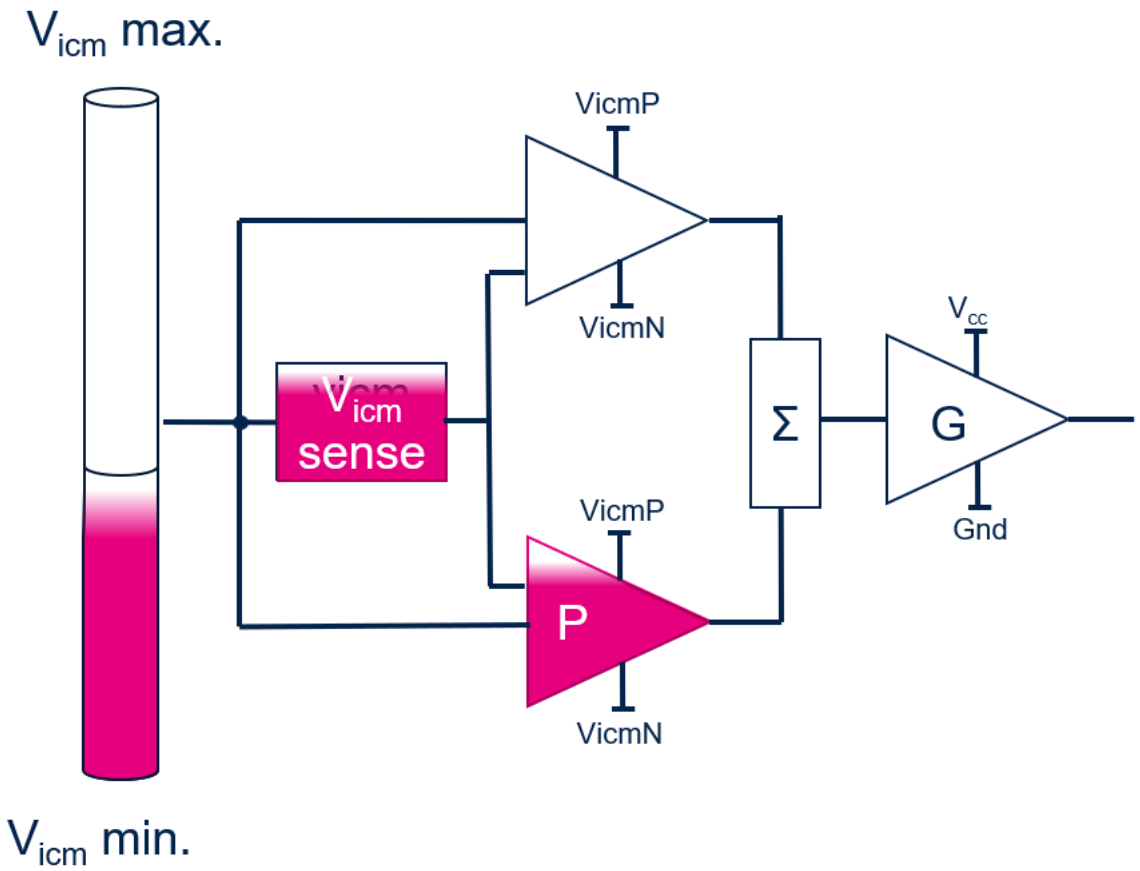


$$CMRR(dB) = 20.\log\left(\frac{\Delta V_{io}}{\Delta V_{icm}}\right)$$

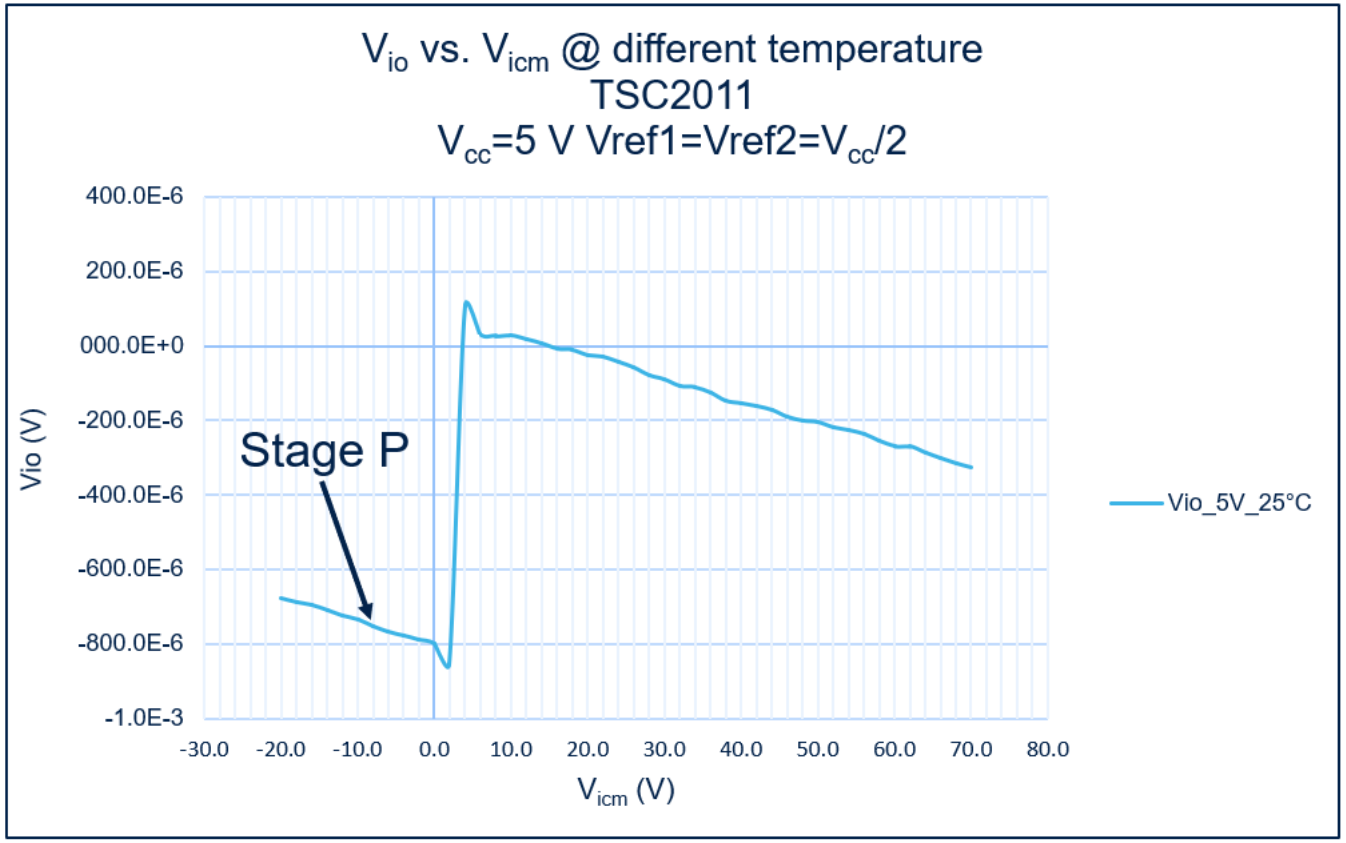
Explanation

Common-mode rejection ratio origin 1

Input stage of current sensing



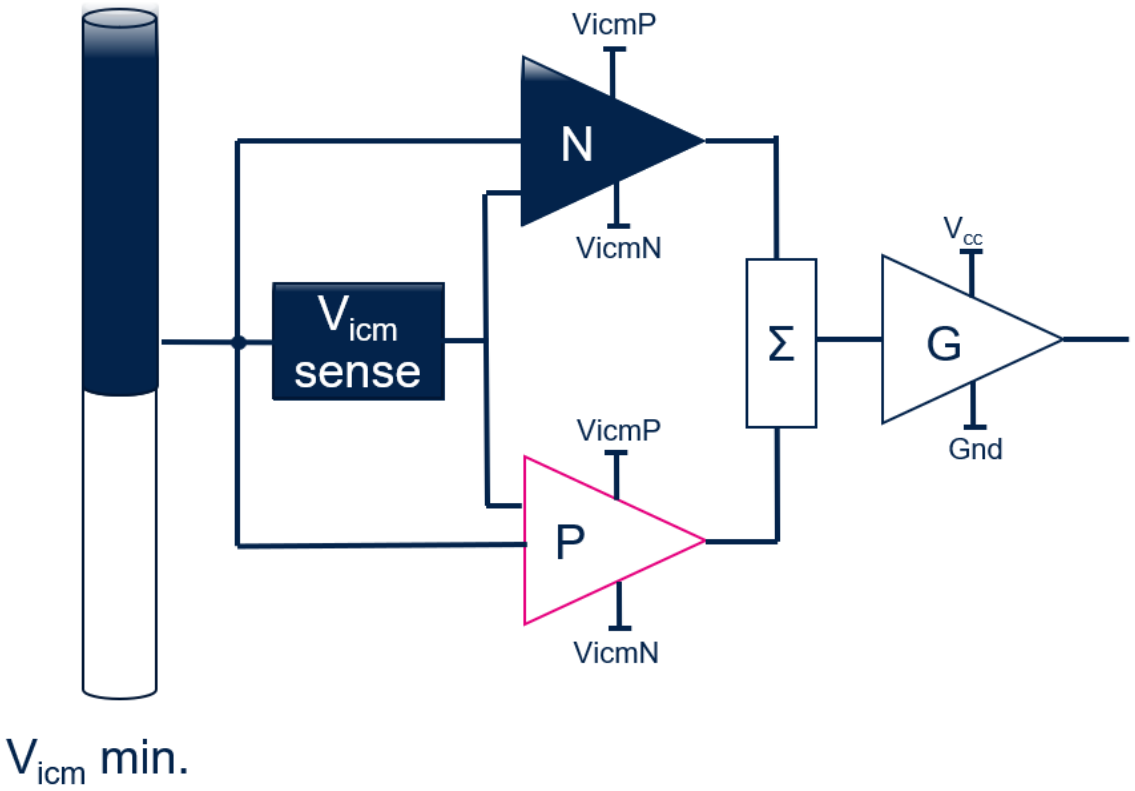
TSC2011



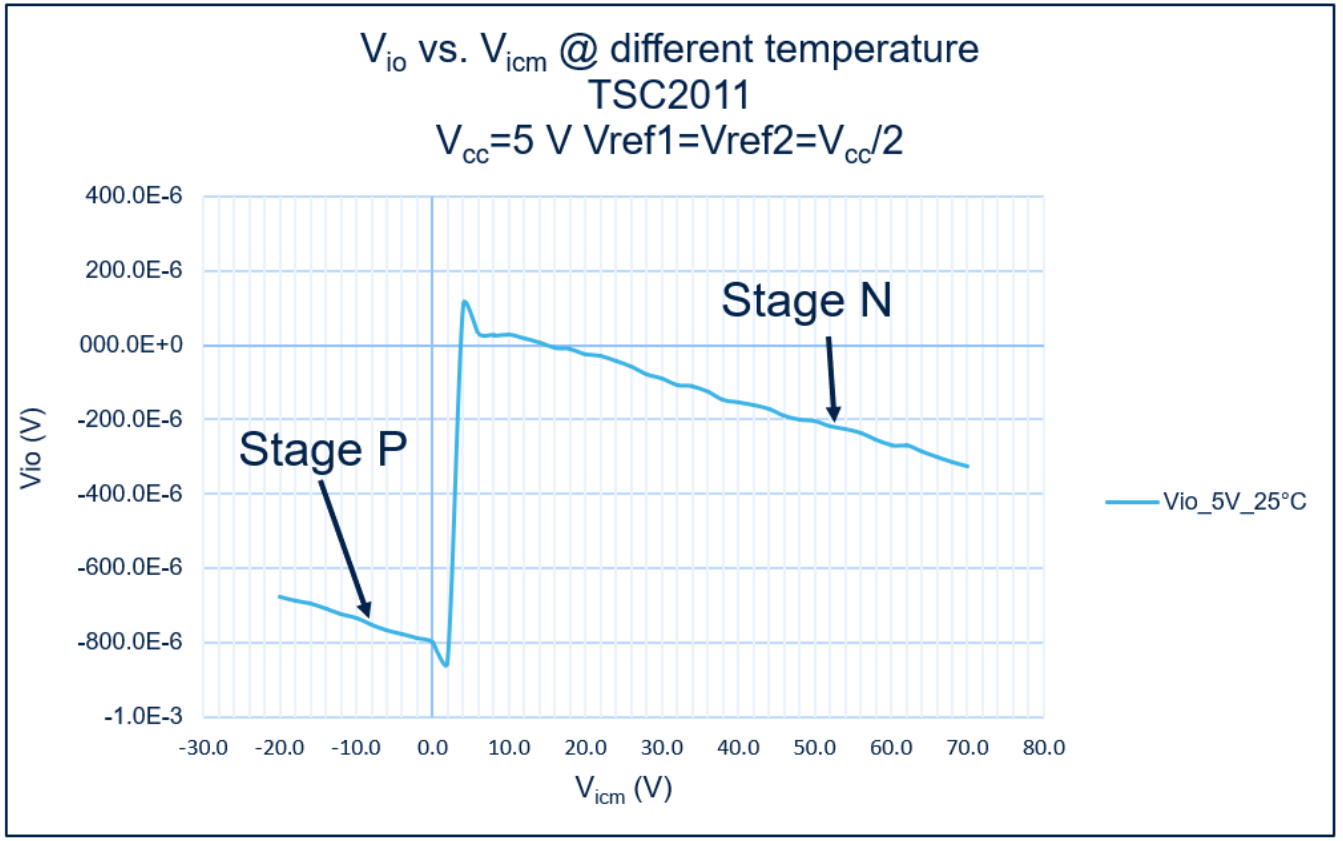
Explanation

Common-mode rejection ratio origin 1

Input stage of current sensing



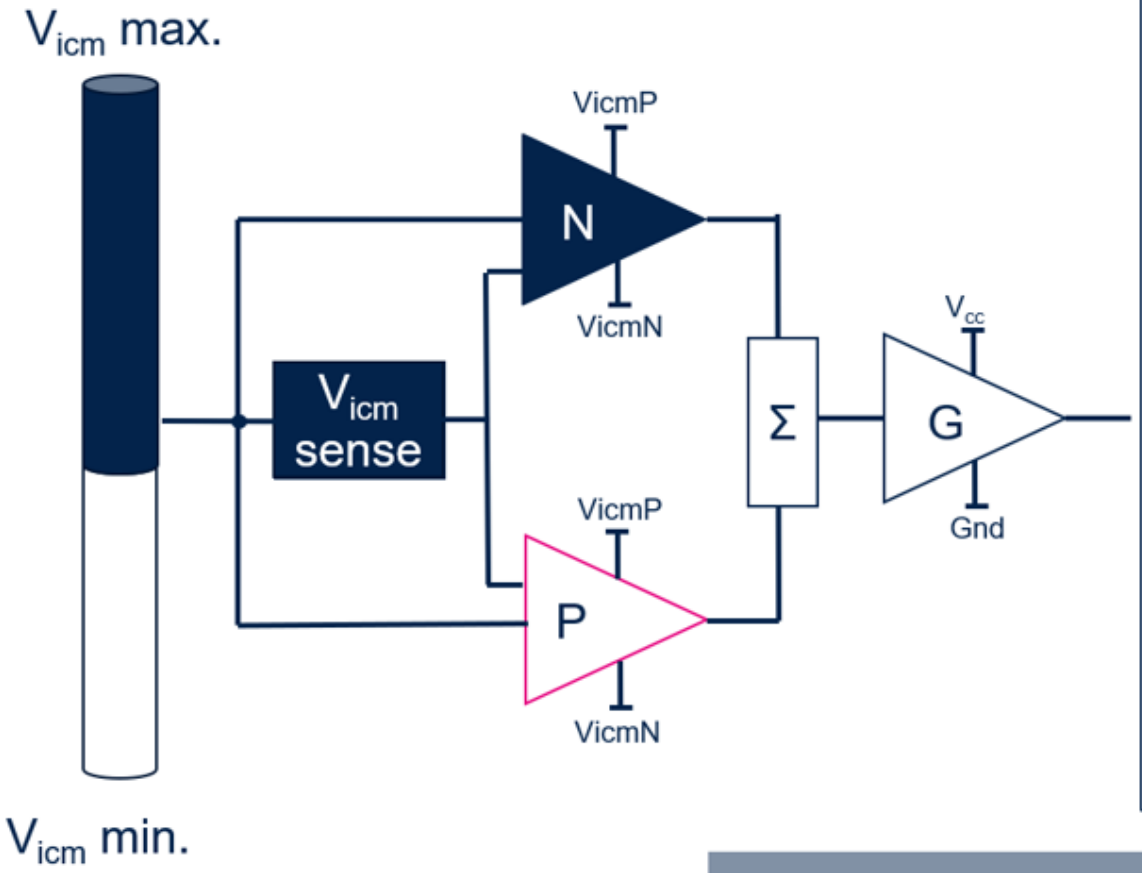
TSC2011



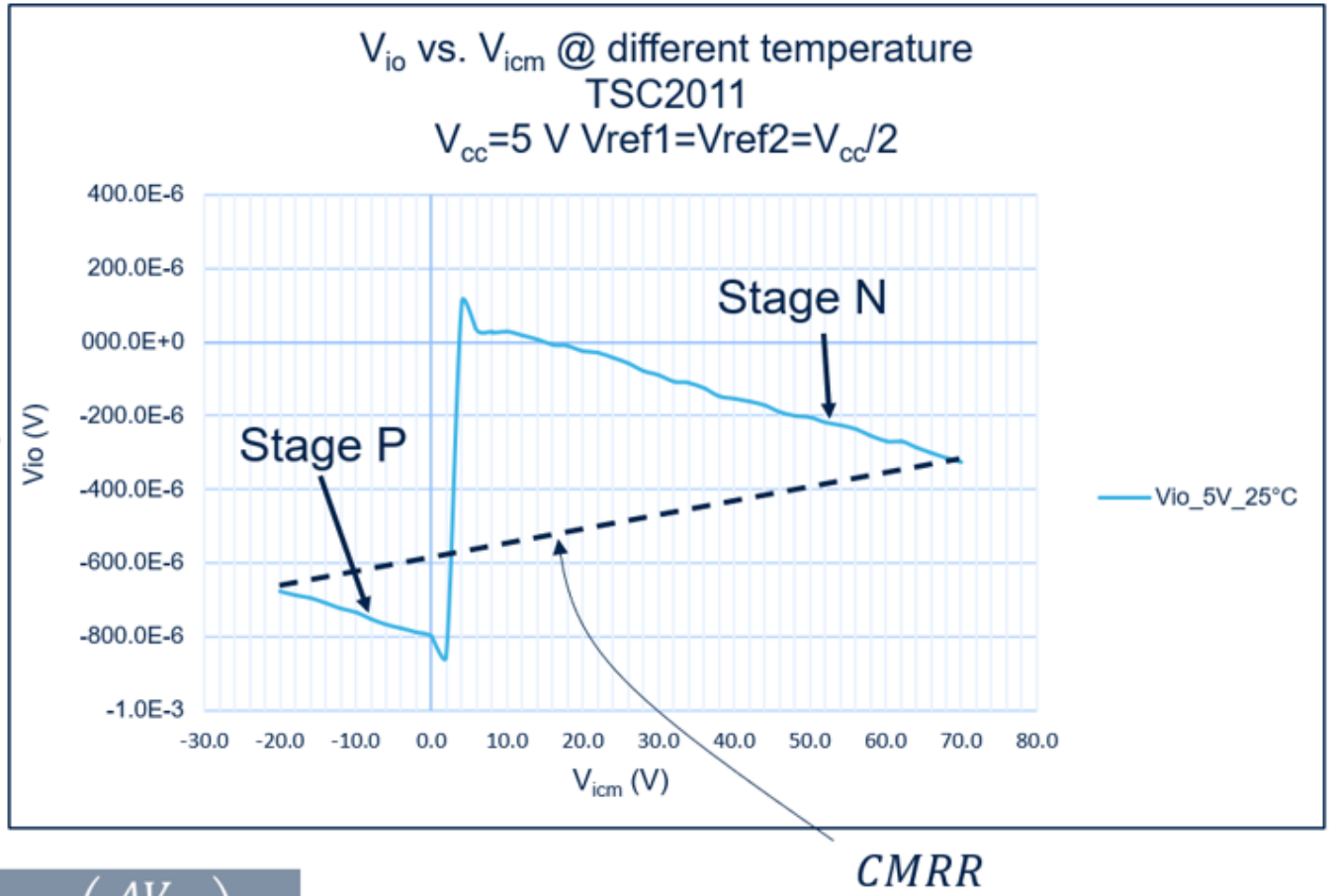
Explanation

Common-mode rejection ratio origin 1

Input stage of current sensing



TSC2011



$$CMRR(dB) = 20.\log\left(\frac{\Delta V_{io}}{\Delta V_{icm}}\right)$$

Explanation

Common-mode rejection ratio origin 1

Explanation of pages 8–11

In current-sense amplifiers, **CMRR** has several origins.

A first one is that the **input common-mode voltage** sets the **bias point** of the input differential pair.
Due to inherent **mismatches** in the circuitry, changing this bias point changes the **input-offset voltage** V_{IO} ,which in turn changes the **output voltage**.

It also depends on the **input architecture**.
To support a **wide common-mode range**, a classical current-sensing front end can use **two stages**:

- an **N-stage** for the **upper** V_{ICM} range
- a **P-stage** for the **lower** V_{ICM} range

As seen previously, mismatch between two NMOS devices, or between two PMOS devices, generates V_{IO}.
There is **no correlation** between NMOS mismatch and PMOS mismatch.

Common-mode rejection ratio origin 1

Explanation of pages 8–11

(page 9) – P-stage offset

Each stage therefore generates its own V_{IO}.
At **low common-mode voltage**, the **P-stage** is active and adds its own the offset.

(page 10) – N-stage offset

At **high common-mode voltage**, the **N-stage** becomes active and its own V_{IO} dominates.
Depending on the application V_{ICM} ,the effective V_{IO} can thus be different.

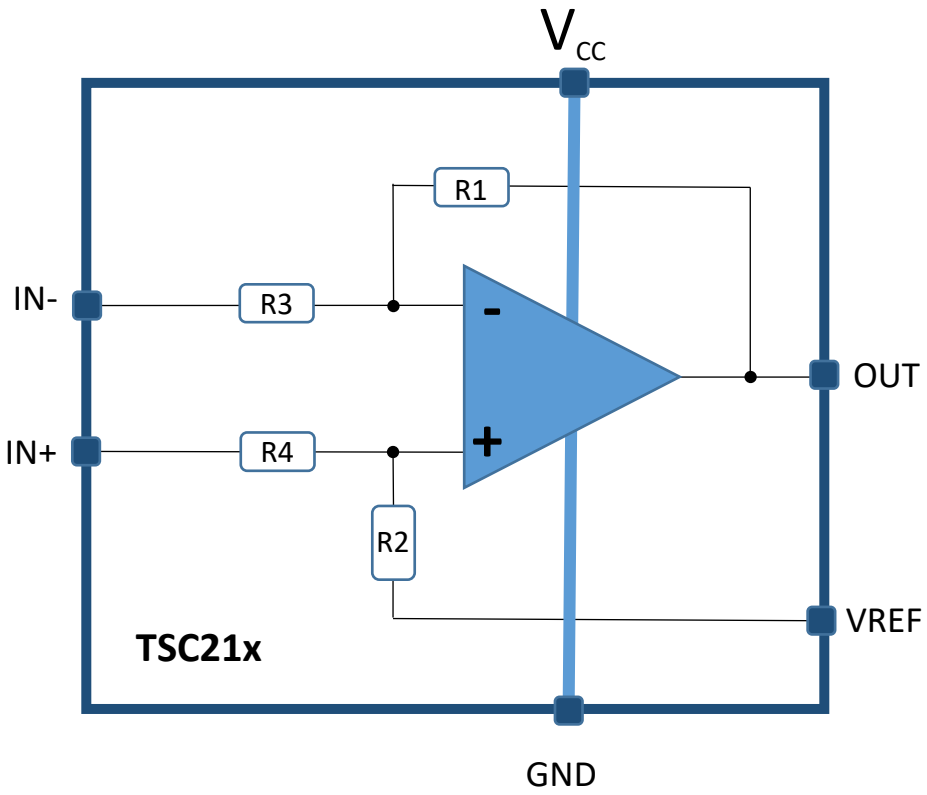
In precision applications, the key objective is to **minimize the jump in** V_{IO} when the signal switches from one stage to the other.

(page 11) – CMRR as slope

On the V_{IO} versus V_{ICM} curve, **CMRR** corresponds to the **slope between** $V_{ICM,min}$ **and** $V_{ICM,max}$.
The **flatter** this slope, the **more precise** the device.

Common-mode rejection ratio origin 2

Gain resistance mismatch



1 $$out = IN_+ * \frac{R2}{R4} * \frac{1+\frac{R1}{R3}}{1+\frac{R2}{R4}} - IN_- * \frac{R1}{R3}$$

2 $$out = (IN_+ - IN_-) * \frac{R1}{R3}$$

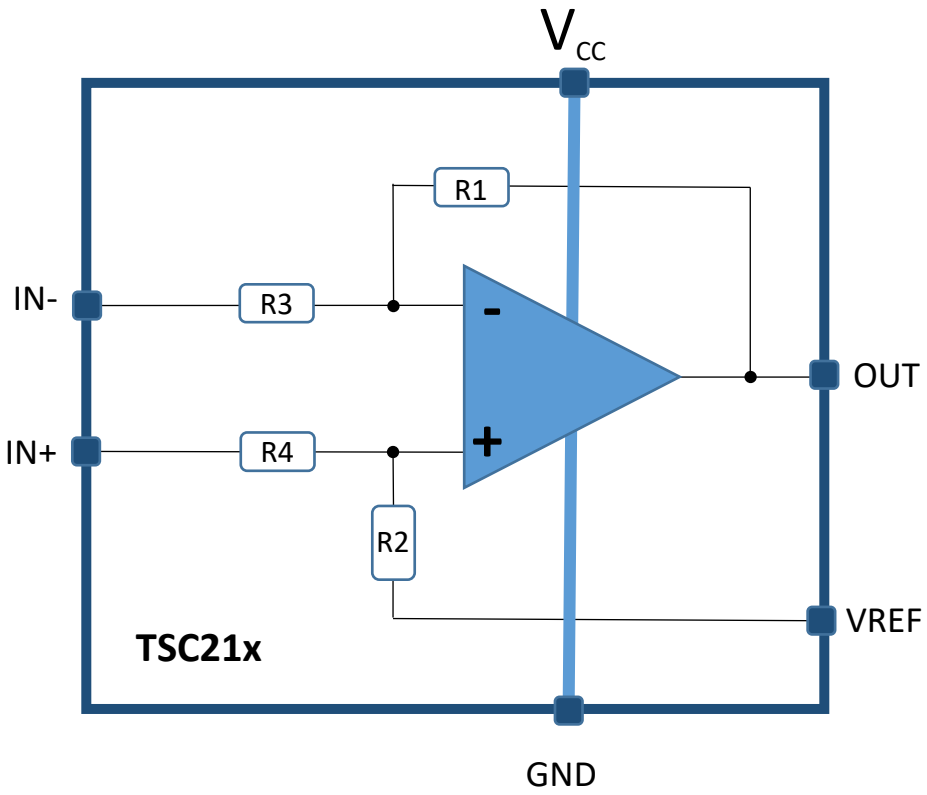
3 $$out = (IN_+ - IN_-) * \frac{R1}{R3} * (1 \pm 2\varepsilon) + \frac{IN_+ + IN_-}{2} * \frac{R1}{R1+R3} * 4\varepsilon$$

More than precision,
Resistor matching is the key to CMRR accuracy

Explanation

Common-mode rejection ratio origin 2

Gain resistance mismatch



$$out = (IN_+ - IN_-) * \frac{R1}{R3}*(1 \pm 2\varepsilon) + \frac{IN_+ + IN_-}{2} * \frac{R1}{R1+R3} * 4\varepsilon$$

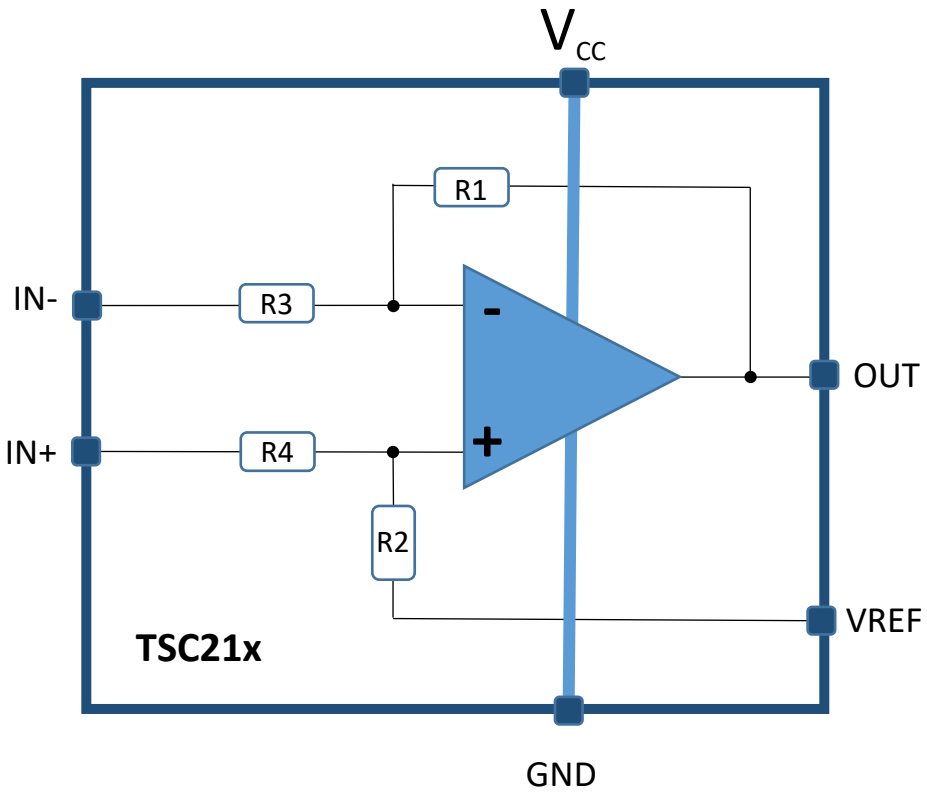
Differential gain is given by: $G_{diff} = \frac{R1}{R3}(1 \pm 2\varepsilon)$

More than precision,
Resistor matching is the key to CMRR accuracy

Explanation

Common-mode rejection ratio origin 2

Gain resistance mismatch



$$out = (IN_+ - IN_-) * \frac{R1}{R3} * (1 \pm 2\varepsilon) + \frac{IN_+ + IN_-}{2} * \frac{R1}{R1+R3} * 4\varepsilon$$

Differential gain is given by: $G_{diff} = \frac{R1}{R3}(1 \pm 2\varepsilon)$

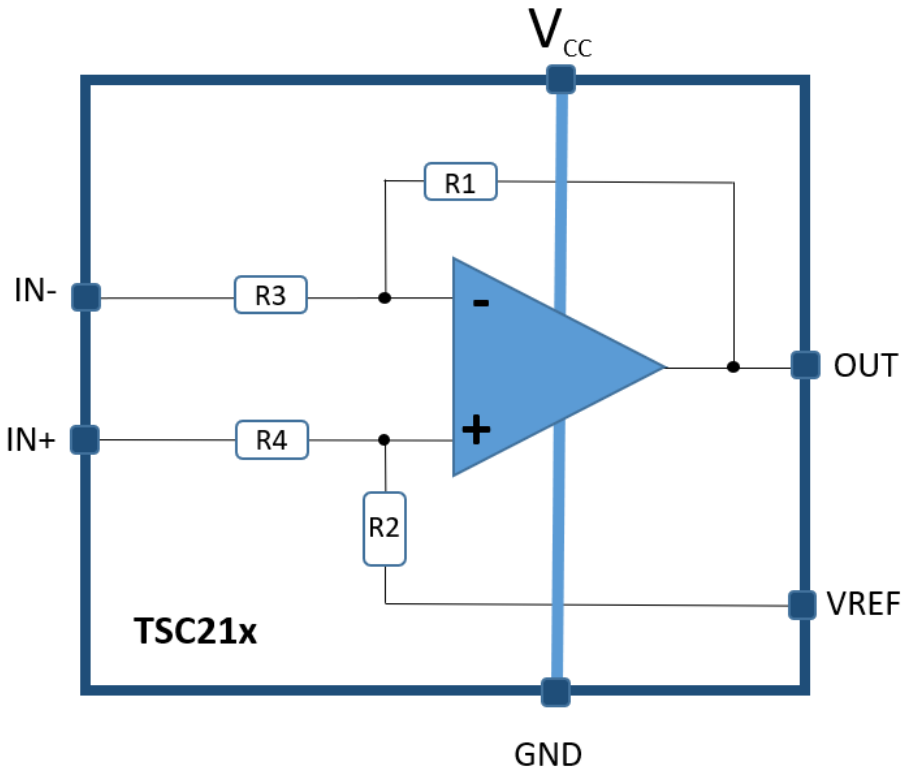
Common-mode gain is given by: $G_{CM} = \frac{R1}{R1+R3} * 4\varepsilon$

More than precision,
Resistor matching is the key to CMRR accuracy

Explanation

Common-mode rejection ratio origin 2

Gain resistance mismatch



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Differential gain is given by: $G_{diff} = \frac{R1}{R3}(1 \pm 2\varepsilon)$

Common-mode gain is given by: $G_{CM} = \frac{R1}{R1+R3} * 4\varepsilon$

$$CMRR = 20log\frac{G_{diff}}{G_{CM}} = 20log\frac{1 + \frac{R1}{R3}}{4\varepsilon}$$

Where ε represents the resistance ratio error

More than precision,
Resistors matching is the key for CMRR accuracy

Explanation

Common-mode rejection ratio origin 2

Explanation of pages 14–17

(page 14) - Differential architecture and resistor matching

1 Differential-amplifier model
A traditional current-sense stage can be modeled, to first order, as a **differential amplifier**. Its transfer function is given by the equation shown.

2 Ideal case vs. real resistor matching
If the gain resistors are ideally matched ($R_1 = R_2$ and $R_3 = R_4$) , this expression simplifies to the ideal differential-amplifier equation.
In reality, as already seen with V_{IO} ,perfect matching is impossible: the gain resistors always exhibit a **matching error**, which depends on the technology. Thin-film resistors offer very good native matching, but still not perfect.
By introducing this mismatch as a resistance-ratio error ε, we obtain the modified transfer function shown.

3 Separation into two terms
In this final equation, we can clearly identify two contributions: a **differential term** and a **common-mode term**, which will be analyzed on the next slides.

Continue

Common-mode rejection ratio origin 2

Explanation of pages 14–17

(page 15) – Differential gain
The first term is the **differential gain**.
It amplifies the difference $(IN_+ - IN\_)$ and represents the useful part of the signal for current sensing.

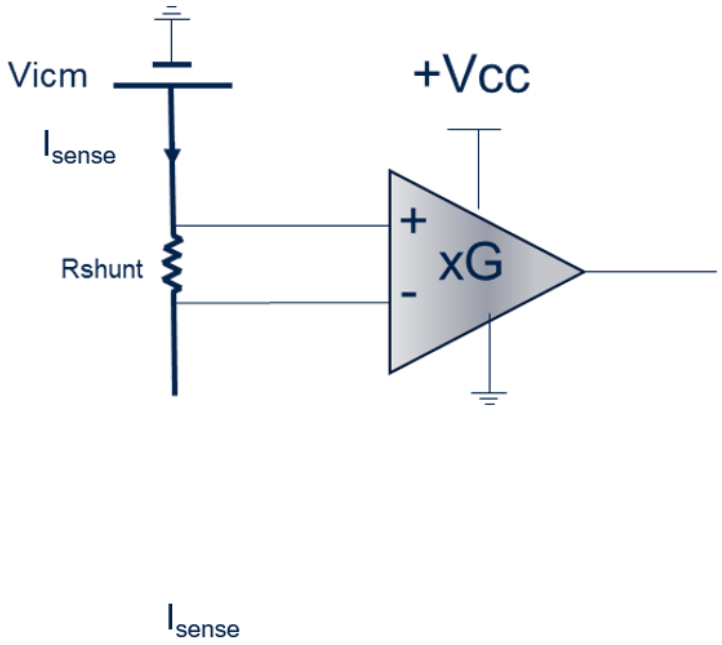
(page 16) – Common-mode gain
The second term is the **common-mode gain**.
It converts the common-mode input voltage into an additional output component and therefore degrades the measurement accuracy.

(page 17) – CMRR and impact of resistor mismatch
The **common-mode rejection ratio (CMRR)** is the ratio between differential gain and common-mode gain. The higher this ratio, the more accurately common-mode signals are rejected.

In a differential configuration, **any mismatch of the gain resistors directly affects the output** and thus the CMRR: if the resistors are not perfectly matched, the common-mode voltage V_{CM} is only partially rejected.

Consequently, **resistor matching is a key determinant of CMRR in current-sense amplifiers**, often even more critical than input-stage mismatch.

How CMRR affects precision



TSC2010 series

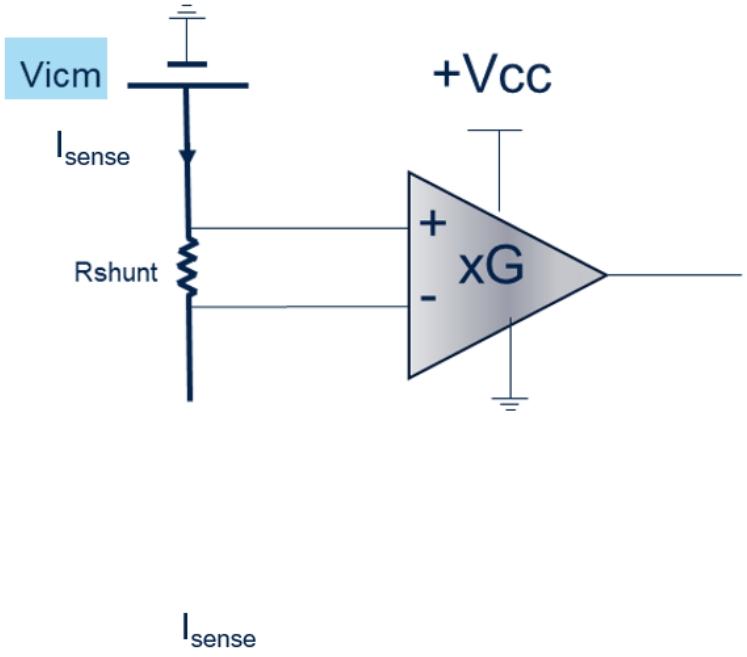
Table 5. **Electrical characteristics (V_{cc} = 5 V, V_{icm} = 12 V, T = 25 °C unless otherwise specified)**

CMR	Common mode rejection	V_{icm} = -20 to 70 V, DC mode T_{min} < T < T_{max}	90 85	120		dB

$$Offset\ due\ to\ CMRR = \pm \frac{|V_{icm} - V_{icmDS}|}{10^{\frac{CMRR}{20}}}$$

Note: higher the CMRR, higher the precision

How CMRR affects precision



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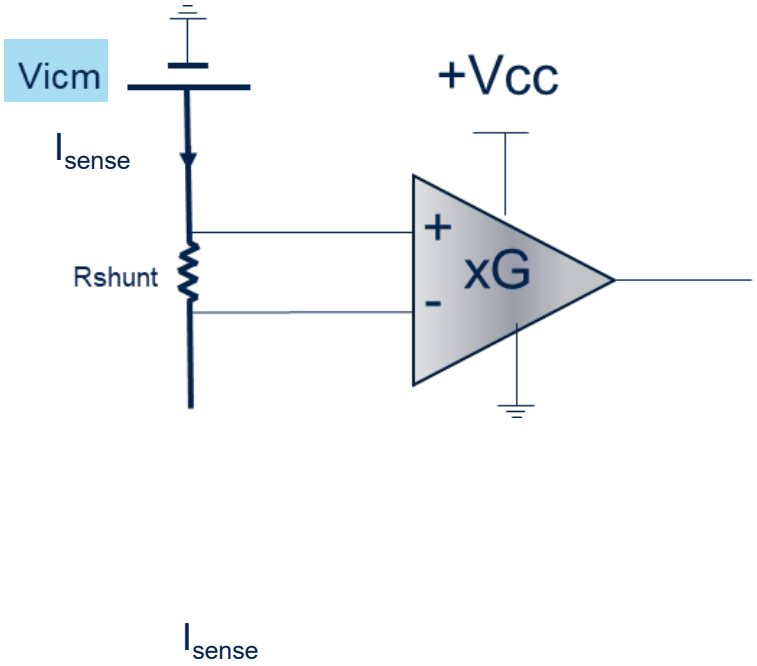

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$$Offset\ due\ to\ CMRR = \pm \frac{|V_{icm} - V_{icmDS}|}{10^{\frac{CMRR}{20}}}$$

$$CMRR\ impact\ (\%) = \frac{|Vicm - V_{icmDS}|}{R_{shunt} * I_{sense} * 10^{\frac{CMR}{20}}} * 100$$

Note: the higher the CMRR, the higher the precision

How CMRR affects precision

Explanation of pages 20–22

We have identified the different internal origins of common-mode related errors in a current-sense amplifier.
Now we examine **how CMRR affects the accuracy of the current measurement.**

(page 20) – From datasheet CMRR to offset at our Vicm

Let us consider the **TSC2010** **bidirectional current-sense amplifier**.
In the datasheet, unless otherwise specified, parameters are defined and guaranteed for a **common-mode voltage** $V_{\mathrm{icmDS}} = 12\ \mathrm{V}$.

The input offset voltage V_{IO} given in the datasheet is therefore valid **only at this common-mode voltage**.
If our application uses a different common-mode V_{icm} ,we need to estimate the new offset. We do this by using the **CMRR value** specified in the datasheet.

Because CMRR is usually expressed in dB, we first convert it to a gain ratio, then we apply:

$$\text{Offset due to CMRR} = \pm \frac{|V_{\mathrm{icm}} - V_{\mathrm{icmDS}}|}{10^{\frac{\mathrm{CMRR}}{20}}}$$

Continue

How CMRR affects precision

Explanation of pages 20–22

(page 21) – Using the offset variation

We must clearly distinguish:

- the **application common-mode** V_{icm} ,and
- the **reference common-mode** V_{icmDS} used for V_{IO} in the datasheet.

The equation above gives the **additional offset** caused by operating at V_{icm} instead of V_{icmDS}.
This extra term must be **added to the datasheet** V_{IO} when calculating the total error on the current measurement.

(page 22) – Expressing the CMRR error in %

The error due to CMRR can also be expressed **as a percentage**. In this case, it is appropriate to express this error as a ratio of the voltage at the shunt terminals.
On the slide, the formula is:

$$\boldsymbol{CMRR\ impact}\ (\%) = \frac{|Vicm - V_{icmDS}|}{R_{\mathrm{shunt}} * I_{sense} * 10^{\frac{CMR}{20}}} * 100$$

Continue

How CMRR affects precision

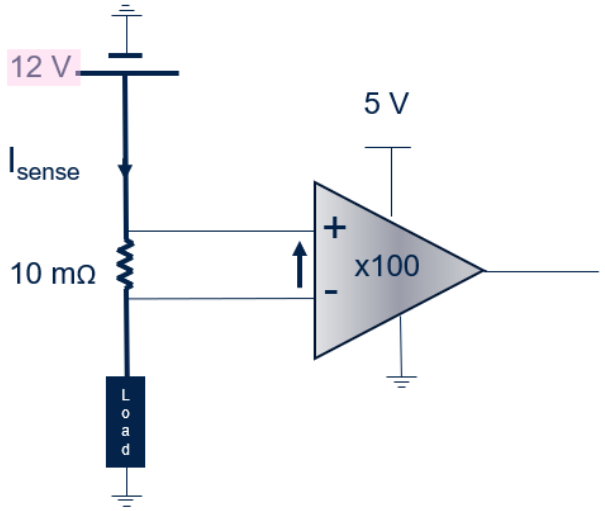
Explanation of pages 20–22

where:

- V_{icm} is the common-mode voltage in the application,
- V_{icmDS} is the common-mode voltage used in the datasheet for V_{IO} parameter,
- $R_{\mathrm{shunt}} \times I_{\mathrm{sense}}$ is the shunt voltage, and
- $10^{\mathrm{CMRR}/20}$ is the CMRR converted from dB to a linear ratio.

When evaluating accuracy, this CMRR-related error should be compared with the error due to V_{IO} ;ideally both should be of the **same order of magnitude**.

Example



TSC2012

Table 5. **Electrical characteristics (V_{cc} = 5 V, V_{icm} = 12 V, T = 25 °C unless otherwise specified)**

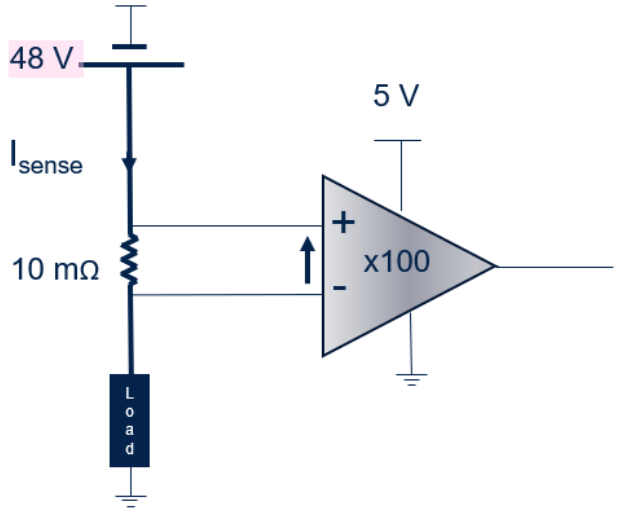
$\|V_{os}\|$	Offset voltage (RTI) (1)	V_{icm} = 1 V T_{min} < T < T_{max}			200 700	µV
		V_{icm} = 12 V T_{min} < T < T_{max}		3	500 1100	µV
CMR	Common mode rejection	V_{icm} = -20 to 70 V, DC mode T_{min} < T < T_{max}	90 85	120		dB

1 $$CMRR\ impact\ (\%) = \frac{12\,V - 12\,V}{10m\Omega * Isense * 10^{\frac{90}{20}}} * 100$$

2 $$CMRR\ impact\ (\%) = \frac{12\,V - 12\,V}{10m\Omega * Isense * 10^{\frac{90}{20}}} * 100$$

Explanation

Example



TSC2012

$$CMRR\ impact\ (\%) = \frac{48\ V - 12\ V}{10\ m\Omega * Isense * 10^{\frac{90}{20}}} * 100$$

Table 5. **Electrical characteristics (V_{cc} = 5 V, V_{icm} = 12 V, T = 25 °C unless otherwise specified)**

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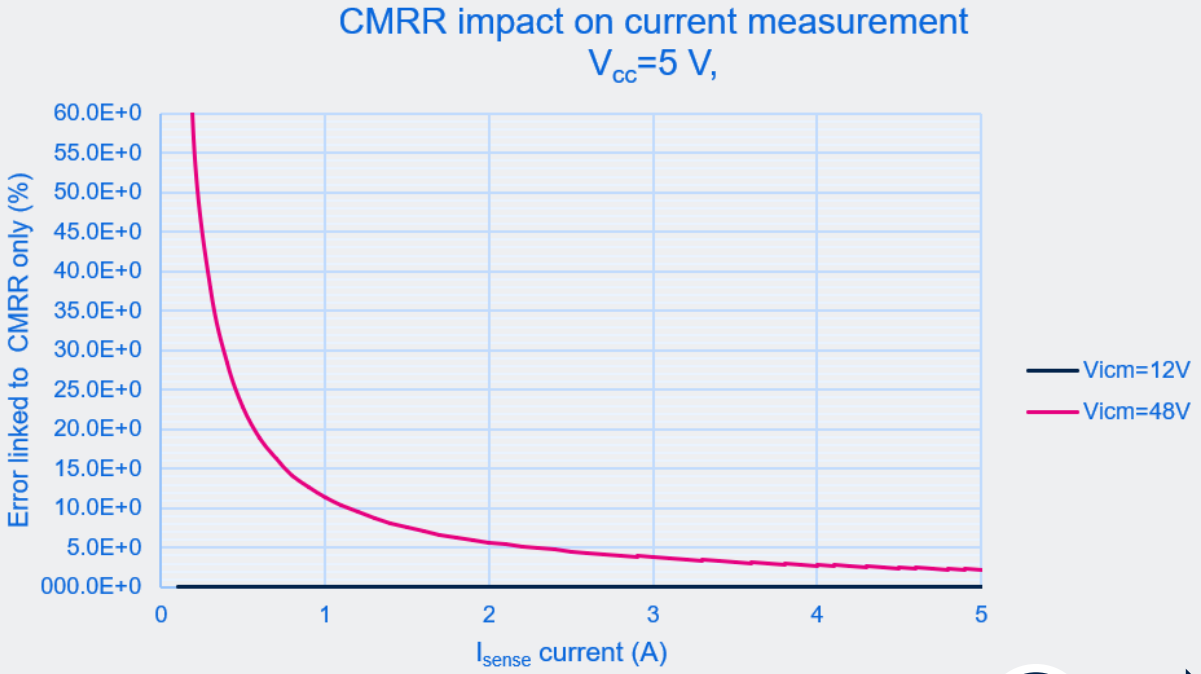


Explanation

Example

Explanation of pages 26–27

(page 26) – Example with Vicm = 12 V

To illustrate the impact of CMRR on current-measurement accuracy, let us analyze a practical example.

We use the **TSC2012**, a bidirectional current-sense amplifier with a gain of 100, operating at room temperature with a common-mode voltage of **12 V**.

1. **Datasheet common-mode condition**
   From the datasheet, the specified input common-mode voltage for this test condition is **Vicm = 12 V**.

2. **Application common-mode condition**
   In our application, the **common mode voltage is set to 12V**. As shown in the CMRR impact equation, when the application Vicm is equal to the datasheet Vicm, the CMRR term becomes zero and therefore has **no impact** on the measurement error.

3. **Resulting error contributor**
   In this situation, the only contributor is the **input offset voltage Vio** specified at **Vicm = 12 V**, which is **500 µV max at 25 °C**.

Continue

Example

Explanation of pages 26–27

(page 27) – Example with Vicm = 48 V

The blue curve on the graph shows the error **due solely to CMRR**. For **Vicm = 12 V**, there is no offset variation linked to common-mode voltage, so CMRR does not affect the measurement.

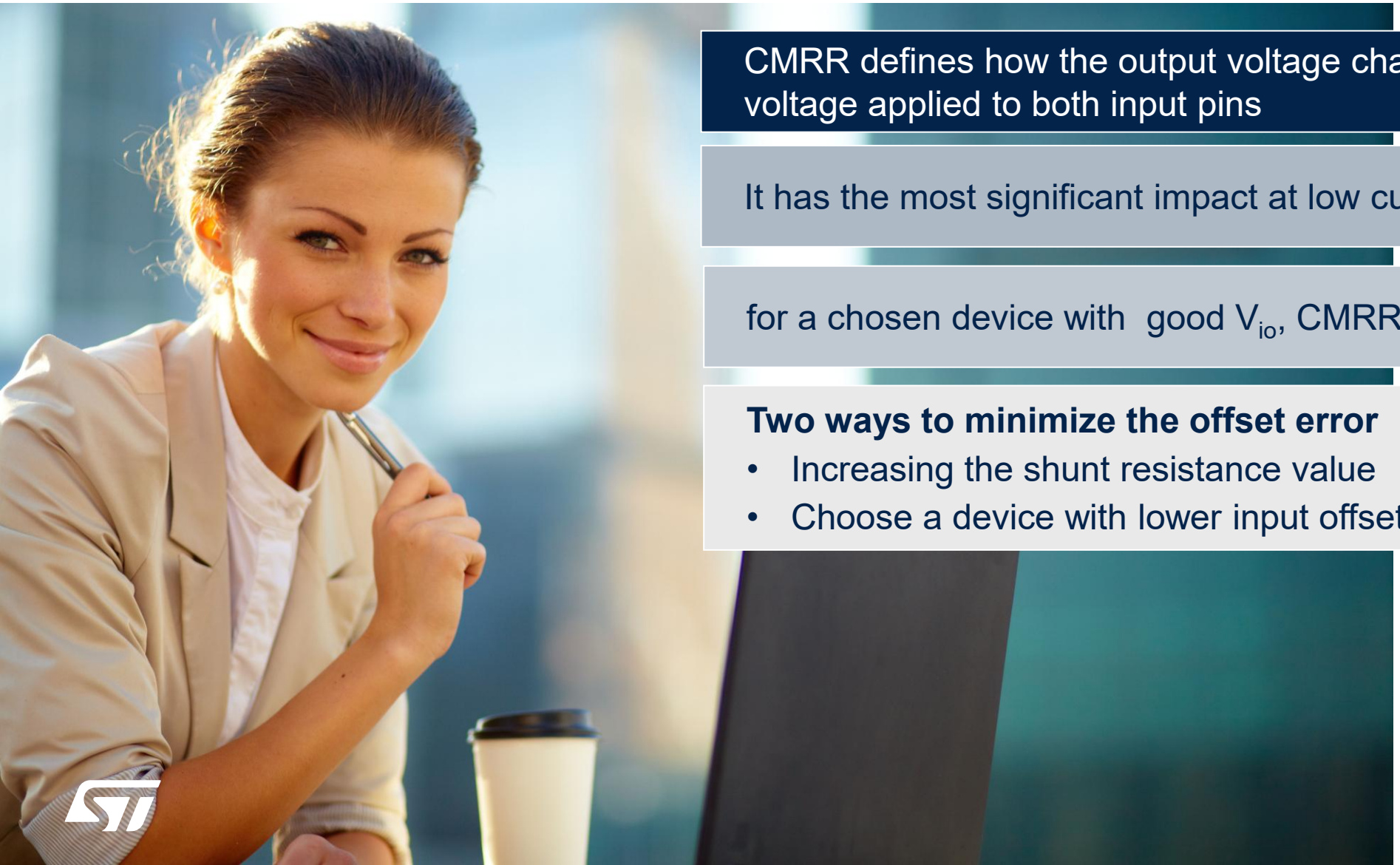
Now consider the same application, but with a **48 V common-mode voltage**. Since **Vio is not specified at 48 V** in the datasheet, we estimate its variation using the CMRR equation.

For a **36 V change in common-mode voltage** (from 12 V to 48 V), the input offset voltage increases by **1.4 mV**.

The red curve represents the error due only to the CMRR effect, that is, the error introduced by the **input offset voltage corresponding to the actual common-mode voltage of the application**.

Therefore, whenever the application operates at a **common-mode voltage different from the datasheet test condition**, it becomes essential to include the **CMRR-induced error** in the overall accuracy calculation.

CMRR error summary



CMRR defines how the output voltage changes depending on the voltage applied to both input pins

It has the most significant impact at low current

for a chosen device with good V_{io}, CMRR must also be good

Two ways to minimize the offset error

- Increasing the shunt resistance value
- Choose a device with lower input offset voltage and higher CMRR

Explanation

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