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POWERING YOUR INNOVATION

3.6kW Totem-Pole PFC with ICL Solution

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Agenda

1 Why is Totem-Pole PFC preferred?

2 Digital Power Solution for 3.6kW Totem-Pole PFC with Inrush Current Limit Control

3 EVM Board Performance

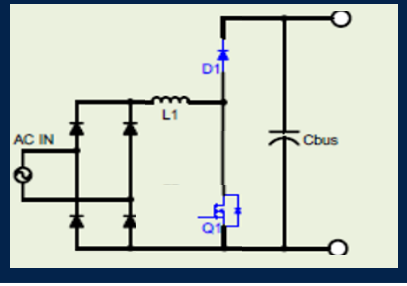
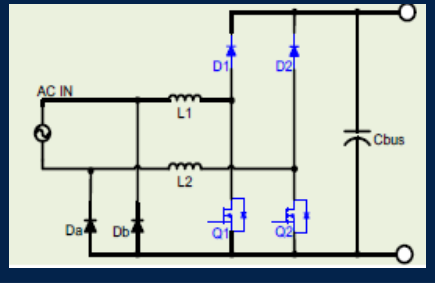
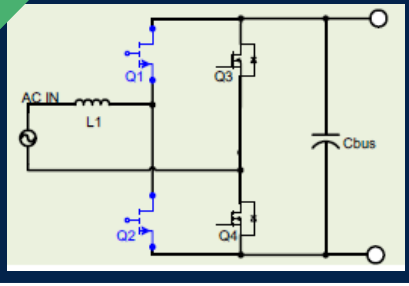
4 ST Product for Totem-Pole PFC

5 Summary

Why is Totem-Pole PFC preferred?

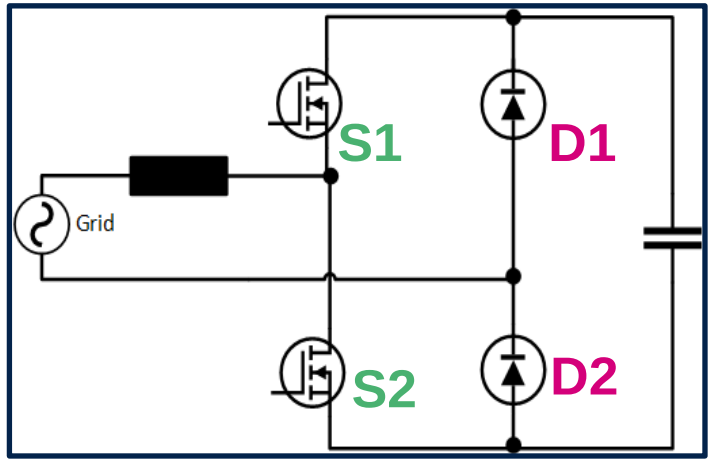
PFC topology comparison

Totem-Pole configuration is commonly used in PFC topology to achieve high efficiency and high-power density

Configuration			
Topology	Traditional Boost	Semi-Bridgeless Boost	CCM Totem-Pole
Transistor	Si MOS	Si MOS	SiC / GaN FET
Peak Efficiency	97.3%	98.0%	98.5% - 99.0%
Pros	• Simple control mechanism • Well-known Technology • Low BOM cost	• Simple bridgeless PFC • Good Efficiency • Simple control mechanism	• Highest Efficiency • High Power density • Low Component Count
Cons	• Low efficiency	• High BOM cost (2x components & larger size) • Complicated sensing circuit	• Critical PCB layout • Complicated driver circuit and control algorithm

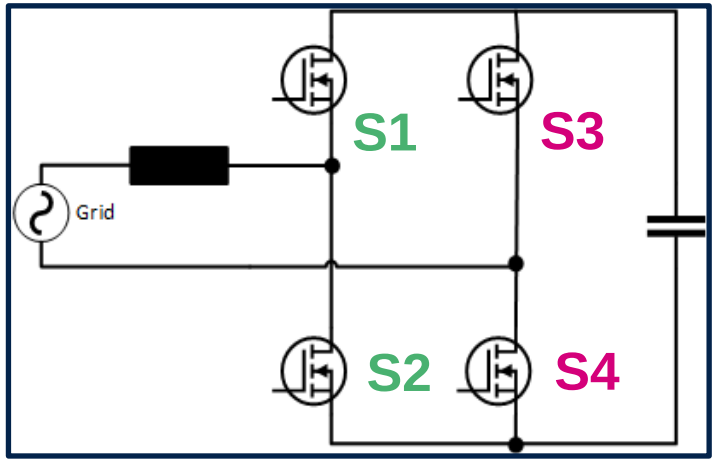
Totem Pole PFC configurations

Config. 1 – Cost Orientation



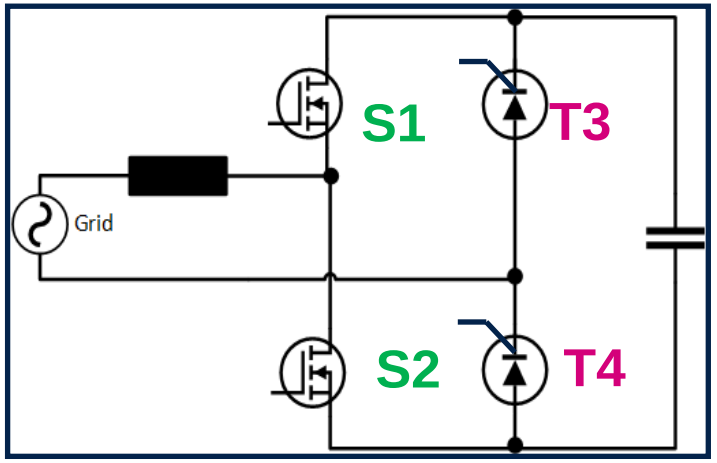
Device	Technology	ST Proposal
S1/S2	SiC MOS	SCTxxN65
D1/D2	Rectifier	STBRxx12W
	Driver	STGAP2S/D
	Control	STM32

Config. 2 – Performance Orientation



Device	Technology	ST Proposal
S1/S2	SiC MOS	SCTWxxN65
S3/S4	SJ MOS	STxxxxN65
	Driver	STGAP2S/D
	Control	STM32

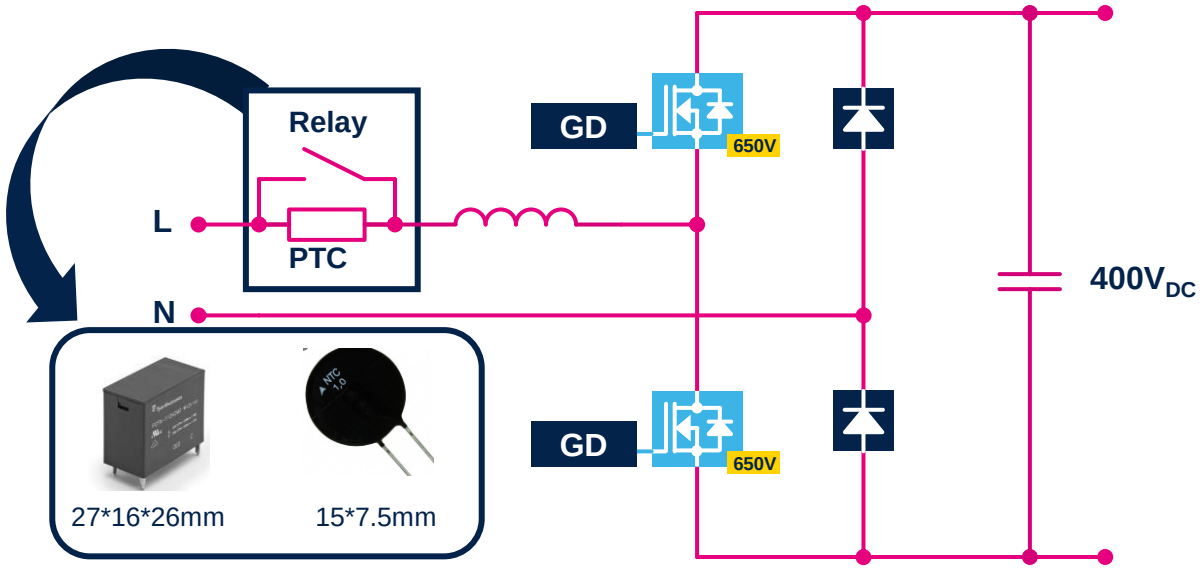
Config. 3 – **Relay-less Orientation**



Device	Technology	ST Proposal
S1/S2	SiC MOS	SCTxxN65
T3/T4	SCR	TNxx50-12
	Driver	STGAP2S/D
	Control	STM32

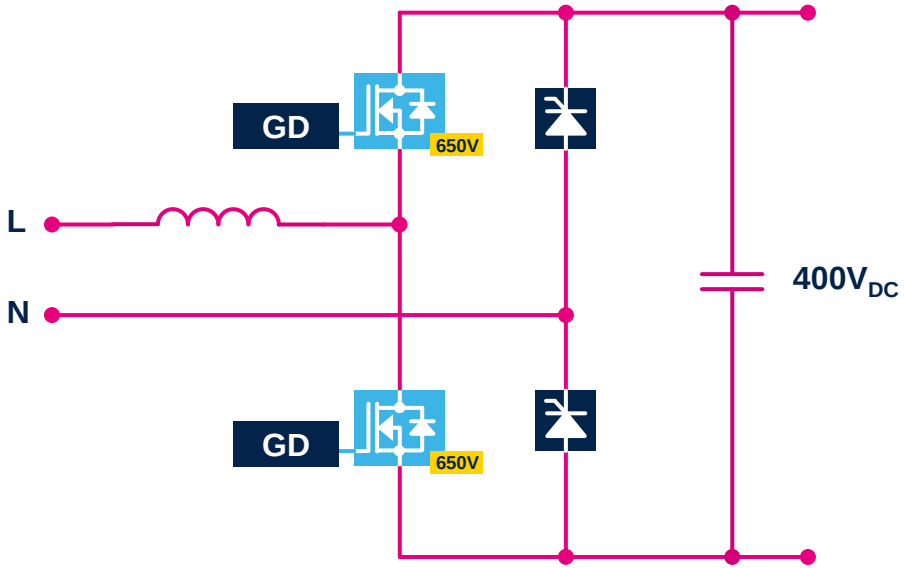
Inrush current limiter with SCRs in Totem-Pole PFC

ICL with PTC and bypassing relay



+ Relay can be driven by simple circuit
- Relay cause audible noise when switching
- Relay metal contact aging
- Slower charging time

ICL with SCRs



+ Remove bulky relay and PTC/NTC
+ Remove coil and conduction loss of relay
+ Faster startup procedure
+ Active current limitation at line-drop recovery
- Need exact SCR pulse timing

Digital Power Solution for 3.6kW Totem-Pole PFC with Inrush Current Limit Control

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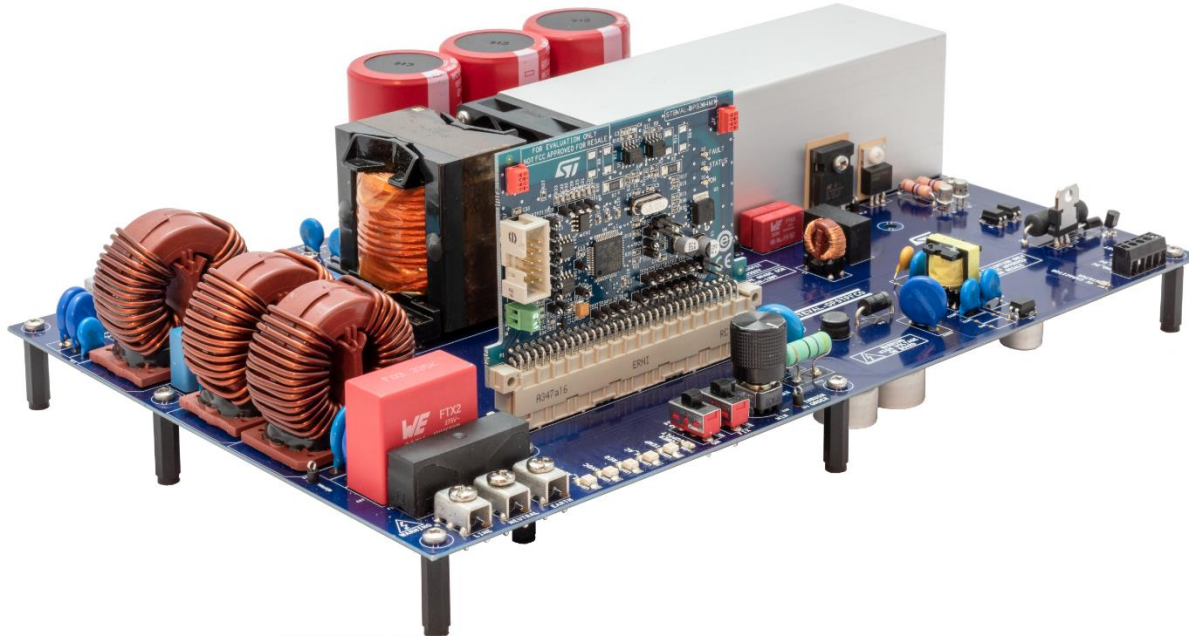
3.6 kW CCM Totem Pole PFC with ICL control

STEVAL-DPSTPFC1

Key Specs

- Input AC voltage: 85VAC up to 264VAC
- DC output voltage: 400VDC
- Maximum input current: 16A
- Switching Frequency : 72kHz
- Operation Mode: CCM
- Peak Efficiency ~ 97.7% @ 230VAC, 50% load
- iTHD < 10% @ 230VAC, >30% Load
- Digital inrush current limit control

Prototype Available



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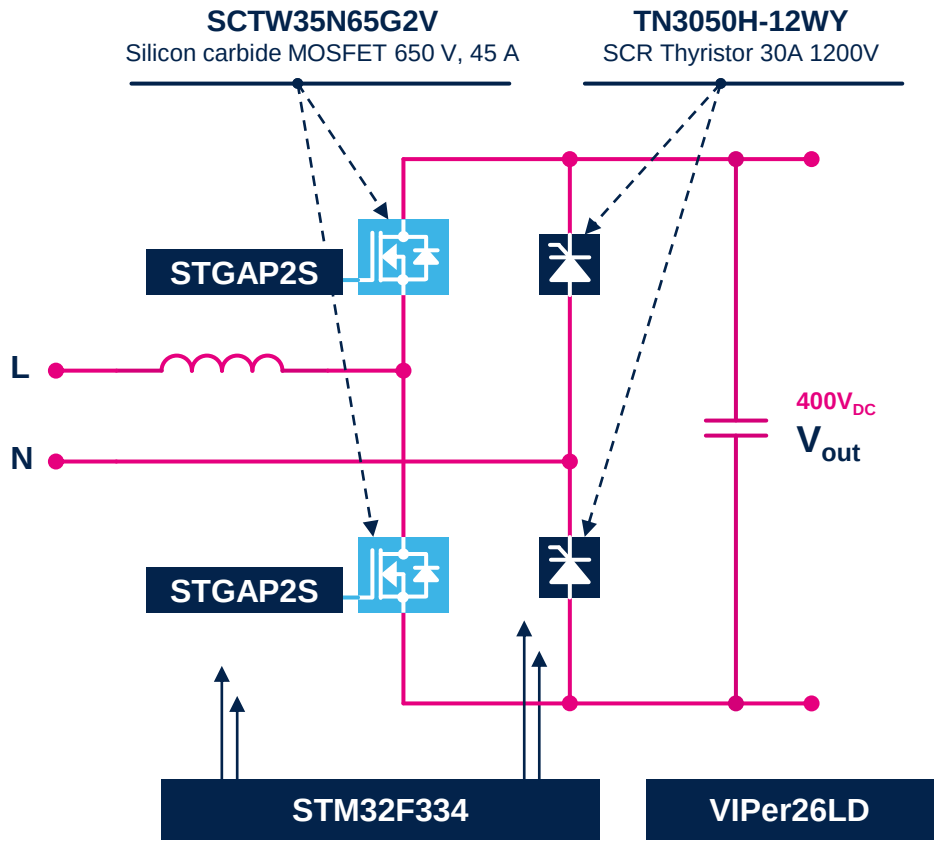
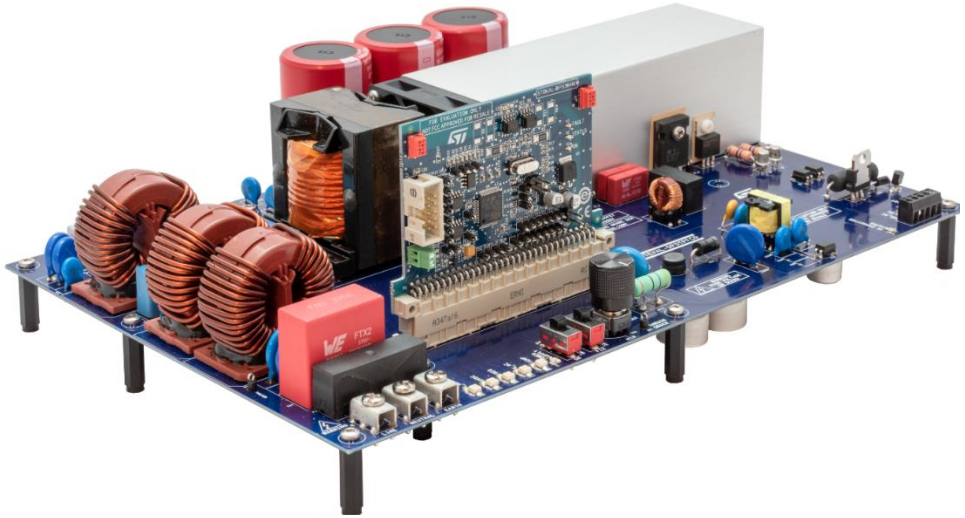
3.6 kW CCM Totem Pole PFC with ICL control

STEVAL-DPSTPFC1



Key Products:

- SCTW35N65G2V (SiC MOSFET)
- TN3050H-12GY (SCR Thyristor)
- STGAP2S (Galvanic insulated gate driver)
- STM32F334 (32-bit MCU)
- VIPer26LD (converter for aux. PS)



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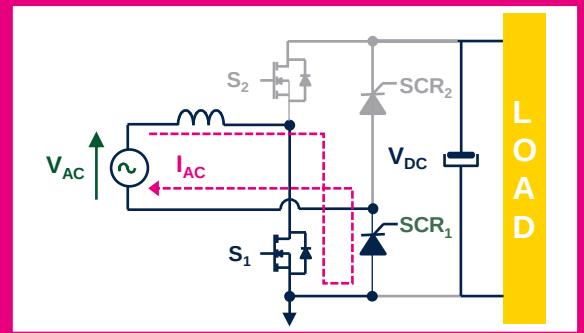
Operation mode for Totem-Pole PFC

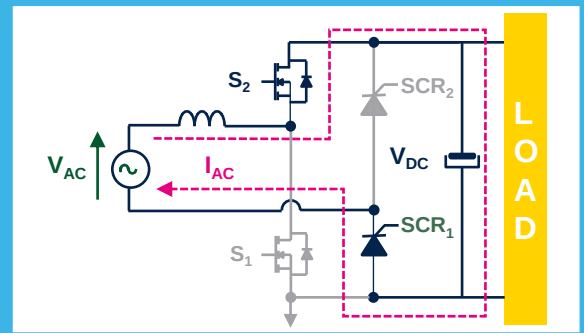
$V_{AC} > 0$

S1 controls PFC choke charging
S2 body diode is used only for discharging choke to the output
S2 can be switched on during t_{off} to reduce voltage drop of the body diode

S1 on, inductor current rising



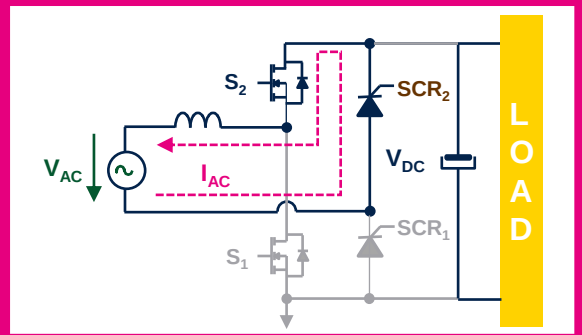
S1 off, inductor current falling



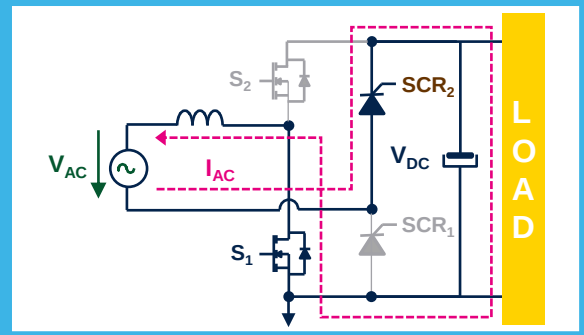
$V_{AC} < 0$

S2 controls PFC choke charging
S1 body diode is used only for discharging choke to the output
S1 can be switched on during t_{off} to reduce voltage drop of the body diode

S2 on, inductor current rising



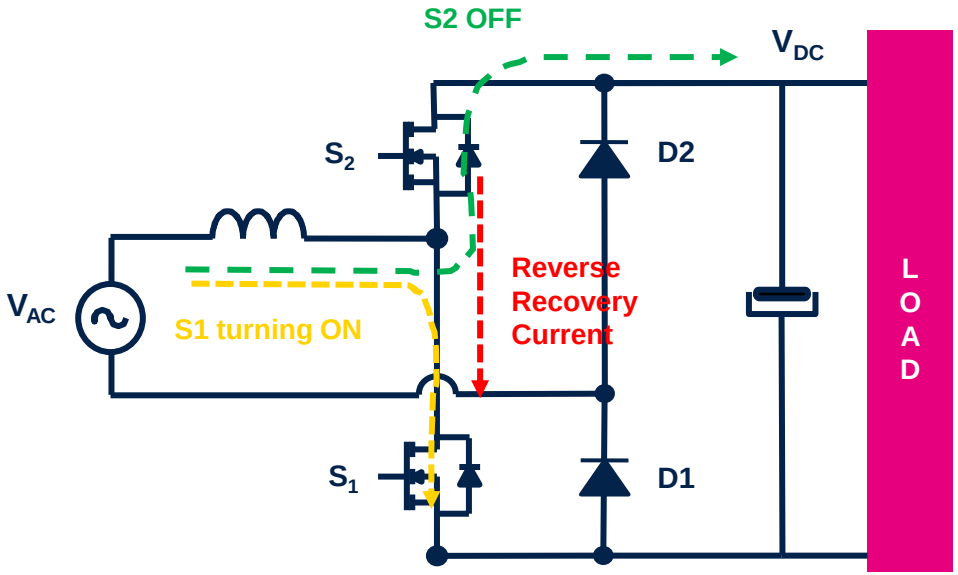
S2 off, inductor current falling



SCRs are controlled according to the AC line polarity in PFC steady state operation

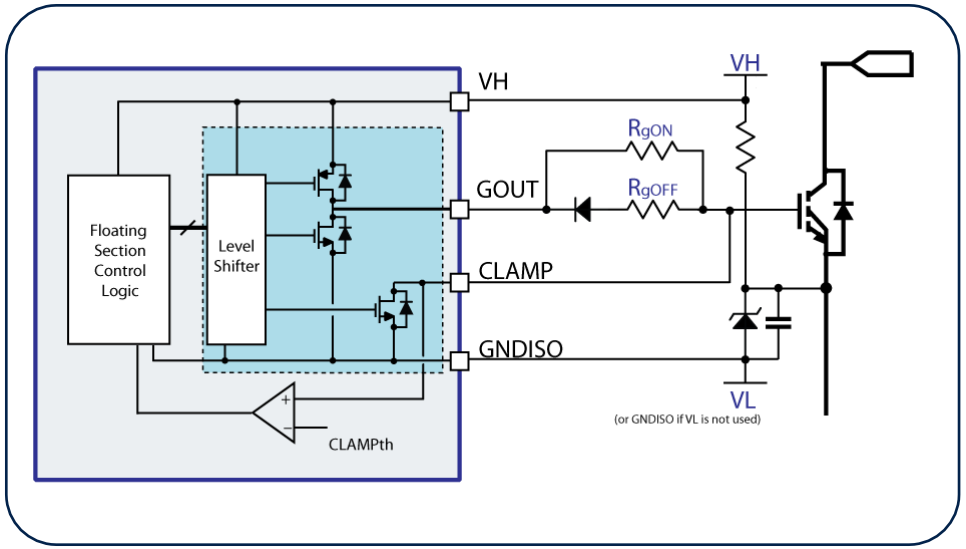
SiC MOSFET and driver IC

650V/1200V Gen2 SiC MOSFET



- Low body diode reverse recovery.
- Low switching loss due to outstanding figure of merit
- Low power loss at high temperature due to less temperature dependence of on resistance

Simple Isolated Driver w/wo Miller Clamp

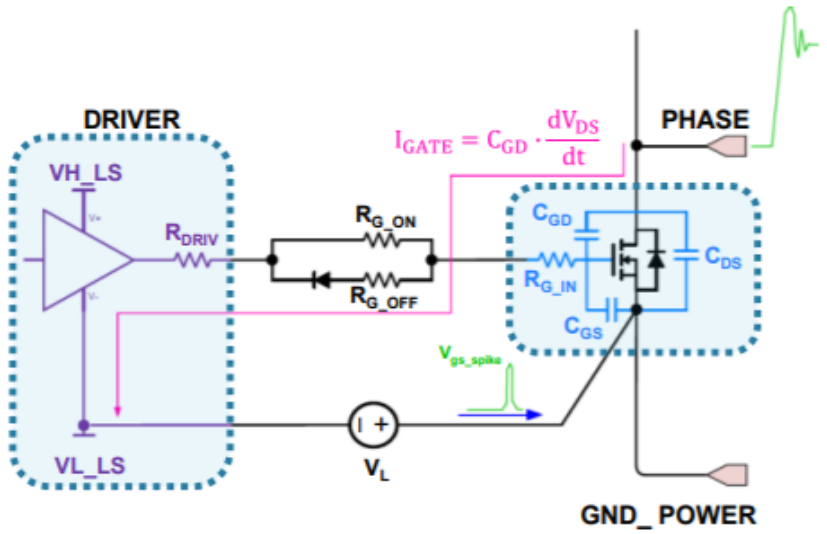


- Positive gate drive: +18V
- Negative gate drive: -3V or -5V
  and / or Miller Clamp
- CMTI : ± 100 V/ns
- High current capability: 4A.

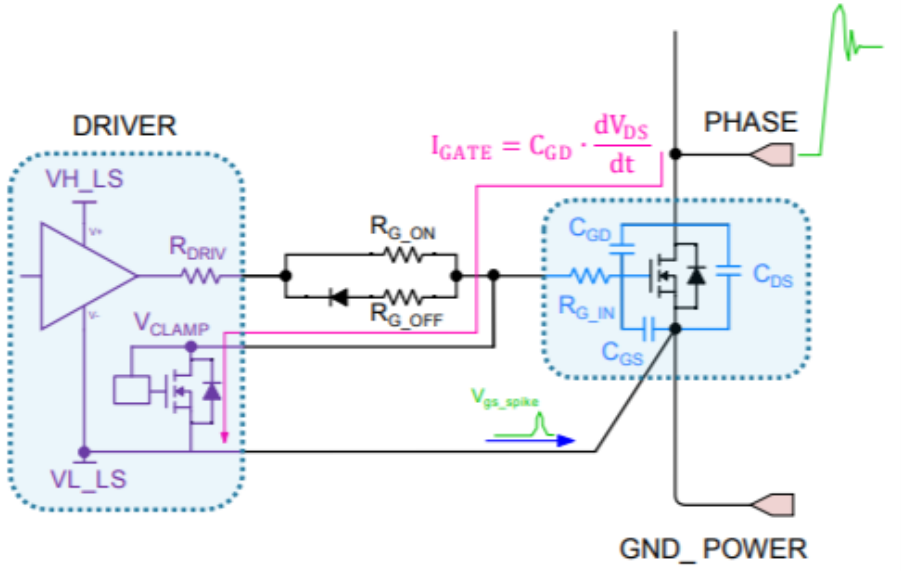
Mitigation techniques for induced G-S glitches

- SiC MOSFET can generate high slew rate dv/dt transients
- High slew rate dv/dt may generates Miller turn-on spike at gate terminal
- Active miller clamp feature minimizes Vgs glitch
- Negative turn-off bias also helps to prevent fault trigger due to Vgs glitch

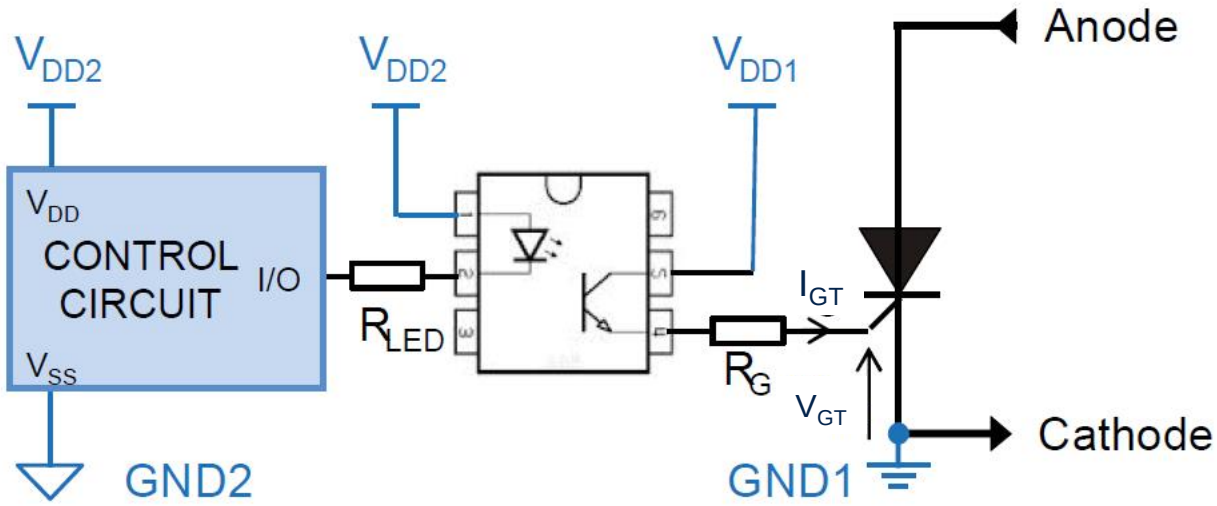
Negative gate driving



Active Miller Clamp



Insulated control circuit for driving SCR Thyristors



$$R_G \leq \frac{V_{DD1\ \min} - V_{CE_{(sat)}\ max} - V_{GT(Tamb\ min)}}{I_{GT(Tamb\ min)}}$$

$$R_{LED} \leq \frac{V_{DD2\ \min} - V_{F\ max}}{\frac{I_{GT(Tamb\ min)}}{CTR,min}}$$

- I_{GT} : Current to apply between gate and cathode to turn-on the device
- V_{GT} : The voltage to apply across gate and cathode

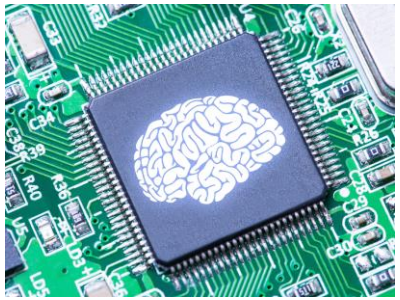
- Opto transistor can be used to develop the SCR triggering circuit insulated from the control unit (which is usually the MCU).
- VDD2 is the supply of the control circuit. VDD1 is the supply used to provide SCR with a gate current. VDD1 and VDD2 supplies have to be insulated from each other.
- VDD1 supply can easily be implemented using a secondary winding added to a flyback transformer

STEVAL-DPSTPFC1 digital solution

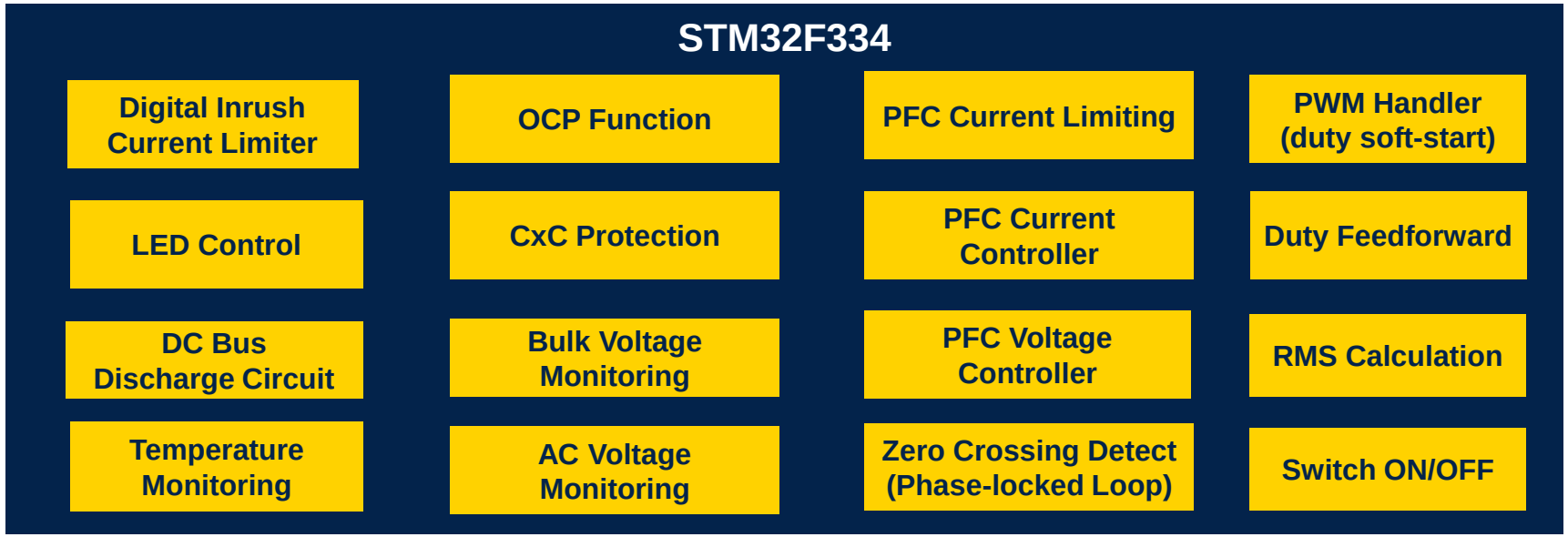
- Feature rich STM32F334 MCU for digital control

72MHz Cortex-M4 with FPU and High-resolution timer (**217ps**) for precise control

Rich analog peripheral set for power conversion applications including fast ADCs (**5Msps**), comparators, DACs and op-amp



- Functional block

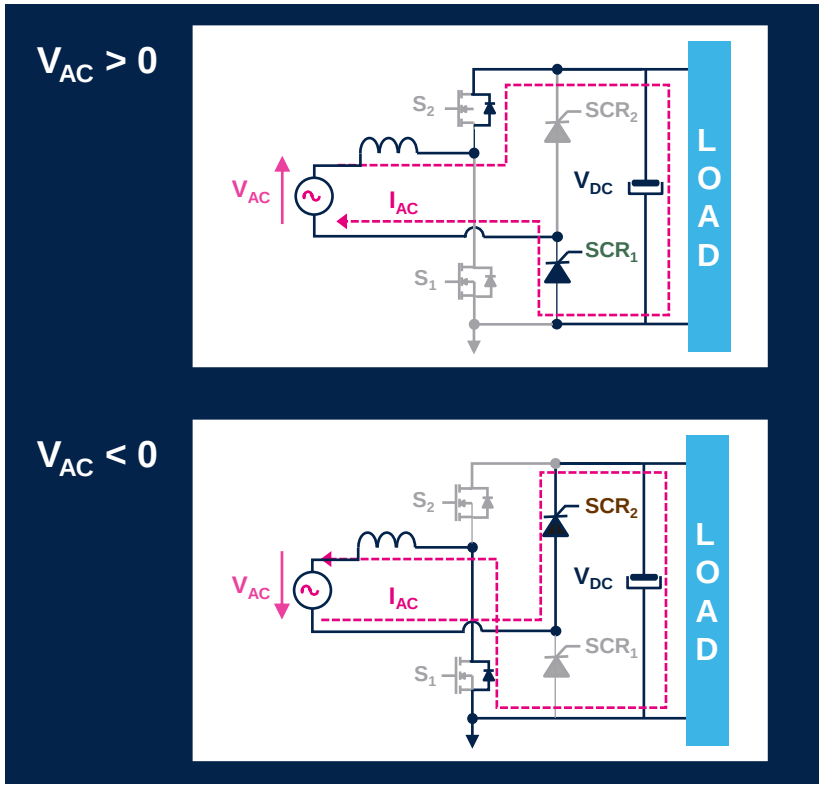


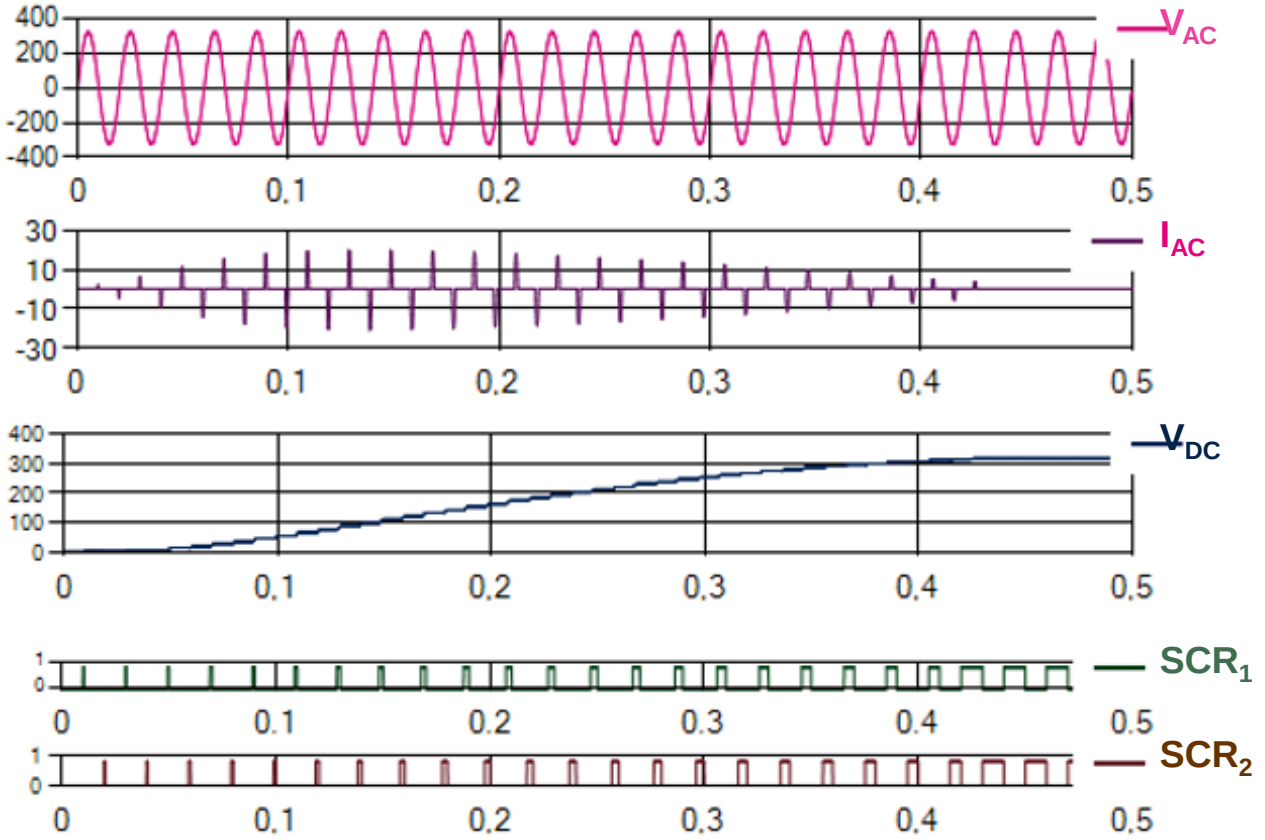
Advantages of Digital Power Control:

- High flexibility and good adaptability
- Reduced BOM and downsizing
- Improved time to market and customization
- Intelligent and safety
- High reliability

Digital Inrush Current Limit (ICL) control

The SCR gate signals limit the AC inrush current by progressive phase control on SCR



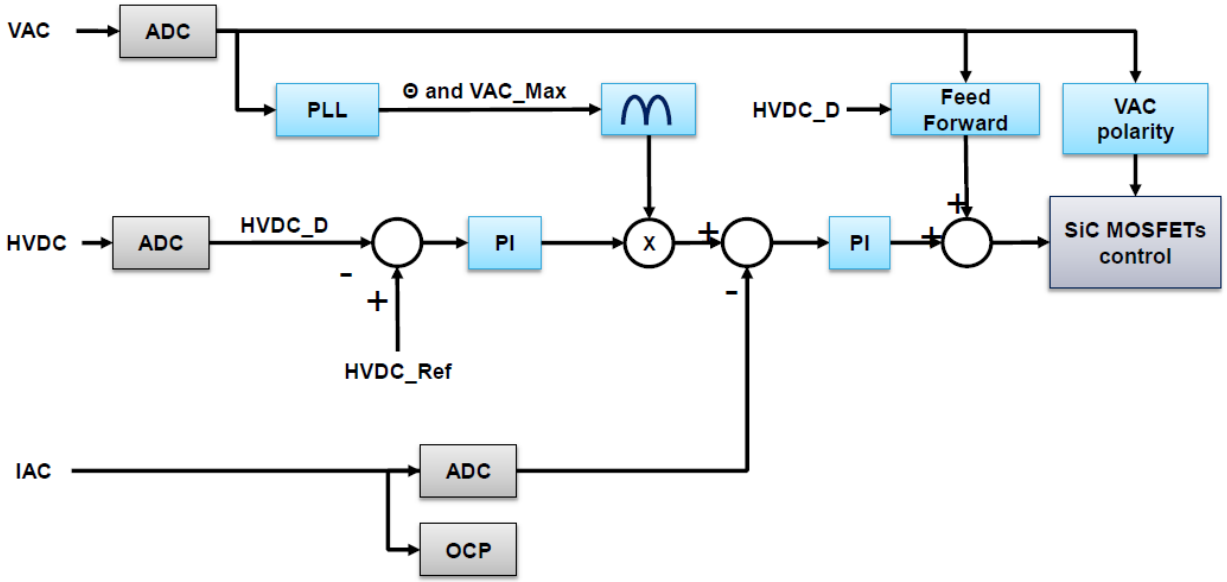


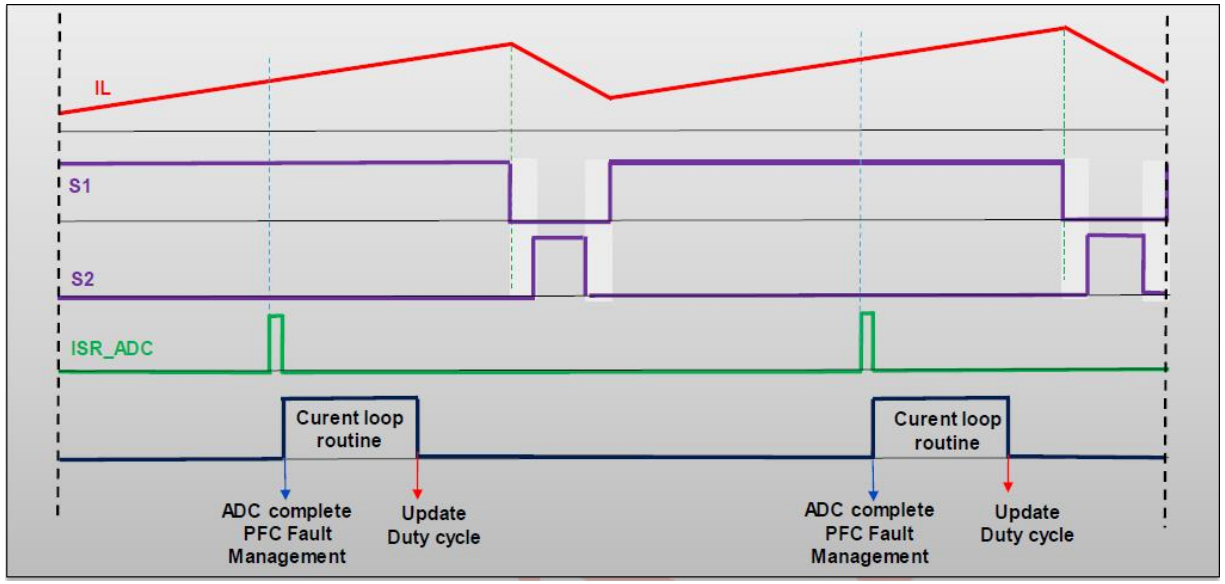
Control block diagram

PFC Control Algorithm

- Voltage (outer) loop: performed at 2 times of AC line frequency
- Current (inner) loop: performed at 72kHz
- PLL: to synchronize the phase of AC line for generation of current reference and for ICL control
- Duty-feedforward is used for PF/iTHD improvement and transient response

$$d_{FF} = \frac{HVDC - VAC}{HVDC}$$

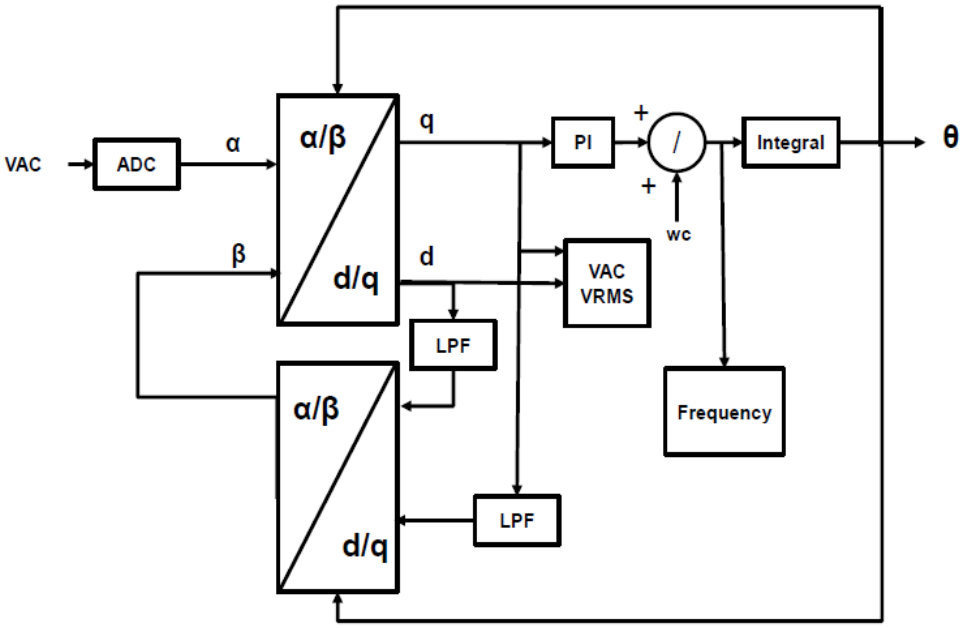


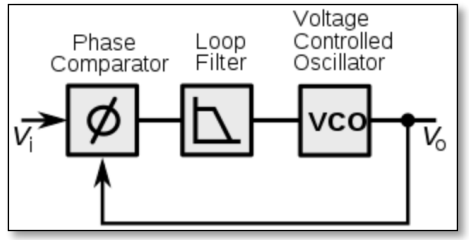


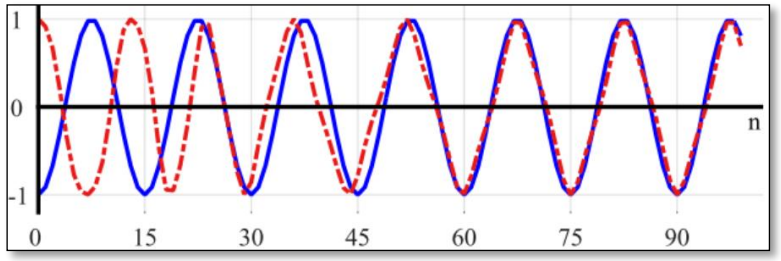
Zero Crossing Detection by PLL

PLL (phase-locked loop) - Synchronous Reference Frame (SRF)

- PLL based on SRF is one of the widely used algorithms for grid synchronization
- Quick and accurate phase detection
- Better noise immunity compared to hardware ZCD circuit

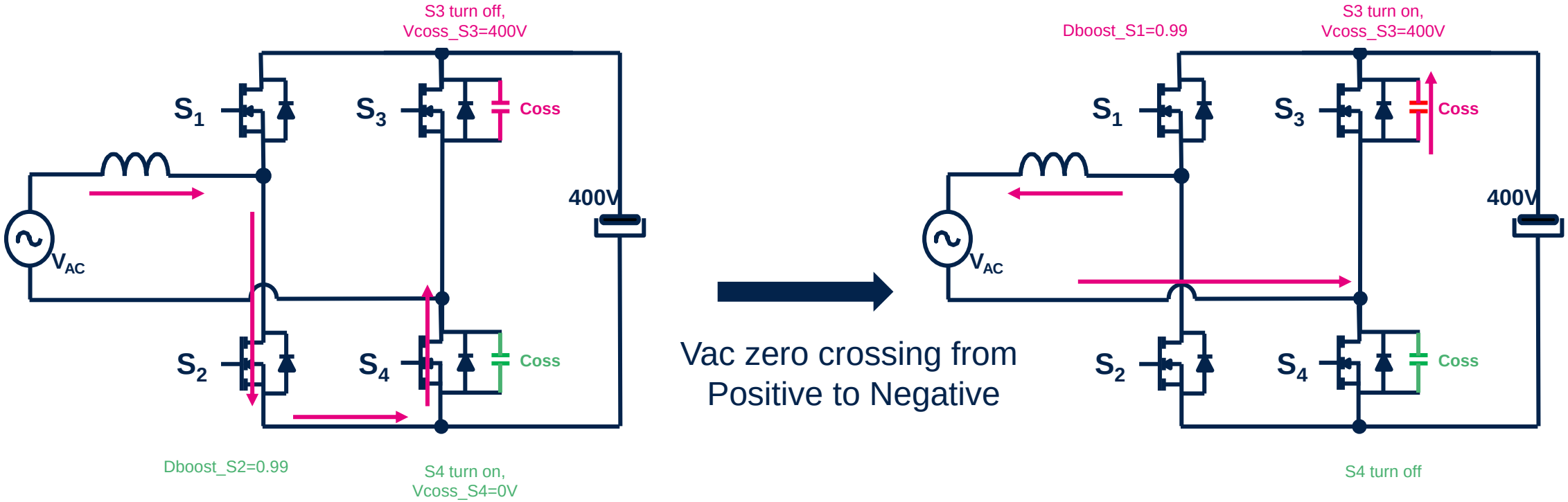






- Inverse d-q transformation for single-phase system is employed here:
  - PLL execution at 18kHz
  - Accuracy of line synchronization: +/- 55.5us
  - Θ is used for PFC current reference generation and for soft-start control at line zero crossing
  - To measure RMS voltage

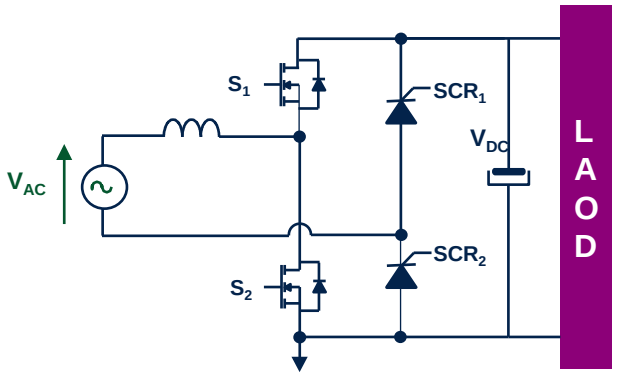
Design challenge
Current spike at AC zero crossing

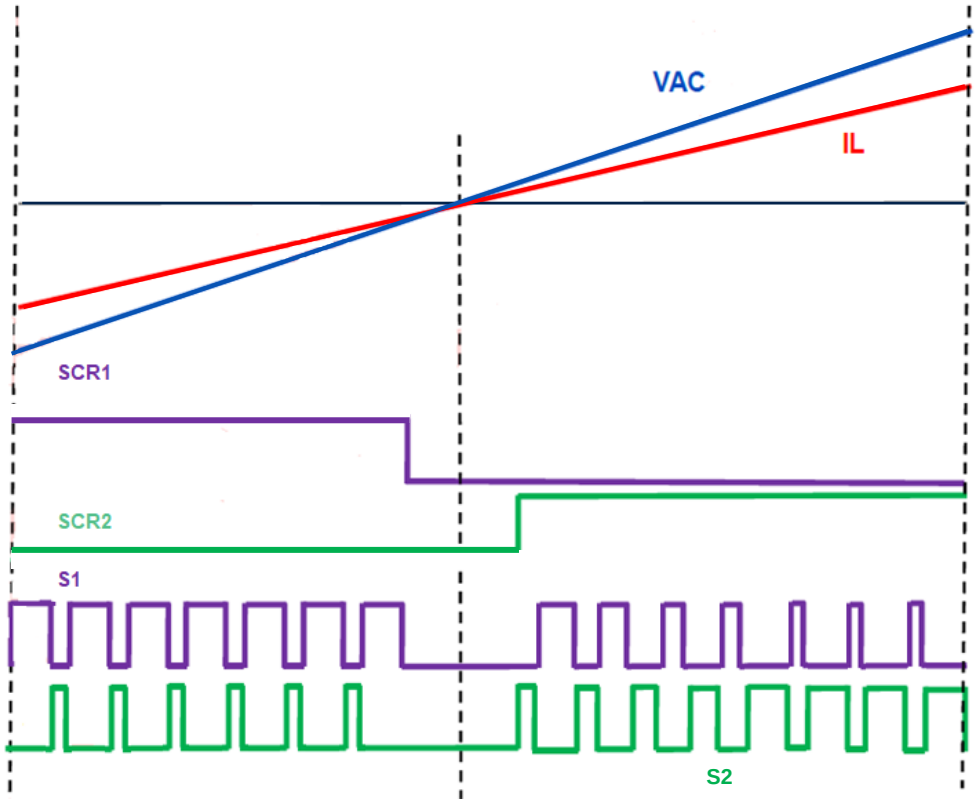


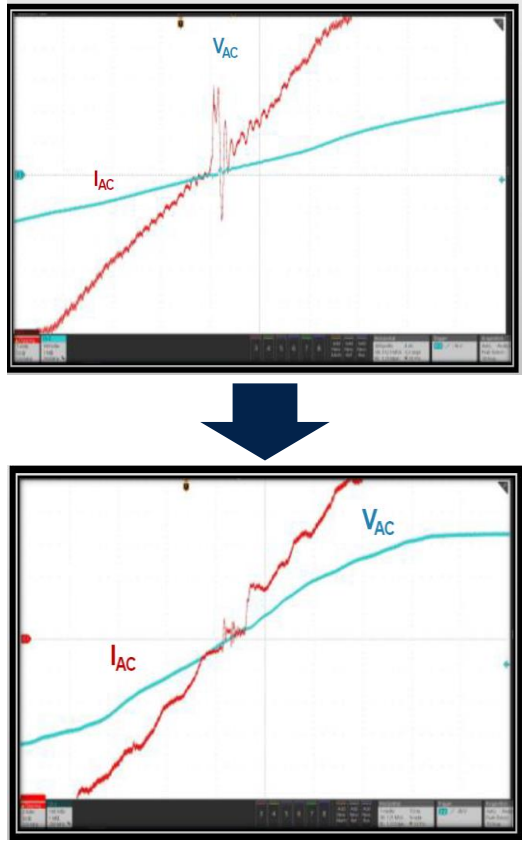
- At a zero-crossing when the AC input is going from positive to negative.
  - Before zero-crossing, Vcoss_S3=400V, Dboost=0.99 to S2, (1-Dboost)=0.01 to S1
  - After zero-crossing, Vcoss_S4=400V, Dboost=0.99 to S1, (1-Dboost)=0.01 to S2
- Right at zero-crossing, if Dboost changes abruptly, the Vcoss_S3 will cause a current spike.

Soft duty cycle control to reduce current spike

To reduce this current spike at each zero crossing of the AC line voltage, S1 or S2 active switches are controlled with a soft duty cycle.





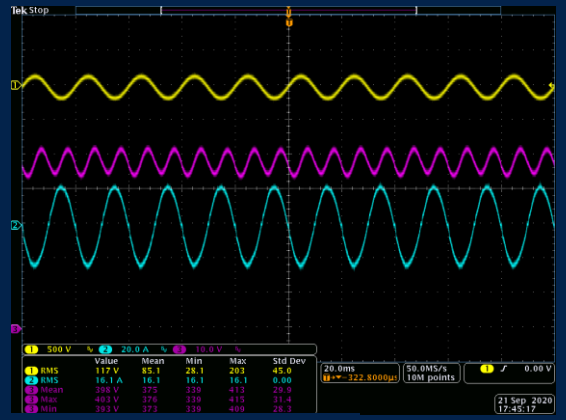


EVM Board Performance

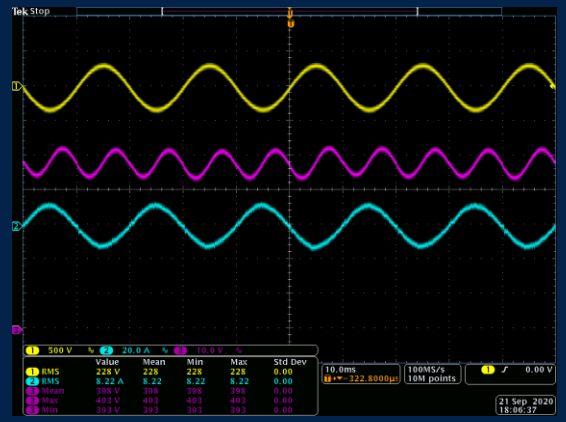
AC input current measurement

- 115Vac, 800W

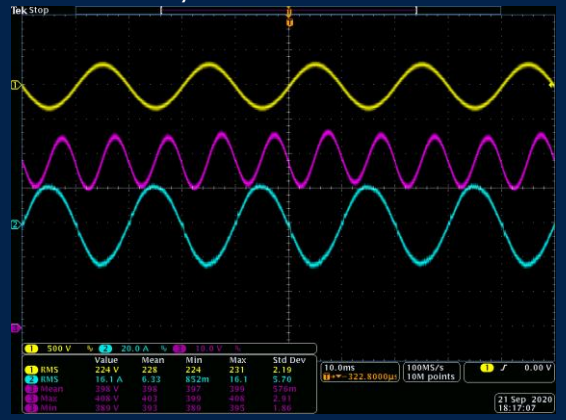
- 115VAC, 1600W



- 230Vac, 1800W

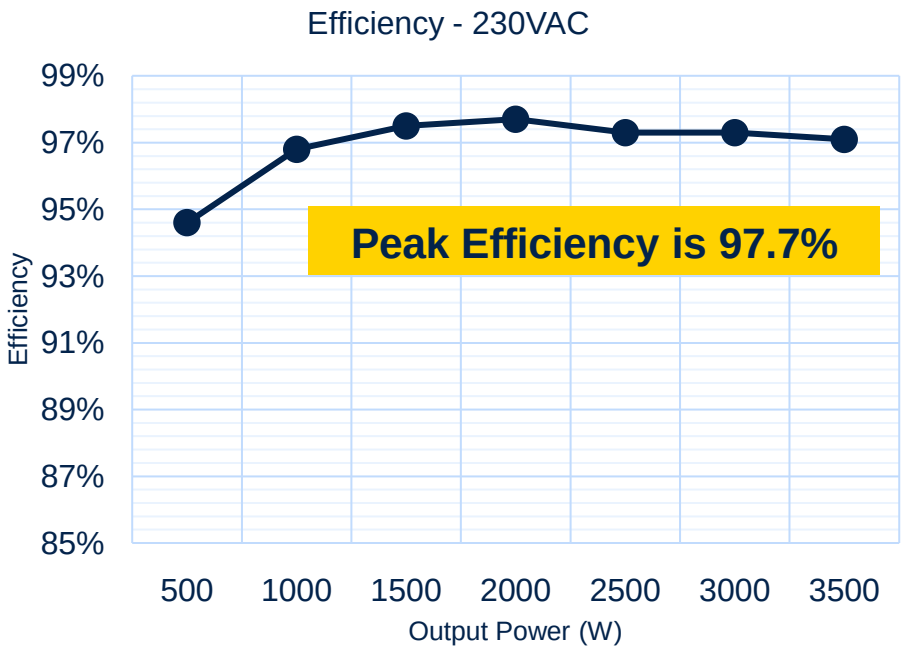


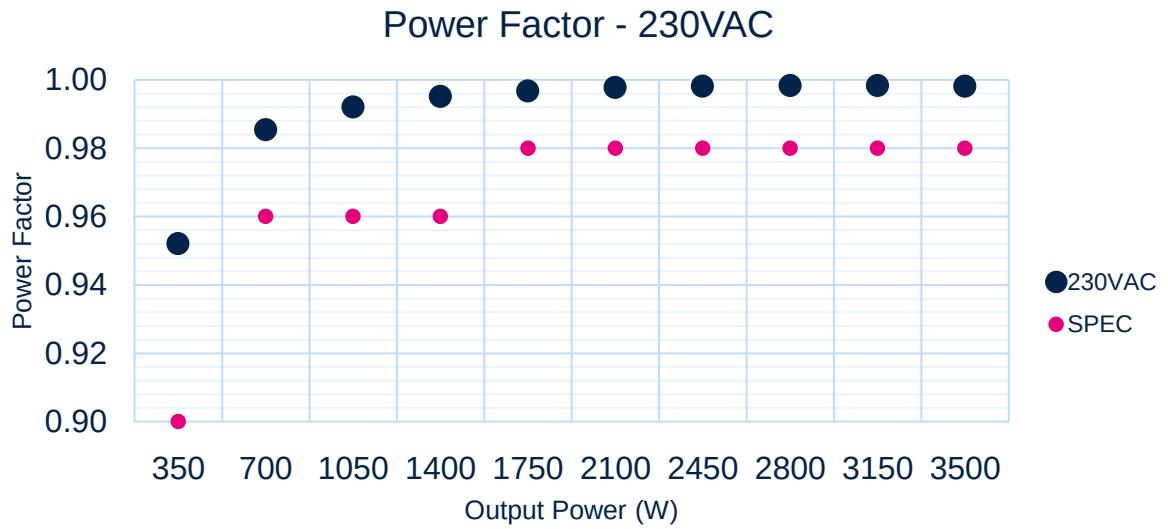
- 230VAC, 3500W

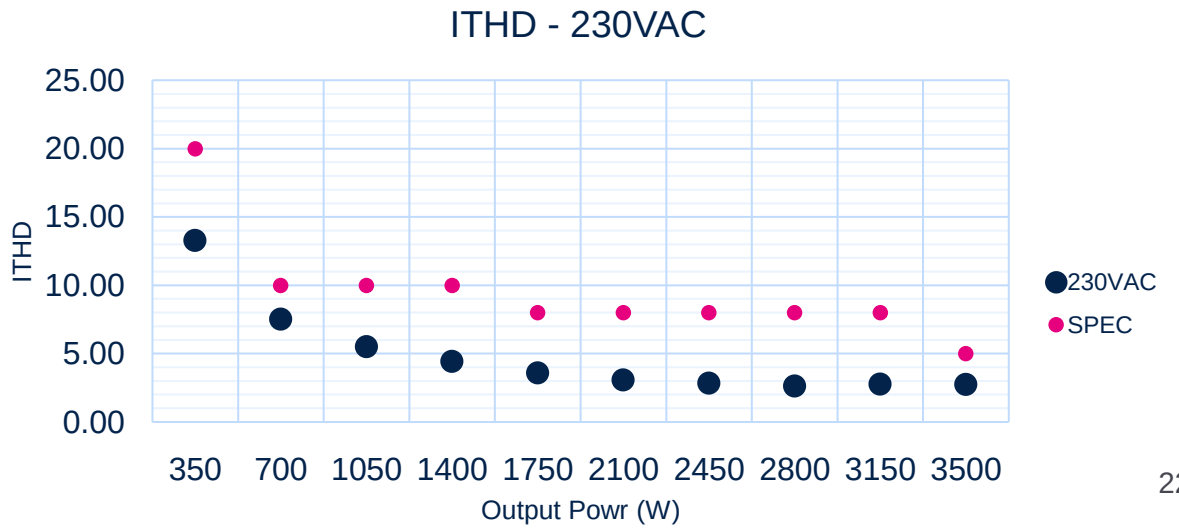


CH1: Input Voltage
CH2: Input Current
CH3: PFC Output Voltage

Efficiency / ITHD / power factor

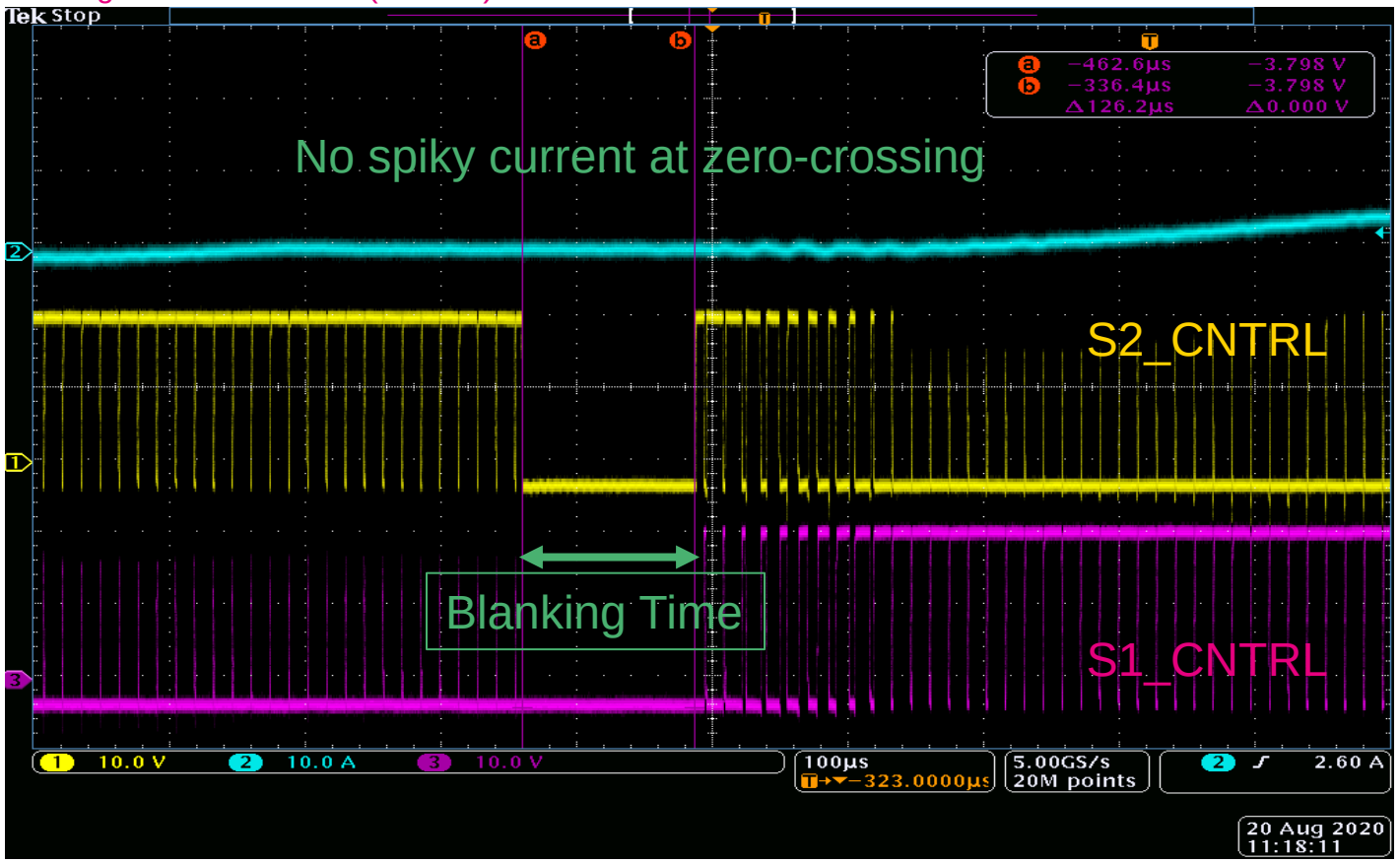






Soft duty cycle control to reduce current spike

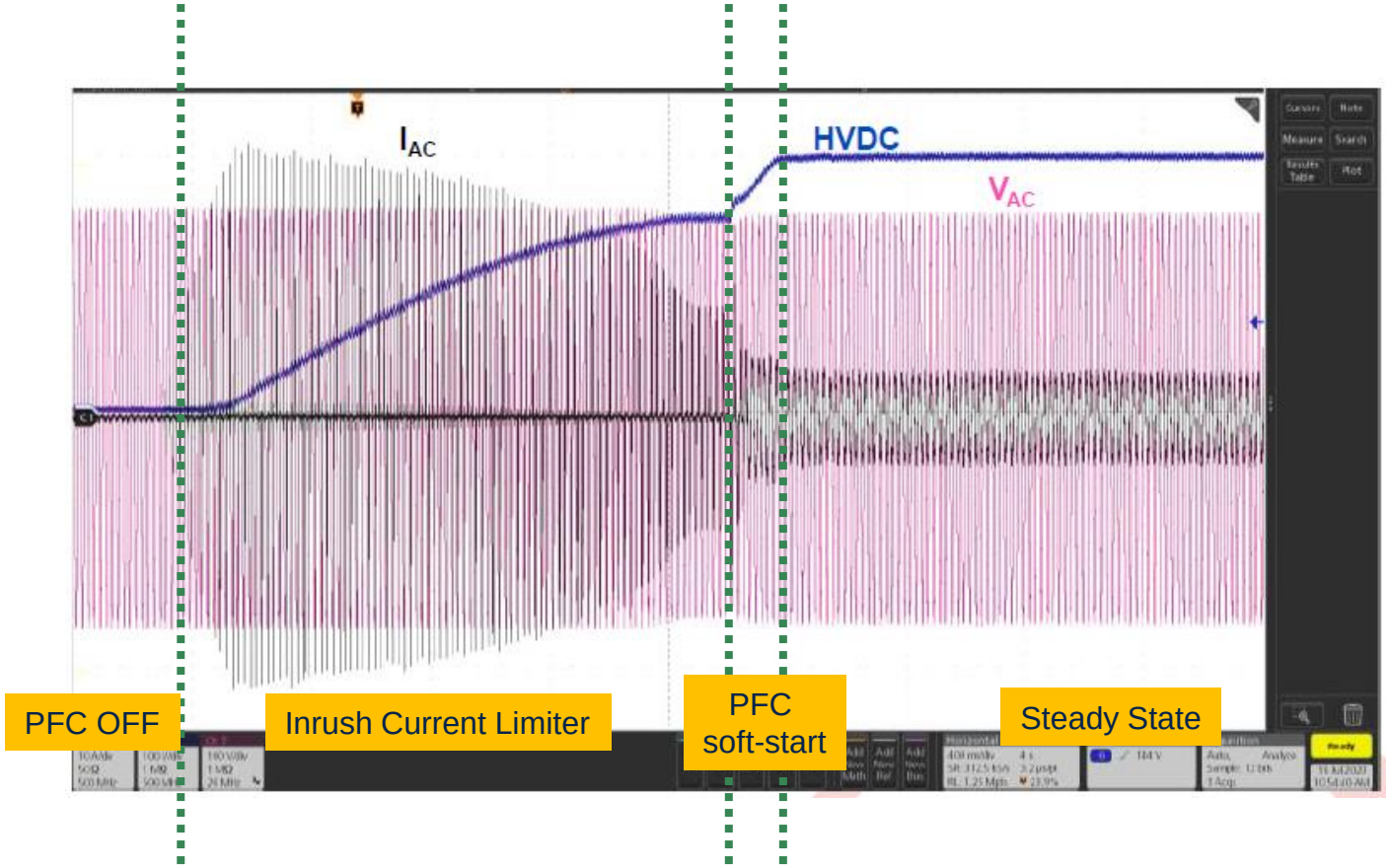
CH1: Vgs of high-side SiC (10V/div)
CH2: Input Current (10A/div)
CH3: Vgs of Low-side SiC (10V/div)



- S1 or S2 (according to AC line polarity) starts a soft turn-on with a small pulse width and gradually increases.
- The control loop should freeze during this blanking time to avoid the integrator of the current loop generating a large PWM pulse, which can cause a large current spike.

Inrush Current measurement

VAC = 230VRMS @ 50Hz, POUT = 1kW



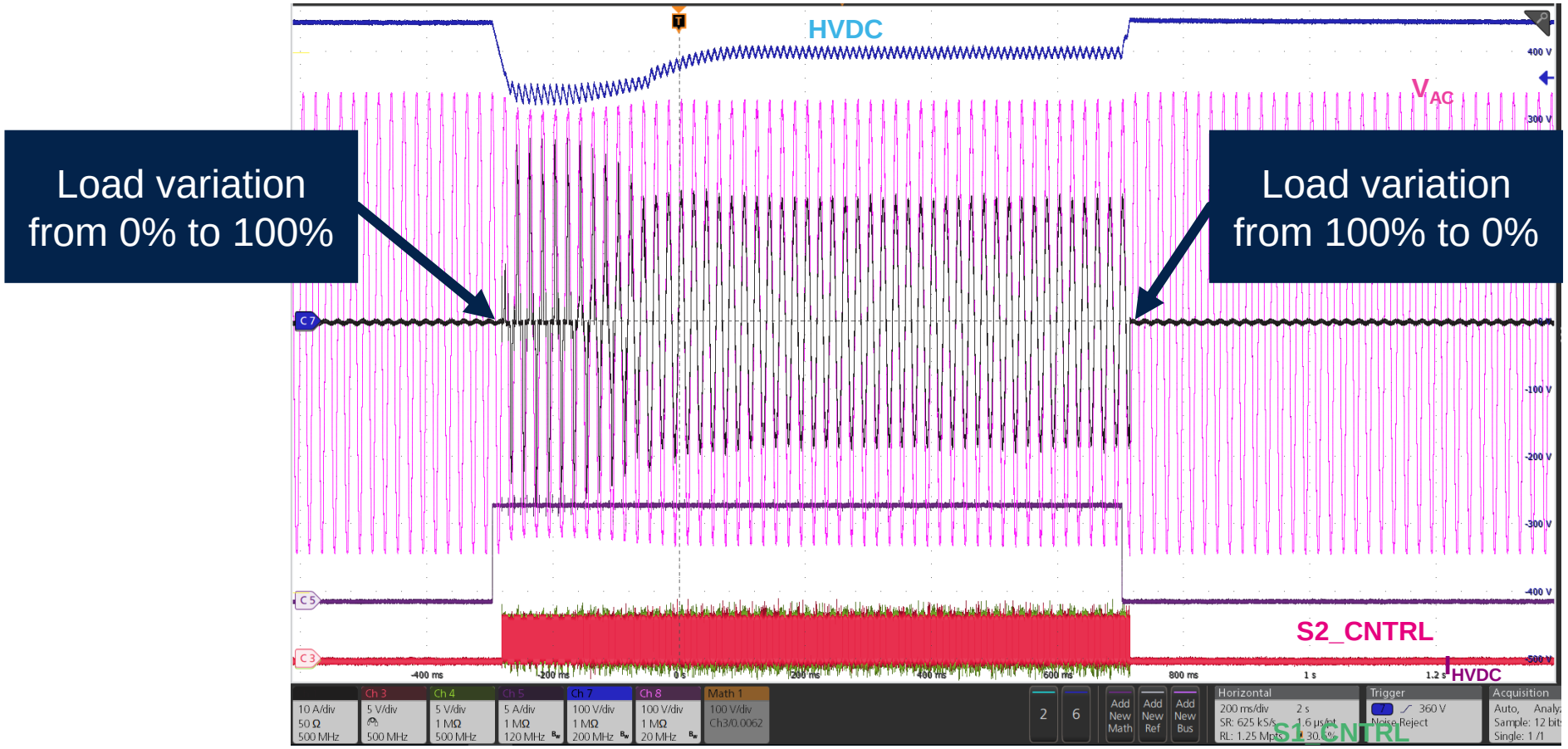
To ensure a smooth PFC start-up, a soft start routines has been implemented on the MCU firmware:

- **Inrush current limiter**: SCRs are controlled with a progressive phase control and the output capacitor can be smoothly up to the AC line peak voltage.
- **PFC soft start**: The output voltage reference is controlled from AC line peak voltage to 400V dc with a smoothly voltage ramp.

Load variation

Excellent transient load variation thanks to feed forward digital implementation

VAC = 230VRMS @ 50Hz

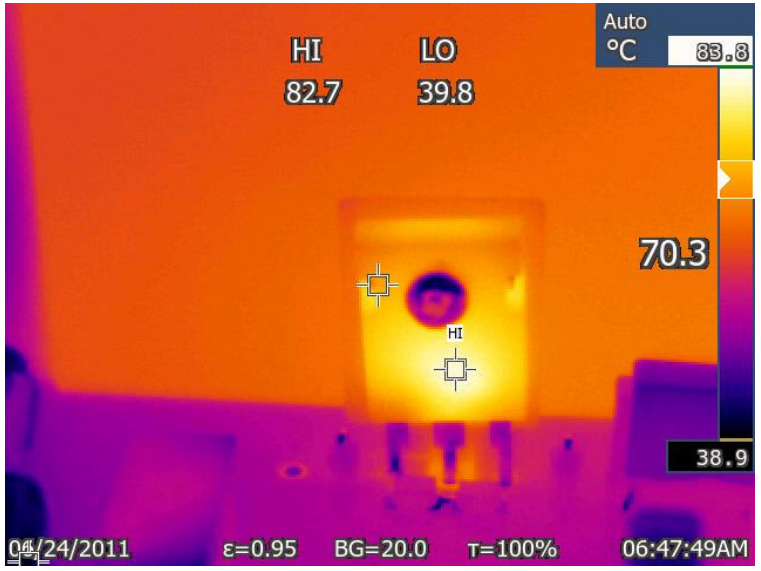


Power device temperatures

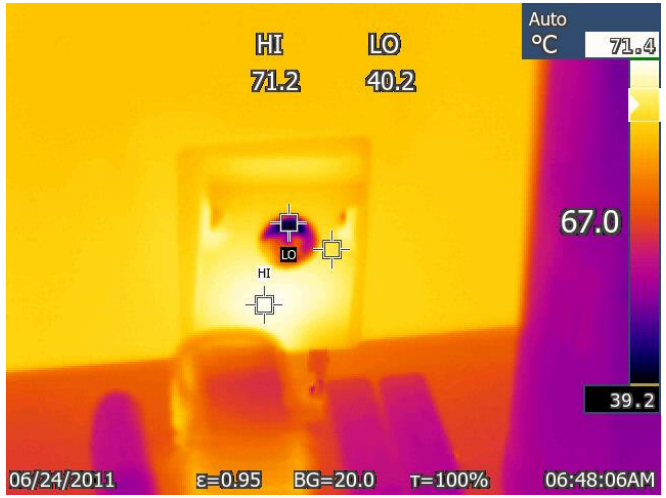
The board is equipped with overtemperature protection mounted on the heatsink

VAC = 230VRMS @ 50Hz
Pout = 3600W @ 28C ambient

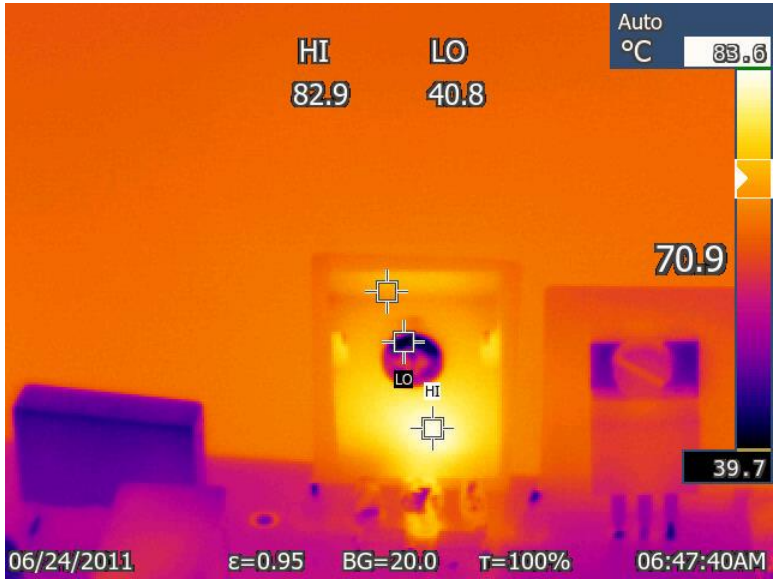
Low side SiC MOSFET



High side SCR



High side SiC MOSFET



ST Product for Totem-Pole PFC

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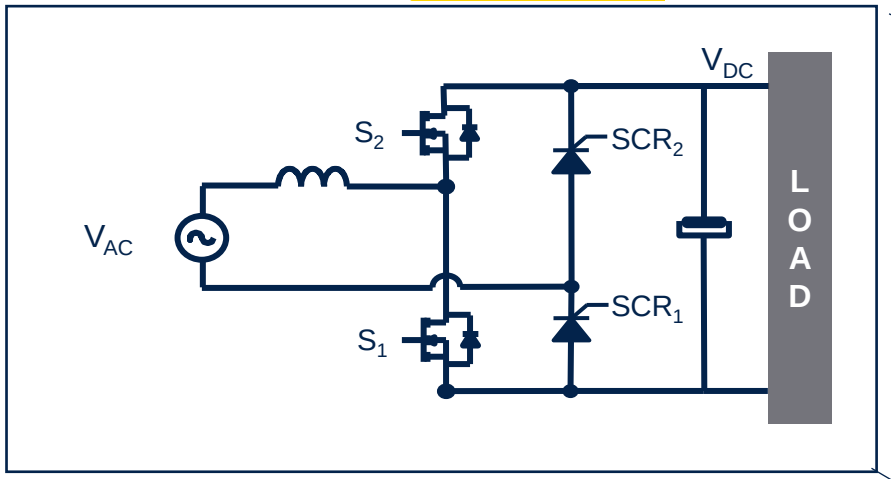
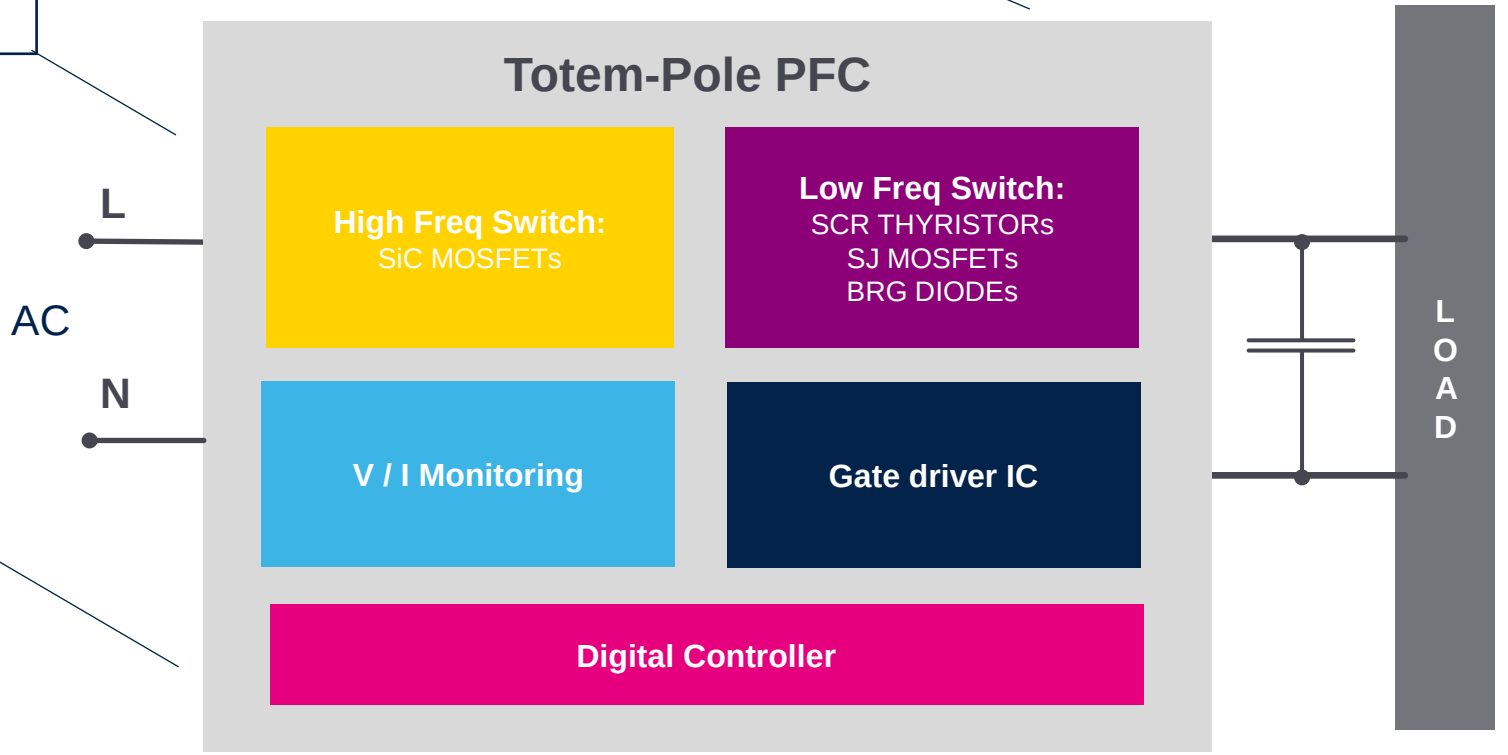
ST product for Totem-Pole PFC





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SiC MOSFETs

STPOWER SiC MOSFET: 650 V Gen2

Part Number	V_{DS} (V)	$R_{DS(ON)}$ Typ @ 25° C (Ω)	I_D (A)	Package			
				HiP247	HiP247-LL	HiP247-4LL	H2PAK-7L
				T_J MAX= 200°C			T_J MAX= 175°C
SCTx35N65G2V	650	0.55	45	X	X		
SCTWA35N65G2V-4*						X	
SCTH35N65G2V-7							X
SCTW35N65G2VAG*				X			
SCTH35N65G2V-7AG							X
SCTx90N65G2V	650	0.018	119	X	X		
SCTWA90N65G2V-4*						X	
SCTH90N65G2V-7							X
SCTW100N65G2AG		0.020	100	X			
SCTH100N65G2-7AG							X

STPOWER SiC MOSFET: 1200 V Gen2

Part Number	V_{DS} (V)	$R_{DS(ON)}$ Typ @ 25° C (Ω)	I_D (A)	Package			
				HiP247	HiP247-LL	HiP247-4LL	H2PAK-7L
				T_J MAX= 200°C			T_J MAX= 175°C
SCTW40N120G2VAG	1200	0.075	33	X			
SCTW40N120G2V*		0.070	45	X			
SCTWA40N120G2V-4*						X	
SCTW60N120G2AG		0.045	60	X			
SCTW70N120G2V		0.025	95	X			
SCTWA70N120G2V-4*						X	


H²PAK-7L


HiP247 LL


HiP247-4L

KEY FEATURES

- Very low switching losses
- Low power losses at high temperatures
- Higher operating temperature (up to 200 °C)
- Body diode with no recovery losses
- Easy to drive

KEY BENEFITS

- Smaller form factor and higher power density
- Reduced size/cost of passive components
- Higher system efficiency
- Reduced cooling requirements and heatsink size

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Isolated gate drive for SiC MOSFET

1700 V Galvanic isolated Single & Dual channel

SO-8

STGAP2S
STGAP2SC

SO-16

STGAP2D

- Galvanic isolated, up to 1700 V high voltage rail
- Extreme Transient Immunity up to ± 100 V / ns
- Fast Switching Frequency (Tp 80ns only)
- High current capability 4A Isink / Isource

6000 V Galvanic isolated Single & Dual channel

SO-8W

STGAP2HS
STGAP2HSC

STGAP2SiCS
STGAP2SiCSC

- Galvanic isolated, up to 6000 V high voltage rail
- Extreme Transient Immunity up to ± 100 V / ns
- Fast Switching Frequency (Tp 80ns only)
- High current capability 4A Isink / Isource

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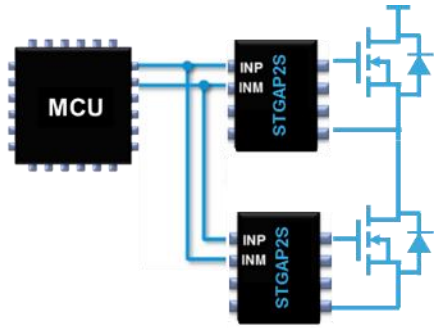
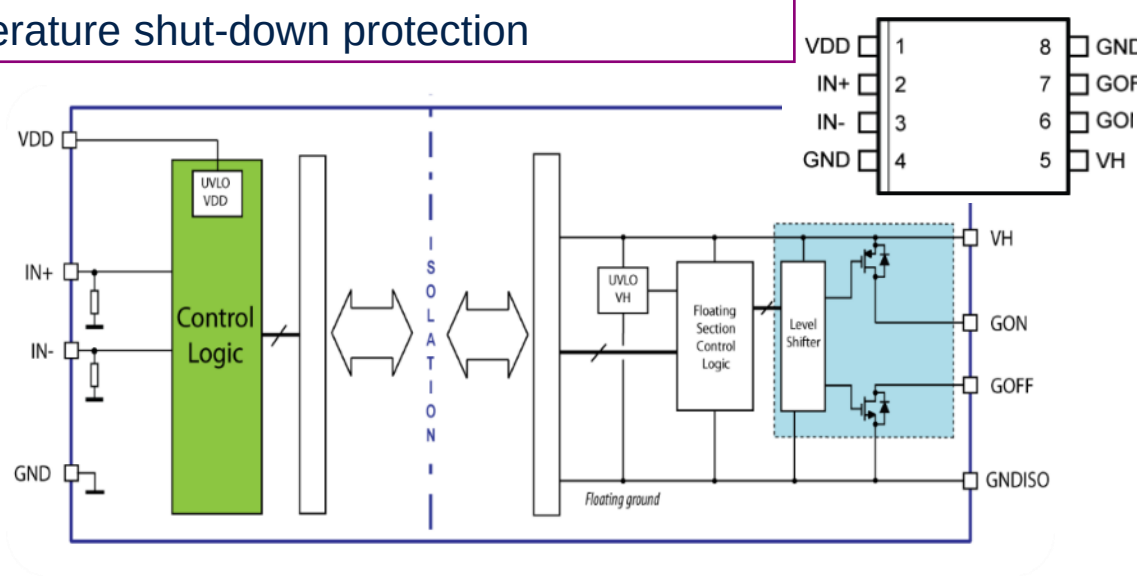
STGAP2S, STGAP2SC

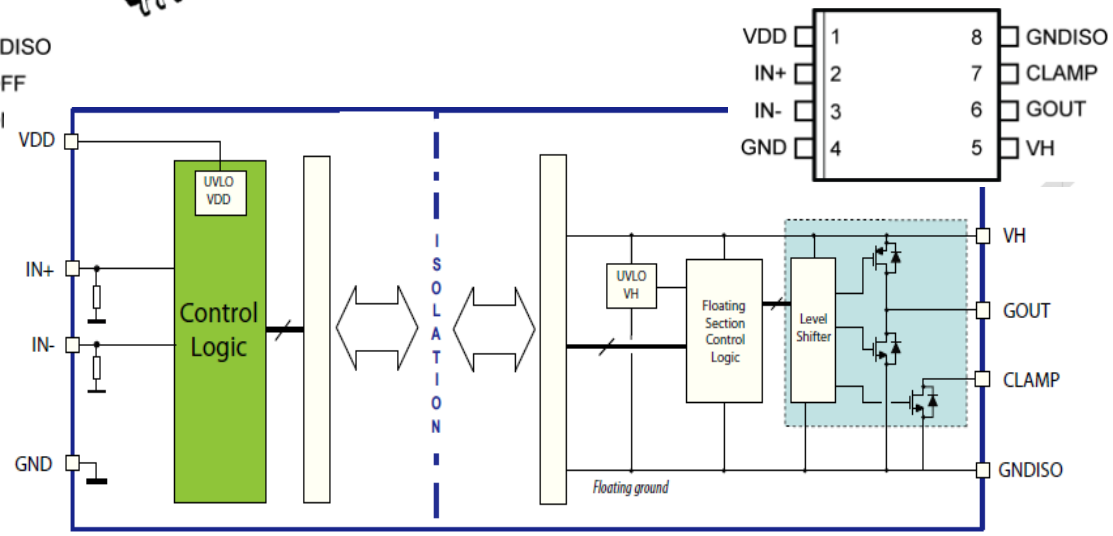
1700 V, 4A isolated gate drivers

- 3V3 / 5 V logic inputs (logic thresholds 1/3, 2/3 of VDD)
- **Up to 26 V supply voltage**
- **4 A Sink/Source current capability**
- Short propagation delay: 80 ns
- UVLO Function
- Stand-by function
- 100 V/ns CMTI
- High voltage rail up to 1700 V
- Temperature shut-down protection

- Active High & Active Low input pins, for HW interlocking
- **STGAP2S**: Separated Outputs option for easy gate driving tuning
- **STGAP2SC**: Miller CLAMP pin option to avoid induced turn-on
- Negative gate drive ability
- SO8 Package







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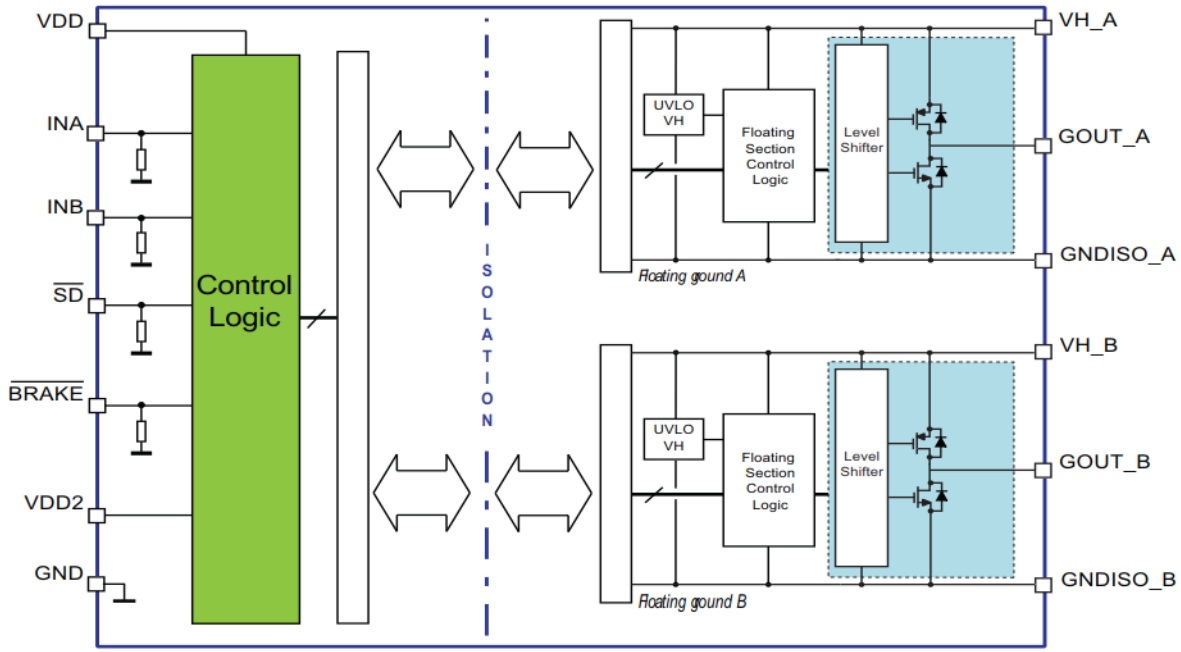
STGAP2D

1700 V, 4A isolated gate drivers

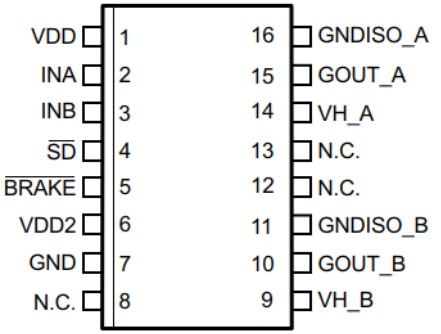
- 3V3 / 5 V logic inputs (logic thresholds 1/3, 2/3 of VDD)
- **Up to 26 V supply voltage**
- **4 A Sink/Source current capability**
- Short propagation delay: 80 ns
- UVLO Function
- Stand-by function
- 100 V/ns CMTI
- High voltage rail up to 1700 V
- Temperature shut-down protection

- Single input pin, in phase with output
- Shut-Down SD pin, with integrated pull-down
- BRAKE pin
- Interlocking
- Negative gate drive ability
- SO16 Package



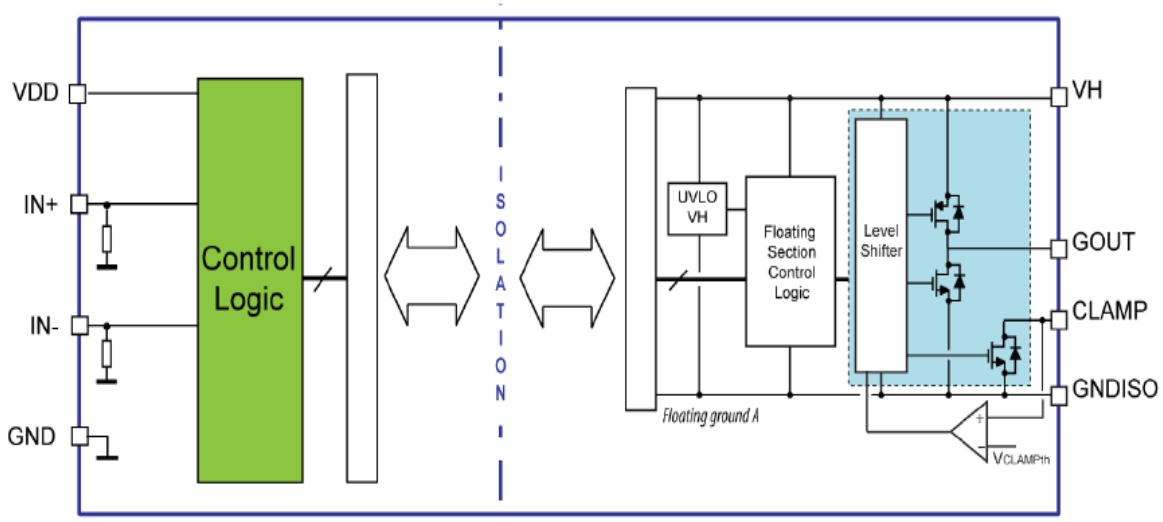
KEY APPLICATIONS

- Motor control
- Factory automation
- Industrial drives and fans
- DC-DC converters
- Induction heating
- Welding



STGAP2SiCS, STGAP2SiCSC

6k Galvanic isolated single channel, 4 A gate driver for SiC



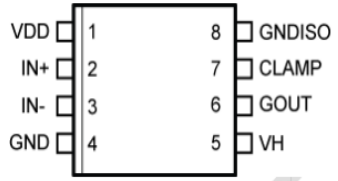
Key benefits & features

High performance **for SiC**

- Galvanic isolated up to 6kV
- 4 A sink / source driver current capability
- **> 100 V / ns transient immunity**
- 3.3 to 5 V TTL/ CMOS inputs with hysteresis
- **Propagation delay 80ns**

Robustness

- UVLO **optimized for SiC**
- Miller Clamp
- Thermal Protection



Minimum footprint and lightweight

- Compact and simplified layout SO8W package

KEY APPLICATIONS

- Motor control
- Factory automation
- Industrial drives and Fans
- DC/ DC converters
- Welding

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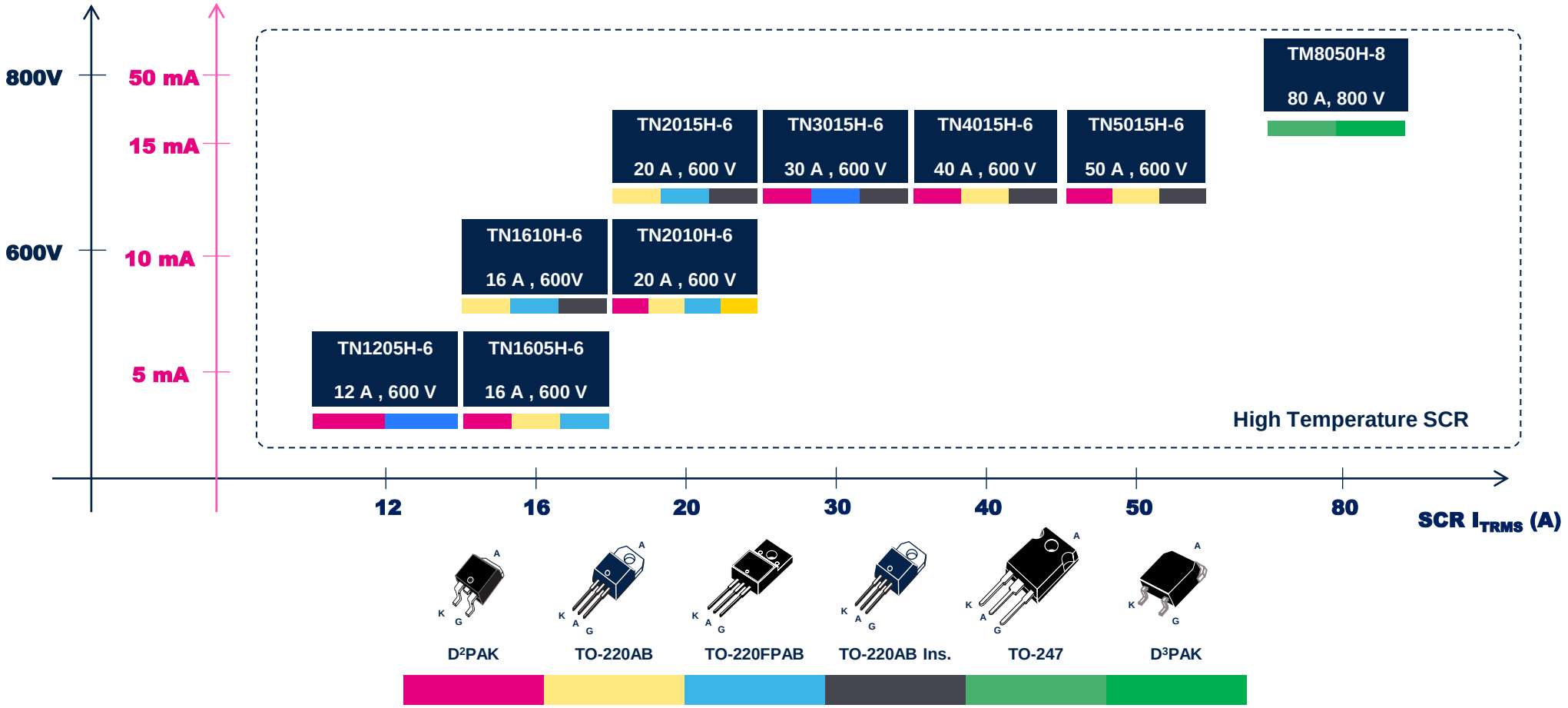
600V - 800V SCR Thyristors



STMicroelectronics, ADG-DFD , Thyristor line

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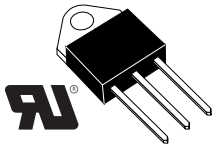
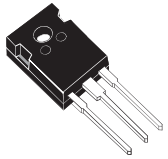
1200V SCR Thyristors

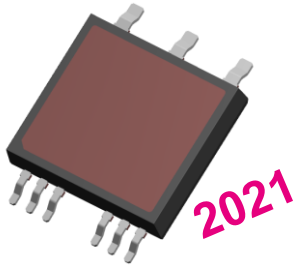
Versatile and robust devices for EV OBC, charging stations, UPS
Fast and controlled inrush current limitation



TOP3 Insulated



TO-247 Long Lead



ACEPACK SMIT

Part Number	I_{TRMS}	I_{TAV}	I_{TSM}	Package				App Power	$I_{AC\ RMS}$
	(A)	(A)	(A)	TO-247	D^2PAK	TOP3I	A-SMIT	(kW)	(A)
TN3050H-12Y	30	20	300	●	●			3.7	16
TN5050H-12	50	30	450	In dev		●		6	24
TN6050HP-12Y	60	40	600	●			In dev	7.4	32
TN8050H-12	80	50	720	Next		Next		10	45

150°C reliability with over time stability

High switching life expectancy

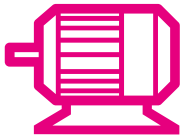
Enable system to resist 6kV surge

Robustness against inrush currents

High speed power up / line drop recovery

Critical Power UPS

IE3 Motor Starters



Charging Stations

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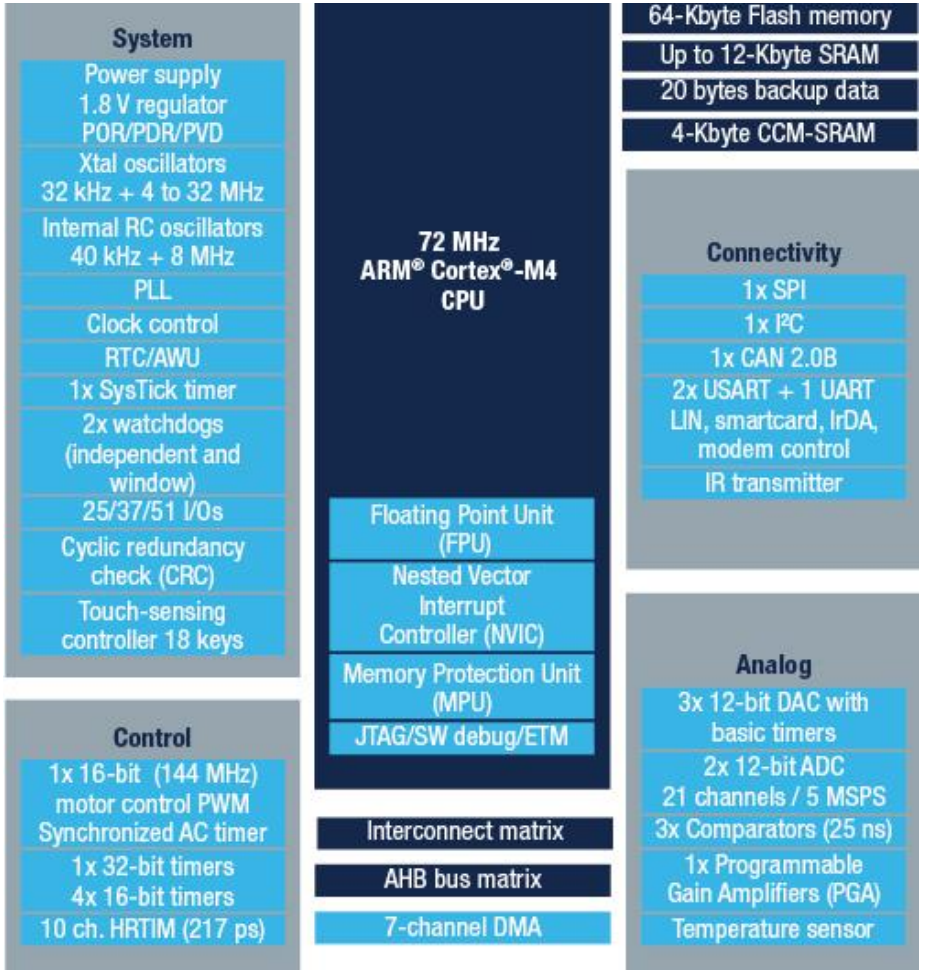
STM32F334 MCU

The STM32F334 product line is ideal for digital power conversion applications like D-SMPS, lighting, welding, inverters for solar systems and wireless chargers

72MHz Cortex-M4 with FPU and High-resolution timer (**217ps**) for precise control

Rich analog peripheral set for power conversion applications including fast ADCs (**5Msps**), comparators, DACs and op-amp

MAIN APPLICATIONS



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Digital Power Supply and PFC Design Workshop with STM32 MCUs in collaboration with the company partner Biricha (from Q4 2019)

BIRICHA DIGITAL

Summary

Summary

- This evaluation board focuses on Totem-Pole PFC converter, which increases the efficiency by eliminating the diode bridge loss.
- Using SCRs operating at low frequency leg to allow inrush current limit control and also to help remove bulky NTC/Relays.
- ST provides the latest technologies (SiC/STGAP/SCR/STM32) for high power and high efficiency solutions on Totem-Pole PFC.
- This reference design offers:
  - Digital power solution for totem-pole PFC converter
  - Peak efficiency is about 97.7%
  - iTHD distortion lower than 5% at maximum load
  - Inrush-current limitation is based on a soft-start procedure of the SCRs controlled.

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Industrial Summit 2020
Shenzhen, China | 2 December
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Thank you

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