Design considerations of 65W active clamp flyback adaptor with MasterGaN

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1. Travel adapter developing
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3. ACF Used in smart charger product
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6. Gate drive signal
7. Noise prevent-PCB layout
8. dv/dt Adjustment
Travel adapter development

- **Power Level Increasing**
  - 5W → 65W → 120W

- **Power Density Increasing**
  - 5W/in3 → 20W/in3 → 30W/in3

- **Switching frequency Increasing**
  - 60kHz → 150kHz → 350kHz
Drawbacks of traditional Flyback

- High power loss and spike caused by leakage inductance of the transformer
- High switching loss of the main MOSFET due to the spike

\[ P_{ON} = I_P^{2(RMS)}R_{DS(ON)} \]

\[ P_{SW-ON(Coss)} = f_{SW} \int_0^{V_{DS(OFF)}} C_{OSS}(V_{ds})V_{ds}dV_{ds} \]

\[ P_{SW-OFF} = \frac{I_P^{2T_{FALL}^2}}{6C_{OSS(eq)}f_{SW}} \]
ACF used in smart charger

- The leakage inductance energy is recycled with clamp circuit, while the Turn-OFF voltage stress across the power switch is minimized.
- The ZVS of the power switch is achieved and subsequently the switching losses are minimized.
- Decrease the stress of the secondary rectifier diode.
ACF used in smart charger

**PROs**

- The energy of the leakage inductance is recycled
- ZVS is achieved and switching losses are minimized → High efficiency and high switching frequency achievable
- Soft-switching architecture

**CONS**

- Additional clamp power switch with dedicated high-side driver
- Increases the complexity of the controller
- Much more difficult to design and optimize compared with a standard flyback
GaN vs. Silicon based transistors

- Gallium Nitride (GaN) is a wide-bandgap (WBG) material. HEMT (High Electron Mobility Transistor) gallium nitride (GaN) transistors, or simply GaN transistor, represents a major step forward in power electronics, providing high frequency operation, increased efficiency and higher power density compared with silicon-based transistors.

<table>
<thead>
<tr>
<th>Comments</th>
<th>GaN</th>
<th>Silicon</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>Qg-Gate charge</td>
<td>Lower</td>
<td>Higher</td>
<td>GaN with lower driver loss to achieve higher frequency &amp; efficiency</td>
</tr>
<tr>
<td>Coss-Output capacitance</td>
<td>Lower</td>
<td>Higher</td>
<td>GaN with lower switching loss to achieve higher frequency &amp; efficiency</td>
</tr>
<tr>
<td>Qrr-Reverse recovery charge</td>
<td>Lower</td>
<td>Higher</td>
<td>GaN suitable for higher frequency &amp; efficiency</td>
</tr>
<tr>
<td>Vgs- gate voltage</td>
<td>Difficult</td>
<td>Easy</td>
<td>GaN need better gate drive circuit and PCB layout</td>
</tr>
<tr>
<td>Vsd-body diode conduction</td>
<td>Higher</td>
<td>Lower</td>
<td>GaN need better control of deadtime</td>
</tr>
</tbody>
</table>
High power density half-bridge 650V GaN with embedded driver

**Features**

- Power system-in-package integrating half-bridge gate driver and high-voltage GaN transistors:
  - BVDSS = 650 V
  - RDS(ON) = 150 mΩ
  - IDS(MAX) = 10 A
- Reverse current capability
- Zero reverse recovery loss
- UVLO protection on low-side and high-side
- Internal bootstrap diode
- Interlocking function
- Dedicated pin for shutdown functionality
- Accurate internal timing match
- 3.3 V to 15 V compatible inputs with hysteresis and pull-down
- Overtemperature protection
- Bill of material reduction
- Very compact and simplified layout
- Flexible, easy and fast design
## MasterGaN1 pinout

### Pin Number | Pin Name | Type | Function
--- | --- | --- | ---
15, 16, 17, 18, 19 | VS | Power Supply | High voltage supply (high-side GaN Drain)
12, 13, 14, EP3 | OUT | Power Output | Half-bridge output
4, 5, 6, 7, 8, 9, 10, 11, EP2 | SENSE | Power Supply | Half-bridge sense (low-side GaN Source)
22 | BOOT | Power Supply | Gate driver high-side supply voltage
21 | OUTb | Power Supply | Gate driver high-side reference voltage, used only for Bootstrap capacitor connection. Internally connected to OUT.
27 | VCC | Power Supply | Logic supply voltage
1 | PVCC | Power Supply | Gate driver low-side supply voltage
28, EP1 | GND | Power Supply | Logic ground
3 | PGND | Power Supply | Gate driver low-side driver reference. Internally connected to SENSE.
26 | HIN | Logic Input | High-Side driver logic input
24 | LIN | Logic Input | Low-Side driver logic input
25 | SD/OD | Logic Input-Output | Driver Shutdown input and Over-Temperature
2 | GL | Output | Low-Side GaN gate.
20 | GH | Output | High-Side GaN gate.
23, 29, 30, 31 | N.C. | Not Connected | Leave floating
MasterGaN1 applications and benefits

### Key benefits

- Compact system solution and simplified layout
- BOM reduction: SiP with offline driver optimized for GaN
- Robust solution: driver and GaN power transistors integration
- Package GQFN 9x9
- Flexible, easy and fast design
- Scalable p2p solution for power range 30-500 W

### Applications

- Telecom/Server Power
- Power Supply for 5G Communication Infrastructure
- EV/HEV Charging Stations
- Energy Storage Systems (UPS)
- Solar DC-AC Converters
- PC Power, OLED TV
- High-Density AC-DC Adapters, Fast Charging, USB-PD
MasterGaN family roadmap
QFN 9x9 mm² pin-to-pin scalable

One driver, many standard transistors for HB configuration

From 45 up to 400 W

MasterGaN1
Symmetrical
150 + 150 mΩ
Mass production
MP Dec 2020

MasterGaN2
Asymmetrical
150 + 225 mΩ

MasterGaN3
Asymmetrical
225 + 500 mΩ
Development

MasterGaN4
Symmetrical
225 + 225 mΩ
Development

MasterGaN5
Symmetrical
500 + 500 mΩ
Development

Whole product family to be released by H1 2021
65W ACF Application example - MasterGaN
Suggested 6V typ

Suggested 10ohm

Hi performance Ceramic Cap to be as close as possible between HV and Sense and between HV and VS

RC network for OTP extended time constant

Shunt is very common: LS driving is guaranteed until the voltage difference between PGND and GND is within +/-2V ☺

(*) External 6.2V Zener is suggested to protect the GaNs from transient high voltage stresses

(**) In case of very small Duty cycles, external, Low RD, high speed Bootstrap Diode is recommended. In case of intense negative voltage on OUT, even Linear regulator is possible
65W ACF application example efficiency

Efficiency performance at low Line and high Line
65W ACF application example typical waveform

230 Vacin 20V/3.25A
Gate drive logic inputs – truth table

<table>
<thead>
<tr>
<th>Input pins</th>
<th>GaN transistors status</th>
</tr>
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<tbody>
<tr>
<td>SD/OD</td>
<td>LIN</td>
</tr>
<tr>
<td>L</td>
<td>X</td>
</tr>
<tr>
<td>H</td>
<td>L</td>
</tr>
<tr>
<td>H</td>
<td>L</td>
</tr>
<tr>
<td>H</td>
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1. X: Don’t care
MASTERGAN has an interlocking feature to prevent contemporary activation of high side and low side.

HIN and LIN high never occurs, normal condition

HIN and LIN high in black square → Interlock
GL and GH are both low
- When Interlock condition is applied to the input, the active driver is shut down after T(OFF)
- When Interlock condition is removed from the input, the new input configuration is applied on the output after T(OFF)
• VCC Filter caps placed to close VCC-GND Pins
Noise prevention - PCB layout

- Keep signals traces away from OUT trace
- Keep bulk voltage—transformer-OUT-SENSE-GND loop as small as possible
During the design of power converters, the adjustment of dV/dt of middle point of OUT pin is important to:

- Reduce EMI
- To avoid undesired oscillations when parasitic elements cannot be further minimised
- Reduce secondary side stress
dv/dt adjustment

OUT pin dv/dt at turn on: GaN turn-on when resonance has sufficient amplitude to obtain ZVS
OUT pin dv/dt at turn off: Turn off dV/dt can be reduced using proper selection of MASTERGAN biasing components
dv/dt adjustment
adding cap on GaN’s gate

- Adding a capacitor between GL (GH) and PGND (OUTb), is equivalent to increase GaN’s Gate Charge
- Maximum value must be found to avoid driver’s dynamical overstress and considering the operating frequency $F_{sw}$
  - $C_{Gx} < \frac{80\text{mW}}{(P_{vcc}^2 \cdot F_{sw})} - (330\text{pF})$

<table>
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<th>PROs</th>
<th>CONs</th>
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<tr>
<td>Fine tuning of the obtained effect</td>
<td>Additional operating consumption to PVCC and Vbo, especially at high frequency</td>
</tr>
<tr>
<td>High repeatability of the effect thanks to the accuracy of the available discrete components</td>
<td>Not suitable for very high frequency solutions</td>
</tr>
<tr>
<td>Effect is also on EMI associated with normal operation</td>
<td></td>
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</tbody>
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Adding a resistor on PVCC

- A resistor in series with PVCC or VBO decreases the driving current.
- A very short drop is evident on PVCC / VBO at driver turn on.

### PROs
- Fine tuning of the obtained effect
- High repeatability of the effect thanks to the accuracy of the available discrete components
- Effect is also on EMI associated with normal operation

### CONs
- PVCC / VBO drop can increase the propagation delay
- Short-on time can result into worse Rdson because of the reduced Gan’s gate overdrive voltage (i.e. PVCC-Vgsth)
- Duration of VBO drop must be shorter than 2 µs to prevent UVLO activation
An RC network feedback can be added between OUT node and GL in order to reduce the GL voltage in case of intense negative dV/dt.

Consider to use PCB, especially for thin PCBs, instead of the added Ck

Example

0.8mm 4 layer PCB, 0.1mm inner core thickness, \( \varepsilon_r=4.4 \)

10pF -> 30mm2: can fit below MasterGaN

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<td>Acts on high dV/dt only: the dV/dt value is then balanced over entire operating conditions</td>
<td>High voltage component needed</td>
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</table>
Adding dV/dt limiter – design tips

- The value of the Capacitor \( (Ck) \) limits the dV/dt during hard switching thanks to Miller effect

- During turn on the rate is limited to \( \sim \frac{V_{PVCC}-V_{TH}}{R_{ONG}Ck} = \frac{V_{PVCC}-1.7}{50 \cdot Ck} \)

- During turn off, it is limited to \( \sim \frac{V_{TH}}{R_{OFFG}Ck} = \frac{0.85}{Ck} \)

- A resistor in series is required to avoid oscillations due to stray inductance

- \( R_{DAMP} \gg \sqrt{\frac{L_{stray}}{Ck}} \)

- Capacitor required is typically 5pF to 10pF (600V rated)

- E.g.: Using PVCC = 6V and max dV/dt = 10V/ns \( \rightarrow Ck = 8.6pF \)
dv/dt adjustment - adding dv/dt killer

- Startup waveforms at 230VAC compared
  - dv/dt changed from original 37V/ns to 6V/ns

Original
dV/dt equal to 37V/ns

With dV/dt limiter cap 10pF / 200Ω
dV/dt limited to 6V/ns
dv/dt adjustment - adding dv/dt killer

Example of the 65W board: $R_{pvcc}=15\Omega$  $C_g=470\text{pF}$  $R_{43}=200\Omega$  $C_{57}=10\text{pF}$

220V/50Hz input  20V/3.25A output

Turn on: 1.85V/nS  Turn off: 6.6V/nS
Thank you