Robust Design With Major Power Discrete Technologies

Giovanni Tomasello – Applications Engineer

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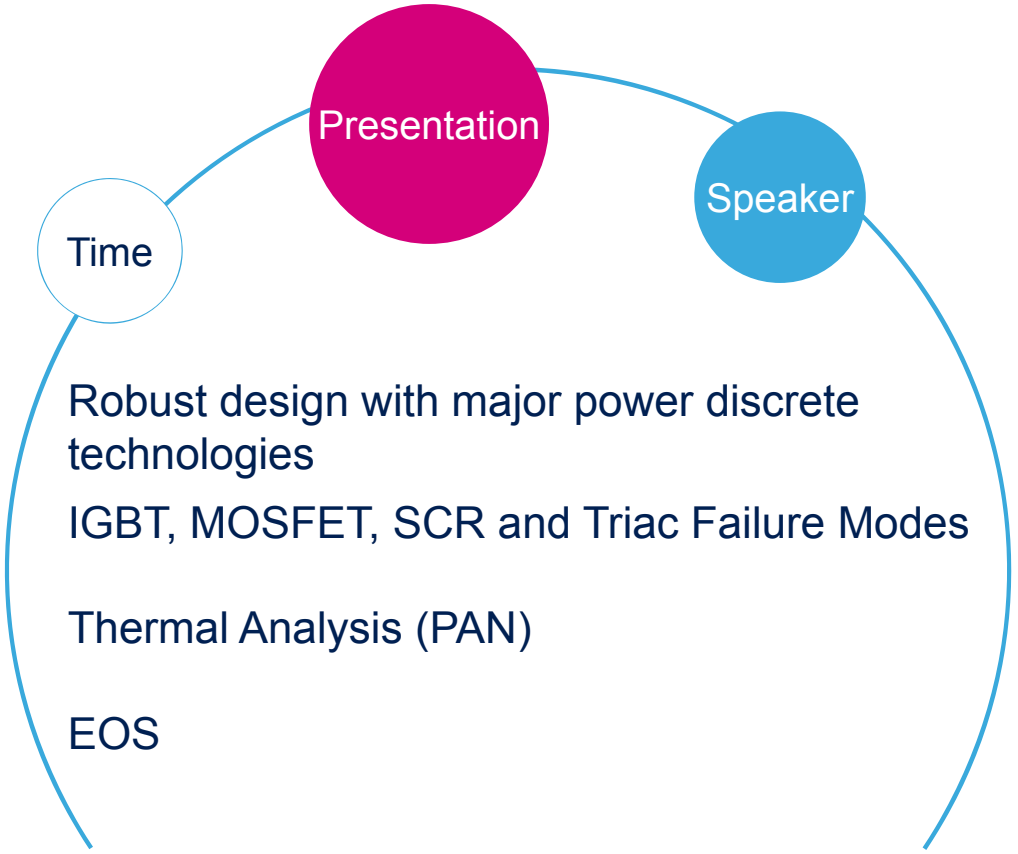
Technology Tour 2017

Agenda



Time	Presentation	Speaker
• 4:20PM	Robust design with major power discrete technologies IGBT, MOSFET, SCR and Triac Failure Modes Thermal Analysis (PAN) EOS	Giovanni Tomasello

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Common Failure Modes for IGBTs and MOSFETs

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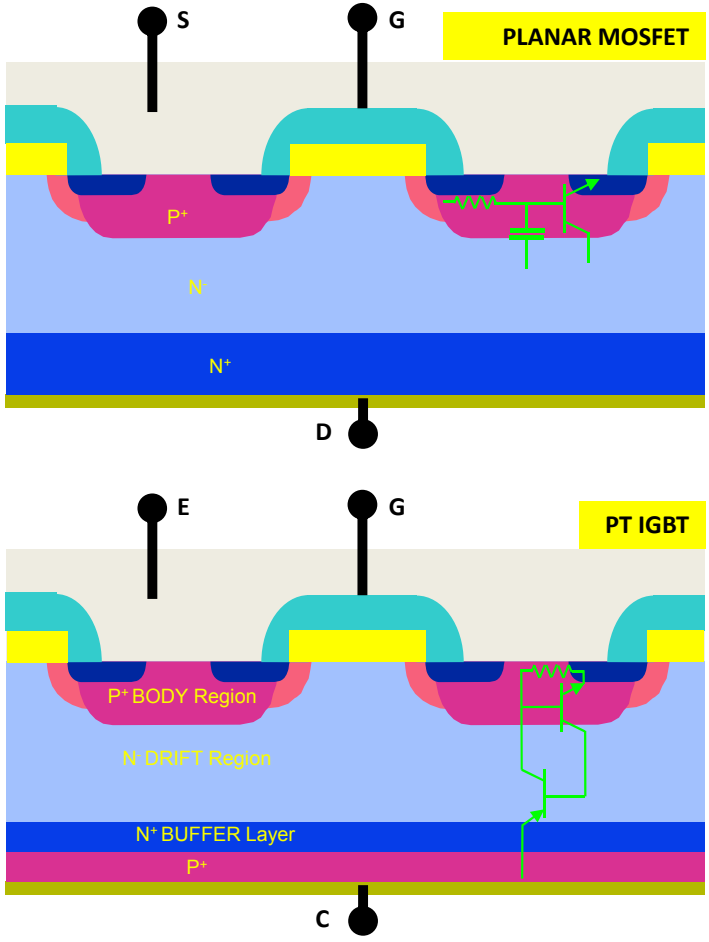
Basic Structure of a MOSFET and IGBT

Let's have a look at their internal structure….



Both IGBTs and MOSFETs have an unavoidable parasitic component inherent to their structure.

The parasitic NPN bipolar (MOSFET) and the parasitic PNPN thyristor (IGBT) are responsible for some of the most common failure modes

Please note the P+ layer of an IGBT's structures

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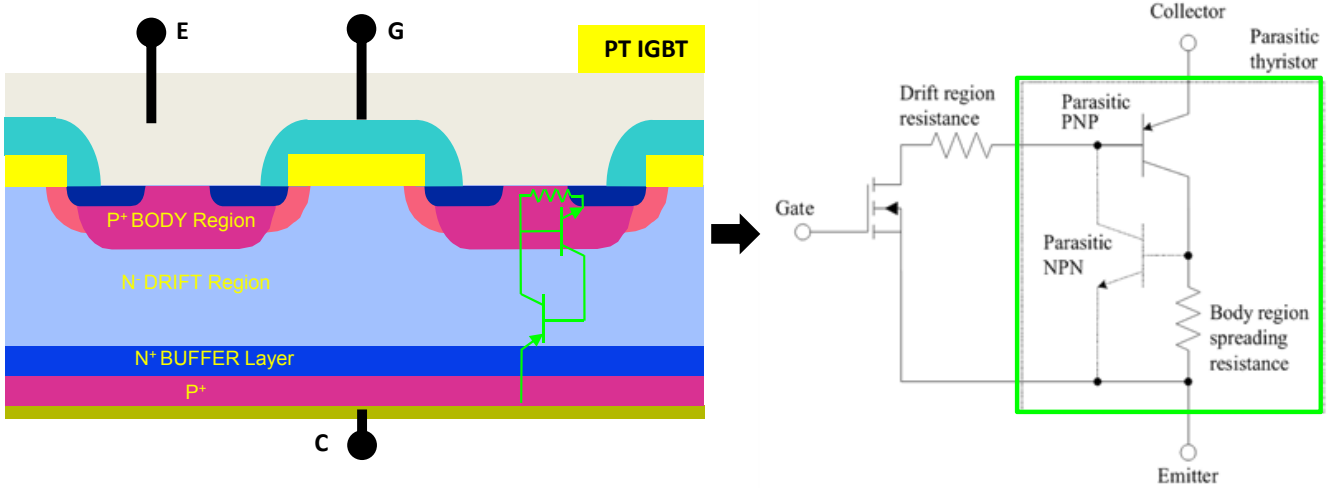
Equivalent IGBT Circuit

Let's briefly review the PT IGBT's structure.



Please note how the parasitic PNPN thyristor is hidden inside the power transistor's design

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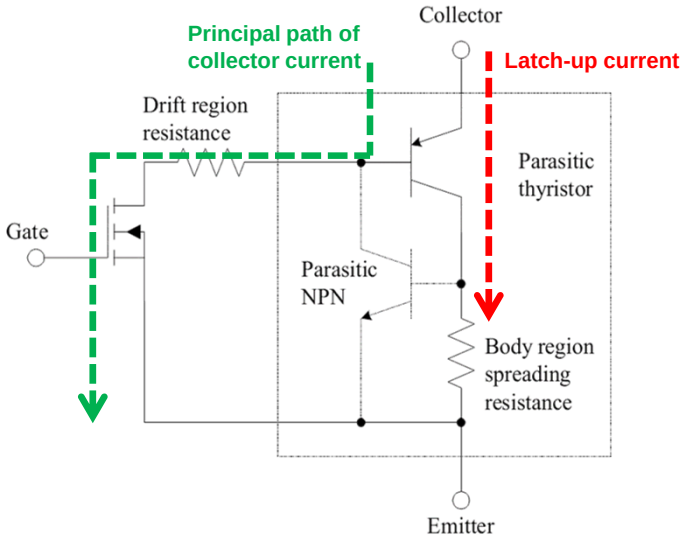
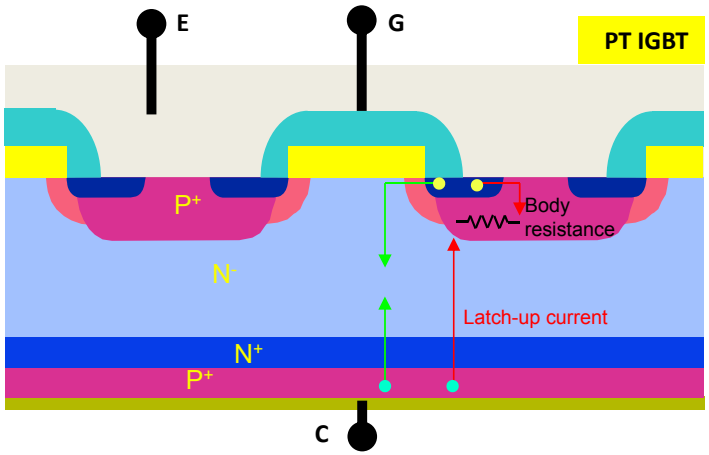
IGBT Failure Mode: Static Latch-up

Latch-up results from turning on of the parasitic PNPN thyristor. At that point, the IGBT current is no longer controlled by the MOS gate. The IGBT would be destroyed unless the current is externally forced OFF





Electron current
Hole current

During normal operations, a lateral current can flow into the body region resistance generating a voltage drop

If the voltage drop is high enough, the parasitic NPN could turn ON

If the sum of the two NPN, PNP parasitic transistors' current gain becomes $\alpha_{NPN} + \alpha_{PNP} \geq 1$, latch-up occurs

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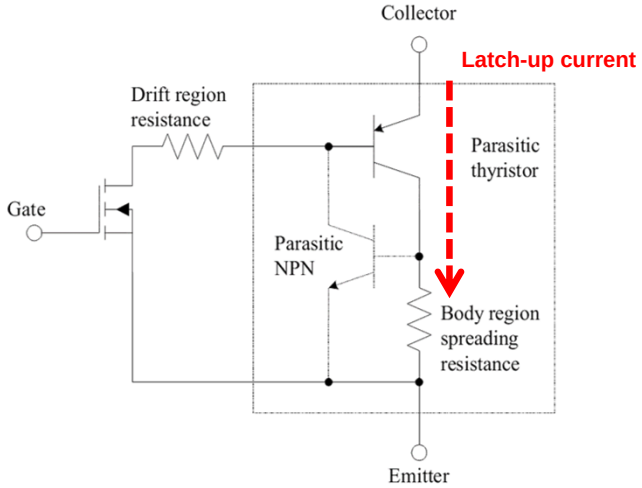
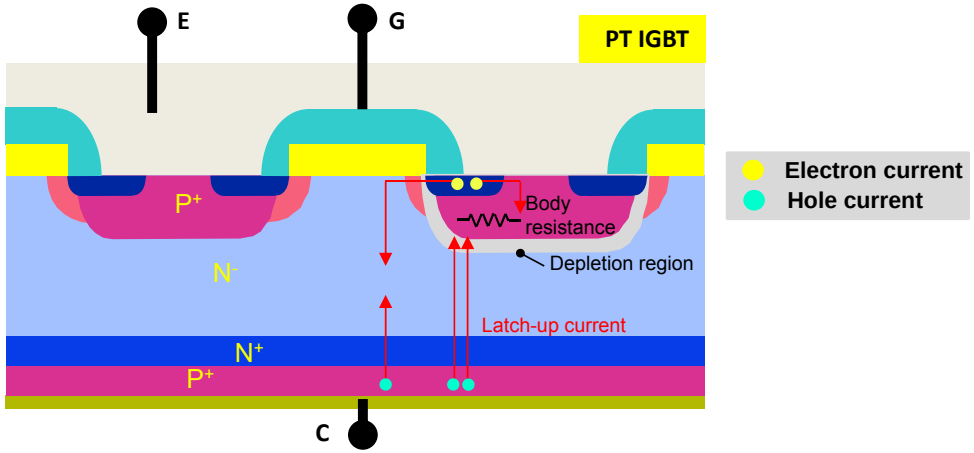
IGBT Failure Mode: Dynamic Latch-up

Dynamic latch-up is associated with a high dv/dt at turn-OFF. This is actually what limits the SOA of an IGBT since the dynamic latch-up current is lower than the static one





MOSFET section turns off and the depletion region of junction BODY-DRIFT expands into N- layer, the base region of the PNP BJT. The α_{PNP} increases because the base width decreases →More injected holes survive traversal of drift region and become "collected" at the BODY-DRIFT junction

Increased PNP BJT collector current increases lateral voltage drop in p-base of NPN BJT. High dv/dt during turn-off combined with excessive collector current can effectively increase gains and turn on the parasitic NPN transistor

Dynamic latch-up can happen with a load current lower than the static one (key factors are dv/dt and temperature)

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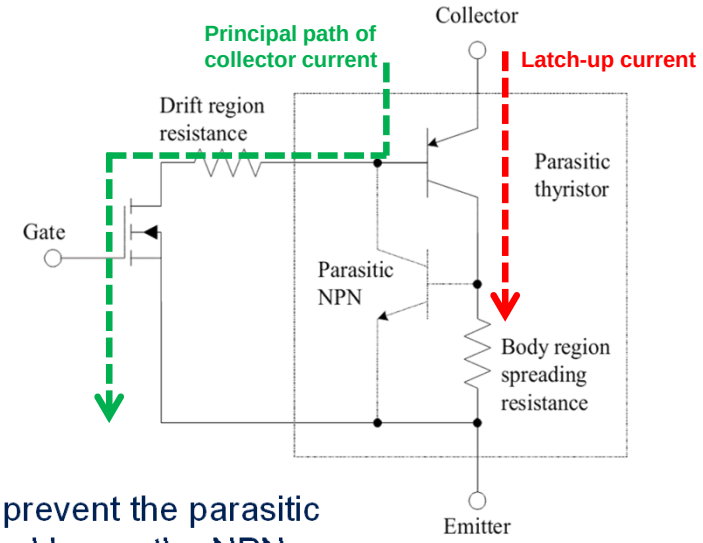
How to Avoid IGBT Latch-up

Today's IGBTs are considered (static) LATCH-UP free since the limit current is usually higher than 5 times the nominal current. On the other hand, with the increasing cells density and speed of newer technology, dynamic latch-up might affect high current applications.



- Technology helps us to prevent the parasitic NPN from turning ON and keeps the NPN and PNP gains <1:
  - Application of P+ body
  - P+ double implantation
  - Short N+ emitter
  - Specific doping profiles
  - Layout

KEEP IN MIND:

- **Temperature will affect the body region resistance value as well as the parasitic BJT gains.**
- **Carefully control the switching speed of the IGBT and choose the right IGBT family for your application**

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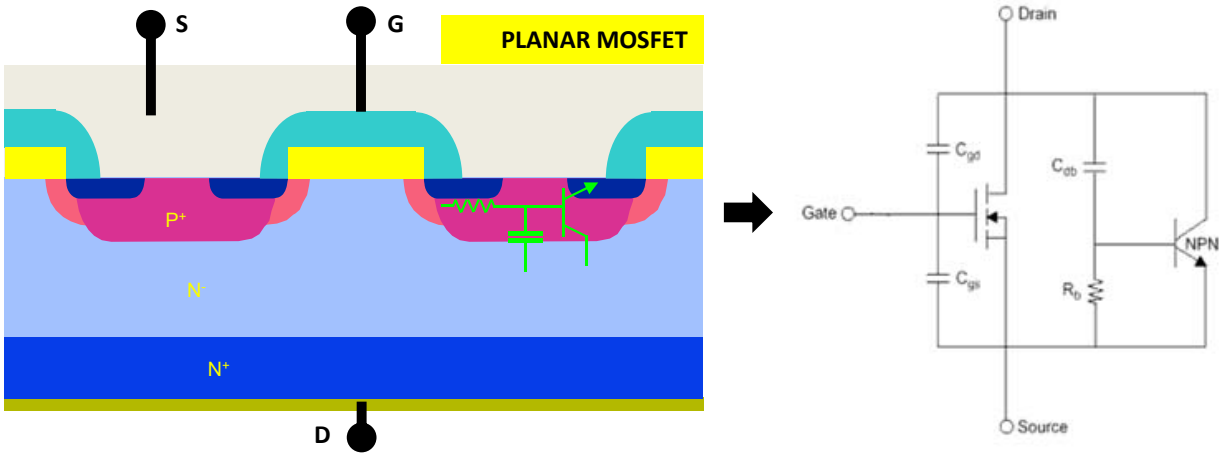
Equivalent MOSFET Circuit

Let's briefly review the planar MOSFET's structure.



Please note how the parasitic NPN is hidden inside the power transistor's design

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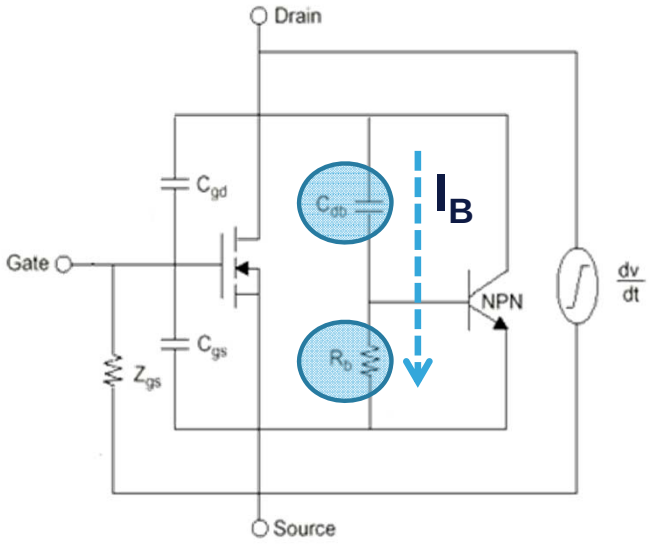
MOSFET Failure Mode 1: dv/dt

Friendly called " Static dv/dt " issue: there are **two possible mechanisms** by which a dv/dt induced failure may take place. The first mechanism is associated to the **parasitic BJT**



The MOSFET is in OFF state

A sudden increase in V_{DS} will generate a displacement current (I_B) due to the C_{bd} capacitance

Flowing into R_B, the I_B current could generate enough voltage to **turn on** the NPN

$$\frac{V_{BE(th)}}{R_B * CDB} = \left[\frac{dV_{DS}}{dt}\right]$$

At that point, t**he breakdown voltage will be reduced** to that of the **open base** breakdown voltage of the NPN

If the applied voltage is greater than the BV_{CEO}, the MOSFET will enter in AVALANCHE a, potentially, destructive condition.

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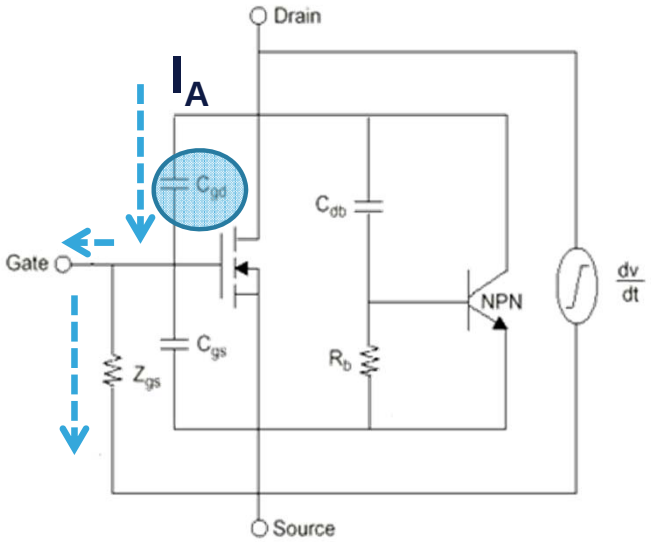
MOSFET Failure Mode 2: dv/dt

The second mechanism becomes active through the feedback action of the gate-drain capacitance C_{GD}



The MOSFET is in OFF state

A sudden increase in V_{DS} will generate a displacement current (I_A) due to the C_{GD} capacitance

Flowing into $Z_{GS,}$ the I_A current could generate enough voltage to **turn on** the MOSFET

$$\frac{V_{GS(th)}}{Z_{GS} * CGD} = [\frac{dV_{DS}}{dt}]$$

This condition is not intrinsically destructive. Its effects are related to the specific working conditions. Of course, the unwanted TURN-ON of the MOSFET could trigger a chain reaction leading to the failure of the application itself

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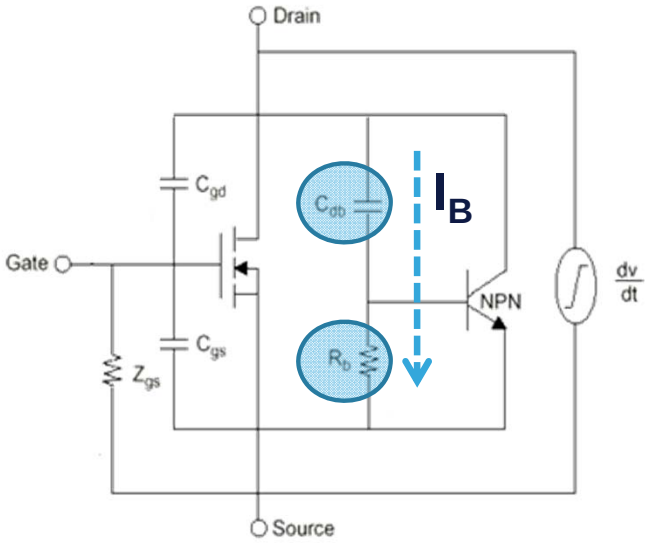
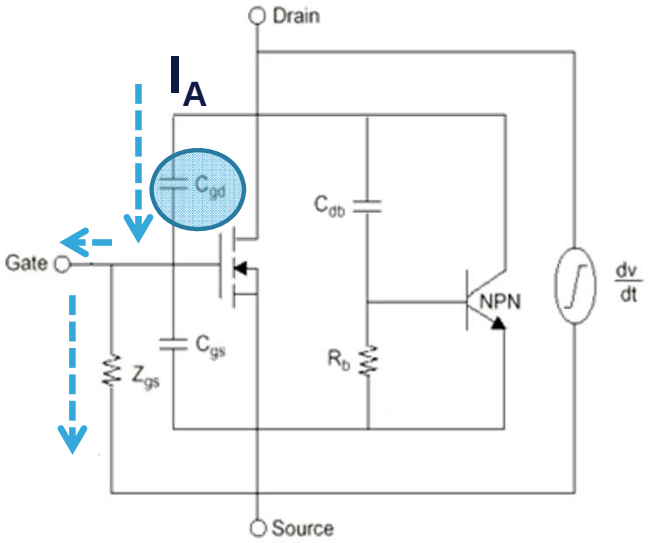
How to Avoid dv/dt Issue

Dv/dt issue is common for half-bridge topologies



- Minimize R_B (technology characteristic)
- Temperature will affect V_{BE} , R_B
- Carefully control the switching speed of the MOSFET (in a HB, the switching MOSFET will generate the V_{DS} variation across the OFF device)



- Low V_{TH} devices are more sensitive
- Temperature will affect V_{TH}
- Gate circuit impedance is extremely important
- Carefully control the switching speed of the MOSFET (in a HB, the switching MOSFET will generate the V_{DS} variation across the OFF device)

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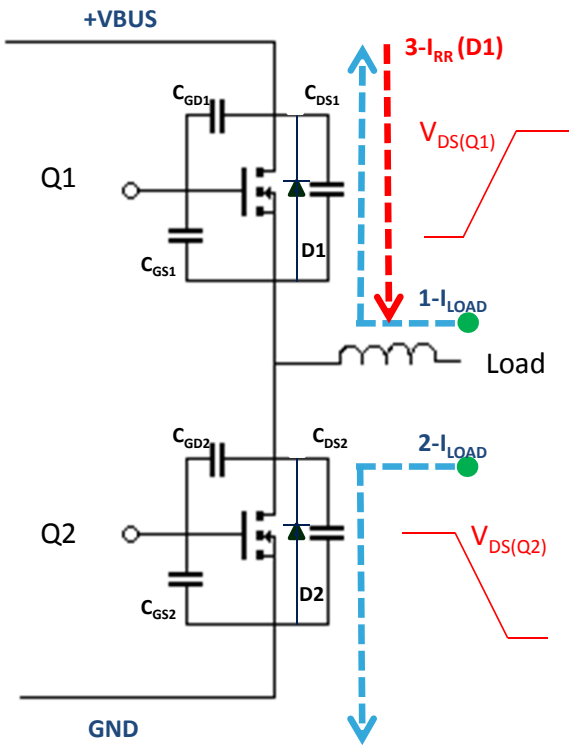
MOSFET Failure Mode 3:Reverse Recovery dv/dt

Let's consider an half-bridge configuration. We all know that this topology is common to a huge variety of power electronic circuits (electric motors, converters, inverters…)



1. Imagine that the load current is flowing through the body diode of Q1, D1. The direction of the current is dictated by the load.
2. Q2 is turned ON and its drain voltage will decrease according to a specific |dV/dt| (the dV/dt is negative on Q2 and depends on RG-on(Q2)). The same |dV/dt| with positive value is applied to Q1.
3. Please consider that:
   - D1 reverse recovery effect will generate a high reverse recovery current (IRR)
   - At the same time, an high dV/dt is applied to Q1 because of Q2 transition.

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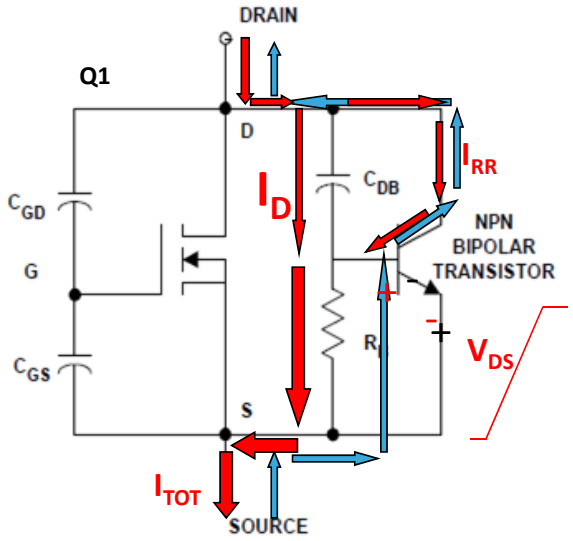
MOSFET Failure Mode 3:Reverse Recovery dv/dt

Let's see what's happening inside Q1…



- The load current is negative and so it flows through the base-drain (or source-drain) diode inherent in the **MOS** structure (D1)
- The base-emitter junction is reverse biased and the parasitic **BJT** is off.
- When Q2 is turned ON, Q1 V_{DS} will change (LOW to HIGH) with a certain dV/dt (dictated by Q2 turn-ON)
- The resulting displacement current (I_D) flows through the drain-base capacitance C_{DB} and the P-base finite resistance (R_B)
- At the same time the diode reverse recovery I_{RR} is flowing through R_B itself in order to remove the charges stored in the drain region
- **I_{RR} is not generated by dV/dt but accompanies it**

$$I_{TOT} = ID + IRR \qquad \text{where} \qquad I_D = C_{DB} * [\frac{dV_{DS}}{dt}] \qquad I_{RR} = Diode\ Characterisitc$$

Again, the parasitic bipolar could be turned ON. This will reduced the "real" clamping voltage leading, potentially, the device in AVALANCHE. Please consider that, compared to Failure mode 1, the triggering current is higher → I_D+I_{RR}

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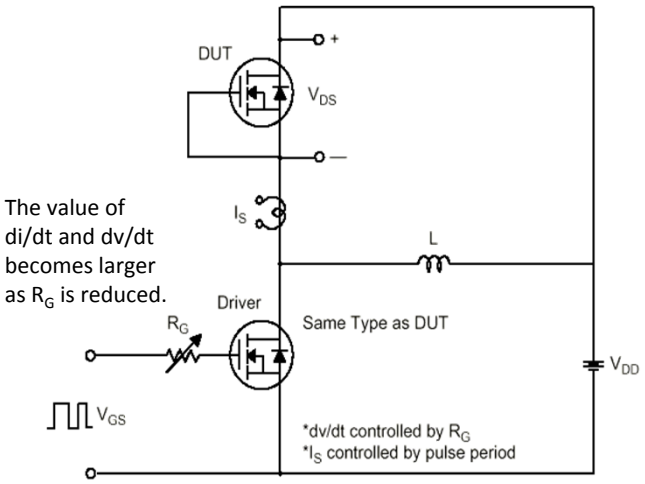
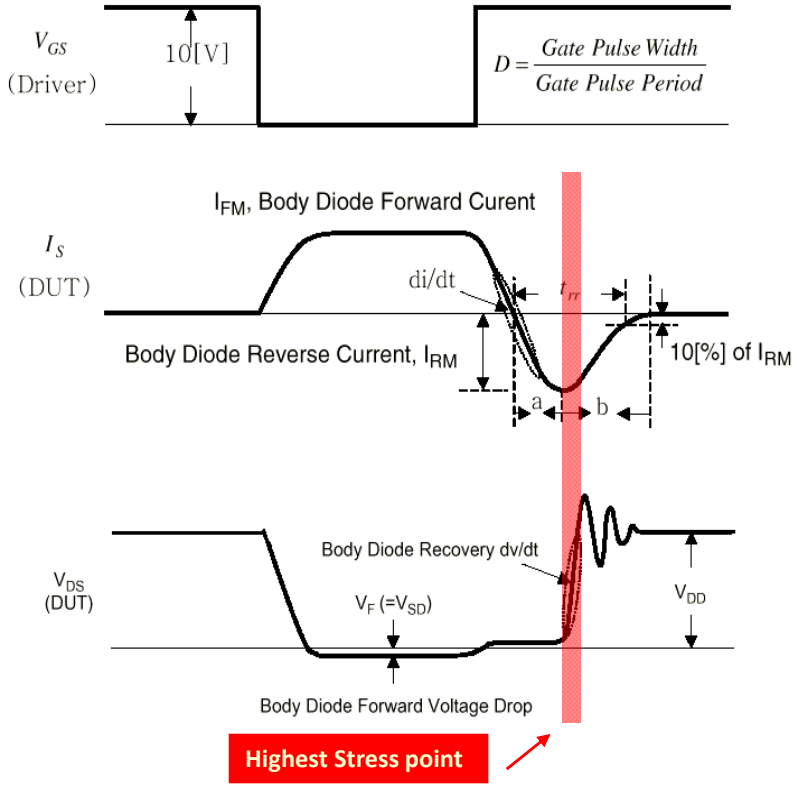
MOSFET Failure Mode 3:Reverse Recovery dv/dt

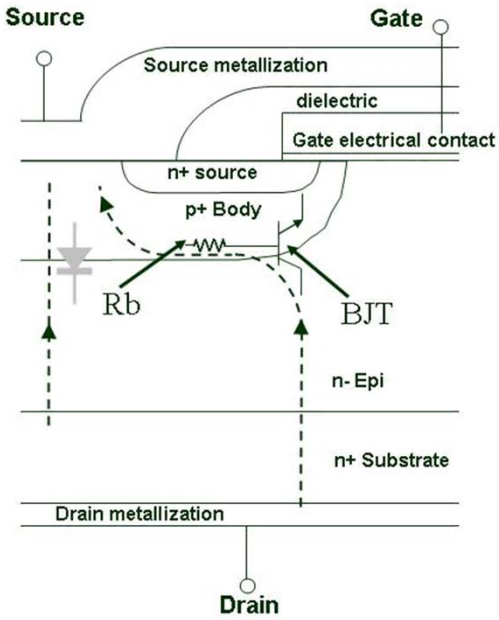


The value of di/dt and dv/dt becomes larger as R_G is reduced.



How to Avoid Reverse Recovery dV/dt

Minimizing RB is always a good idea plus:



- Use a MOSFET with a fast intrinsic diode will minimize Q_{RR} and so I_{RR} ▶ $Irr = f\left(\frac{di}{dt}, Q_{rr}\right)$
- The right MOSFET technology will show a proper dV/dt reducing the I_D current ▶ $\frac{dv}{dt} = f\left(\frac{dn}{dx}\right)$
- Carefully control the switching speed of the MOSFET. Choose the right technology and a proper gate driving network
- Always perform an accurate check of any “dangerous” conditions!

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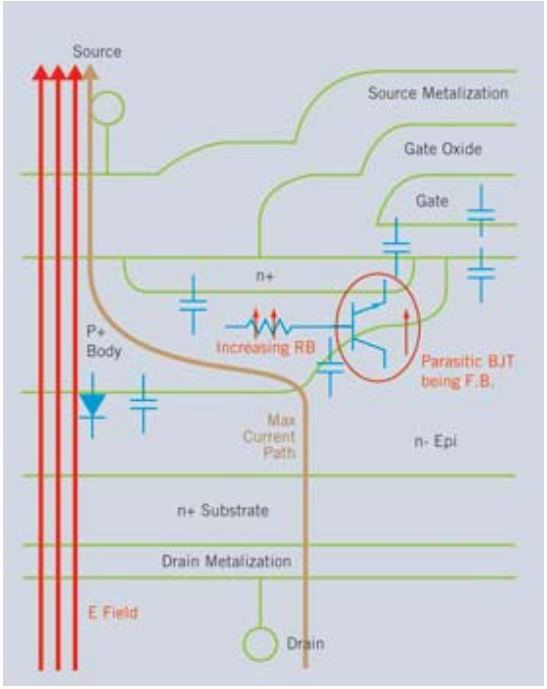
Failure Mode 4: AVALANCHE

The AVALANCHE event is not intrinsically destructive. MOSFETs are designed to survive it (under certain conditions).



If a voltage higher than BV_{DSS} is applied:

1. **A critical electric field** is reached (red lines) where **carrier concentration increases** due to avalanche multiplication
2. The electric field, inside the device, is most intense at the point where the junction bends (brown line) → **Current trough R_B**
3. **The power dissipation** increases the **temperature** thus **increasing the R_B value.** The parasitic NPN could TURN-ON.
4. **The power dissipation could lead to a failure even if the NPN does not latch!**

Failure Mode A: Parasitic Bipolar TURN-ON ▶ **CURRENT FAILURE**

Failure Mode B: Excessive power dissipation (energy is too high) will result in a junction temperature above T_{JMAX} ▶ **ENERGY FAILURE**

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AVALANCHE Rating

Ex: STY139N65M5

I_{AR}	Max current during repetitive or single pulse avalanche (pulse width limited by T_{JMAX})	17	A
E_{AS}	Single pulse avalanche energy (starting T_j = 25°C, $I_D = I_{AR}$, V_{DD} = 50V)	2400	mJ

I_{AR} = maximum current that can flow through the device during the avalanche event without triggering any bipolar latching phenomenon.

E_{AS} = (Energy during Avalanche for Single Pulse) is defined as the maximum energy that can be dissipated in the device, during a *single avalanche operation at the I_{AR} and at the starting junction temperature of 25°C*, to bring the junction temperature up to the maximum one stated in the absolute maximum ratings.

The activation of the bipolar transistor is not always the root cause of an avalanche failure. The temperature, during an avalanche event, could be so high to generate an hot-spot (creation of thermally generated carriers) and a consequently failure of a single cell (or a small group of cells)

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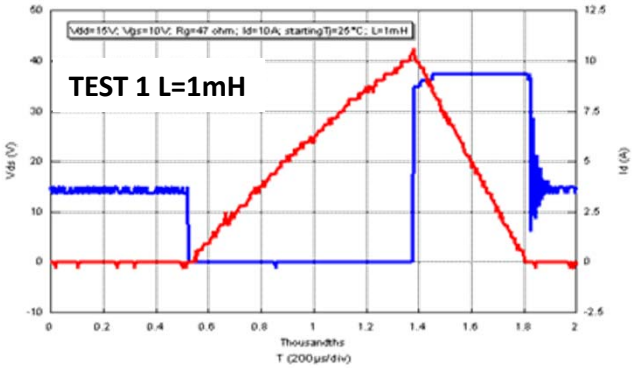
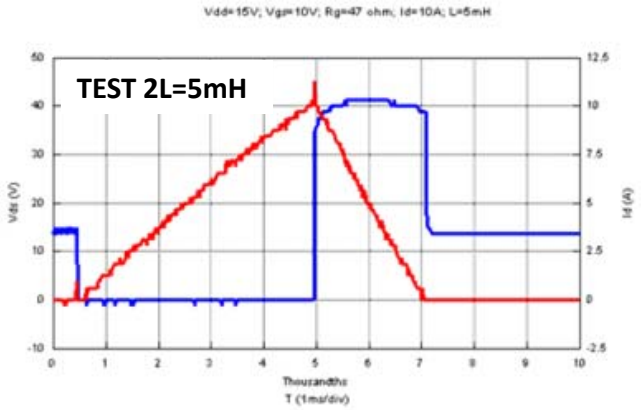
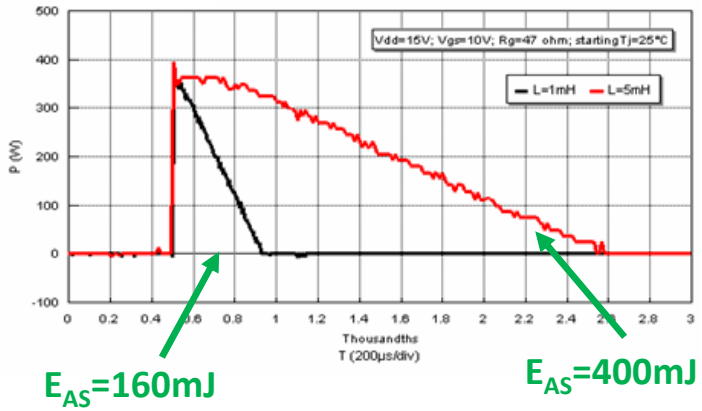
AVALANCHE Rating





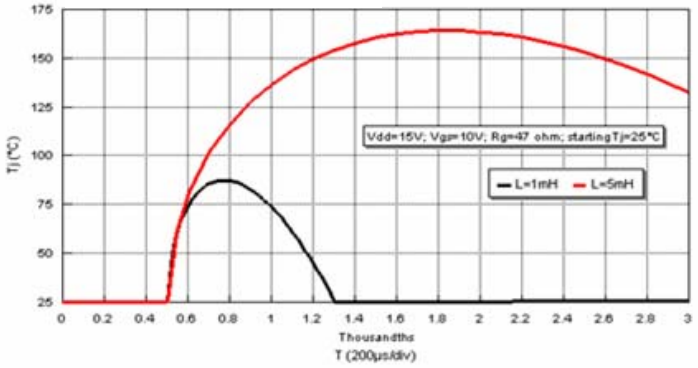
POWER



E_{AS}=160mJ

E_{AS}=400mJ

TEMPERATURE (est.)



IMPORTANT: Please note that starting T_J is 25ºC

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Improve AVALANCHE Robustness

- AVALANCHE can be improved by design (layout):
- Reducing the RB resistance with a proper doping profile\ layout design
- Reducing the “length” of RB with an optimized layout
- Improving the quality of the silicon production process (better uniformity of the wafer thickness, controlled variation…)
- Reducing the die defectiveness
- Performing a 100% test screening process

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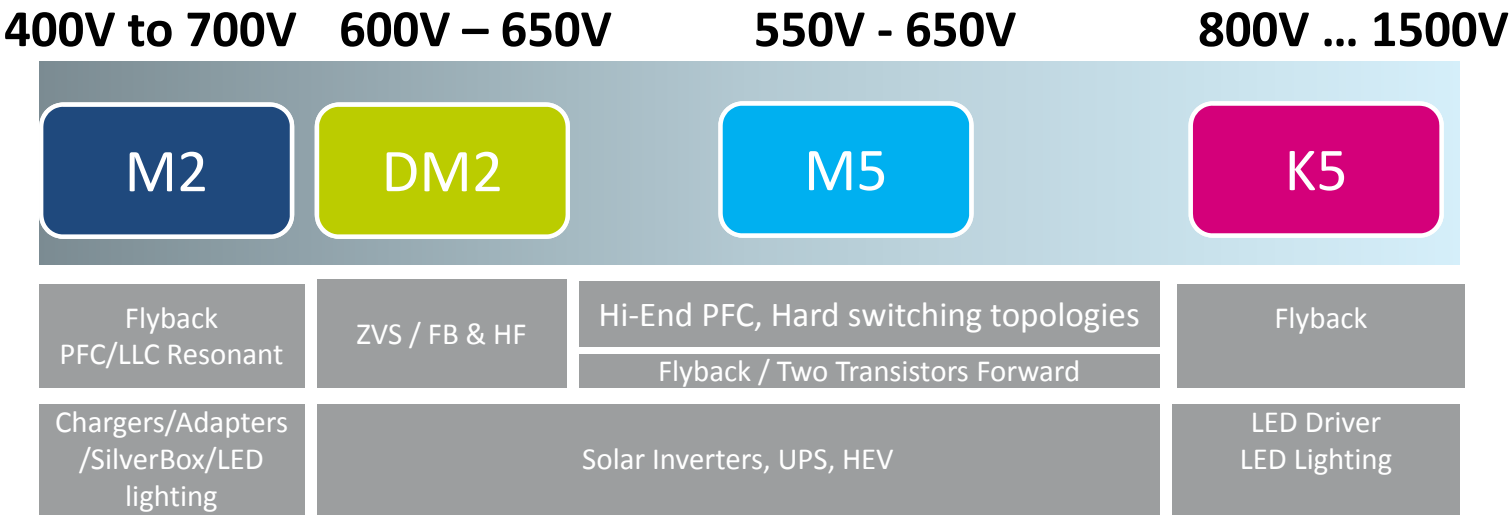
MOSFET Super Junction Technologies: Application / Topology Positioning



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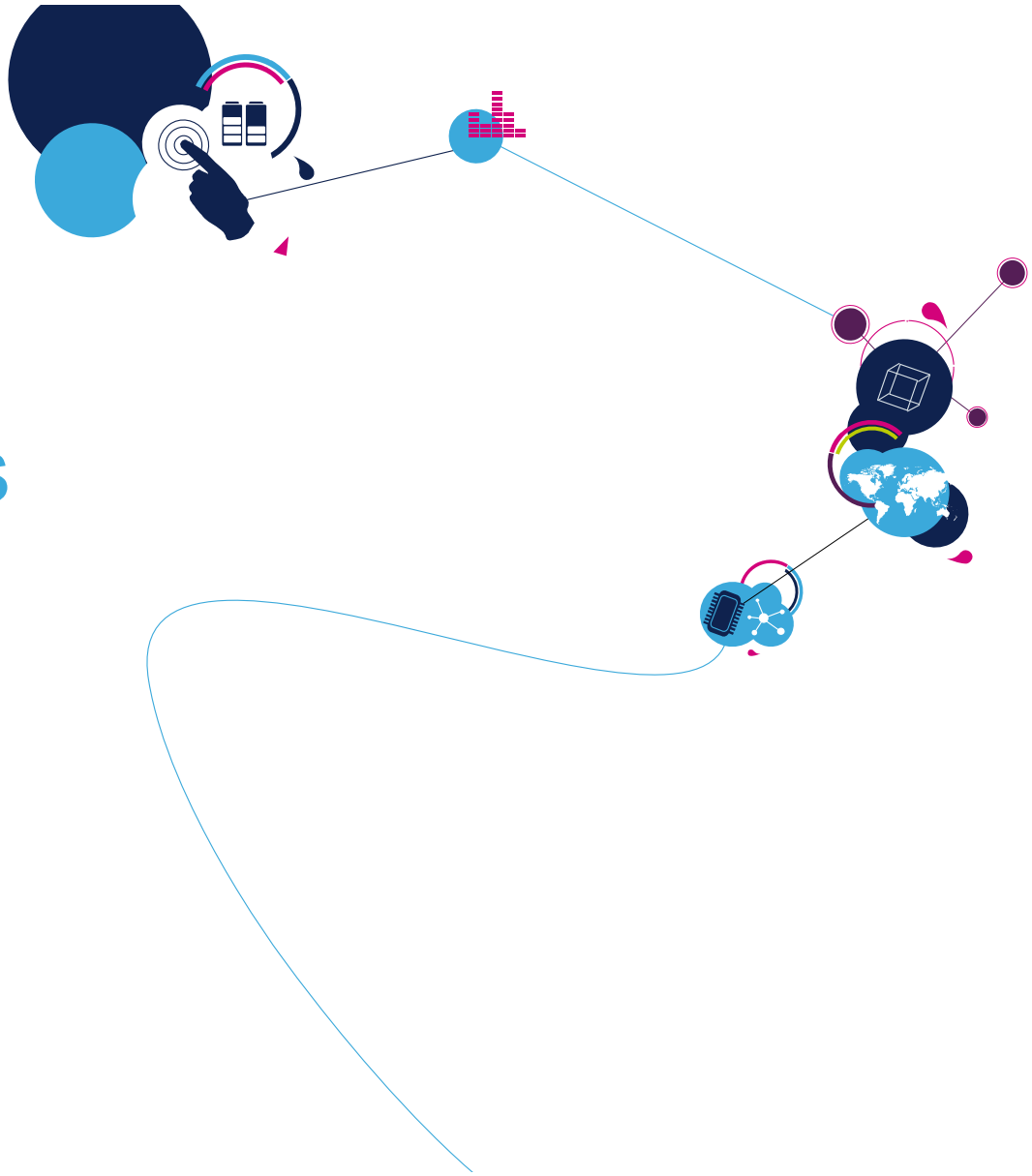
SCR Failure Modes



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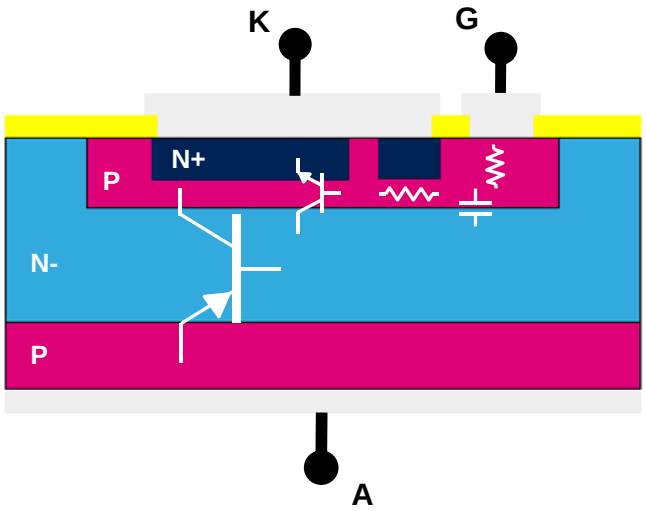
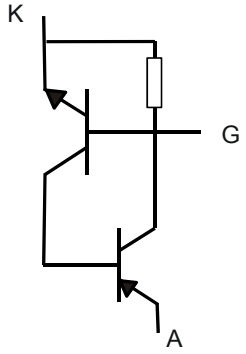
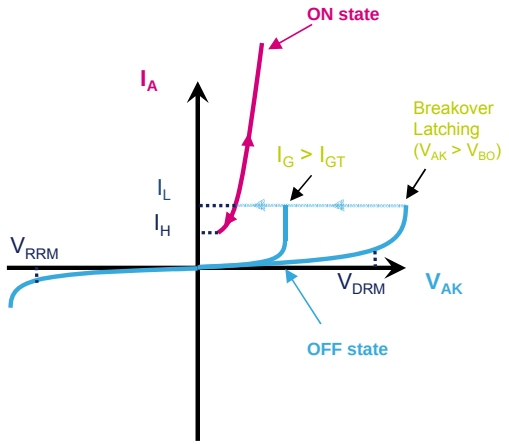
Basic Structure of an SCR







A SCR (Silicon Control Rectifier) is made of 4 PNPN diffusion layers.
The corresponding model is composed of 1 NPN and 1 PNP bipolar transistors.

This specific structure is latching from OFF to ON states when :

- **V_{AK} > 0 and a sufficient gate current is applied**
- **$V_{AK} > V_{BO}$: thyristor is in avalanche mode and triggers when avalanche current is high enough to saturate the both bipolar transistors**
- **High dV_{AK}/dt is applied: triggering occurs due to the displacement current generated by the internal junctions capacitances**

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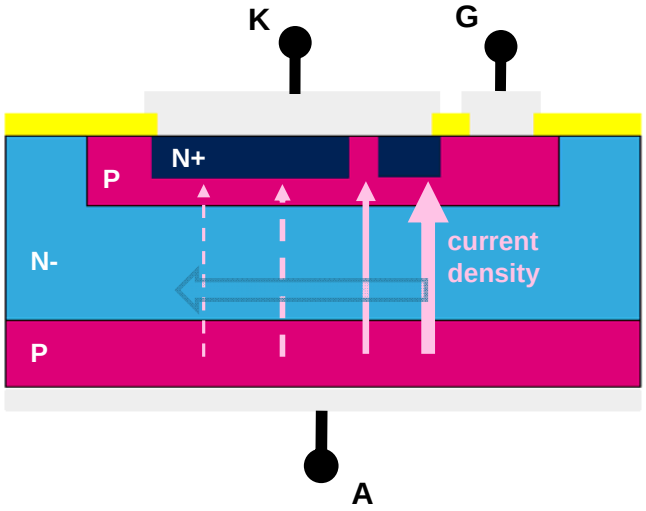
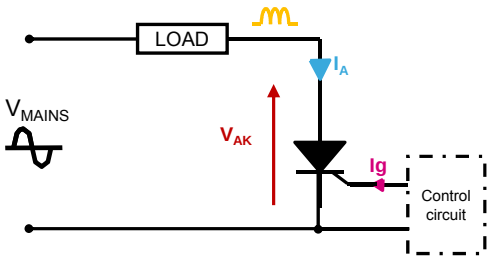
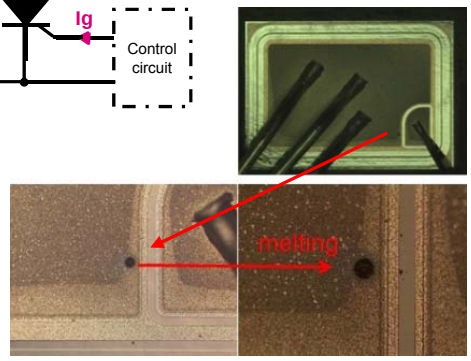
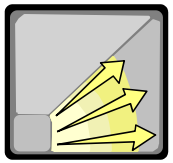
SCR Failure Mode 1: dI/dt at Turn-ON









Triggering first occurs in a single small silicon area.
Then, the conduction extends to the rest of the structure.
Waiting for conduction propagation, the initially conducting area needs to sustain a high current density.

The current focalization at triggering mainly depends on the LOAD and Voltage conditions.
As an example, triggering at peak mains voltage with a high power LOAD will lead to a high current slope at turn-ON (dI/dt) and then a high current density in the initially conducting area.

Although stress is mainly related to the LOAD and can not really be controlled through the gate signal, higher gate current and slope tends to limit the current focalization as it is accelerating the conduction extension.
Additional inductance in series with a LOAD is a common way to deal with very high stressing LOADs.

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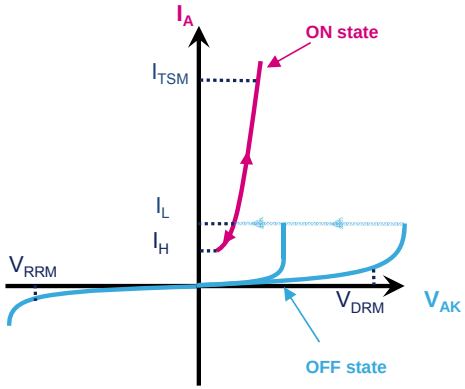
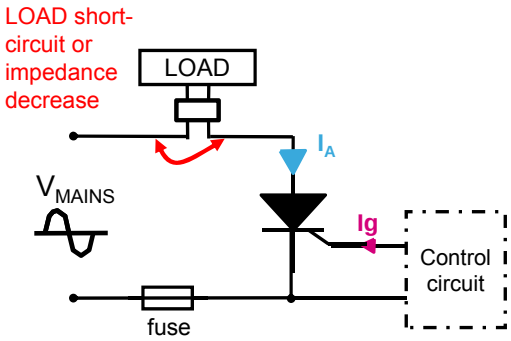
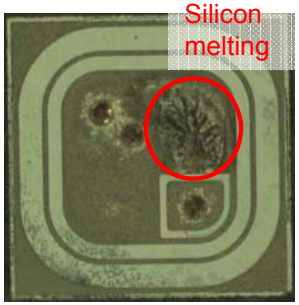
SCR Failure Mode 2: Overcurrent







In case the anode current at ON-state overpasses I_{TSM} parameter specified for the SCR, power dissipation inside the device makes the silicon temperature increase until melting.

This can occur when the LOAD is short-circuited or damaged or in case of very high-energy lightning surge.

Fuses are commonly used to protect the device.
I^2t parameters have to be well balanced between the fuse and the SCR.

Note: SCR is well adapted to high current stress as it remains saturated whatever the anode current level (no linear mode like for the transistors) in its ON-state mode.

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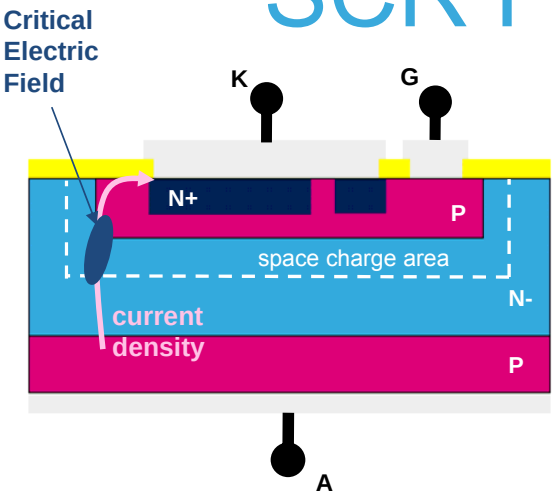
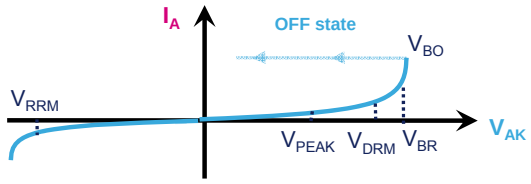
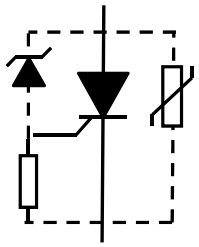
SCR Failure Mode 3: Avalanche







Breakdown voltage (V_{BR}) for an SCR is generally well above the application nominal peak mains voltage.
Therefore avalanche usually only occurs in case of lightning surge coming from the power network.
Inductive LOAD overvoltage at switch OFF is another case, nevertheless the current level in avalanche is lower.

Two possible cases:
- **Avalanche (V_{BR}) is reached but no latching: SCR periphery can be damaged due to current focalization. This case is possible in direct ($V_{AK} > 0$) or reverse ($V_{AK} < 0$) polarizations.**
- **Breakover (V_{BO}) is reached: SCR is triggering with periphery damage risk and possible dI/dt at turn-ON stress.**

Commonly used solutions for SCR protection against high voltage are varistance and transil™.

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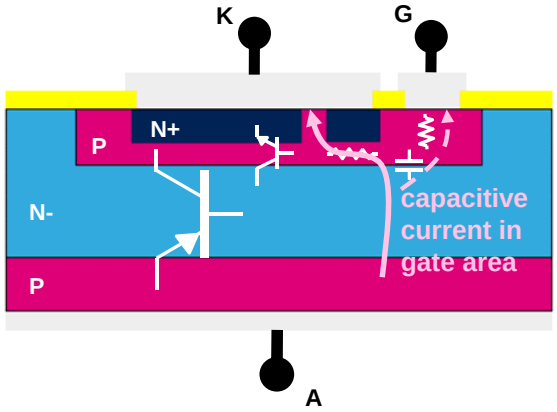
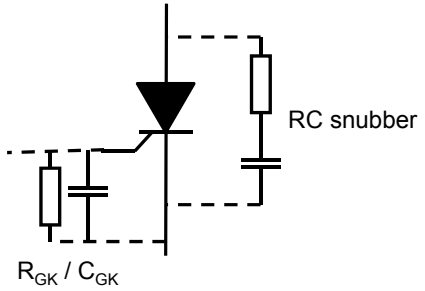
SCR Failure Mode 4: dV/dt





High dV/dt applied across an SCR anode-cathode is not intrinsically destructive.

Nevertheless, undesired SCR triggering can lead to high dI/dt at turn-ON stress (otherwise application malfunction at least).

When a high dV_{AK}/dt is applied to an SCR, an internal displacement current is generated by the junction capacitances. This current can create the conditions for triggering. Especially the current generated in the gate area acts internally as a gate current if gate pin is at high impedance.

Snubber and gate filter (R_{GK} / C_{GK}) are commonly used solutions for avoiding false triggering by dV/dt.

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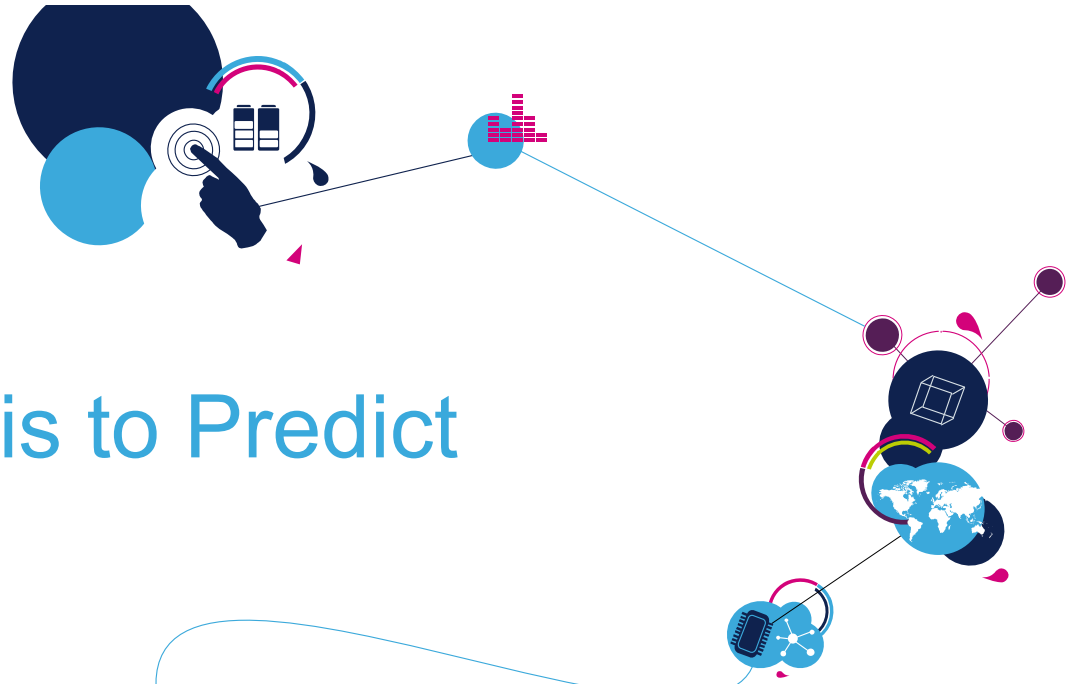
SCR Failure Mode: Other Cases

- Gate over-current
- Gate to cathode over reverse voltage (gate junction avalanche)
- All the described cases are applicable to TRIACs, too. Noticed that switch-OFF controll can be lost with a TRIAC when (didt)c / (dvdt)c commutation conditions are overpassed. This is not destructive but can lead, in some conditions, to LOAD damaging with overcurrent stress at the end.



Thermal Analysis to Predict Device Lifetime

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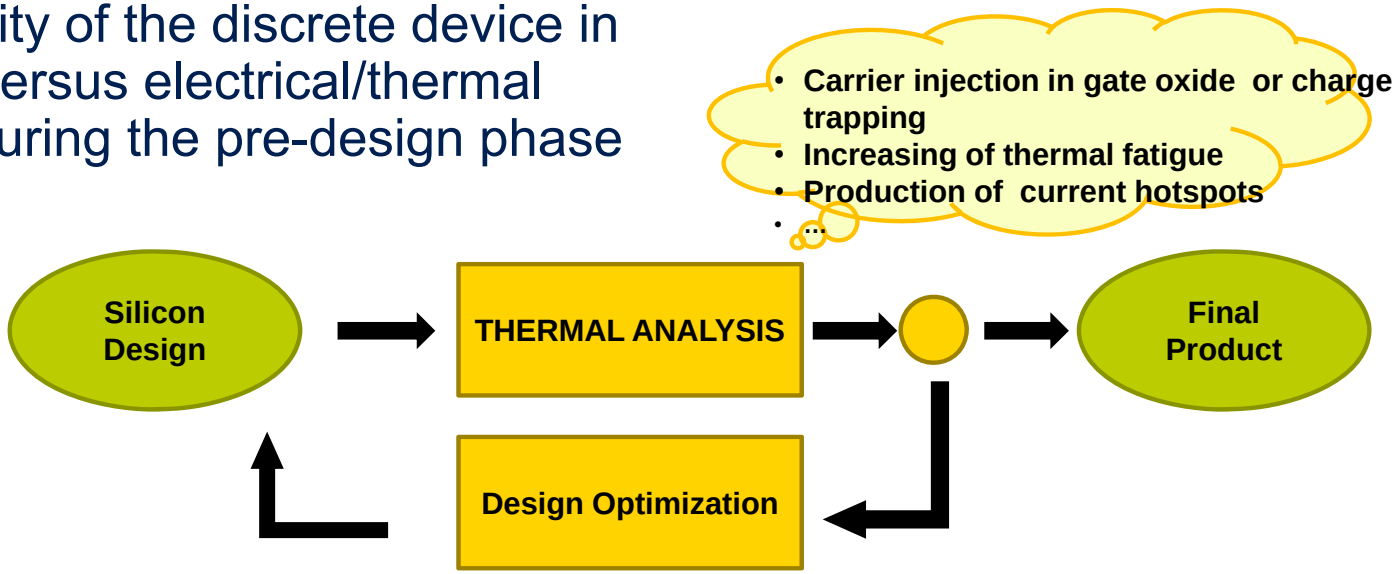
Why Thermal Analysis?

- There is an unbreakable connection between silicon temperature and its lifetime.
- Detailed thermal analysis is a **KEY** factor to design better semiconductors.
- This new approach helps silicon designers to analyze the quality of the discrete device in terms of layout versus electrical/thermal characteristics during the pre-design phase



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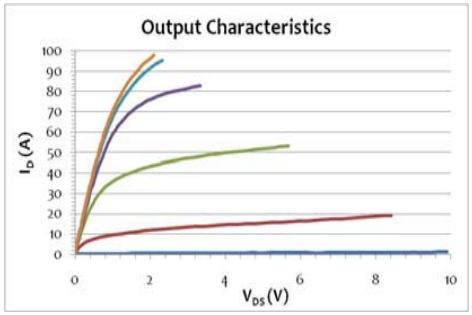
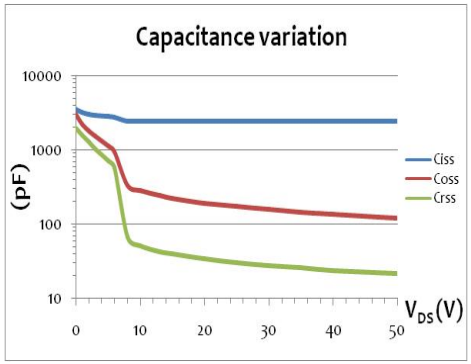
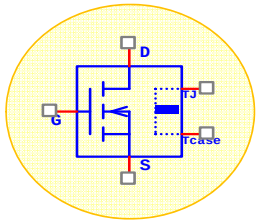
MOSFET Elementary Cell Model

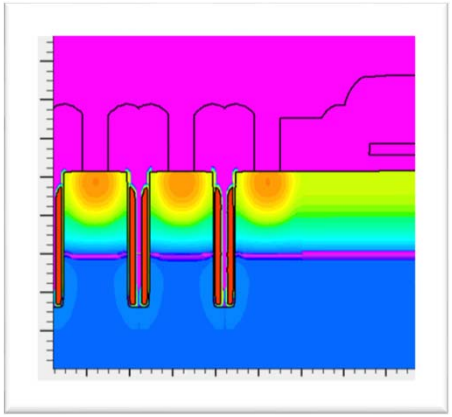
Real world data is the basic info needed to build the SPICE model but…we need more! We need to understand what is happening at every cell constituting the MOSFET itself.







Elementary cell model



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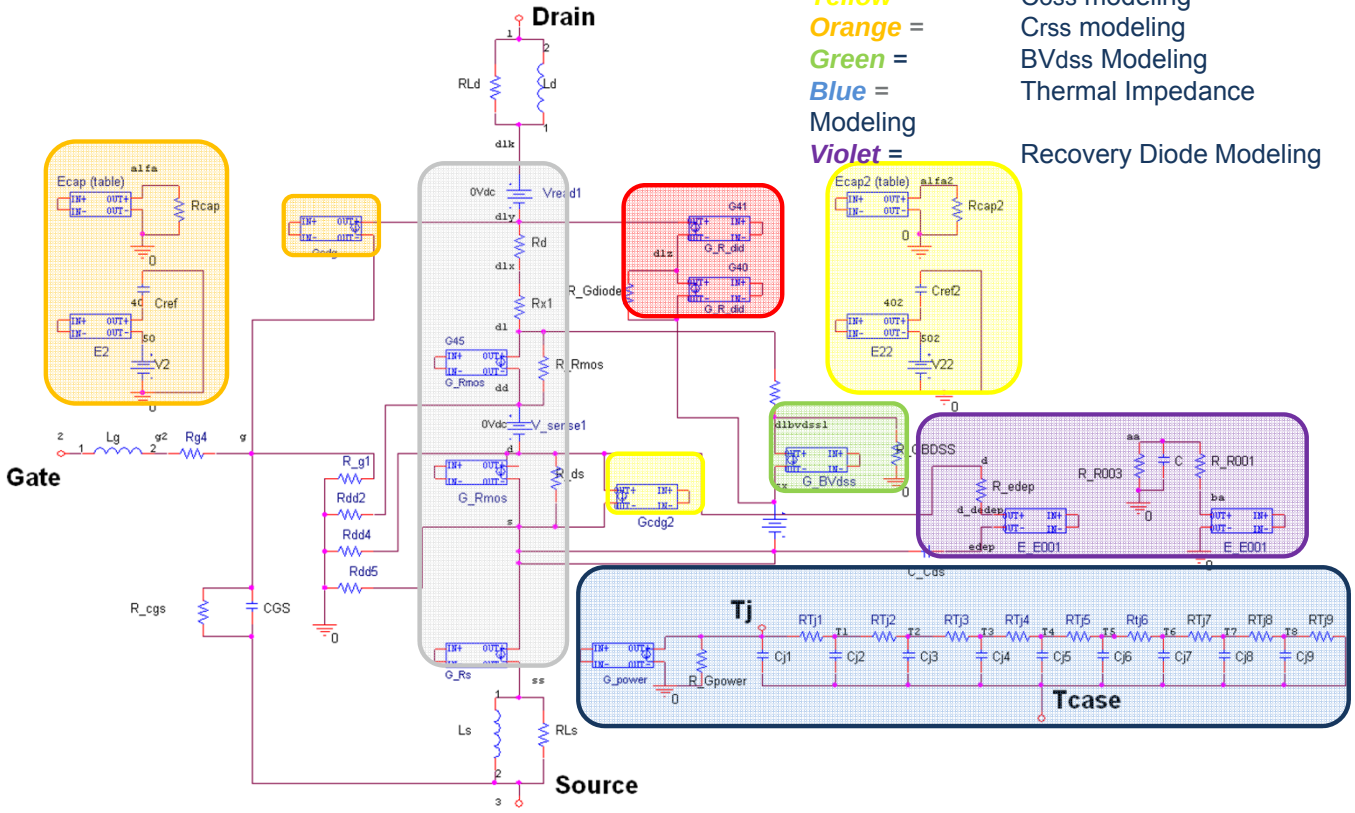
MOSFET Self-Heating SPICE Model Schematic

Grey =	DC modeling
Red =	DC Diode modeling
Yellow =	Coss modeling
Orange =	Crss modeling
Green =	BVdss Modeling
Blue =	Thermal Impedance Modeling
Violet =	Recovery Diode Modeling



SPICE Models are available at www.st.com!

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PAN: Power ANalyzer

- PAN is an internal tool, developed by ST Design Team, for advanced simulations.
- PAN looks at the MOSFET characteristics and allows us to go deep inside the power transistor's structure (down to the basic cell constituting the device).
- PAN can simulate:
  - fast thermal transient during fast switching;
  - current distribution along the device surface;
  - gate signal propagation in the layout.

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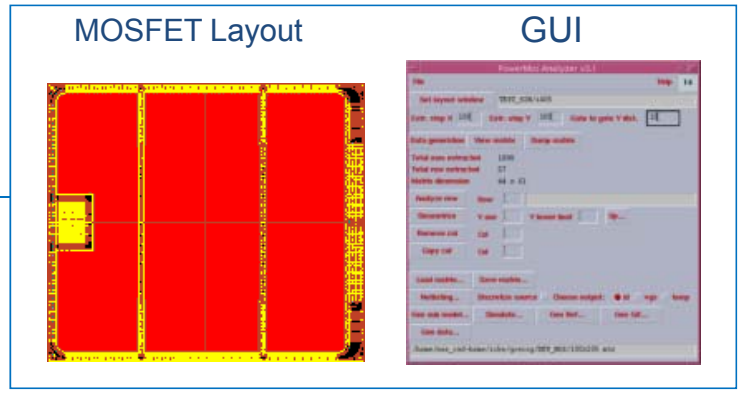
PAN: Electrical and Thermal Analysis



Matrix Extractor Module

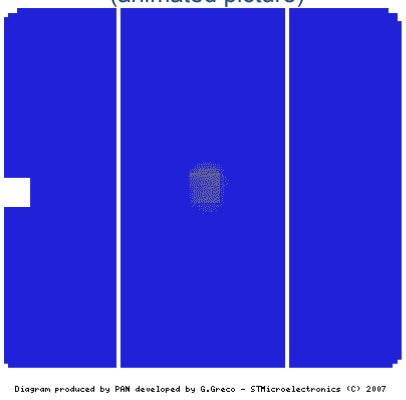
Netlister

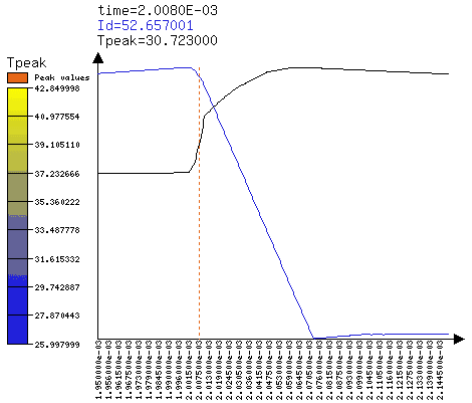
Simulation

Database creation

Graphic postprocessor

Temperature distribution during a switching OFF (animated picture)





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PAN: Electrical and Thermal analysis – UIS test

Temperature distribution during an UIS test
(animated picture)

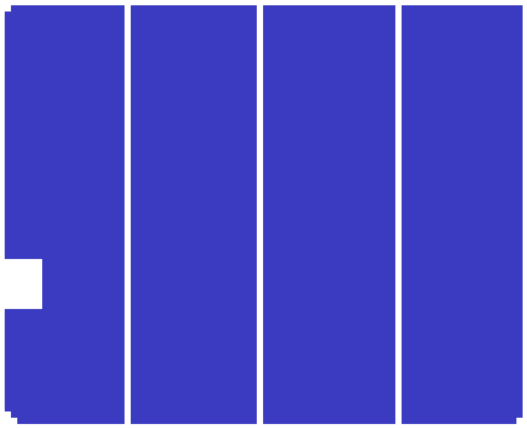
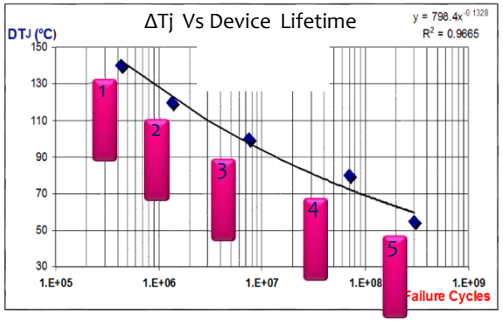
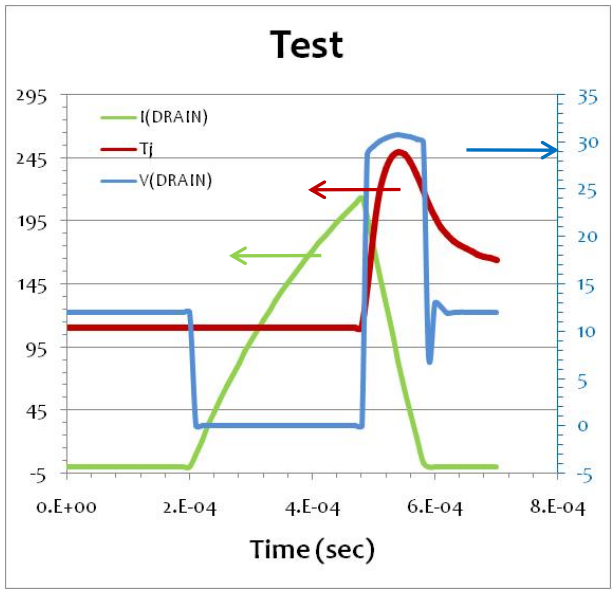


Diagram produced by PAN developed by G.Greco - STMicroelectronics (C) 2007





TEST	ID	ΔTj Self-Heating	ΔTj PAN	Life-time SPICE Self-Heating	Life-time PAN
1	83 A	83°C	84°C	70 Mcycles	70 Mcycles
2	203 A	133°C	140°C	700 Kcycles	450 Kcycles

Please note how the SPICE results differ from PAN results. PAN allows us to perform more accurate analysis and identify potential design issue at an earlier stage of the silicon design

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APPENDIX: EOS (Electrical Over Stress)

EOS: the failure analysis result no one wants to hear!

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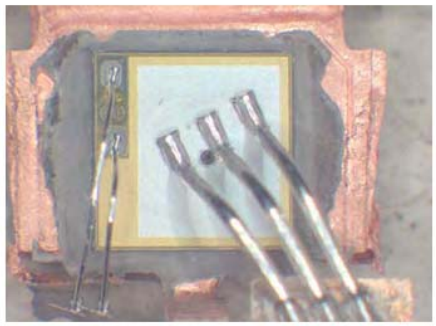
EOS Signature

AVALANCHE



- Failure site is found in an active MOSFET cell.
- The burn-mark is usually round in shape, indicating a central failure site and subsequent thermal damage
- If the avalanche event is long in duration (~ ms),then burn marks locate at central sites on the die, where there is maximum current flow and reduced heat dissipation. The sites are often adjacent to wire bonds/clip bonds where current density is high, but not directly under the wire bond/clip bond as it provides a local heat sink.
- Failure is at the hottest location of the die.
- For short avalanche events (~ us), the burn marks can take on more random locations over the die surface. The temperature rise in the chip is more uniform with negligible chance for current crowding and local heating on these time scales.
- For even shorter avalanche events, the burn marks can locate at die corners due to the discontinuity in cell structure at these locations.

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EOS Signature

LINEAR MODE Operation Signature (1/2)

- A Safe Operating Area (SOA) graph is included in all power MOSFET data sheets. Outside the defined safe region, the power dissipated in the FET cannot be removed, resulting in heating beyond the device capability and then device failure.
- Linear mode operation is common during device switching or clamped inductive switching and is not a fault condition unless the SOA is exceeded. The hottest location of the die is usually at the center of the die (maximum current flow and reduced heat dissipation).
- The sites are often adjacent to wire bonds/clip bonds where current density is high, but not directly under the wire bond/clip bond as it provides a local heat sink.

EOS Signature

LINEAR MODE Operation Signature (2/2)

Fig 45. Sample image 1: 15 V, 3 A

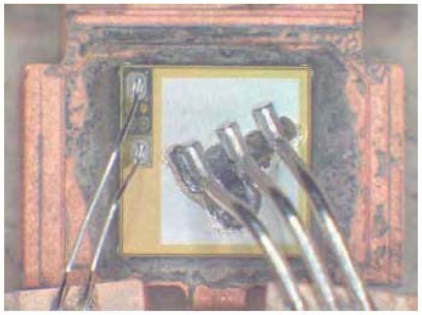

Fig 46. Sample image 2: 15 V, 3 A

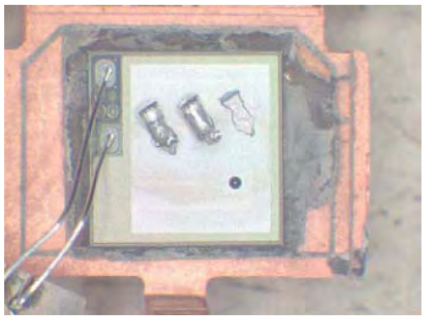

Fig 51. Sample image 3: 30 V, 1.5 A

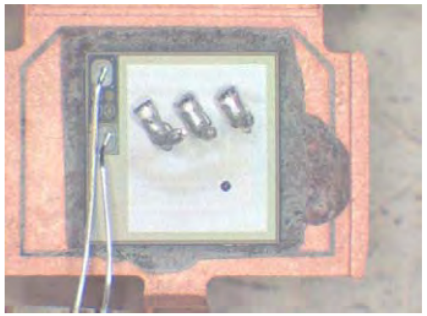

Fig 52. Sample image 4: 30 V, 1.5 A

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EOS Signature

Probable GATE-SOURCE over-voltage

No sign of damage at visual inspection. The unit was de-layered. After nitride/metal removal, the unit revealed signs of fusion on the die

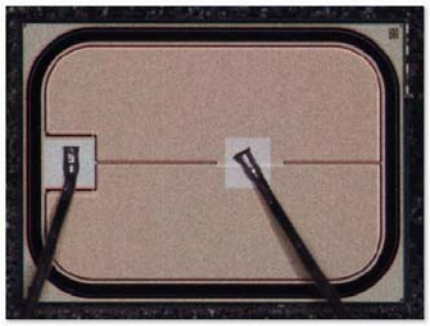

Figure 6- After decap

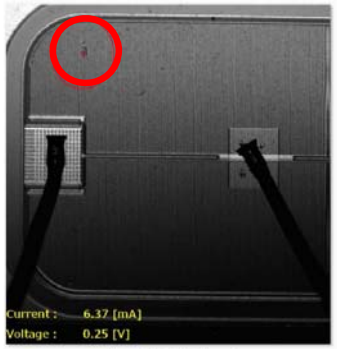

Figure 7- OBIRCH spot

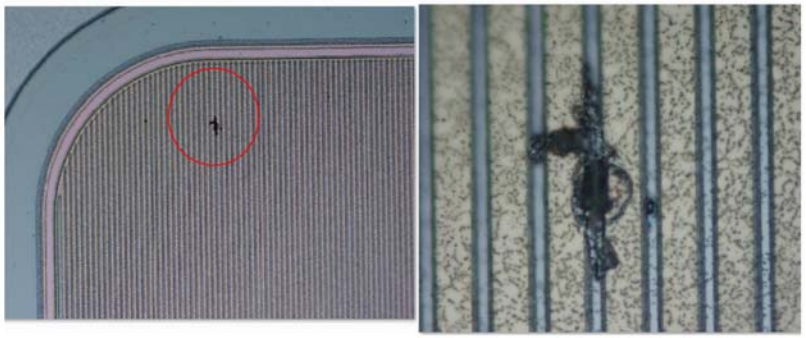

Figure 9- After Metal removal

OBIRCH (Optical Beam Induced Resistance Change) is used for high and low resistance analyses inside the chip. By scanning with a laser beam the IC surface, part of laser energy is absorbed by the IC and converted into heat. In case metal wires in the IC consist of defects or voids, the heat conduction in the place nearby will differ from that in normal areas, which in turn causes an ohmic change ΔR in the metal. If a constant voltage is added to the bonding wire while scanning, its current change can be established as ΔI= (ΔR/R)I. By associating ohmic change (cause by heat) with current change, and converting that value into brightness change of pixels, the pixel position can then be overlapped with the position scanned by the laser beam where the current changes.

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EOS Signature

OVER CURRENT Signature

- The maximum current-handling capability is specified on the data sheet for Power MOSFETs.
- This capability is based on the current handling capability of wires or clips, before which fusing will onset, combined with the ability to dissipate heat. Exceeding this rating can result in catastrophic failure
- Failure site is initially where the current handling connections (wires or clips) meet the die. Normally damage is extensive and spreads over the entire die surface with evidence of melted metallization and solder joints.
- For wire-bonded packages, there is often evidence of fused wires.
- For clip-bonded packages, die crack is commonly observed.

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谢谢

Merci

Grazie

Danke

Thanks

Efharisto

Gracias

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