Migration of applications from STM32MP15x lines to STM32MP13x lines microprocessor

Introduction

STM32MP131, STM32MP133 and STM32MP135 devices are part of the STM32 Arm® Cortex® MPU family; they all feature a single-core Cortex®-A7. These devices are referred to as STM32MP13x in this document.

STM32MP13x devices are lower cost derivatives of the STM32MP15x line devices, with no Cortex®-M4, only 1 Cortex®-A7 and no GPU. However, most architecture concepts and peripheral-register mappings are compatible, which permits easy migration from an STM32MP15x design to a similar device from the STM32MP13x lines.

Like STM32MP15x devices, the STM32MP13x high performance Cortex®-A7 runs open operating systems like Linux®, which provides rich connectivity and the support of the software community. The STM32MP13x offers more advanced security features compared to STM32MP15x devices.

This application note provides information to facilitate the migration from an STM32MP15x device towards an STM32MP13x device.

Table 1. Applicable products

Type	Product series
Microcontrollers	STM32MP1 series

1 General information

This document applies to STM32MP13x and STM32MP15x lines Arm®-based MPUs.

Note: Arm is a registered trademark of Arm Limited (or its subsidiaries) in the US and/or elsewhere.

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Table 2. Reference documents

-	Reference	Title
[1]	AN2867	Oscillator design guide for STM8AF/AL/S, STM32 MCUs and MPUs
[2]	AN1709	EMC design guide for STM8, STM32 and Legacy MCUs
[3]	AN5105	Getting started with touch sensing control on STM32 microcontrollers
[4]	AN4316	Tuning a touch sensing application on MCUs
[5]	AN5275	USB DFU/USART protocols used in STM32MP1 Series bootloaders
[6]	AN5168	DDR configuration on STM32MP1 Series MPUs
[7]	AN5587	STM32MP13x lines and STPMIC1 integration on a wall-adapter supply
[8]	AN5592	STM32MP13x lines DDR memory routing guidelines
[9]	AN5585	STM32MP13x lines and STPMIC1 integration on a battery-powered application
[10]	AN5586	STM32MP13x lines discrete power supply hardware integration
[11]	AN4879	USB hardware and PCB guidelines using STM32 MCUs
[12]	UMXXXX	Discovery kits with STM32MP135 MPUs
[13]	RM0475	STM32MP13x advanced Arm-based 32-bit MPUs
[14]	DSXXXX	STM32MP13xA/Dxx datasheet
[15]	DSXXXX	STM32MP13xC/Fxx datasheet
[16]	ES0539	STM32MP131x STM32MP133x STM32MP135x errata sheet

Table 3. Glossary

Acronym	Description
ADC	Analog to digital converter
AHB	Advanced high-performance bus
AXI	Advanced extensible interface (by extension, interconnect matrix based on AXI)
AXIM	AXI matrix (AXI based interconnect)
AXIMC	AXI matrix configuration control
BKPSRAM	Backup SRAM
BSEC	Boot and security controller (OTP interface)
CEC	Consumer electronics control (part of HDMI standard)
CNT	Generic timer (inside Cortex®-A7)
CRYP	Cryptographic peripheral, supporting DES, triple-DES and AES
CSI	Low-power internal oscillator
CTI	Cross-trigger interface
DAP	Debug access port
DCMI	Digital camera interface (parallel interface)
DCMIPP	Digital camera interface pixel pipeline (parallel interface)

Acronym	Description
DDRCTRL	Double data rate SDRAM controller, supporting LPDDR2 and DDR3/DDR3L protocols
DDRPERFM	DDR performance monitor, linked to DDRCTRL
DDRPHYC	DDR physical interface control
DFSDM	Digital filter for sigma-delta modulators
DLYBQS	Delay block for QUASDPI, compensating external signals timings to reach highest data rates
DLYBSD	Delay block for SDMMC, compensating external signals timings to reach highest data rates
DMA	Direct memory access: bus master able to autonomously transfer data between peripheral and memory, or between memories
DMAMUX	DMA request multiplexer
ETH	Ethernet controller
ETM	Embedded Trace Macrocell™
ETZPC	Enhanced TrustZone® protection controller, used to configure some peripherals and ROM/RAM protection settings
EXTI	Extended interrupt and event controller
FDCAN	Controller area network with flexible data-rate (can also support time-triggered CAN (TT))
FMC	Flexible memory controller
GIC	Generic interrupt controller
GMAC	Gigabit Ethernet media access controller
GPIO	General-purpose input output
GPU	Graphic processing unit
HASH	Cryptographic hash peripheral, supporting secure hash algorithm (SHA)
HDMI	High-definition multimedia interface
HDP	Hardware debug port
HSE	High-speed external quartz oscillator
HSEM	Hardware semaphore, helping multiprocessor resources sharing
HSI	High-speed internal oscillator
I2C	Inter-integrated circuit interface
I2S	Inter-integrated circuit Sound
IPCC	Inter-processor communication controller
IWDG	Independent watchdog
JTAG	Joint test action group (debug interface)
LCD	Liquid crystal display
LPTIM	Low-power timer
LSE	Low-speed external quartz oscillator
LSI	Low-speed internal oscillator
LTDC	LDC TFT display controller
MDIOS	Management data input/output slave, used to control Ethernet physical interface
MDMA	Master DMA
MLAHB	Multi-layer AHB (AHB based interconnect)
OTG	USB On-The-Go, standard USB interface, able to become host or device
OTP	One-time program memory
PKA	Public key accelerator

Acronym	Description
PMB	Process monitor block
PMIC	External power-management circuit that provides various platform power supplies, with large controllability through signals and serial interface
PWR	Power control
QUADSPI	Quad-data-lanes serial-peripheral interface
RCC	Reset and clock control
RNG	Random number generator
ROM	Read-only memory
RTC	Real-time clock
SAI	Serial-audio interface
SDMMC	Secure digital and MultiMediaCard interface, supporting SD, MMC, e.MMC™ and SDIO protocols
SMPS	Switched-mode power supply
SPDIF	Sony/Philips digital interface format
SPI	Serial peripheral interface
SRAM	Static random access memory
STGEN	System timer generator, used for Cortex-A7 timers
STGENC	STGEN control: secure part of STGEN
STGENR	TGEN read: read-only part of STGEN
STM	System trace macrocell
SWD	Serial-wire debug
SWO	Single-wire output (trace port)
SYSCFG	System configuration
SYSRAM	System SRAM
TAMP	Tamper detection peripheral
TEMP	Temperature sensor
TFT	Thin-film transistor: LCD technology process
TIM	Timer
TSGEN	Debug time stamp generator, used to ensure multiple core traces synchronization
TZC	TrustZone address space controller, used to protect access to external SDRAM
UART	Universal asynchronous receiver/transmitter
USART	Universal synchronous/asynchronous receiver/transmitter
USB	Universal serial bus
USBH	USB host controller
USBPHYC	USB physical interface control
VREFBUF	ADC voltage reference buffer
WWDG	Window watchdog

2 STM32MP1 Series overview

This document focuses on the migration of applications from STM32MP15x lines to STM32MP13x lines microprocessors. Both product lines are part of the STM32MP1 Series. When compared to STM32MP15x lines devices, the STM32MP13x lines devices make available the possibility of a higher-cost optimization and propose more advanced security features.

STM32MP13x lines propose the following higher level features compared to STM32MP15x lines devices:

- Advanced security-related peripherals:
  - DDRMCE on the fly encryption/decryption on DDR
  - Secure AES and PKA with DPA protection and hardware bus
  - HASH (SHA-384/512) (versus HASH 256(1))
  - RTC with hardware key bus (versus no HW key bus(1))
  - All GPIOs securable (versus only a few(1))
  - 12 tamper pins (versus only three(1))
  - Display interface with secure layer (LTDC) (versus no secure layer(1))
- Dual gigabit ethernet MAC interface (ETH1, ETH2) (versus single ETH1(1))
- DMAMUX extension to DMA3 for secured accesses (versus DMA1/DMA2(1))
- Improved camera interface (DCMIPP) (16-bits, improved bandwidth) (versus 14-bits(1))
- CPU DVFS and LPLV-Stop2 mode (can reduce CPU core subsystem power supply in Run mode and power down in Stop mode)

1. *On STM32MP15x lines.*

STM32MP15x lines, propose the following higher level features compared to STM32MP13x lines devices:

- Dual-core Arm® Cortex®-A7 subsystem (versus single-core(1))
- Arm® Cortex®-M4 subsystem and associated hardware semaphore (HSEM)
- 3D graphic processing unit (GPU)
- External LPDDR2/LPDDR3/DDR3/DDR3L 16 or 32-bit interface (versus 16-bit (1))
- Serial display interface controller (DSI)
- High-definition multimedia interface - consumer electronics control (HDMI-CEC)
- Three SDMMC, four SAI, six SPI, six I2C interfaces (versus respectively 2, 2, 5 and (1))
- Digital filter for sigma delta modulators (four channels, two filters) (DFSDM1) (versus eight channels and six filters(1))
- Eight to 16-bitaAnalog-to-digital converters (ADC1/ADC2) (versus 12-bit(1))
- Two D/A 12-bits analog converters

1. *On STM32MP13x lines.*

The STM32MP13x line devices are part of the MPU family. This is as an easy stepladder from STM32 MCUs to benefit from the high-performance Cortex®-A7 running open operating systems like Linux®, providing rich connectivity and software community.

This migration guide covers specifically the migration from the STM32MP15x to STM32MP13x lines. For new features present on the STM32MP13x devices while not already present on STM32MP15x devices, these are not covered in this document. Refer to the STM32MP13x lines reference manual and datasheets for more details.

3 Hardware migration

There is no package compatibility between STM32MP15x lines and STM32MP13x lines.

STM32MP13x lines propose three packages with the following parameters:

- Size: the package size (from 9x9 to 14x14)
- PCB: the PCB technology cost (TFBGA pitch 0.5 or LFBGA pitch 0.8)

The following table summarizes the key package parameters for both STM32MP15x and STM32MP13x lines.

Table 4. STM32MP15x compared to STM32MP13x packages

Product	GPIO	Package	Size (mm)	Ball pitch (mm)	DDR bus width	Product	GPIO	Package	Size (mm)	Ball pitch (mm)	DDR bus width
STM32MP15xxAD	98	TFBGA257	10x10	0.5	16	STM32MP13xxAG	135[1]	TFBGA289	9x9	0.5	16
STM32MP15xxAB	98	LFBGA354	16x16	0.8	16	STM32MP13xxAF		TFBGA320	11x11	0.5	
STM32MP15xxAC	148	TFBGA361	12x12	0.5	32	STM32MP13xxAE		LFBGA289	14x14	0.8	
STM32MP15xxAA	176	LFBGA448	18x18	0.8	32	-		-	-	-	

1. *Including four JTAG and three BOOT signals that can be used as GPIO if JTAG or BOOT signal is not needed.*

4 Boot modes selection

The STM32MP15x and STM32MP13x lines devices have similar boot mechanism. They always start from internal BootROM, based on the boot pins as well as on internal OTP fuses configuration:

- Boot from external Flash memory:
  - SD-Card (SDMMC1)
  - eMMC (SDMMC2)
  - SLC-NAND (FMC)
  - Serial NOR-Flash memory (QUADSPI)
  - Serial NAND Flash memory (QUADSPI)
- Boot from UART or USB OTG on high-speed PHY port #2
  - Used to access the device from the STM32CubeProgrammer (for example to program the external Flash memory or the internal OTP fuses)

Note: USART2 is a possible boot interface on STM32MP15x but not on STM32MP13x line devices.

On STM32MP13x lines devices, it is possible to use the same GPIOs for a default FMC Nand8 boot interface or for QUASPI single bank1 boot.

On STM32MP13x lines devices, the boot pins are now GPIOs (BOOT[2:0] signals respectively on PI[6:4] pins). As a result, those pins are controlled by different registers compared to STM32MP15x devices.

Table 5. Boot mode selection for STM32MP13x and STM32MP15s devices

Figure 1. Boot mode selection for STM32MP13x devices

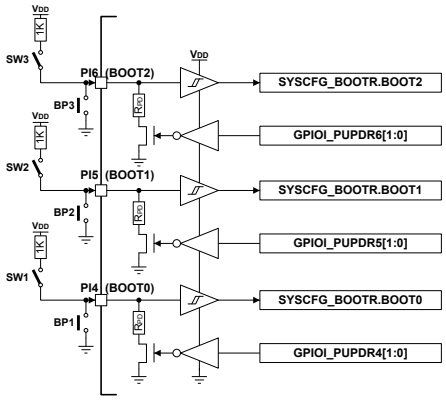
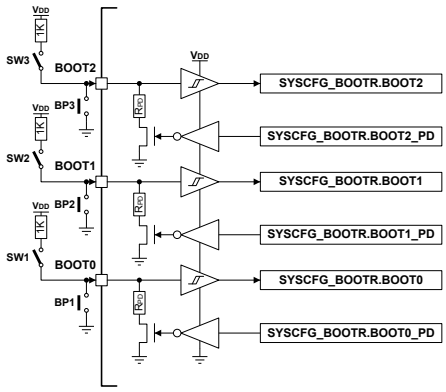


Figure 2. Boot mode selection for STM32MP15x devices



Refer to *Getting started with STM32MP13xx MPUs hardware development (*AN5474) and to the STM32MP1 Series wiki articles below:

- https://wiki.st.com/stm32mpu/index.php/Boot_chains_overview
- https://wiki.st.com/stm32mpu/index.php/STM32MP15_ROM_code_overview

5 Peripherals migration

The following table shows the peripherals available on STM32MP15x lines devices and that are different on STM32MP13x line devices (either not present, with a different number of instances, or of a different type). It does not list new peripherals or new features released on STM32MP13x lines devices and not present in STM32MP15x lines.

Table 6. STM32MP15x lines features and peripheral counts compared to STM32MP13x lines

Product / Peripherals		STM32MP157 line				STM32MP153 line				STM32MP151 line				STM32MP135 line	STM32MP133 line	STM32MP131 line
		STM32MP157xAD	STM32MP157xAB	STM32MP157xAC	STM32MP157xAA	STM32MP153xAD	STM32MP153xAB	STM32MP153xAC	STM32MP153xAA	STM32MP153xAD	STM32MP153xAB	STM32MP153xAC	STM32MP153xAA			
SRAM in Kbytes	System Cortex®-M4 and Cortex®-A7	448 256[1]												N/A 128+32[2]		
	Backup	4												8		
DRAM controller		16-bits		32-bits		16-bits		32-bits		16-bits		32-bits		16-bits		
FMC memory controller[3]		Yes												Yes		
Quad-SPI		Yes												Yes		
Ethernet [4]		Single (GMII, RGMII, MII, RMII)												Dual (RGMII, MII, RMII)		
Timers	General purpose	10												10		
	Advanced control	2												2		
	Basic	2												2		
	Low power	5												5		
Random number generator		Yes												Yes		
Communication interfaces	SPI / I2S	6/3 (full duplex)												5/4		
	I2C	6												5		
	USART/ UART	4/4												4/4		
	USB OTG FS	Yes[5]												No		
	USB OTG HS	Yes[6]												Yes		
	CAN	2 (FDCAN)								No				2 (FDCAN)		
	SAI	4												2		
	SDIO	Yes[7]												Yes[8]		
	MDIO	Yes												No		
	SPDIFRX	4 inputs												4 inputs		
Camera interface		Yes (14-bits)												Yes (16-bits)		
MIPI-DSI host		Yes				No								No		

Product / Peripherals	STM32MP157 line				STM32MP153 line				STM32MP151 line				STM32MP135 line	STM32MP133 line	STM32MP131 line
	STM32MP157xAD	STM32MP157xAB	STM32MP157xAC	STM32MP157xAA	STM32MP153xAD	STM32MP153xAB	STM32MP153xAC	STM32MP153xAA	STM32MP153xAD	STM32MP153xAB	STM32MP153xAC	STM32MP153xAA			
HDMI-CEC	Yes												No		
LCD-TFT	Yes												Yes[9]		
3D GPU	Yes				No								No		
Cryptography	Yes[10]												Yes[11]		
Hash	Yes (up to SHA 256)												Yes (up to SHA-512)		
GPIOs	98		148	176	98		148	176	98		148	176	135[12]		
ADC	2 (up to 16-bits)												2 (up to 12-bits)		
Number of ADC channels	17		22		17		22		17		22		18		
12-bit DAC	Yes												No		
Number of DAC channels	2												N/A		
Maximum Cortex-M4 frequency	209 MHz[13]												N/A		
Maximum Cortex-A7 frequency	800 MHz[14]												1000 MHz[15]		
Operating voltage	1.71 to 3.6V														
Operating temperatures	Junction temperature: −40 to 105 °C / −40 to 125 °C														
Package	TFBGA257	LFBGA354	TFBGA361	LFBGA448	TFBGA257	LFBGA354	TFBGA361	LFBGA448	TFBGA257	LFBGA354	TFBGA361	LFBGA448	TFBGA289 TFBGA320 LFBGA289		

1. *STM32MP15x lines devices include 256 Kbytes Cortex-A7 L2 cache SRAM.*
2. *STM32MP13x lines devices include 128 Kbytes Cortex-A7 L2 cache SRAM.*
3. *NAND and PSRAM only, SDRAM on dedicated 16/32-bits DDR interface.*
4. *Gigabit Ethernet.*
5. *Only if OTG HS is not used.*
6. *Only if OTG FS is not used. Two embedded High-Speed PHYs (shared with Cortex-A7 USB host ports).*
7. *Only SDMMC3 instance with 4-bit data available for Cortex-M4 (three instances in total: 8 + 8 + 4 bits).*
8. *Two instances in total: 8 + 8 bits. Possibility to remove external level shifters in SDMMC UHS_I modes by using dedicated power supplies on the STM32MP13xxx device.*
9. *Including 1 secure layer.*
10. *On STM32MP15xC/Fxx devices.*
11. *On STM32MP13xC/Fxx devices. BSEC, RNG, CRYP, RTC support hardware key bus to secure AES (SAES). SAES supports differential power analysis (DPA) protection.*
12. *All GPIOs are secure. 135 GPIO including three boot signals and four JTAG signals.*
13. *In addition to dual-Cortex-A7 up to 650 MHz (single Cortex-A7 on STM32MP151 line).*
14. *On STM32MP15xD/Fxx devices (STM32MP15xA/Cxx devices are limited to 650 MHz).*
15. *On STM32MP13xD/Fxx devices (STM32MP13xA/Cxx devices are limited to 650 MHz).*

6 STM32 product cross-compatibility

The STM32MP13x lines do not include a Cortex®-M4 subsystem. Hence, all peripherals are operating under the supervision of the Cortex®-A7.

Cortex®-A7 subsystem can either run on an OpenOS operating system (Linux®), on some bare metal or on RTOS software.

Some more peripherals have been made secure on STM32MP13x versus STM32MP15x. The next table shows the differences.

Table 7. Securable peripherals on STM32MP13x versus STM32MP15x

Peripheral	STM32MP15x number of securable instances	STM32MP13x number of securable instances	Data transfer securable(1)
USART/UART	1	2	N/A
I2C	2	3	N/A
SPI	1	2	N/A
SDMMC	3	2	No
USB HS OTG	1	1	No
ETH	0	2	Yes
LCD secure layer	0	1	Yes
TSC	N/A	1	N/A
ADC	0	2	N/A
SAES	N/A	1	N/A
CRYP	1	1	N/A
HASH	1	1	N/A
TRNG	1	1	N/A
PKA	N/A	1	N/A
Watchdog	1	1	N/A
GPIO	8	All	N/A
DDR ctrl + PHY	1	1	Yes
FMC	0	1	No
Dual QUADSPI	0	1	No
GP Timer LP Timer	0	6 2	N/A N/A
MDMA	1	1	Yes
Dual port DMA	0	1	Yes
PWR, RCC, EXTI	1	1	N/A
Backup SRAM, backup registers	All	All	Yes
ML-AHB SRAM	0	1	Yes for STM32MP13x No for STM32MP15x
A7 MPU system SRAM	All	All	Yes

1. *N/A: not applicable, only register interface.*

6.1 Memory mapping

The peripheral address mapping is very similar on both STM32MP13x and STM32MP15x lines devices.

The main changes on STM32MP13x compared to STM32MP15x are:

- Removal of Cortex®-M4 related mappings.
- SRAM3 (8 Kbytes) is aliased next to the SYSRAM (128 Kbytes) to allow continuous memory-map space.
- APB6 is new for some secure timers and low-speed communication interfaces. It is mapped at the same location than the former AHB3. It is no longer present on STM32MP13x devices.

This is transparent when using the STM32CubeMX software package for Cortex®-A7.

6.2 GPIOs HSLV management

HSLV (high-speed low voltage) GPIO management has been modified on STM32MP13x compared to STM32MP15x:

- SYSCFG_IOCTRLSETR and SYSCFG_IOCTRLCLRR have been changed to several SYSCFG_HSLVENxR. Refer to the HSLV output buffers paragraph on the SYSCFG section from the corresponding reference manual for details.

7 Application software migration strategy

In some areas, the STM32MP13x lines devices are considered as a subset of the STM32MP15x lines devices. However, in other areas the STM32MP13x lines devices carry additional and multiple functional and security features.

The main target customers for STM32MP13x lines are those who are not concerned about the Cortex®-M4 embedded in the STM32MP15x lines. They are usually strict Linux® microprocessors, running on a single Cortex®-A7.

For those previously using the Cortex®-M4 who want to move to STM32MP13x lines to benefit from additional features, it is possible to use another external STM32 MCU as companionship.

OpenSTLinux RPMsg framework used to make the intercommunication between the Cortex®-A7 and the Cortex®-M4 cores on STM32MP15x lines can be ported from a shared RAM-based solution to a UART or SPI-based physical layer. This allows an easy migration to STM32MP13x lines devices.

With the GPU removal on STM32MP13x lines, products based on this MPU are unable to achieve the same graphical complexity than its predecessor, since all the composition must be done by the Cortex®-A7.

OpenSTLinux Distribution relies on the GPU when it is present, or on software libraries when it is absent. The porting is completely transparent for the user as far as the performance level of the processor alone supports the complexity level of the user interface.

The display pipe is able to generate the same images flow on STM32MP13x lines and was extended with YUV support as input and output.

The DSI interface is not present on STM32MP13x lines, so the parallel output port is the only option.

Beyond the hardware impacts of the DSI deletion but also the SDMMC3 instance removal or the lighter ADC and DFSDM peripherals configurations available on STM32MP13x compared to STM32MP15x, for instance, the OpenSTLinux Distribution exposes the same user land interfaces enabling a smooth move of devices from one product line to another.

STM32MP13x lines devices embed many new functional and security features. Such as dual Ethernet or new power domains for the functional, or new tampers, and DDR encryption for the security. These new features are deeply integrated in the OpenSTLinux drivers to extend the existing OpenSTLinux Distribution without drastic changes.

STM32MP13x lines are the most recent members of the STM32 MPU family, fully supported byOpenSTLinux Distribution. STMicroelectronics extends its MPUs portfolio and ensure to keep the same ease of use on its products with the support of the STM32 MPU wiki online documentation and with the rich ecosystem available for customers constituted of well-known tools such as STM8CubeMX and STM32CubeProgrammer.

Revision history

Table 8. **Document revision history**

Date	Revision	Changes
13-Feb-2023	1	Initial release

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