AN2046
APPLICATION NOTE

STR71X CLOCK CONFIGURATIONS EASY SETUP

INTRODUCTION

This application note describes how to use the "*STR71x_Calculation.xls*" file which is intended as a tool to assist in the configuration of the STR71x clocks and baud rates.

The STR71x microcontroller contains a variety of peripherals running at different frequencies. Some peripherals have a prescaler to adjust their working frequency, but some others don't and need a specific frequency to run correctly.

The file *"STR71x_Calculation.xls"* calculates all the working frequencies and shows the related register values for each peripheral.

Note: This application note doesn't substitute the fact that it is mandatory to read the reference manual before the use of this tool.

1 PRCCU

This peripheral allows the configuration of the clock Prescaler values to adjust the needed frequencies for the CPU, the APB1 and the APB2.

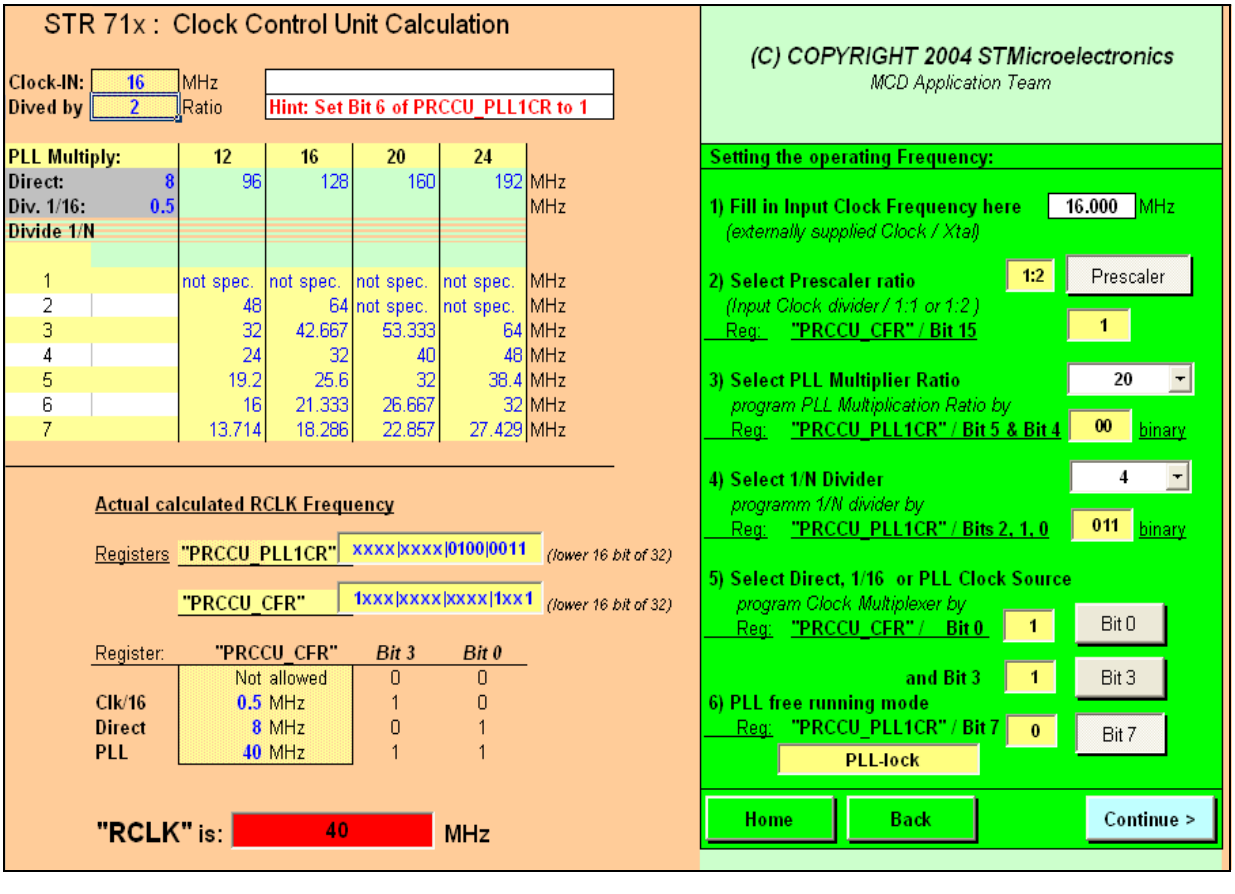
This peripheral contains two calculation sheets:

- CCU: Clock Control Unit calculation
- CDU: Clock Distribution Unit calculation

1.1 CCU

In this calculation sheet, it is necessary to enter the input clock frequency and the PLL configuration parameters (the Prescaler ratio, the PLL multiplier ratio, the PLL divider factor, the input clock source and the running mode).

Figure 1. CCU calculation sheet



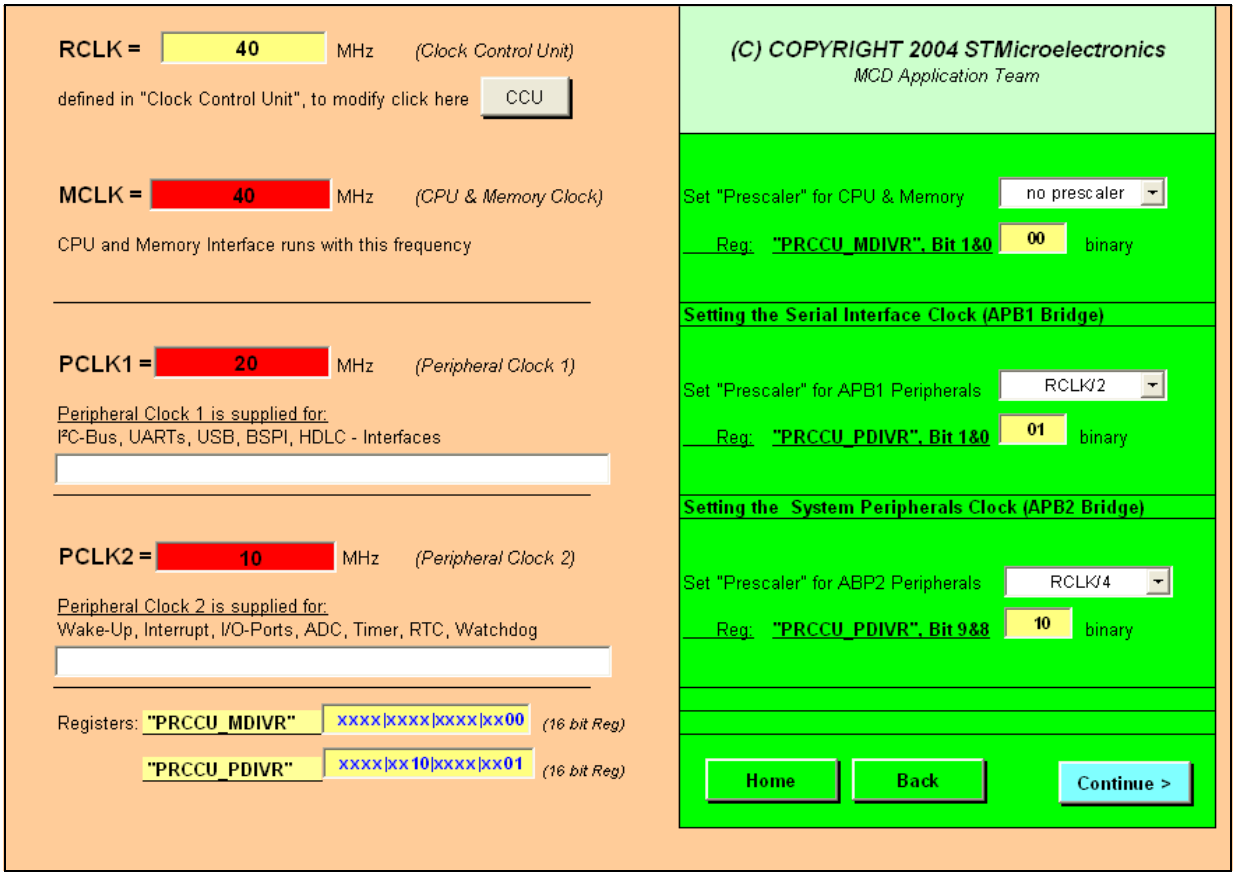
This sheet calculates all the frequencies which can be generated by the PLL.

As an example, as shown in Figure 1, the input frequency is set to 16MHz, the Prescaler ratio (1/2) is activated, the multiplier ratio is set to 20, the divider factor is set to 4 and the PLL is locked. This configuration allows the RCLK frequency to be set to 40MHz.

1.2 CDU

This calculation sheet is used to configure the working clock frequency for the CPU, the APB1 and the APB2.

Figure 2. CDU calculation sheet



Just select the required Prescaler and obtain as a result the MCLK, the PCLK1 and the PCLK2 working frequency values.

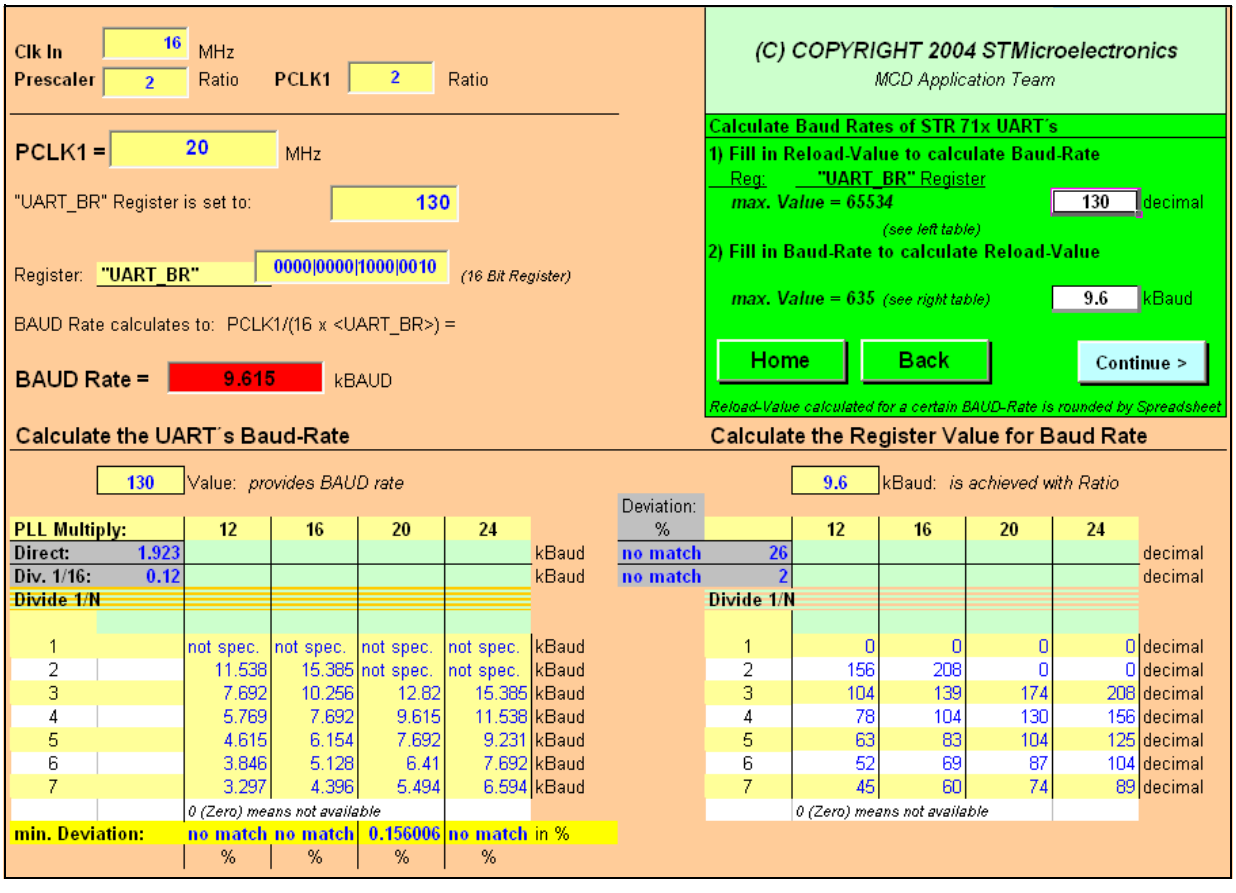
As an example, as shown in Figure 2, the Prescaler for CPU & memory is set to 1, the Prescaler for the APB1 peripherals is set to 2 and the Prescaler for the APB2 peripherals is set to 4. This configuration allows the MCLK to be set to 40MHz, the PCLK1 to 20 MHz and the PCLK2 to 10MHz.

2 UART

In this calculation sheet we have two cases:

- Enter the Prescaler and obtain as a result the correspondent baud rate,
- Or, just enter the required baud rate and obtain as a result the corresponding Prescaler.

Figure 3. UART calculation sheet



In this sheet there are two tables, the first one gives the baud rate for all the PLL frequency for a given Prescaler and the deviation for the actual PLL configuration. The second table calculates the corresponding prescaler for a given baud rate.

Figure 3 shows how to configure the actual baud rate to 9600 BAUD by setting the Prescaler to 130.

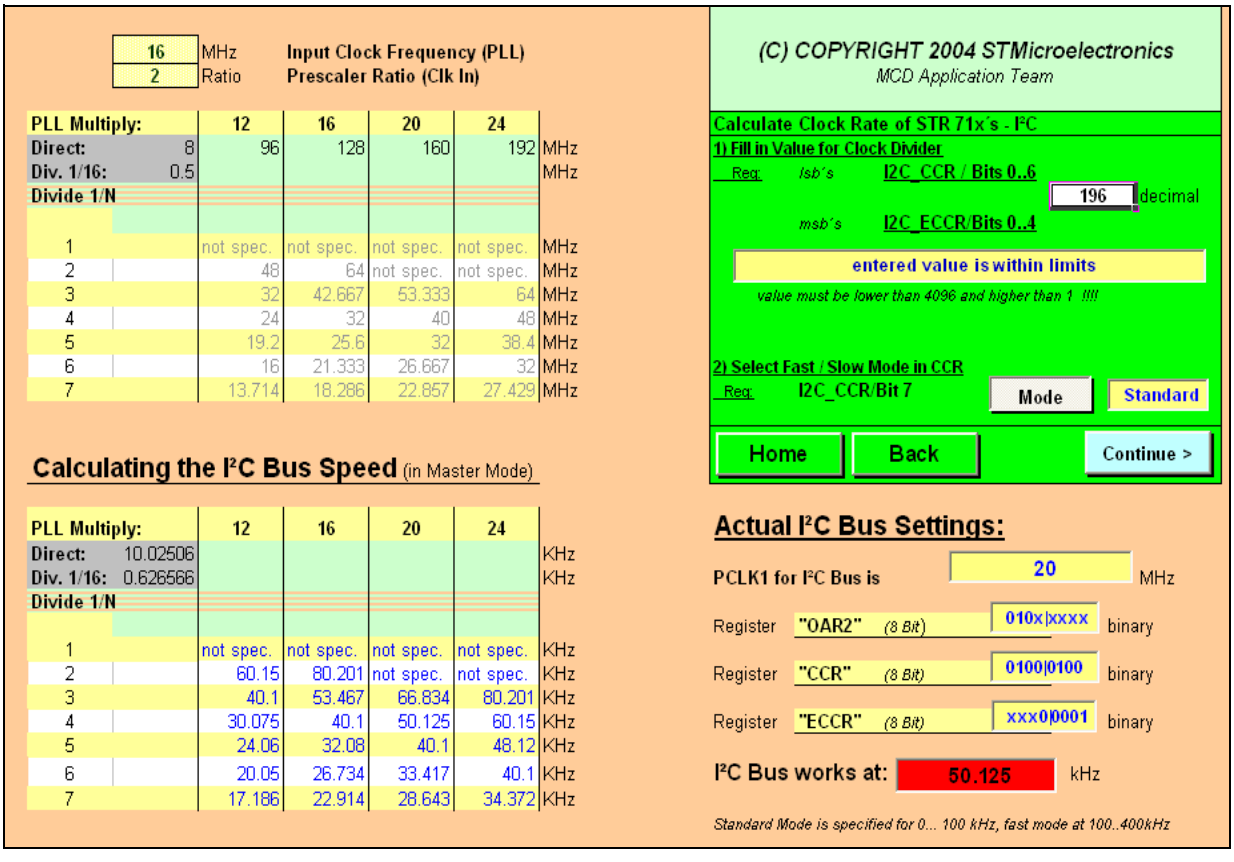
Note: For more details on the allowed value and standard baud rates, refer to the UART section in the reference manual.

3 I2C

The I2C has two functioning modes:

- The Standard I2C mode,
- The Fast I2C mode.

Figure 4. I2C calculation sheet



In this calculation sheet, it is necessary to select the functioning mode (Standard or Fast) by pushing the "*Mode*" button, and then to input the required Prescaler. We obtain as a result the working frequency of the I2C bus.

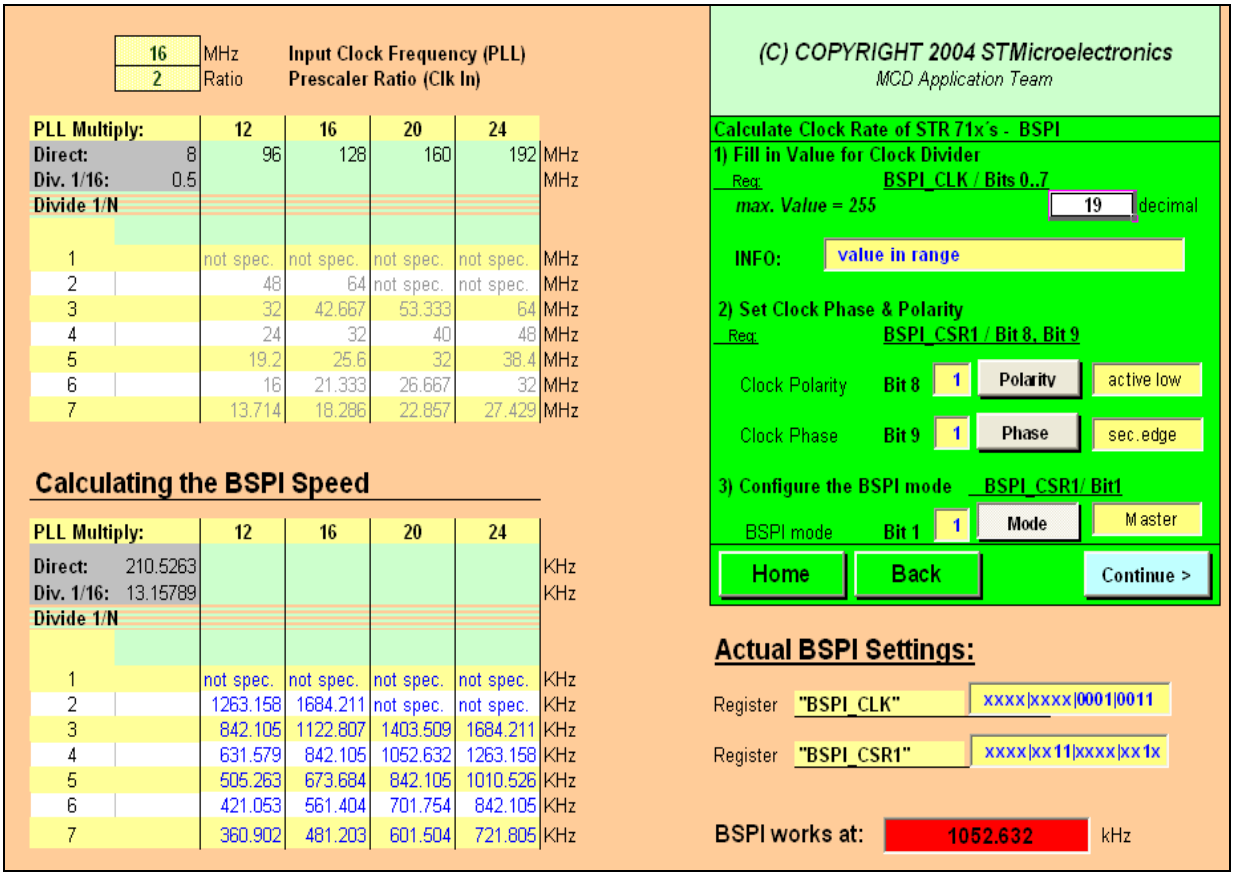
Figure 4 illustrates how to configure the I2C mode to Standard mode and the working frequency of the Bus to 50KHz.

Note: For more information about the calculation formulas, refer to the I2C section in the reference manual.

4 BSPI

In this calculation sheet, it is necessary to enter the corresponding divider factor, to configure the clock polarity, the clock phase and the BSPI mode. We obtain as a result the working frequency of the BSPI bus.

Figure 5. BSPI calculation sheet



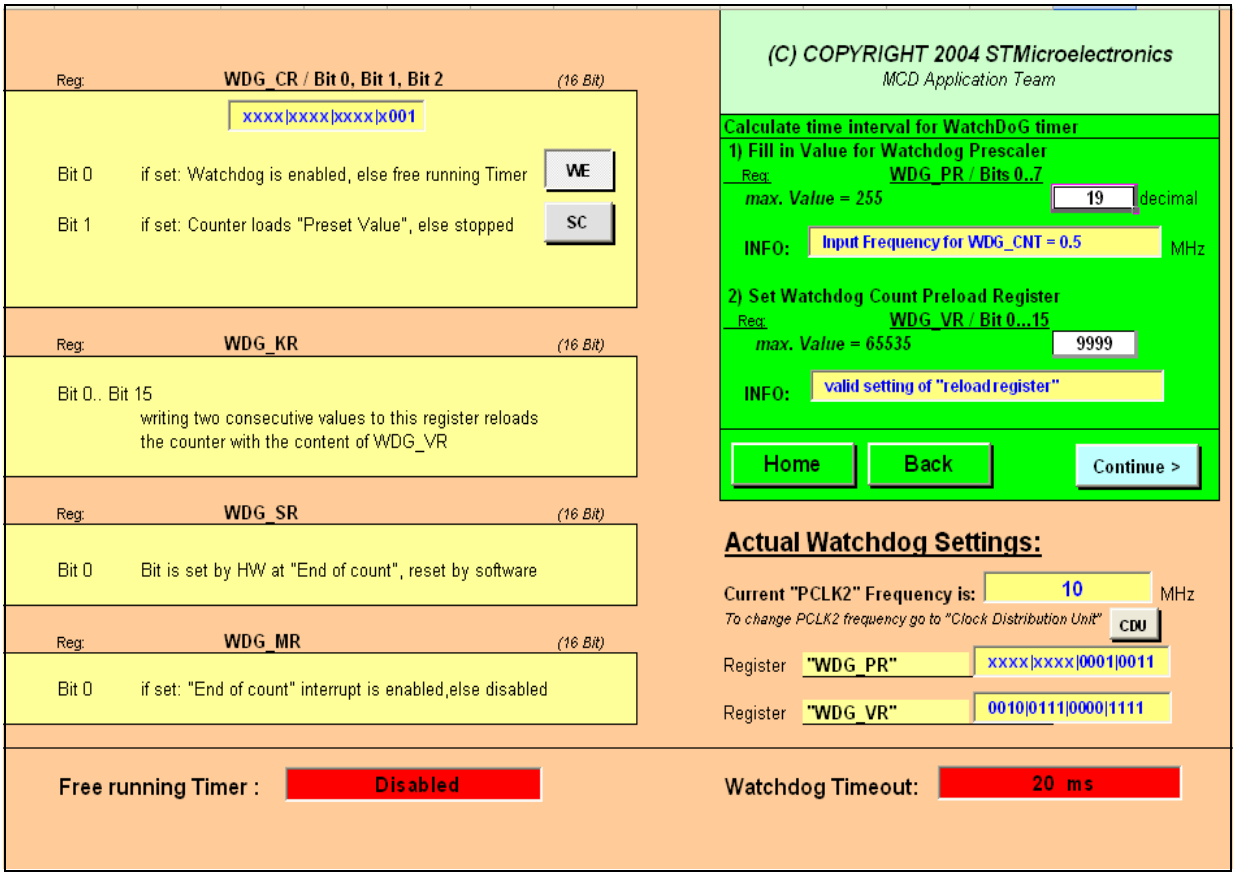
This example, as shown in Figure 5, illustrates how to configure the Clock Divider to 20, to set the BSPI working frequency to 1MHz, to set the polarity to “active low”, to set the phase to “second edge” and to configure the BSPI as master.

5 WDG

In this calculation sheet, it is necessary to enter the corresponding Prescaler, to set the watchdog Preload value, and finally to select the functioning mode (Free Running Timer mode or Watchdog mode).

We obtain as a result the Free running Timer frequency value if this mode is selected or the Timeout value if the Watchdog mode is selected.

Figure 6. WDG calculation sheet



As an example, as shown in Figure 6, this calculation sheet illustrates how to configure the WDG Prescaler to 19, the WDG Count Preload value to 9999 and to select the Free Running Timer mode.

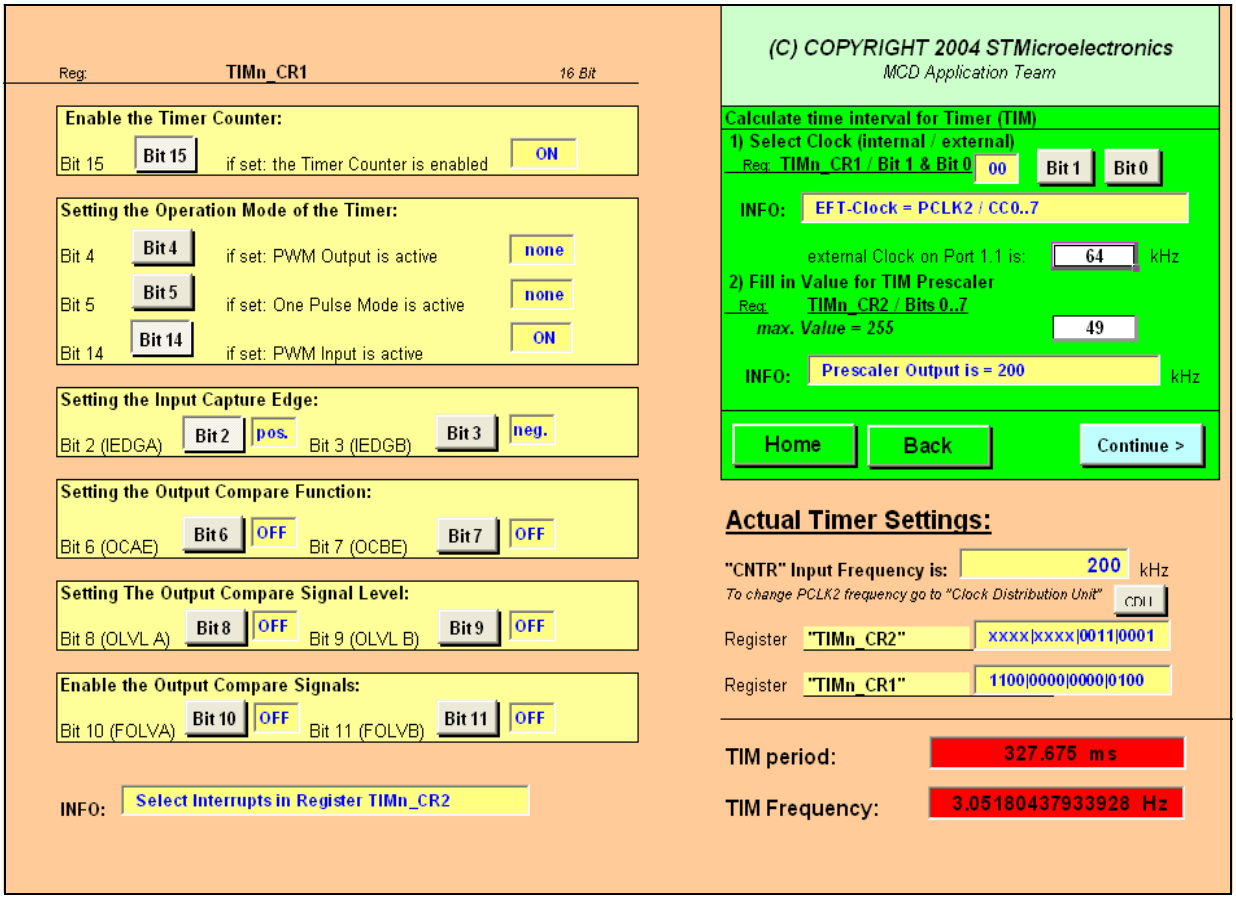
6 TIM

In this calculation sheet, it is necessary to select the clock source (internal or external), to select the external clock edge if external clock was selected, and to configure the needed prescaler. We obtain as a result the counter input frequency and the TIM period.

This sheet shows how to configure the different registers to:

- Enable/Disable the Timer Counter,
- Setting the operation mode of the Timer,
- Setting the Input Capture edge,
- Setting the Output Compare function,
- Setting the Output Compare signal Level,
- Enable the Output Compare signals.

Figure 7. TIM calculation sheet



As an example, as shown in Figure 7, this calculation sheet shows how to configure the TIM as follows:

- Select the Pulse Width Modulation Input mode,
- Configure ICAP A to a positive edge (Rising edge),
- Configure ICAP B to negative edge (Falling edge),
- Select the clock as internal and configure the Prescaler to 49,
- Enable the Timer Counter.

7 USB

The USB controller on STR71x works with an external clock generator supplying 48MHz as defined in the specification.

Note: However, due to USB data rate and packet memory interface requirements, the APB1 clock frequency must be greater than 8MHz to avoid data overrun/underrun problems.

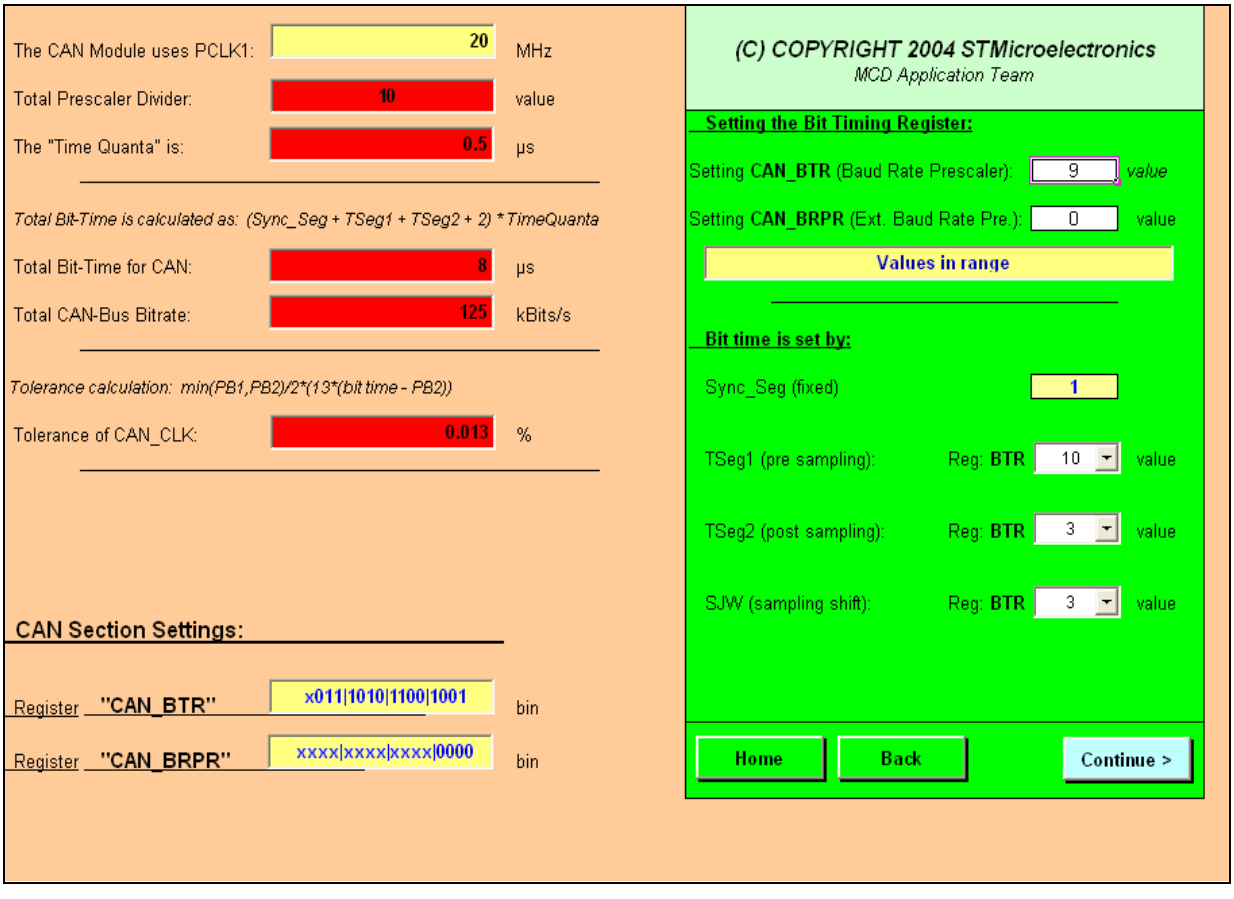
8 CAN

In this calculation sheet, it will be needed to enter the two baud rates Prescaler (Baud Rate Prescaler and Ext. Baud Rate Prescaler) and to configure the bit time parameters (TSeg1, TSeg2 and SJW).

We obtain as a result:

- The total Prescaler Divider,
- The Time Quanta,
- The total Bit-Time for CAN,
- The total CAN-Bus Bitrate,
- The tolerance calculation.

Figure 8. CAN calculation sheet



Note: For further details about the formulas, refer to the CAN section in the reference manual.

As an example, the table 1 lists the different standard bitrates of the CAN with their timing parameters with PCLK1 = 20MHz.

Table 1. Standard bitrate configurations (PCLK1 = 20 MHz)

Bitrate	NTQ	TSEG1	TSEG2	SJW	BRP
100Kbit/s	20	13	4	3	10
125Kbit/s	16	10	3	3	10
250Kbit/s	8	3	2	2	10
500Kbit/s	8	3	2	1	5
1Mbit/s	5	1	1	1	4

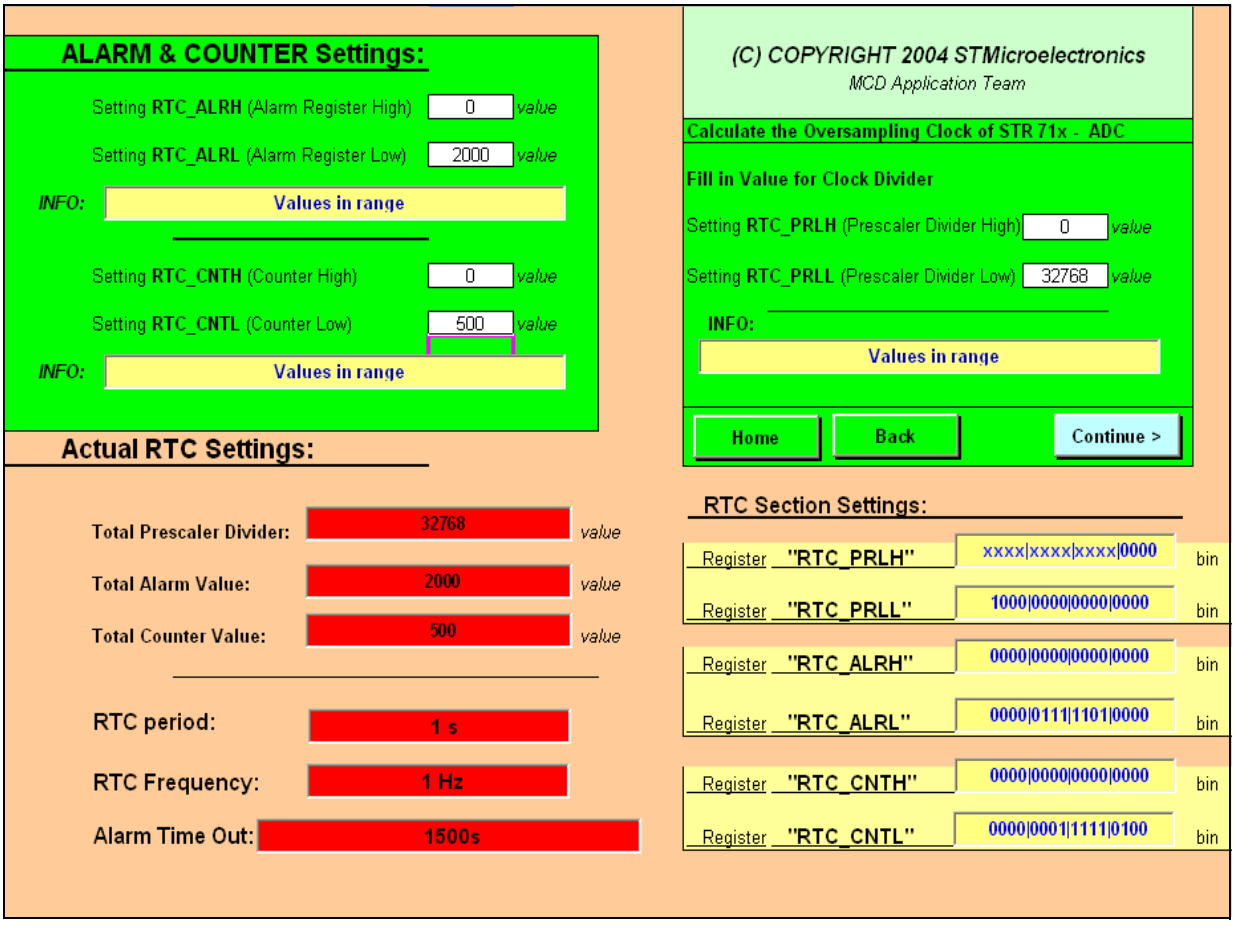
With:
NTQ: TSEG1+TSEG2+3
TSEG1: Time Segment before the sampling point minus Sync_seg
TSEG2: Time Segment after the sampling point
SJW: Synchronization Jump Width
BRP: Baud Rate Prescaler

9 RTC

In this calculation sheet, it will be needed to enter the Prescaler, the Alarm value and the counter value. We obtain as a result:

- The period,
- The frequency of the RTC counter,
- The Alarm time out.

Figure 9. RTC calculation sheet



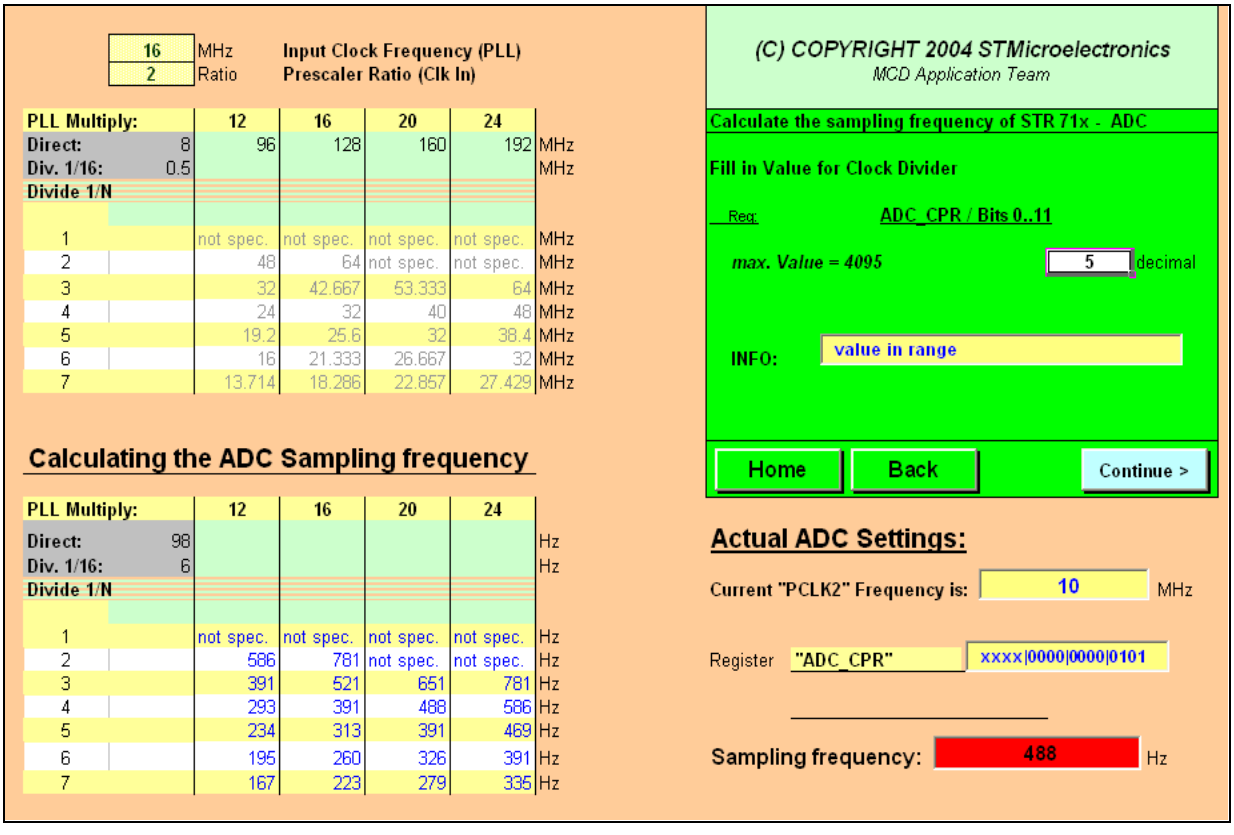
As an example, as shown in Figure 9:

- To configure the RTC period to 1s, just set the Prescaler to 32768;
- To configure the Alarm time out to 1500s just set the Alarm value to 2000 and the Counter value to 500.

10 ADC

In this calculation sheet, it is necessary to enter the clock divider. As a result, we will recuperate the ADC sampling frequency.

Figure 10. ADC calculation sheet



As an example, as shown in Figure 10, setting the Prescaler to 5, configure the sampling frequency to 488 Hz.

11 HDLC

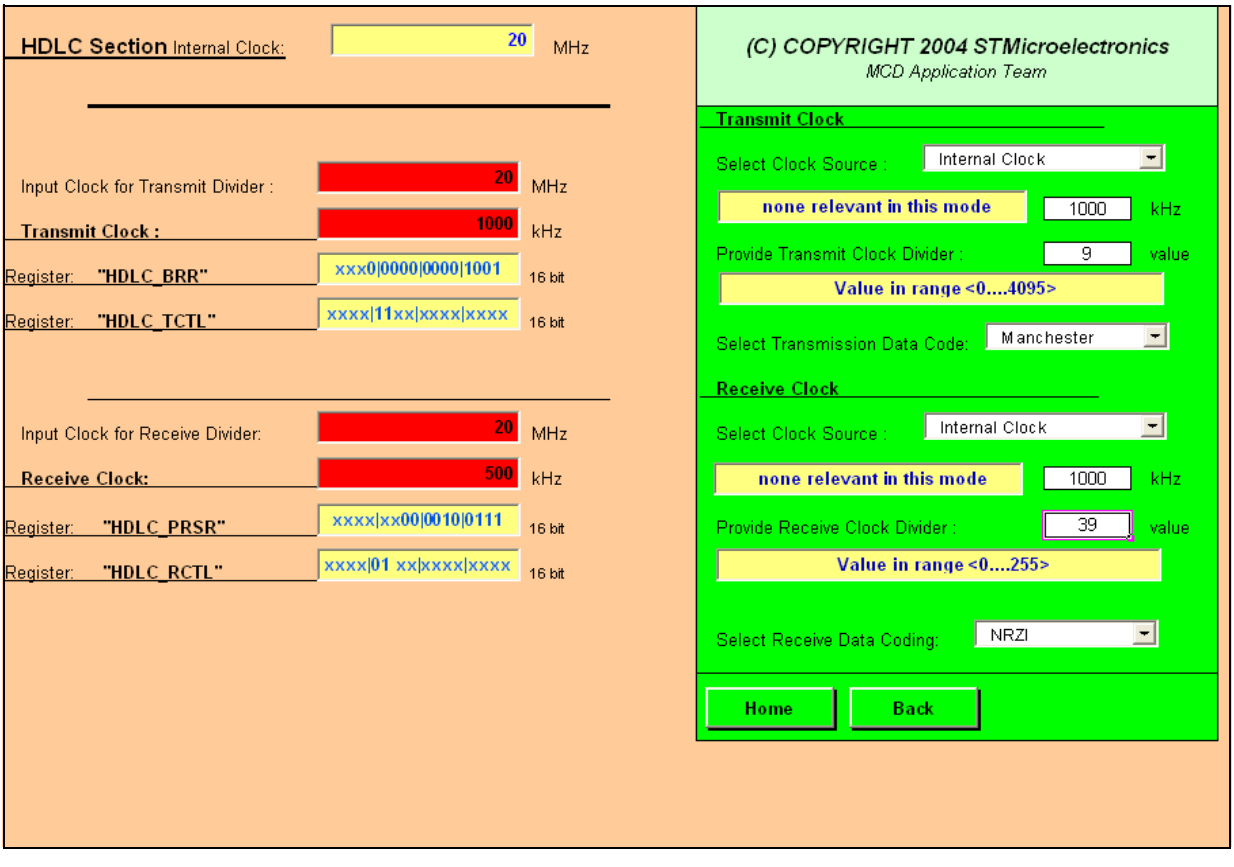
This calculation sheet allows the configuration and calculation of the transmit and the receive clocks.

For the two cases it is necessary to select the clock source (Internal or External), to set the value of the clock source if external clock source was selected, to configure the clock divider value and to select the transmission and the receive data code.

We obtain as a result:

- The transmit and the receive clocks,
- The transmit and the receive registers configuration.

Figure 11. HDLC calculation sheet



Note: For more details, refer to the HDLC section of the reference manual.

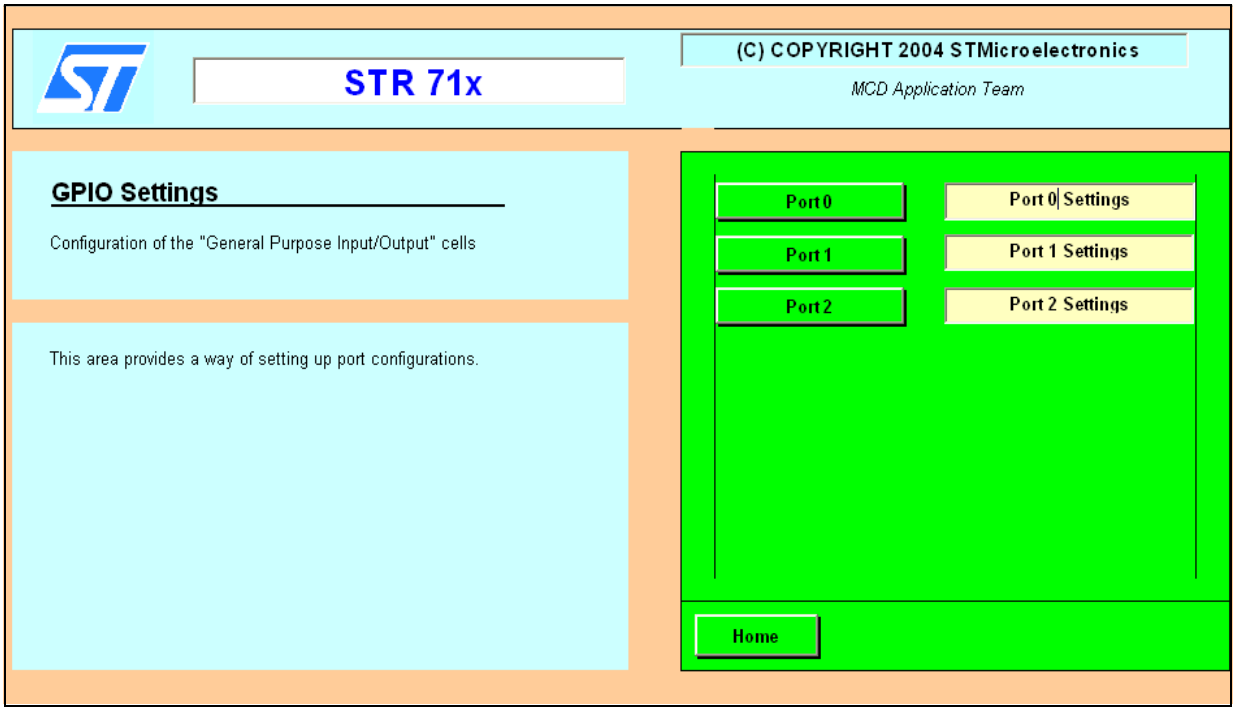
As an example, as shown in Figure 11, the HDLC is configured as follows:

- The transmit clock is set to 1MHz with an internal clock source, a clock divider value set to 9 and with Manchester transmission data code,
- The receive clock is set to 500KHz with an internal clock source, a clock divider value set to 39 and with NRZI transmission data code.

12 GPIO

In this sheet, there are three buttons (Port 0, Port 1 and Port 2) as shown in Figure 12.

Figure 12. GPIO Settings sheet



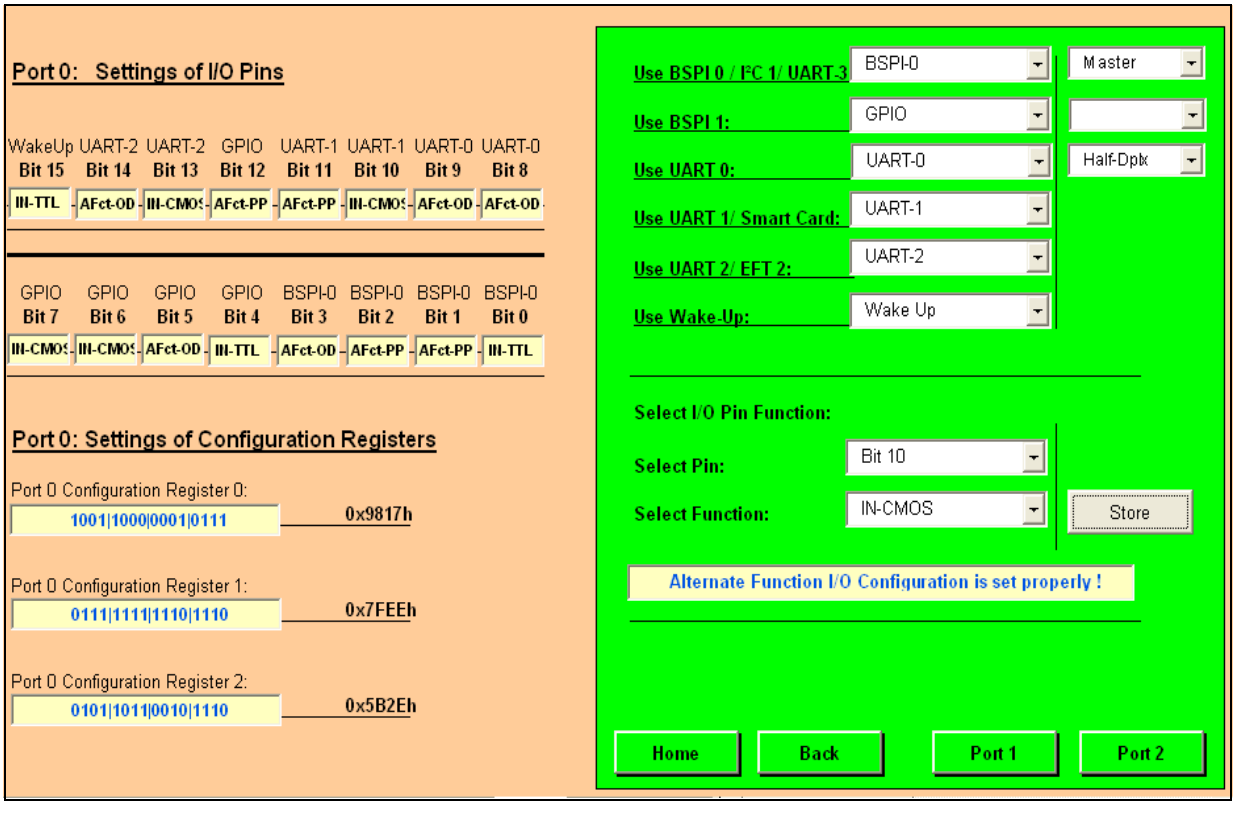
12.1 PORT 0

This sheet allows the configuration of all the port 0 pins independently. We obtain as a result the values to be loaded into the PC0, PC1 and PC2 registers.

Figure 13 shows how to configure the port 0 as follows:

- Bits 0, 1, 2, 3: BSPI0,
- Bits 4, 5, 6, 7, 12: GPIO,
- Bits 8, 9, 10, 11: UART1,
- Bits 13, 14: UART2,
- Bits 15: Wake-Up.

Figure 13. Port 0 configuration sheet



12.2 PORT 1

This sheet allows the configuration of all the port 1pins independently. We obtain as a result the values to be loaded in to the PC0, PC1 and PC2 registers.

The Figure 14 shows how to configure the port 1 as follows:

- Bits 0, 1, 2, 3: Timer 3,
- Bits 4, 5, 6, 7, 8, 9, 15: GPIO,
- Bits 10: USB,
- Bits 11, 12: CAN,
- Bits 13, 14: I2C.

Figure 14. Port 1 configuration sheet

12.3 PORT 2

This sheet allows the configuration of all the port 2 pins independently. We obtain as a result the values to be loaded in to the PC0, PC1 and PC2 registers.

The Figure 15 shows how to configure the port 2 as follows:

- Bits 0, 1: External memory interface: Select memory bank,
- Bits 2, 3, 12, 13, 14, 15: GPIO,
- Bits 4, 5, 6, 7: External memory interface: Address bus,
- Bits 8, 9, 10, 11: External interrupt.

Figure 15. Port 2 Configuration sheet