AN2479
Application note

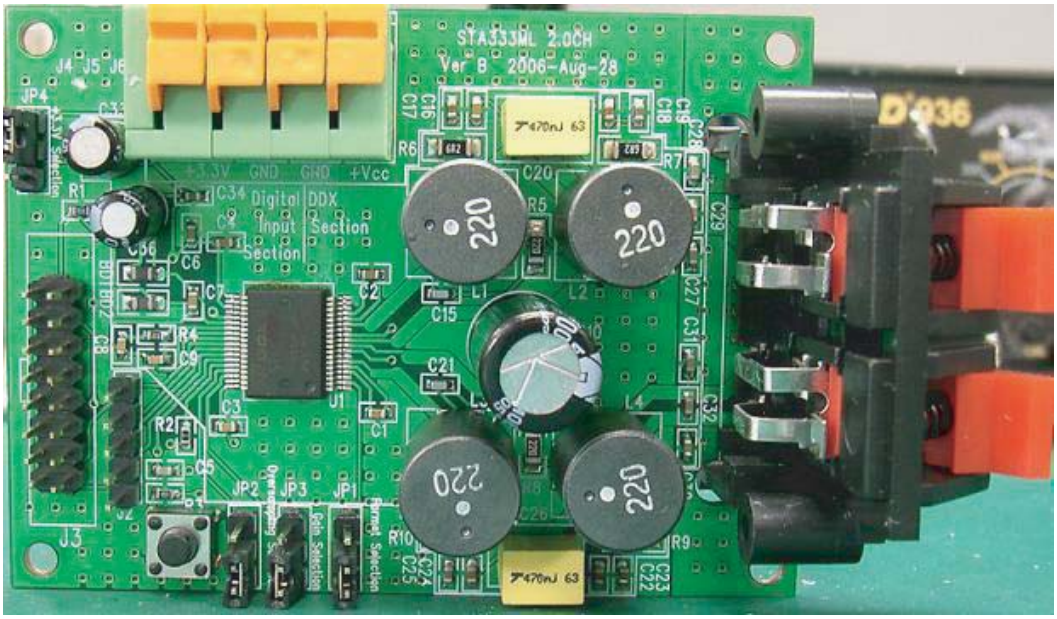
Sound Terminal® 2.0-channel microless high-efficiency digital audio system demonstration board based on the STA333ML

Introduction

The STEVAL-CCA048V1 is a demonstration board designed for the evaluation of the STA333ML Sound Terminal® high-efficiency digital amplifier. The purpose of this application note is to show how to connect the 2.0-channel board and to explain how to avoid critical board and layout issues.

The STEVAL-CCA048V1 demonstration board is configured for 2.0 BTL channels, releasing up to 2 x 20 W into 8 Ω of power output at 18 V supply voltage in the PSSO36 slug-down package. It represents a complete solution for a digital audio power amplifier capable of operating without the aid of an external microcontroller.

Figure 1. STEVAL-CCA048V1



Contents

1 Test conditions and connections of demonstration board

1.1 Test conditions

1.1.1 Jumpers, power supply, signal and interface settings

- JP1 is for format selection: 0* = I^2S, 1* = left justified
- JP2 is for oversampling selection: 0 = 256 Fs, 1 = 384 Fs
- JP3 is for gain selection: 0 = 0 dB, 1 = +24 dB, 0 = connect to outer side, 1 = connect to inner side
- +3.3 V selection: outer side = external +3.3 V, inner side = internal +3.3 V
- Connect positive voltage of 12 V DC power supply to +Vcc pin and negative to GND
- Connect positive voltage of 3.3 V DC power supply to +3V3 pin and negative to GND. If the +3.3V selection is set to inner side, there is no need to connect these wires.
- Connect STEVAL-CCA035V1 (APWLink USB interface board) to the J3 connector of the STA333ML demonstration board or suitable I^2S signals as shown in the schematic diagram (DATA on pin 1, LRCK on pin 4 and BICK on pin 5).
- Connect the S/PDIF signal cable to the RCA jack on the interface board, the other side connecting to the signal source such as Audio Precision equipment or a DVD player.
- Note that the voltage range of the DC power supply for Vcc is from 5 V to 18 V.

1.1.2 Output configuration

The STA333ML demonstration board is configured to 2.0 channels only and requires no software to control it, so it is not necessary to connect STEVAL-CCA035V1 to the PC. When the power supply, signal, interface and output are set up, push the RESET button, and the STEVAL-CCA048V1 demonstration board is ready to operate properly.

1.2 Connections

Figure 2. Board terminals (top view)

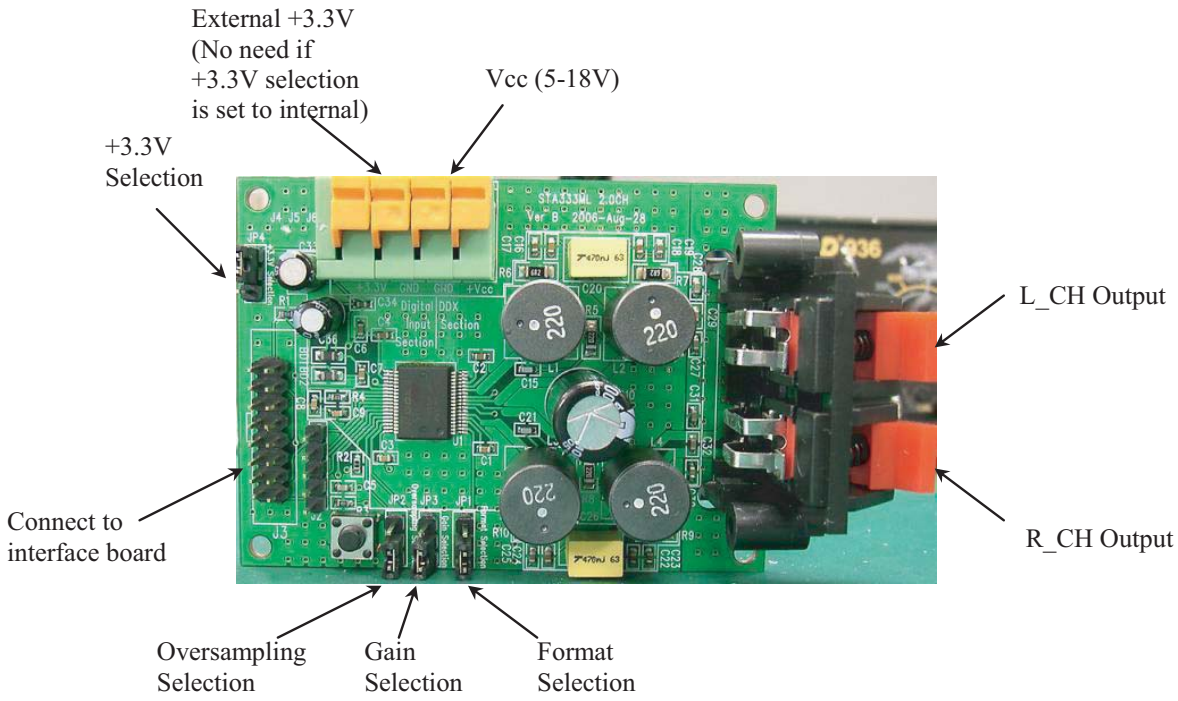


Figure 3. Speaker jack connection

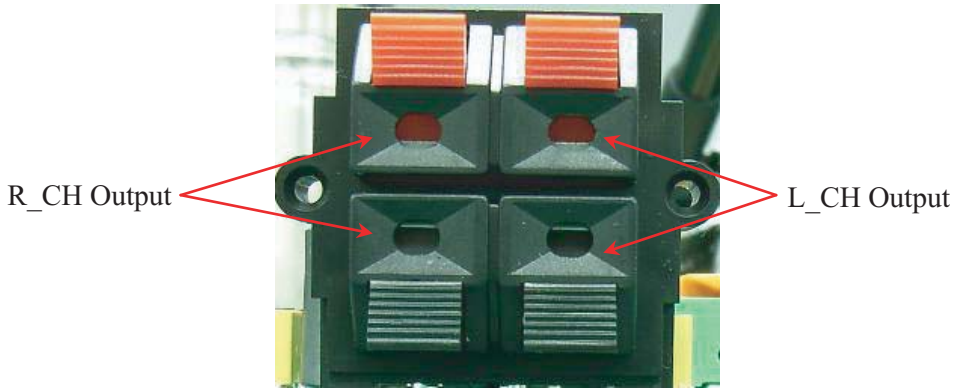
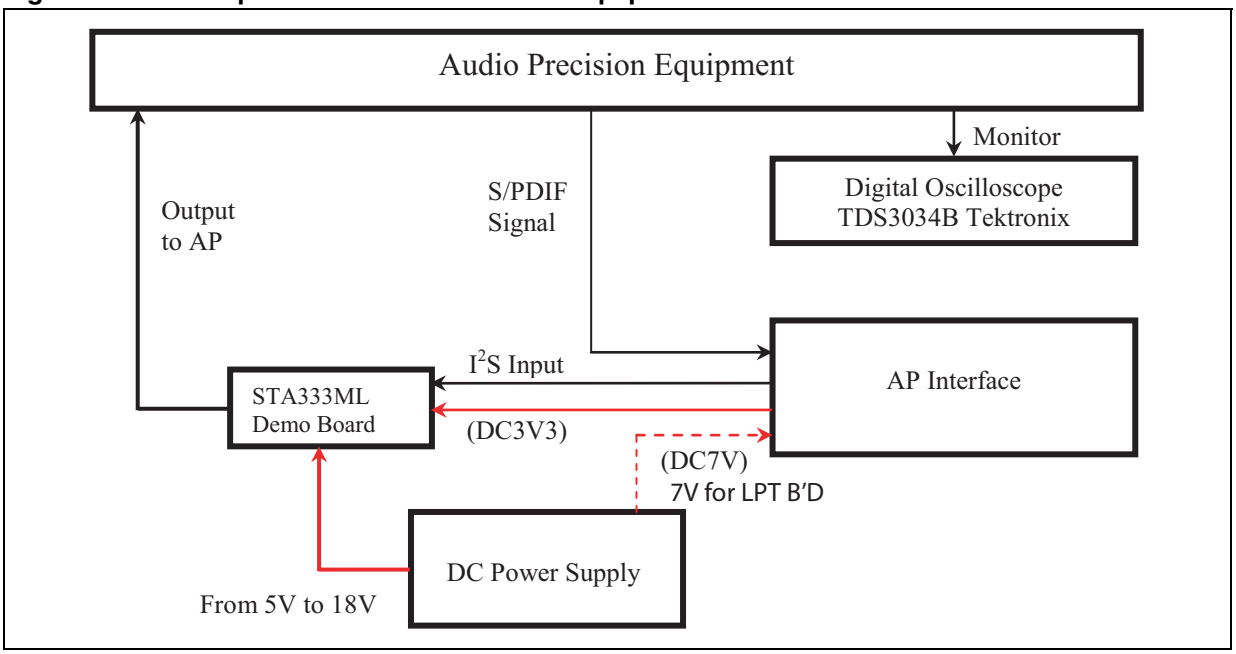


Figure 4. Hookup of test connections with equipment



2 Schematic and bill of material

Figure 5. Board schematic

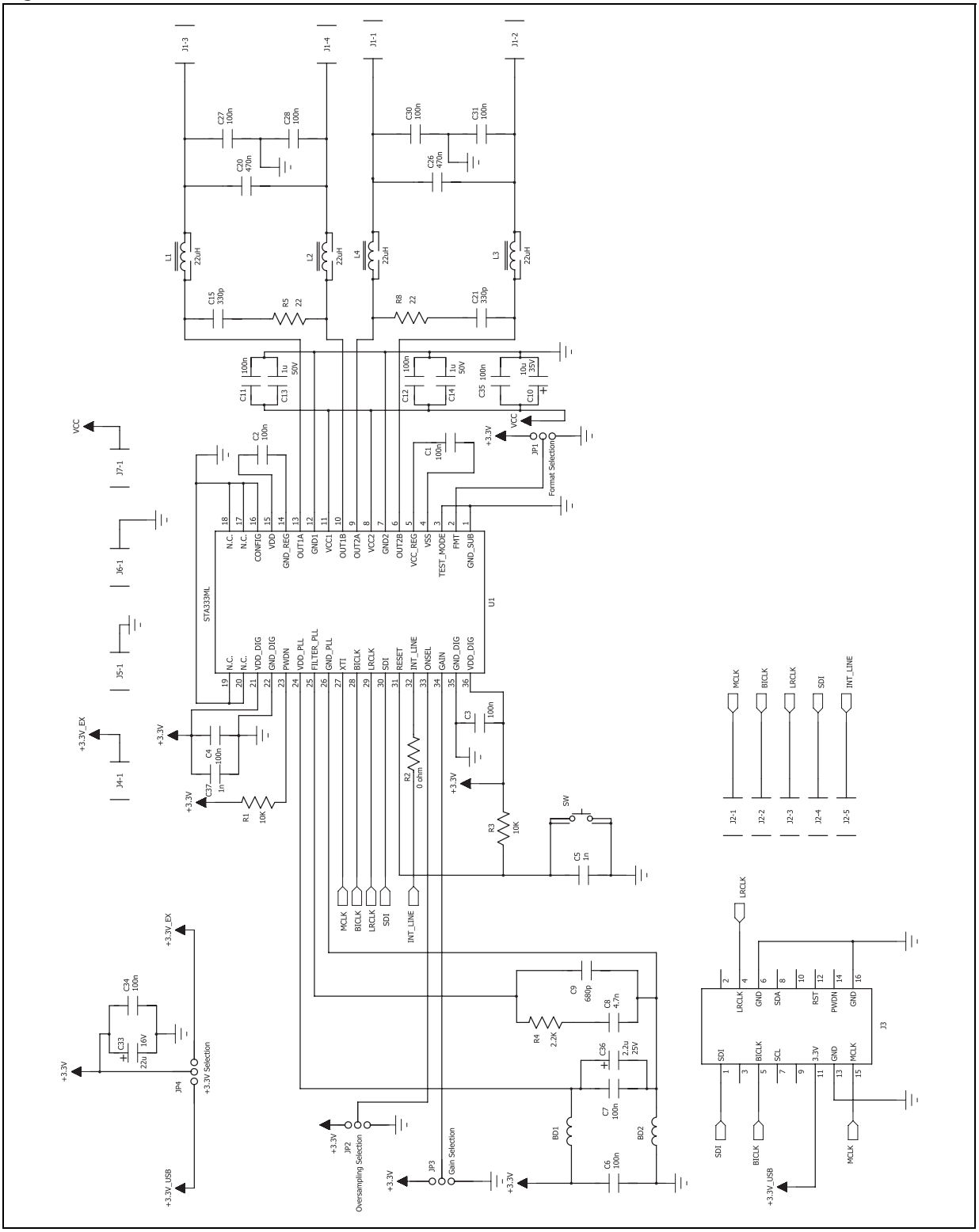


Table 1. Bill of material

Item	Type	Package	Description	Qty	Reference	Manufacturer
1	CCAP	CAP0603	100 nF, 50 V, ±10%	18	C1, C2, C3, C4,C6, C7, C11, C12, C16, C17, C18, C19, C22, C23, C24, C25, C34, C35	Murata
2	CCAP	CAP0603	1 nF, 50 V, ±10%	1	C5	Murata
3	CCAP	CAP0603	4.7 nF, 50 V, ±10%	1	C8	Murata
4	CCAP	CAP0603	680 pF, 50 V, ±5%	1	C9	Murata
5	CCAP	CAP0603	330 pF, 50 V, ±10%	2	C15, C21	Murata
6	CCAP	CAP0603	10 nF, 50 V, ±10%	6	C27, C28, C29, C30, C31, C32	Murata
7	CCAP	CAP1206	1 µF, 50 V	2	C13, C14	Murata
8	ECAP	D = 10 mm	1000 µF, 25 V	1	C10	Rubycon
9	ECAP	D = 7 mm	22 µF, 16 V	1	C33	Rubycon
10	ECAP	D = 5 mm	2.2 µF, 25 V	1	C36	Rubycon
11	CHIP BEAD	L0805	600 ohm @ 100 MHz	2	BD1, BD2	Murata
12	CRES	R0603	10 K, ±5%	2	R1, R3	Murata
13	CRES	R0603	0 ohm, ±5%	1	R2	Murata
14	CRES	R0603	2.2 K, ±5%	1	R4	Murata
15	CRES	R1206	22 ohm, ±5%	2	R5, R8	Murata
16	CRES	R1206	6.2 ohm, ±5%	4	R6, R7, R9, R10	Murata
17	Test point	Through-hole	1x5 2.54 mm pitch	1	J2	Any source
18	Connector	Through-hole	2x8 2.54 pitch male connector	1	J3	Any source
19	Jumper	Through-hole	1x3 2.54 mm pitch	4	JP1, JP2, JP3, JP4	Any source
20	IC	PowerSSO36	STA333ML	1	U1	ST
21	CAP	Through-hole	470 nF	2	C20, C26	
22	Connector	Through-hole	WP4-15	1	J1	Song Cheng
23	Connector	Through-hole	FFKDS/H1-5.08	3	J5, J6, J7	Phoenix Contact
24	Connector	Through-hole	FFKDSA1/H1-7.62	1	J4	Phoenix Contact
25	Coil	Through-hole	22 µH	4	L1, L2, L3, L4	Kwang Sung
26	Tact switch	Through-hole	6x6 tact switch	1	SW	

Figure 6. Top view of PCB layout

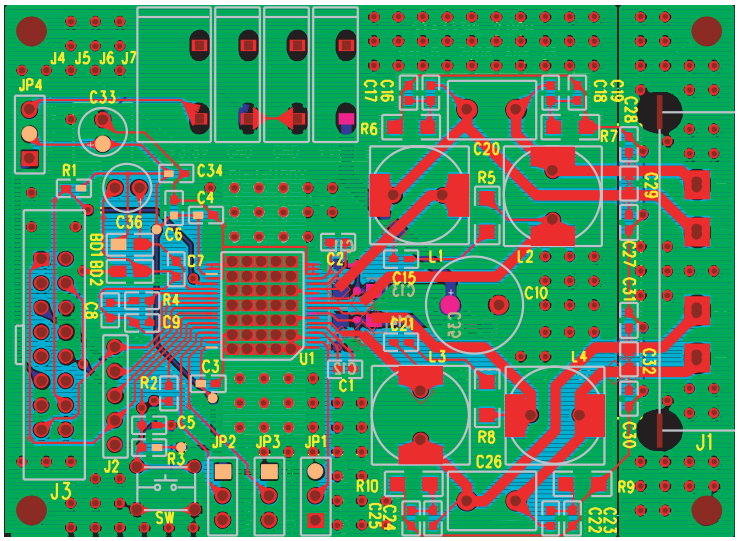
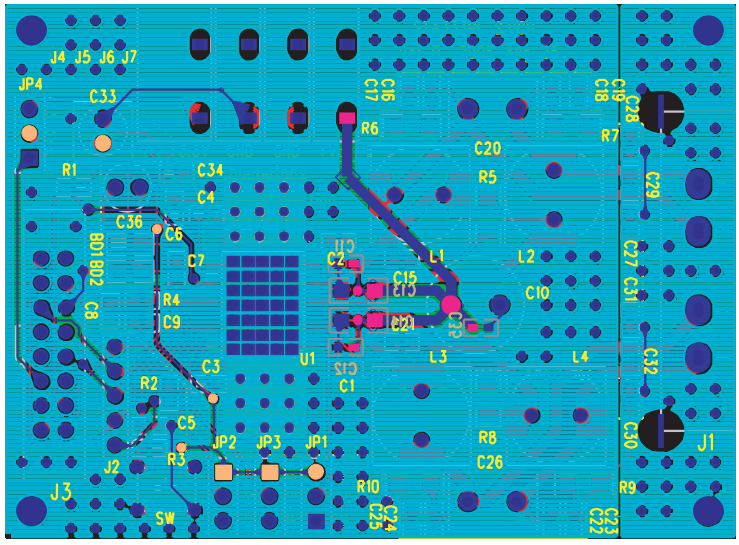


Figure 7. Bottom view of PCB layout



3 Design guidelines for PCB schematic and layout

3.1 Schematic

3.1.1 General

- Absolute maximum rating: 20 V
- Bypass capacitor 100 nF in parallel to 1 µF for each power Vcc branch. Preferable dielectric is X7R.
- Vdd and ground for the PLL filter are separated from the other power supply
- Coil saturation current compatible with the peak current of the application

3.1.2 Decoupling capacitors

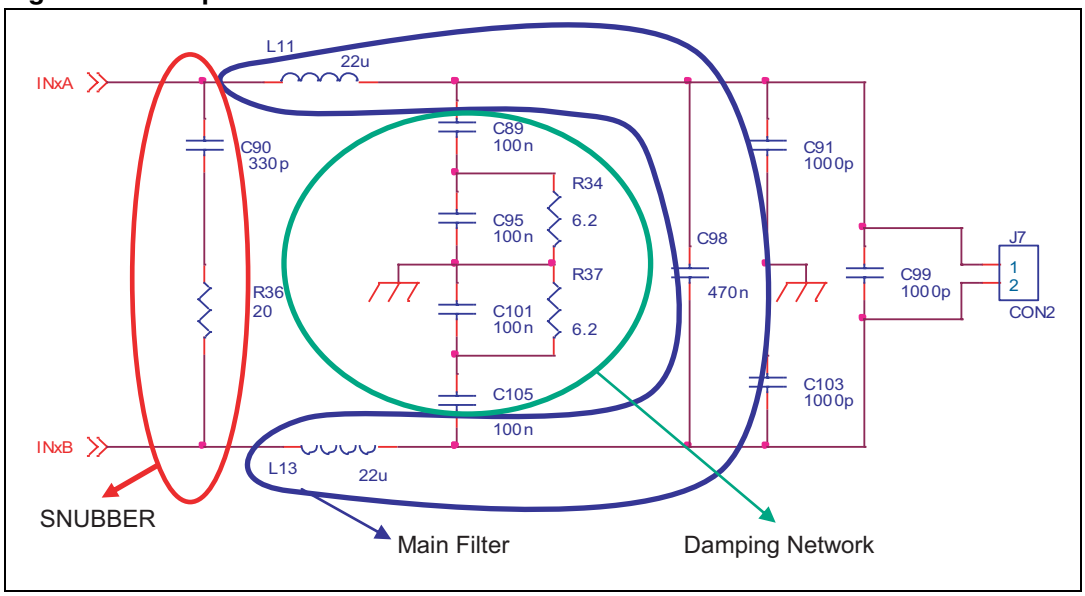
There are two different ways to utilize these as follows:

- The decoupling capacitor(s) can be shared among channels; the "star route" for the PC board layout must be used.
- The decoupling capacitor(s) can be used as one decoupling system per channel; the decoupling capacitor must be placed as close as possible to the IC pins.

3.1.3 Output filter

The IC output circuit contains three filters: a snubber, a damping network, and a main filter.

Figure 8. Output filter



1. The key function of a snubber network is to absorb energy from the reactance in the power circuit. The purpose of the snubber RC network is to avoid unnecessary high pulse energy such as a spike in the power circuit which is dangerous to the system.
2. The purpose of the main filter is to attenuate frequencies higher than the audible range of 20 kHz. The main filter is designed using the Butterworth formula to define the cutoff

frequency, which must be chosen between the upper limit of the audio band (~ 20 kHz) and the carrier frequency (384 kHz), otherwise the frequency response is affected.

3. The purpose of the damping network is to avoid the high-frequency oscillation issue on the output circuit. It can also improve THD and avoid the inductive copper on the PCB route when the system is working in high frequency with PWM or PCM.

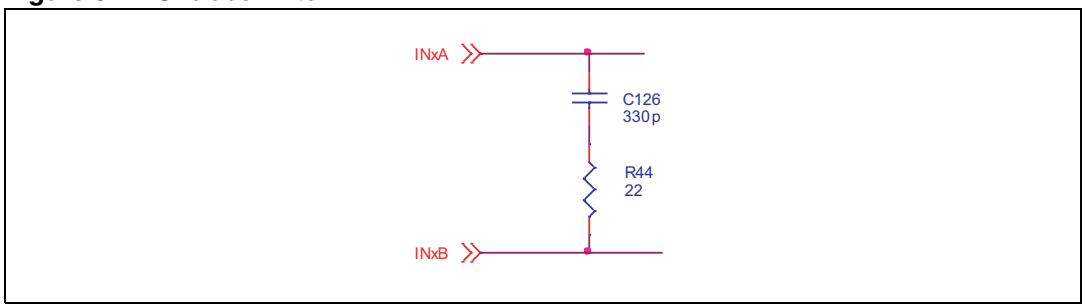
Snubber filter

The snubber circuit must be optimized for the application. Starting values are 330 pF in series to 22 ohm. The power on this network can be defined by the following formula which considers the power supply, frequency and capacitor value:

$P = C * f * (2 * V)^2$

This power is dissipated on the series resistance.

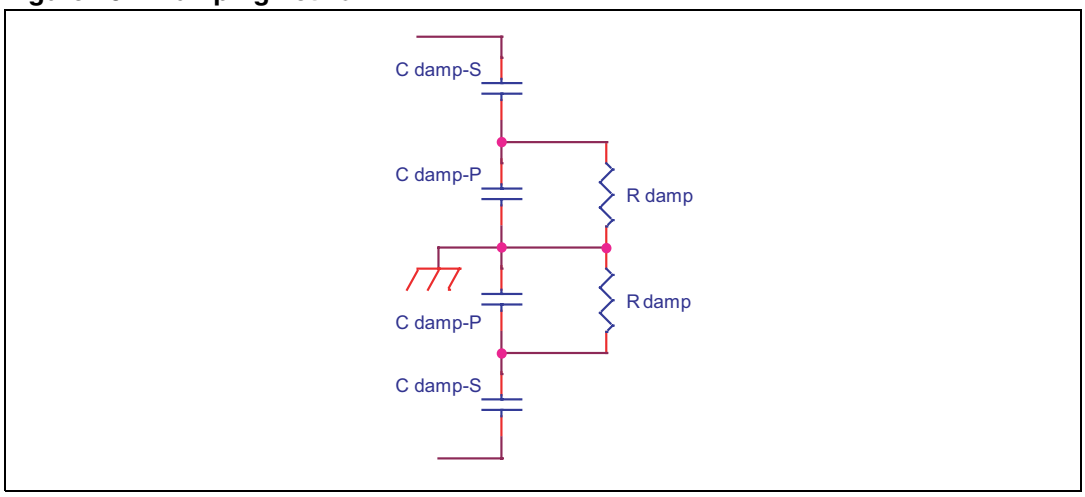
Figure 9. Snubber filter



Damping network

The C-R-C is a damping network and is mainly intended for high inductive loads.

Figure 10. Damping network



Main filter

The main filter is an L-C based Butterworth filter. The cutoff frequency must be chosen between the upper limit of the audio band (~ 20 kHz) and the carrier frequency (384 kHz).

Figure 11. Main filter

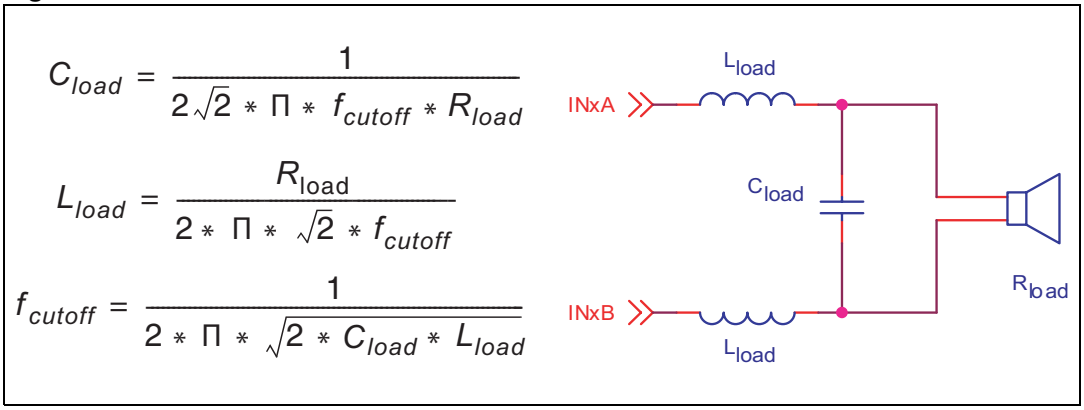
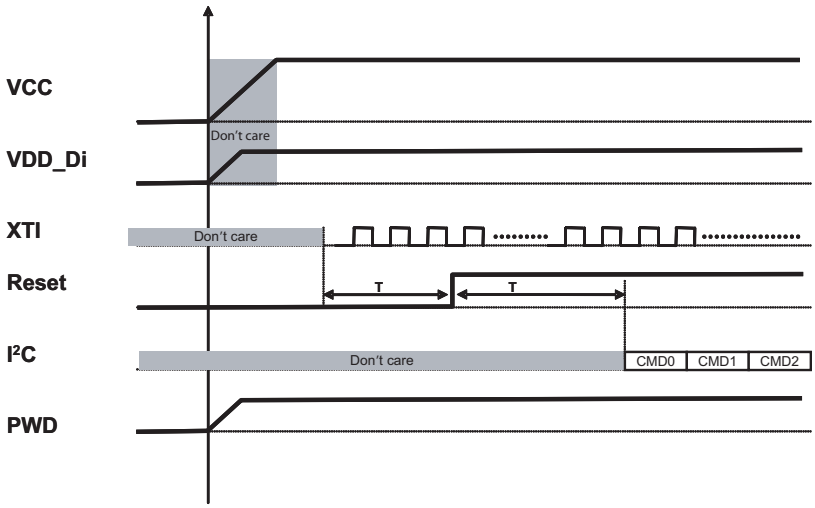


Table 2. Recommended values

Rload	8 ohm	4 ohm
Lload	22 µH	10 µH
Cload	470 nF	1 µF
C damp-S	100 nF	220 nF
C damp-P	220 nF	220 nF
R damp	6.2	2.7

Figure 12. Recommended power-up and power-down sequence



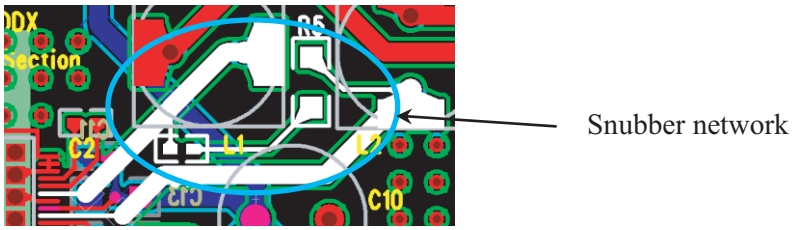
TR = mimimum time between XTI master clock stable and Reset removal: 1 msec
TC = minimum time between Reset removal and I2C program, sequence start: 1msec
Note 1: clock stable means: fmax - fmin < 1 MHz
Note 2: No specific VCC and VDD_Dig turn-on sequence is required

3.2 Layout

This section provides layout recommendations to ensure the optimum performance of the STA333ML.

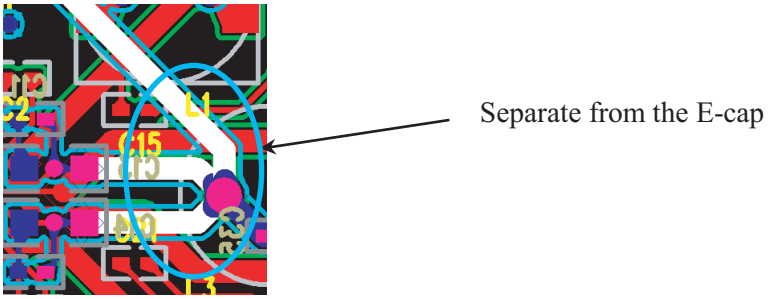
Solder the snubber network as close as possible to the related IC pin.

Figure 13. Snubber network



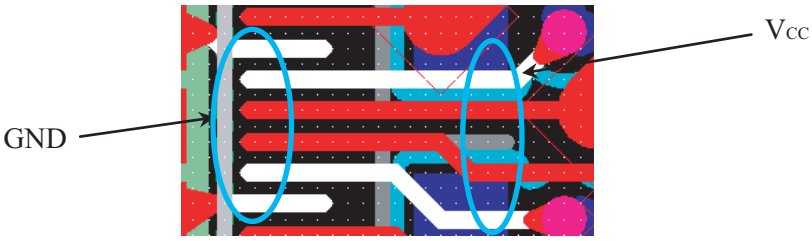
Use an electrolytic capacitor first to separate the V_{CC} branches.

Figure 14. Electrolytic capacitor



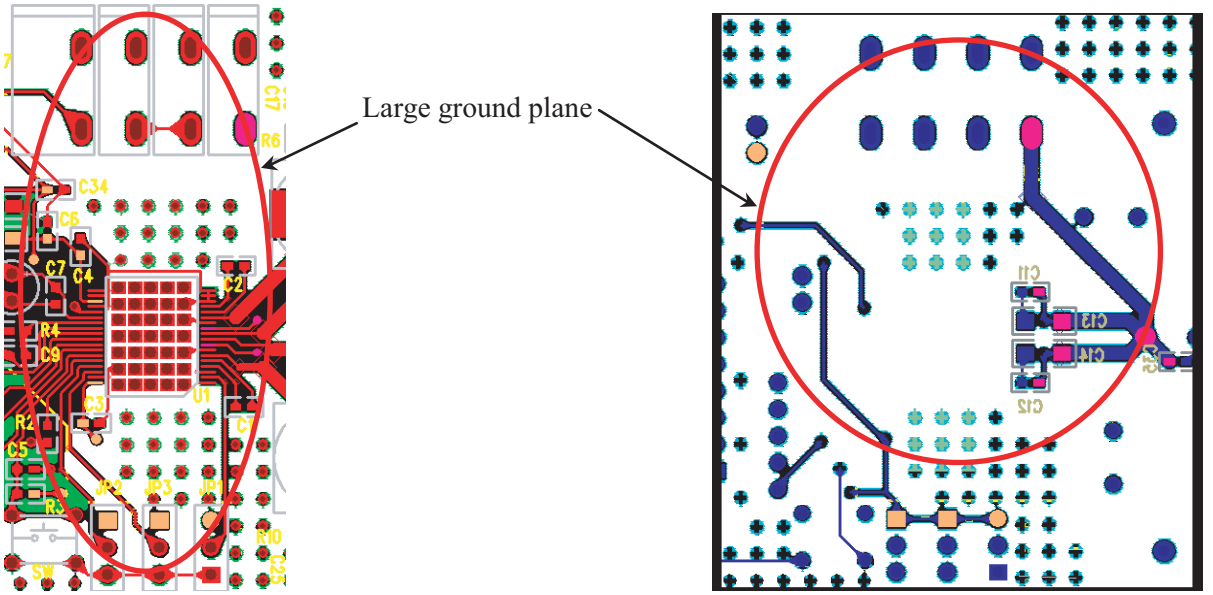
Minimize the path length between the V_{CC} pins and ground pin in order to avoid inductive paths.

Figure 15. Minimized path between V_{CC} and GND



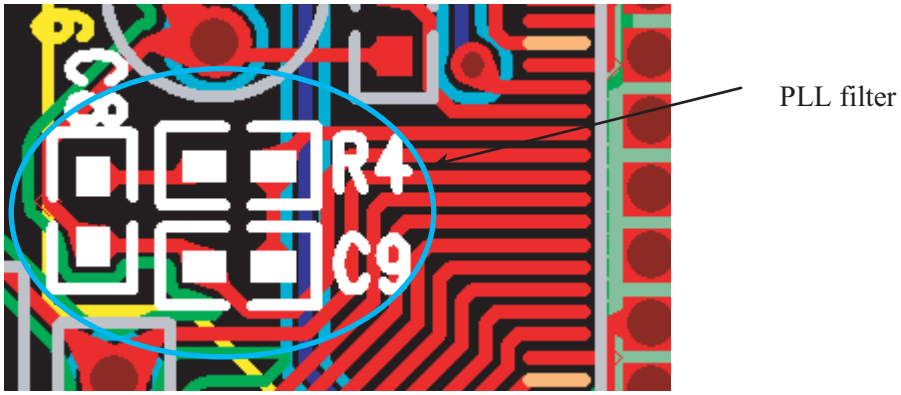
In order to dissipate heat, it is mandatory to have a large ground plane on both layers (top and bottom) and to solder the slug on the PCB.

Figure 16. Dissipating the heat



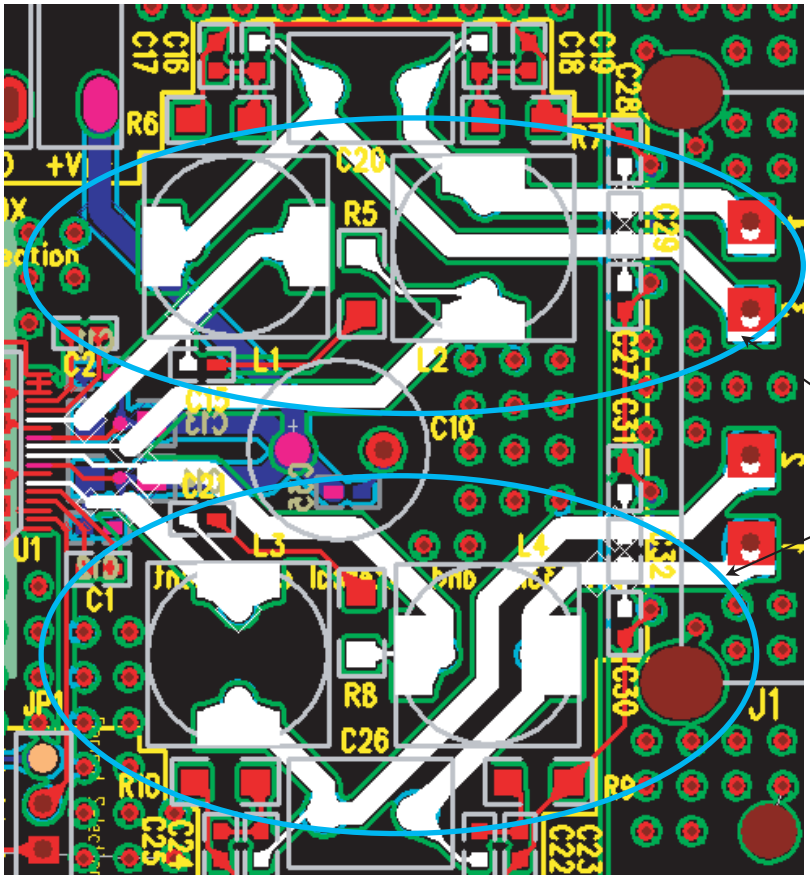
Solder the PLL filter as close as possible to the FILT pin.

Figure 17. PLL filter



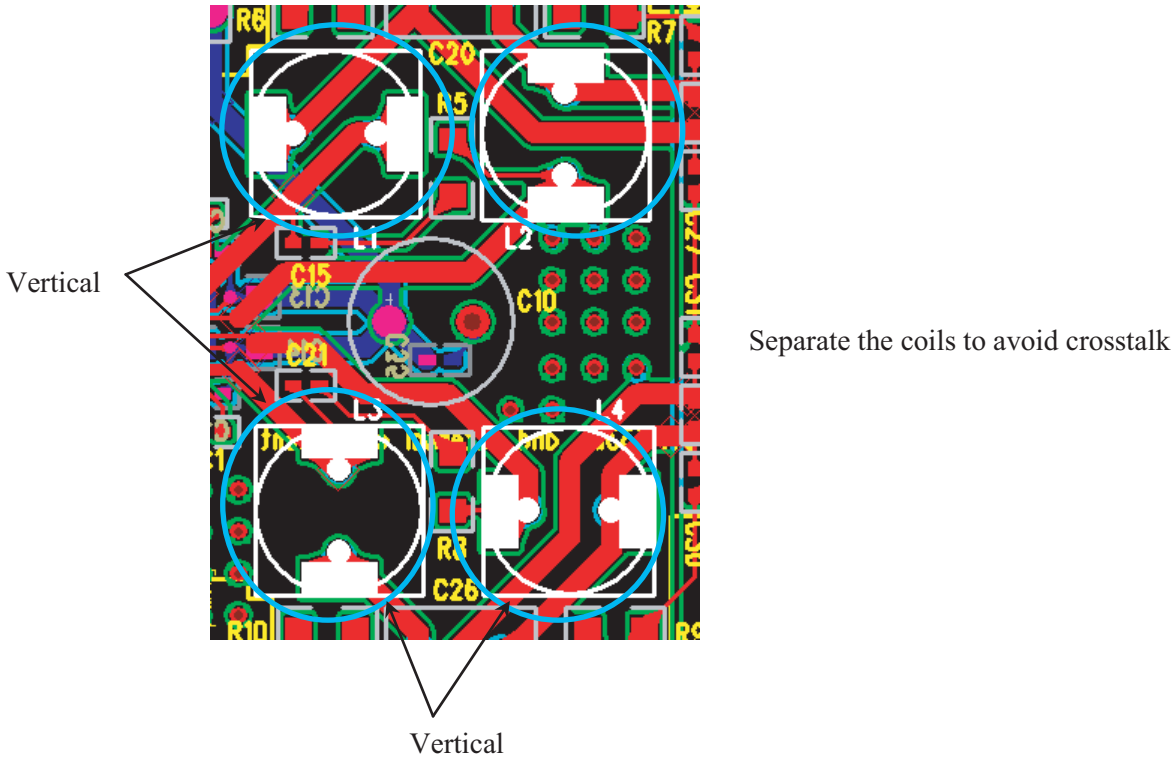
For differential applications, create symmetrical paths for the output stage.

Figure 18. Symmetrical output paths



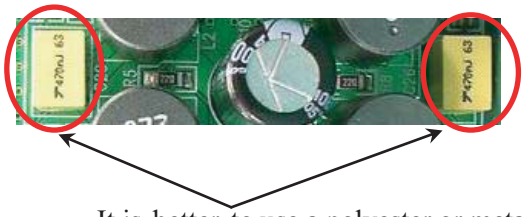
Ensure good separation between adjacent coils and that they have the same orientation (vertical) in order to avoid crosstalk.

Figure 19. Coils



It is better to use a polyester capacitor for the filter capacitors.

Figure 20. Filter capacitors



Consider the ground layout. To avoid interference between power and small signal, grounding for the different ground planes must be separated as shown below.

Figure 21. Ground layout

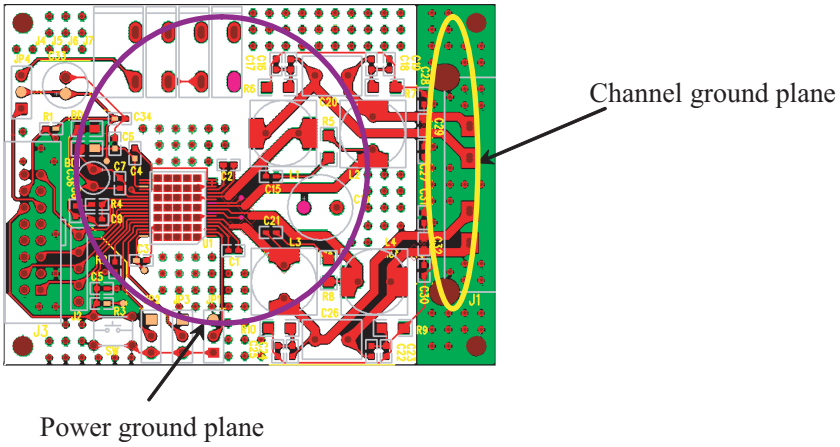
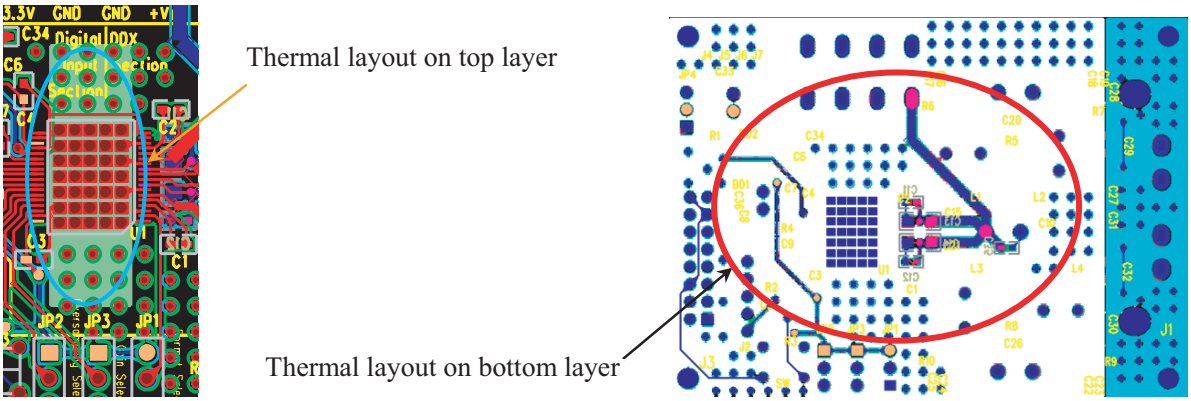
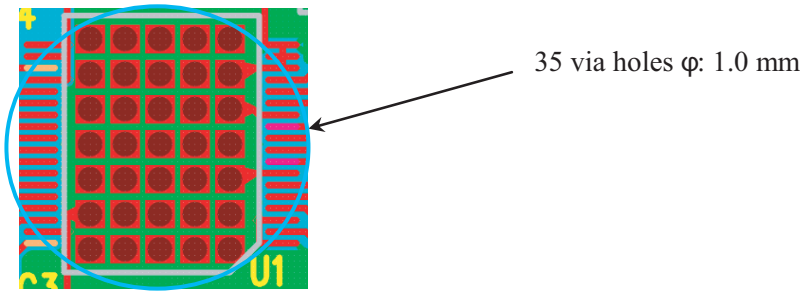


Figure 22. Thermal layout with large ground, top and bottom layers



The thermal resistance junction-to-ambient (at the bottom of the STA333ML) obtainable with a ground copper area of 4 x 4 cm and 35 via holes is shown in *Figure 23*.

Figure 23. Thermal layout with large ground, thermal and soldering holes



A "star route" for Vcc supply is implemented in order to avoid interference between different signals such as when part A is idle and another part B is working with full load, which represent conditions that would cause interference.

Figure 24. V_{CC} star routing

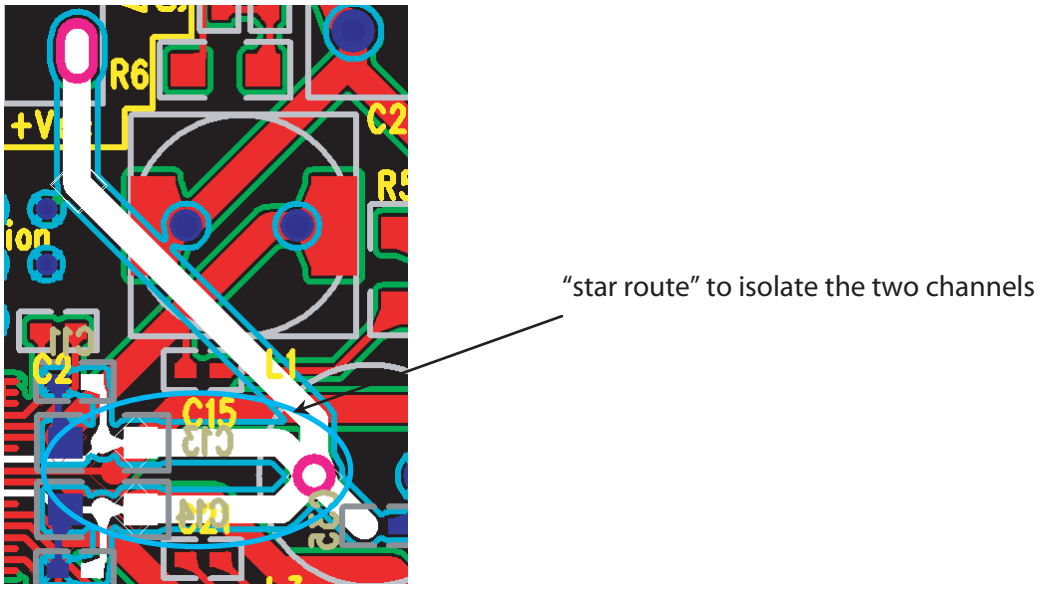
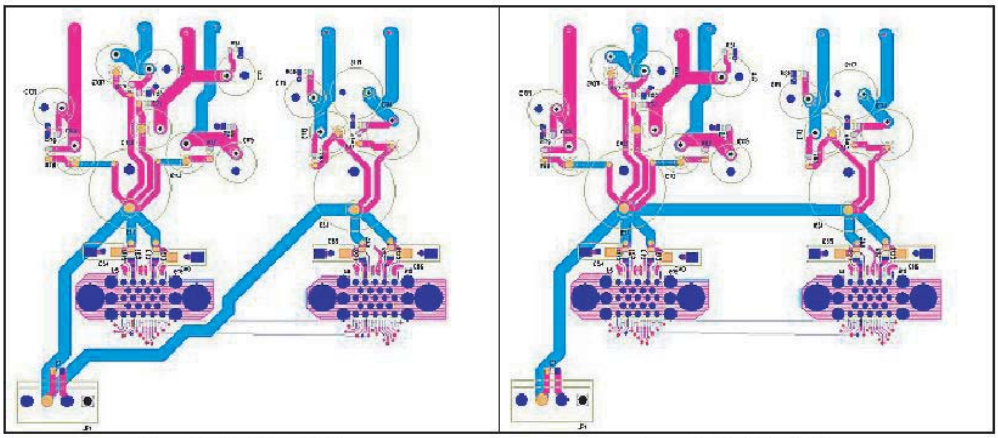
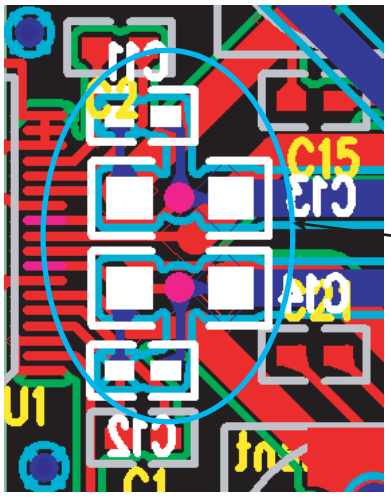


Figure 25. Good and bad examples of V_{CC} routing



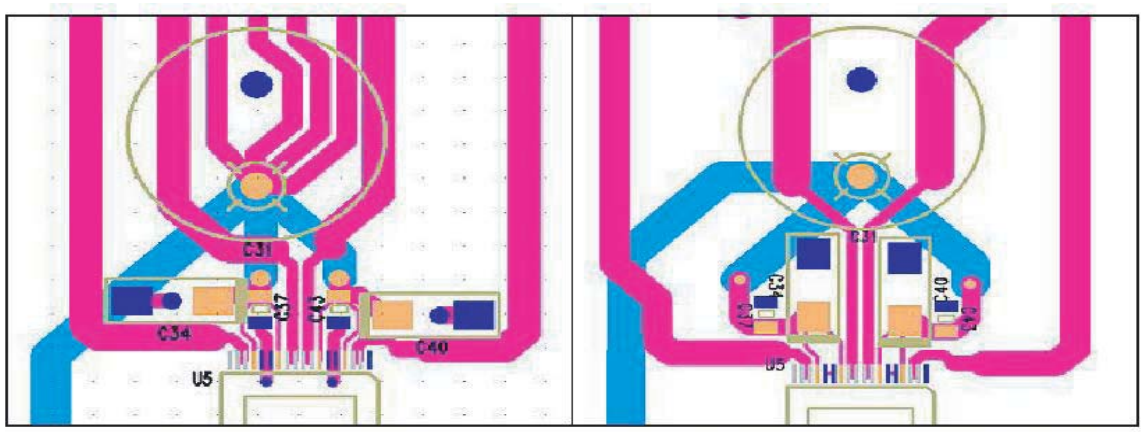
The system is working on PWM with a fast switching frequency of about 340 kHz which causes the long copper wire to behave as a coil. To avoid this we recommend using the ceramic capacitor to balance reactance. The ceramic capacitor must be placed as close as possible, within 5 mm, to the related pins in order to minimize the inductive coil generated by the copper wire.

Figure 26. V_{CC} filter for high frequency



Solder decoupling capacitors as close as possible to their respective IC pins in order to reduce the inductive coil (copper wire).

Figure 27. Good and bad examples of amplifier bypassing



Place snubber filters for high-frequency spike protection on the output circuit.

Figure 28. Snubber filters for high-frequency spikes

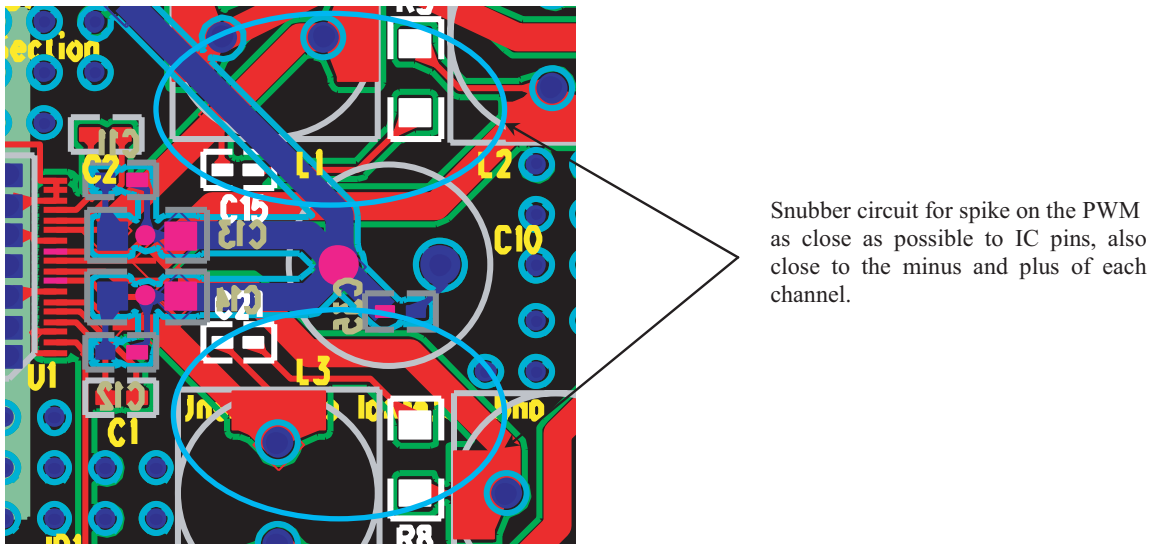


Figure 29. Common-mode and differential snubber placement

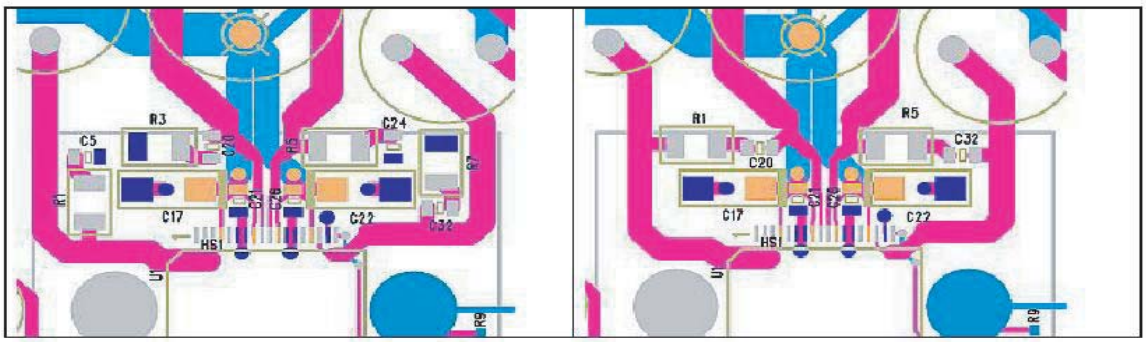


Figure 4: Good Common-Mode Snubber Placement

Figure 5: Good Differential Snubber Placement

A strong spike, which could be sufficient to damage the device, could occur if there is significant distance between the snubber network and the pins. The recommended distance between the snubber network and the IC pins is within 3 mm, which takes into consideration the width of the copper wire.

Figure 30. Good output routing

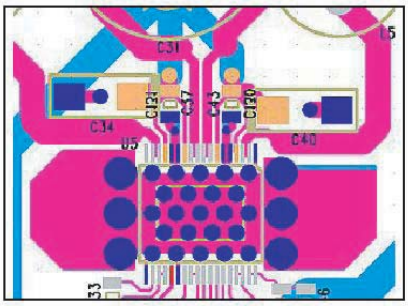
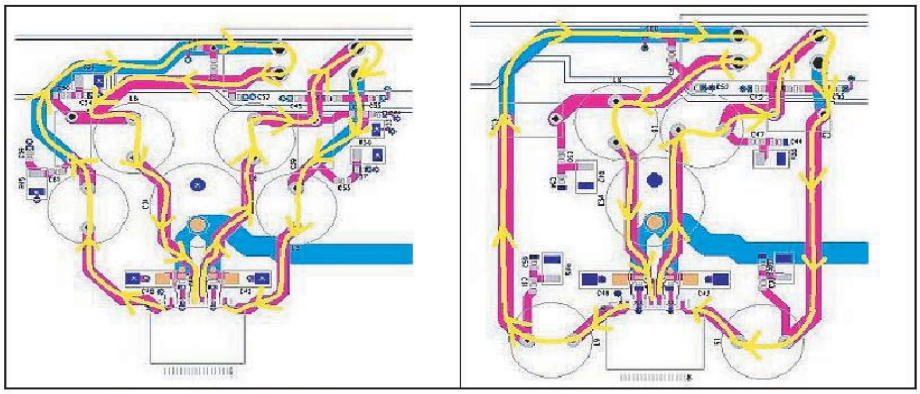


Figure 9: Good Output Routing – Traces grow wider as space allows

Figure 31. Good and bad examples of output routing

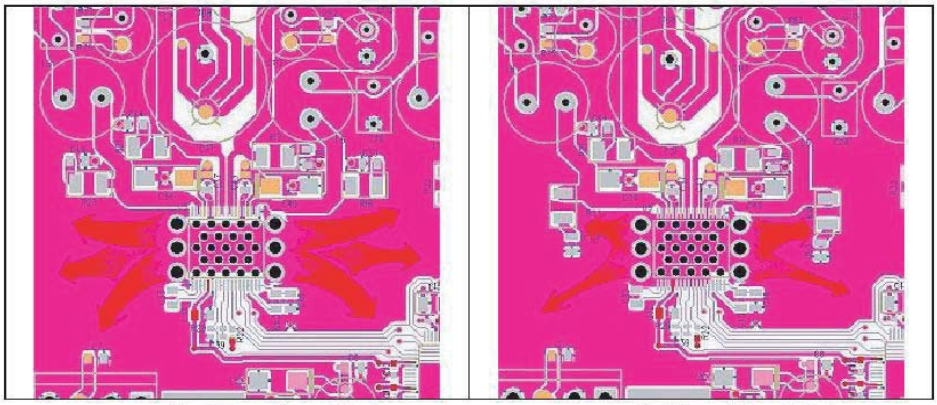


Good Output Routing - Area between outputs is small

Bad Output Routing - Area between outputs is large

Please note that the thermal pad must be connected to ground in order to properly set the IC references. The heat must be able to flow freely to the sides of the IC, not only to the top, but also to the bottom of the board. In order to optimize the heat transfer, it is recommended to use via holes to connect the ground planes.

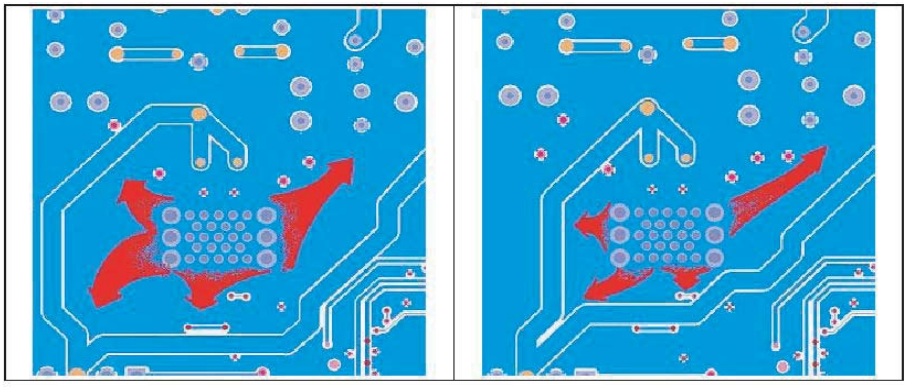
Figure 32. Examples of good and bad thermal layout - top layer



Good Thermal Layout (Top) – Heat can flow freely to the sides

Bad Thermal Layout (Top) – Heat flow is cut off by the snubbers

Figure 33. Examples of good and bad thermal layout - bottom layer



Good Thermal Layout (Bottom) – Plenty of copper area

Bad Thermal Layout (Bottom) – Little copper area on three sides

4 Revision history

Table 3. Document revision history

Date	Revision	Changes
06-Dec-2006	1	Initial release.
29-Nov-2012	2	Document rewritten; removed Section 3: Test curve report.