AN2481
Application note

STA333W demo board application note

Introduction

The purpose in this document is:

- to describe how to connect the AN2481 demo board,
- how to evaluate the demo board performance with electrical curve data,
- how to avoid critical board and layout issues.

Application note can be configured for 2.0 channels of ternary. It is a total solution for the digital audio power amplifier in a TV and portable application.

Note: All the test items and graph data in this document are measured by Audio Precision equipment.

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1 Test conditions and connection of demo board

1.1 Test conditions

1.1.1 Power supply and interface connections

1. Connect positive voltage of 12 V DC power supply to +Vcc pin and negative to GND.
2. Connect positive voltage of 3.3 V DC power supply to +3.3 V pin and negative to GND.
3. Connect GUI LPT interface board to the J1 connector of AN2481 demo board.
4. Connect the S/PDIF signal cable to the RCA jack on the interface board, the other side connecting to the signal source such as Audio precision or DVD player.
5. The voltage range of the DC power supply for Vcc is from 5 V to 18 V.

1.1.2 Output configuration

STA333ML demo board can be configured in the ternary state for 2.0 channels.

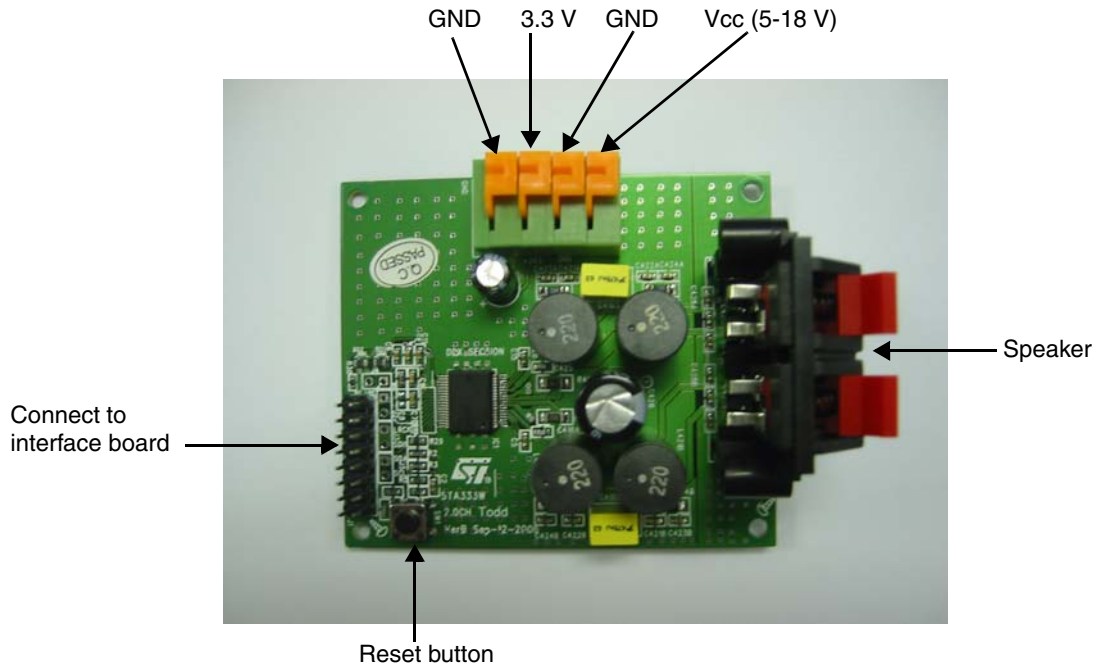
1.2 Equipment requirement

- Audio Precision (System 2700) by AP Co., USA
- DC power supply (5 V to 18 V)
- Digital oscilloscope (TDS3034B) by Tektronix
- PC (with AN2481 GUI control software installed)

1.3 Connection method

Top view of demo board.

Figure 1. Block diagram



1.3.1 Schematic

Figure 2. Schematic diagram

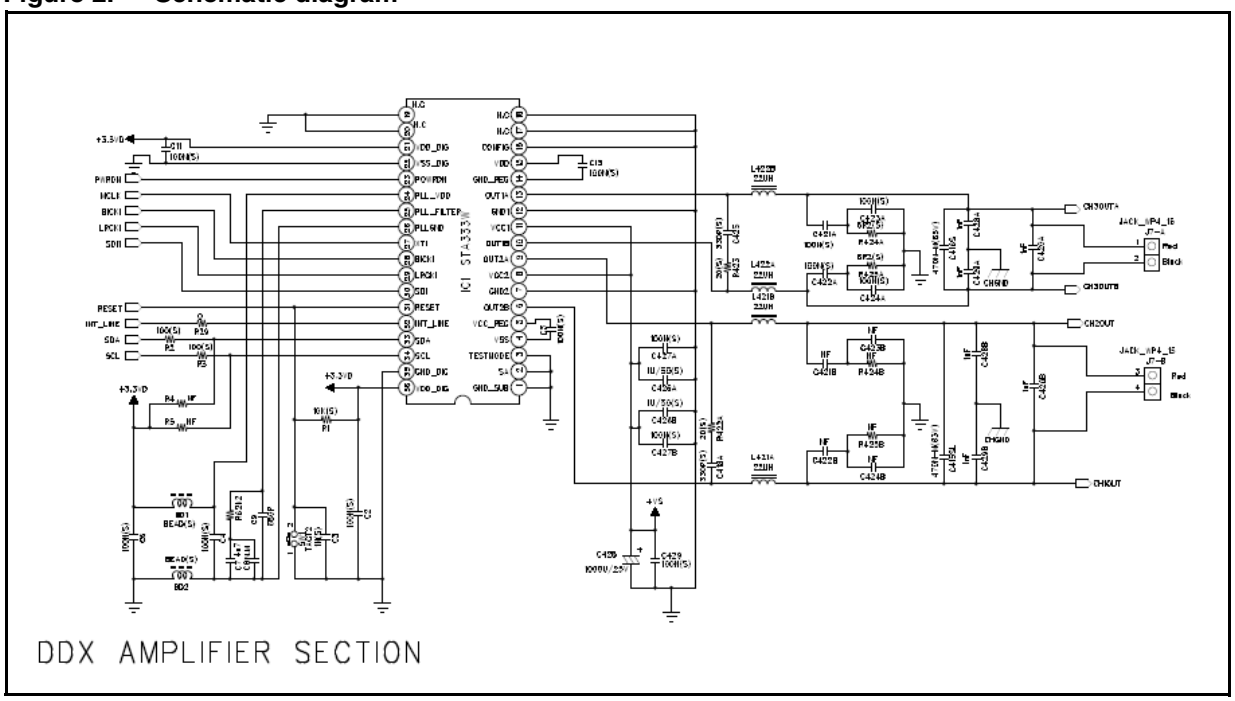
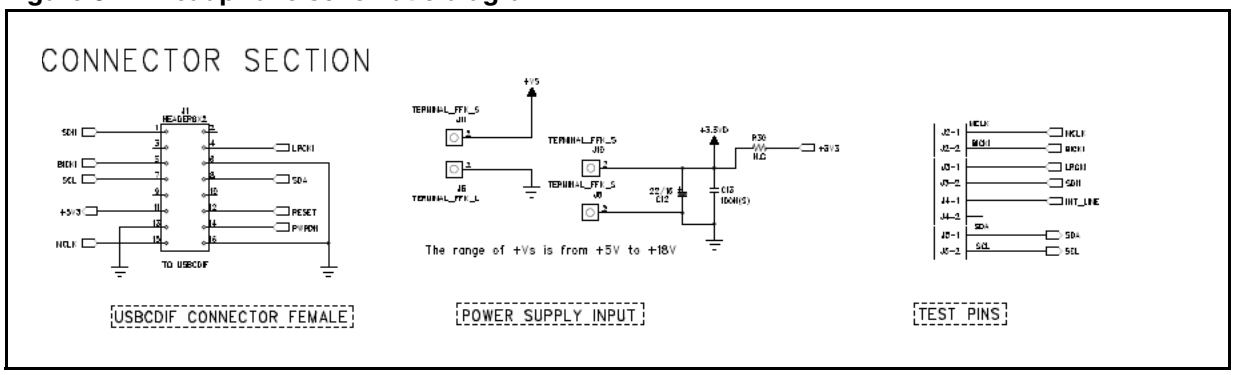


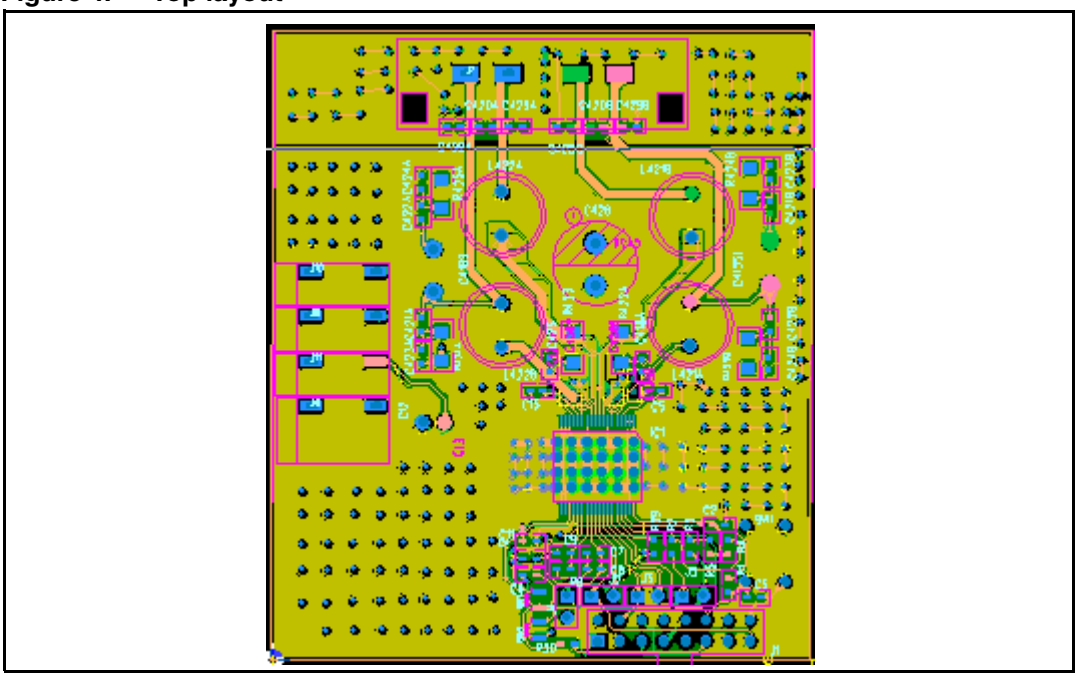
Figure 3. Headphone schematic diagram



1.4 PCB Layout

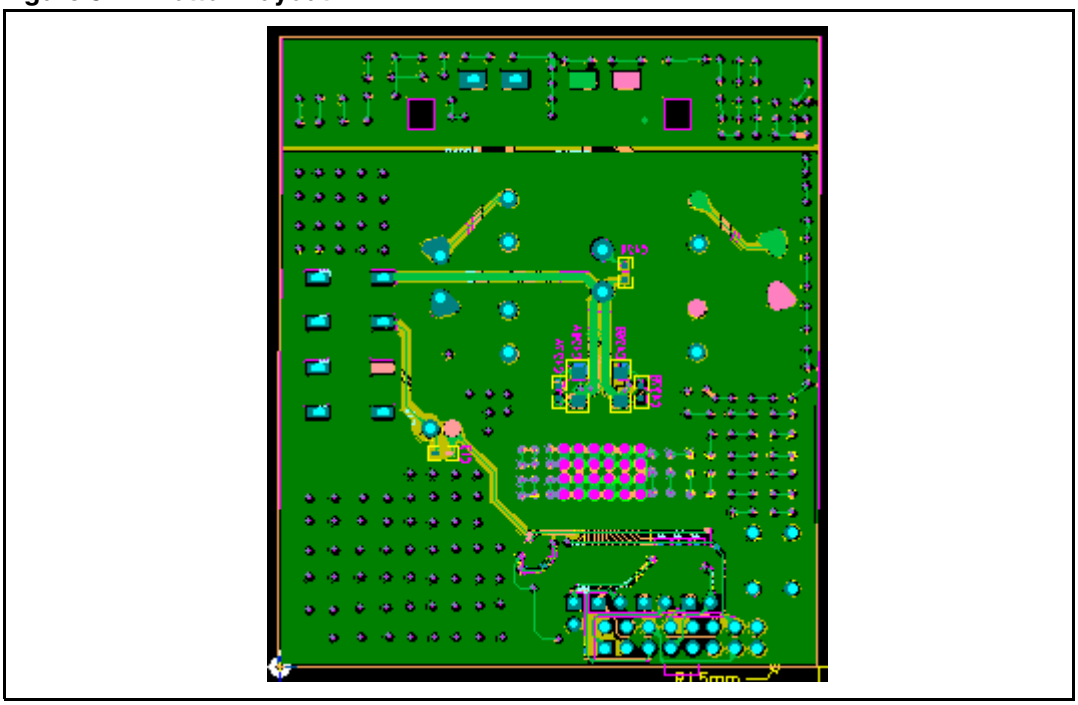
1.4.1 Top view of PCB layout

Figure 4. Top layout



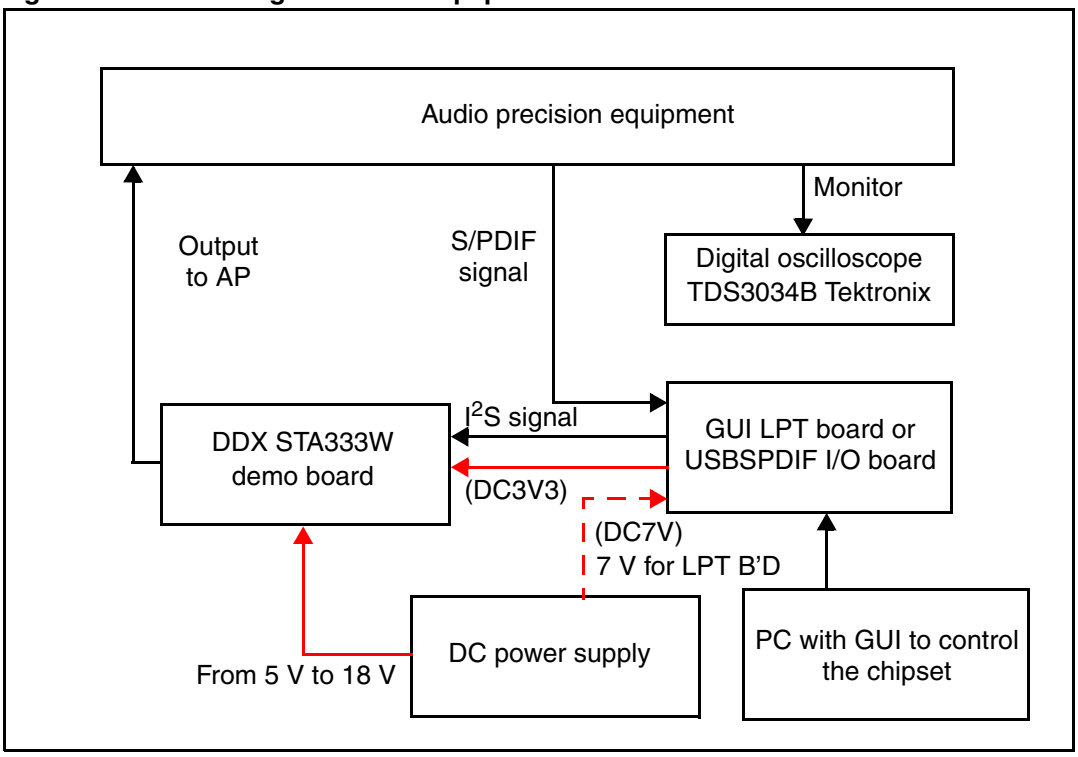
1.4.2 Bottom view of PCB layout

Figure 5. Bottom layout



1.4.3 Test connection

Figure 6. Block diagram of test equipment



2 Electrical characteristics

Table 1. Electrical characteristics(1)

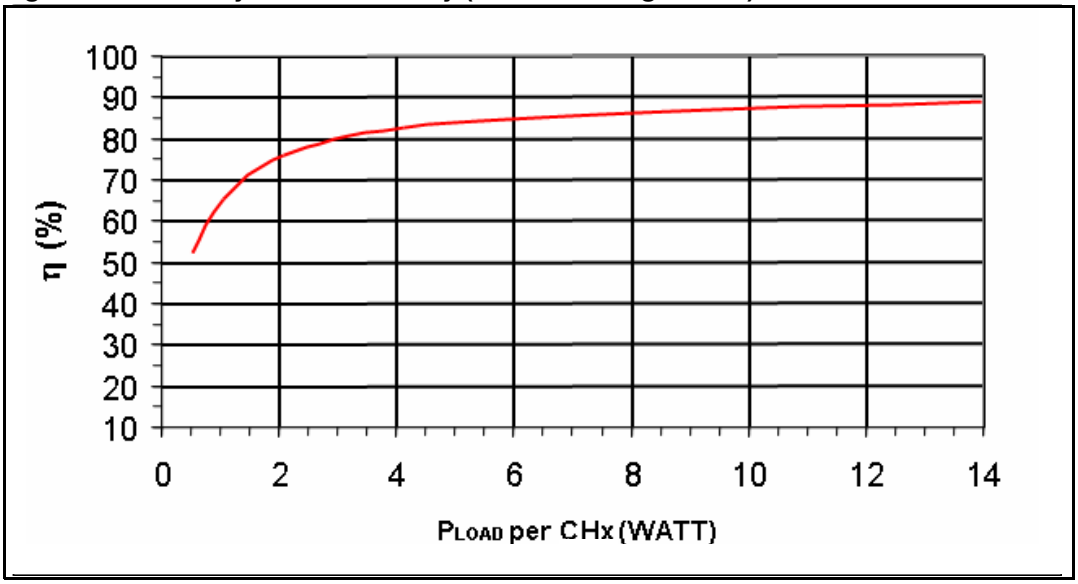
Parameter	Configuration	Test condition	Unit
PSRR (50 Hz - 120 Hz)	BTL configuration	Please refer to measurements section	65 dB
Min SNR	BTL configuration	1 W output, -20 dBFs input, 1 KHz	100 dB
Max modulation index	DDX modulation mode		98.5%
Vcc current (18 V)	BTL configuration	Operating Quiescent Standby/sleep	40 mA 30 mA 0 mA

1. Refer to the STA333W demo board circuit. Vs= +18 V, Tamb = 25.5 °C, f = 1 KHz, Ref = 1 W unless otherwise specified.

Note: THD works better with high impedance loading (based on a fixed value of R_{dsON}).

3 Test curve report

Figure 7. Ternary mode efficiency (2.0 BTL configuration)



Condition: R_{LOAD} =8 ohm; VCC=18 V

3.1 BTL configuration

Figure 8. Output power versus supply voltage

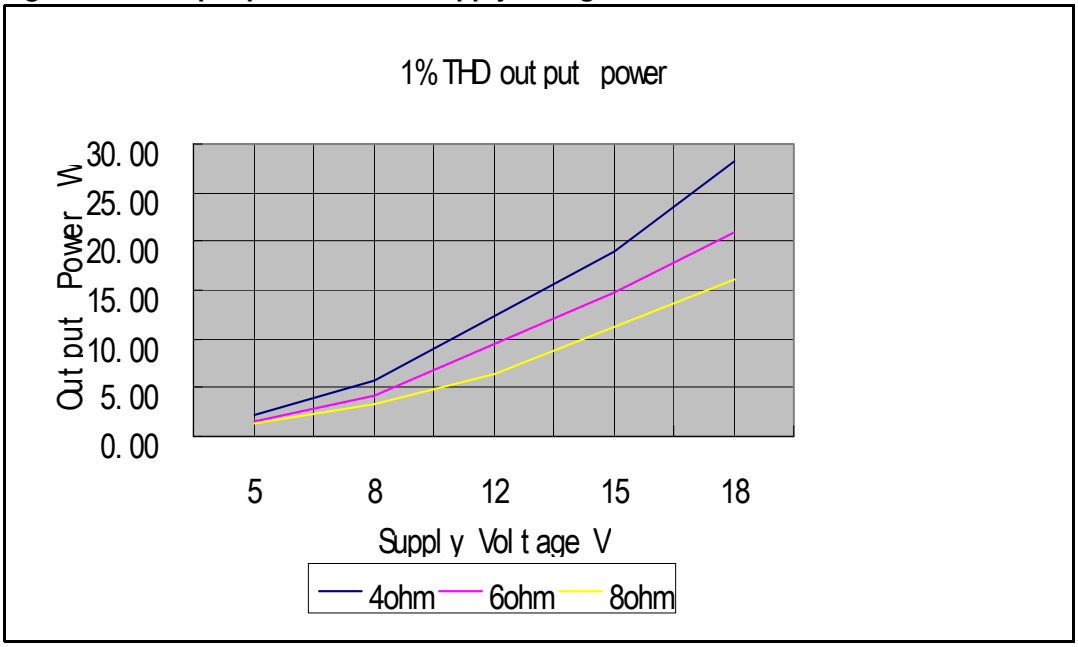


Figure 9. Channel separation 5 V 1 W 4 ohm

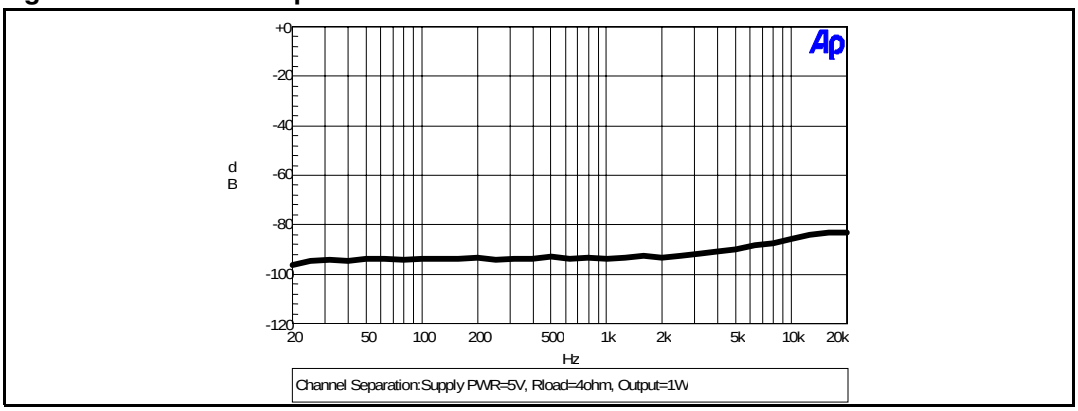


Figure 10. Channel separation 5 V 1 W 6 ohm

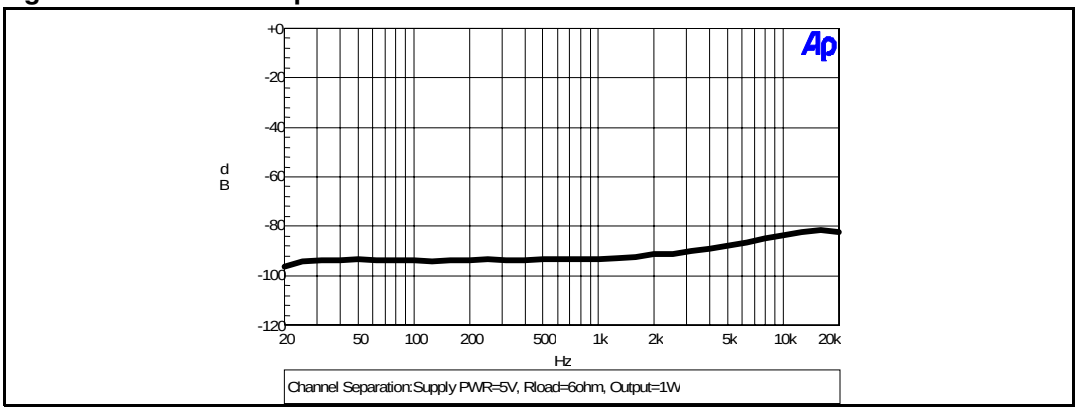


Figure 11. Channel separation 5 V 1 W 8 ohm

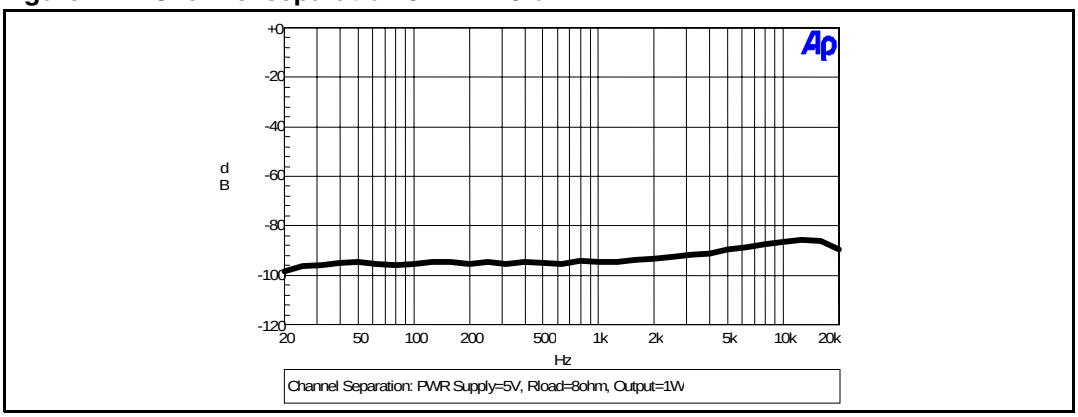


Figure 12. FFT 0 dBFs 1 KHz 5 V 4 ohm

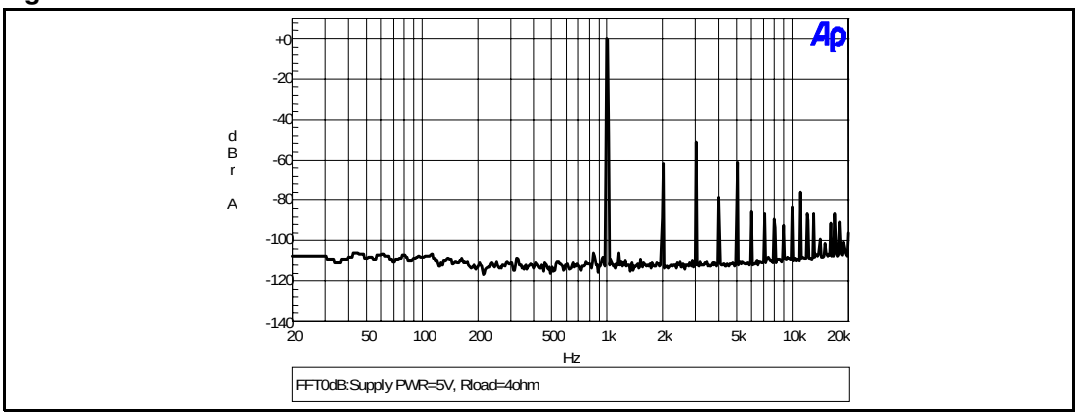


Figure 13. FFT -60 dBFs 1 KHz 5 V 4 ohm

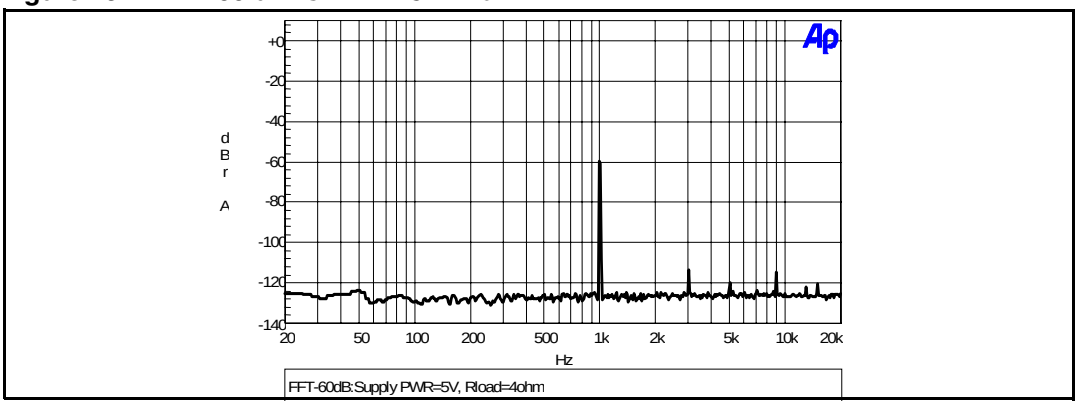


Figure 14. FFT 0 dBFs 1 KHz 5 V 6 ohm

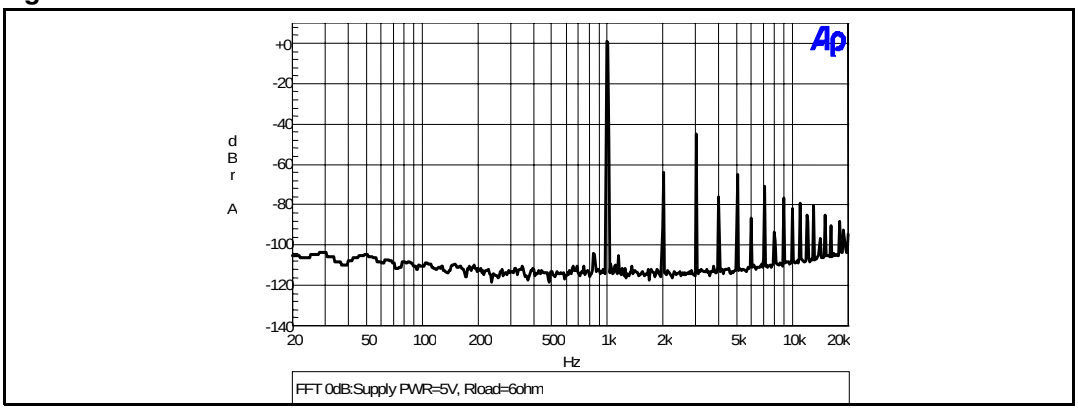


Figure 15. FFT -60 dBFs 1 KHz 5 V 6 ohm

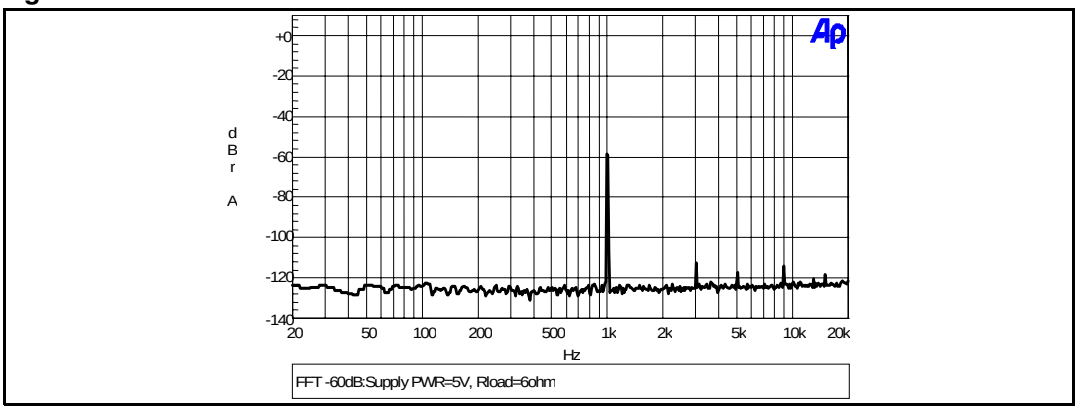


Figure 16. FFT 0 dBFs 1 KHz 5 V 8 ohm

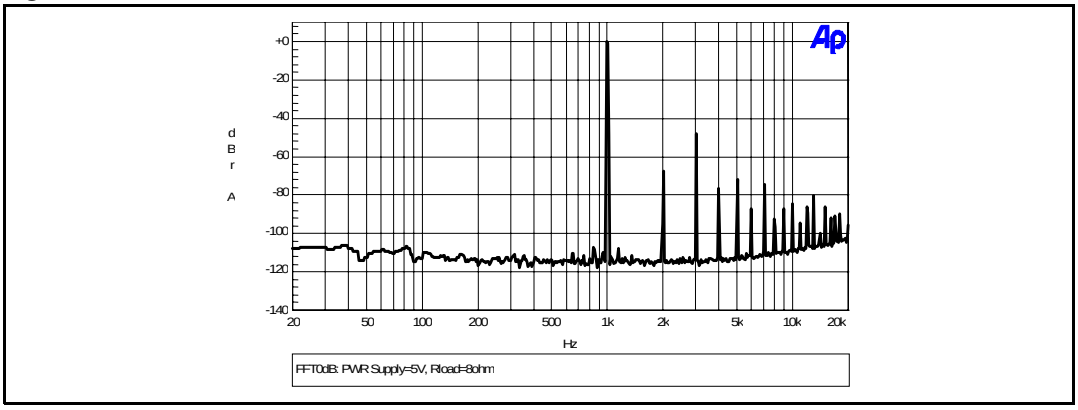


Figure 17. FFT -60 dBFs 1 KHz 5 V 8 ohm

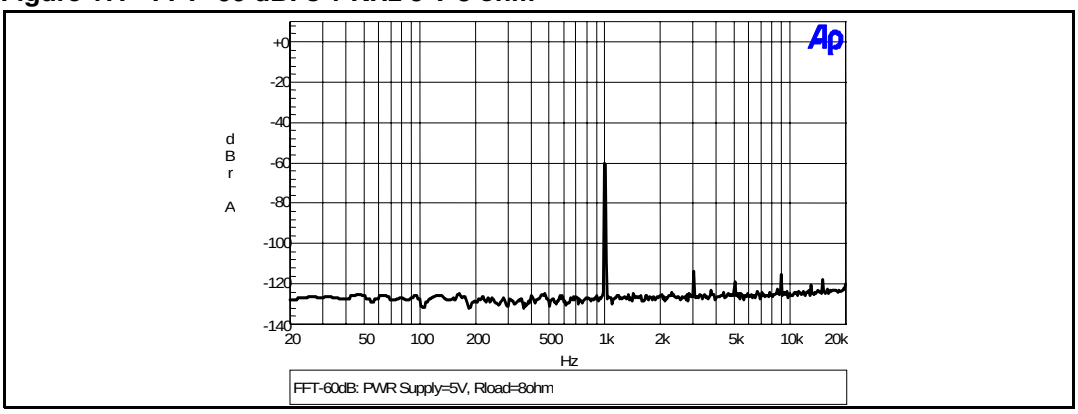


Figure 18. THD + N versus Freq. 5 V Vcc 4 ohm

Figure 19. THD + N versus Freq. 5 V Vcc 6 ohm

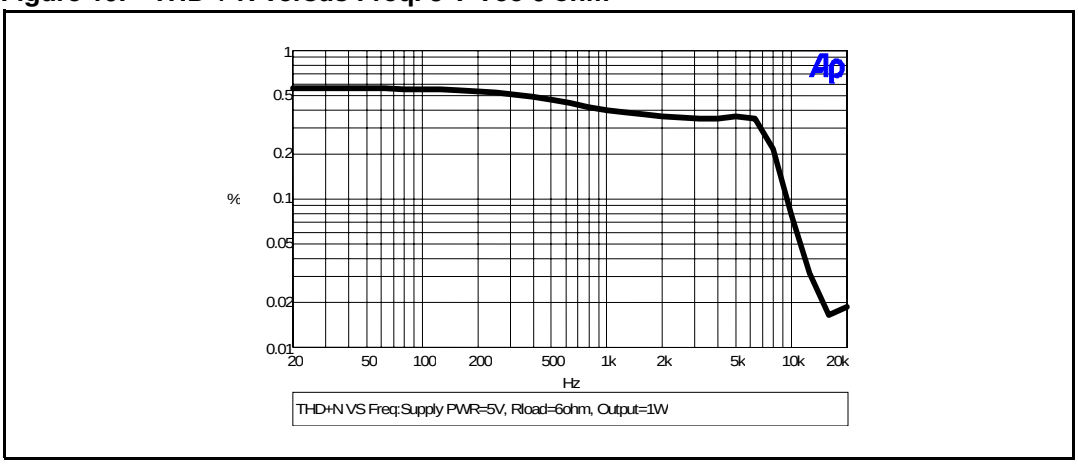


Figure 20. THD + N versus Freq. 5 V Vcc 8 ohm

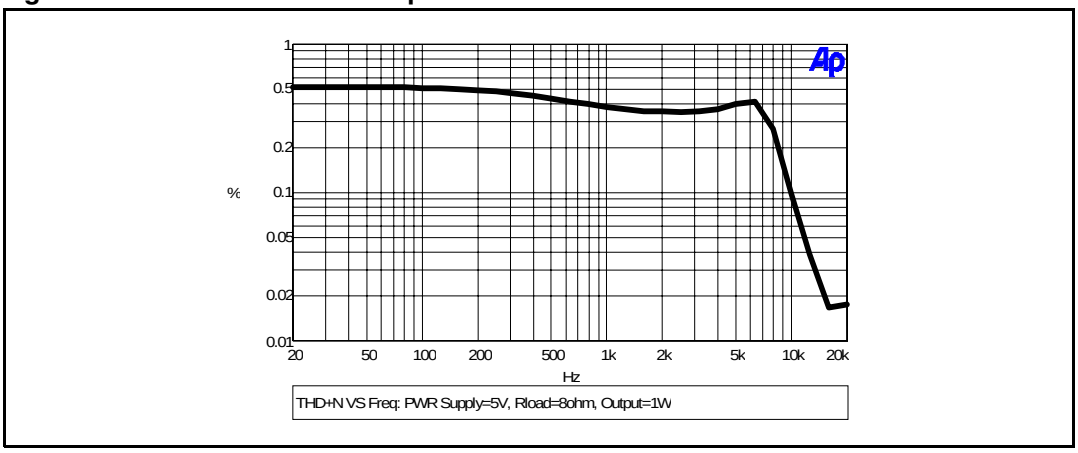


Figure 21. Channel separation 12 V 1 W 4 ohm)

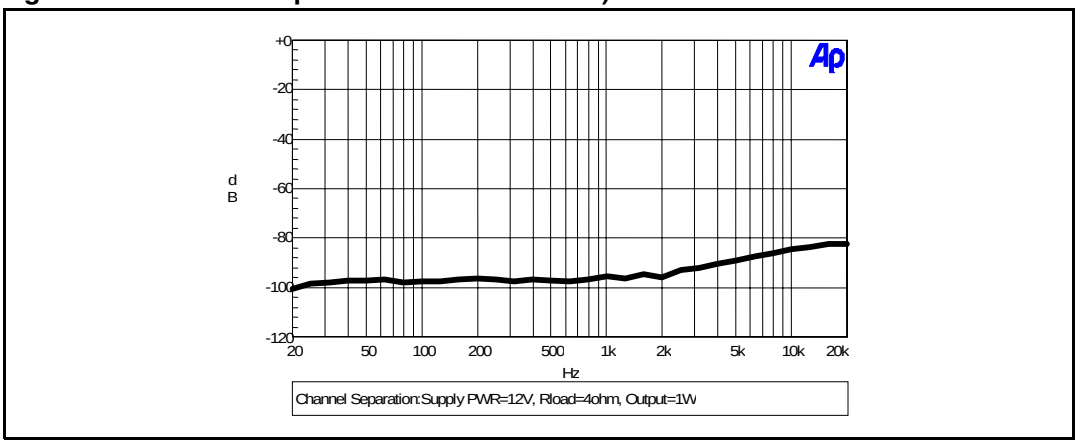


Figure 22. Channel separation 12 V 1 W 6 ohm)

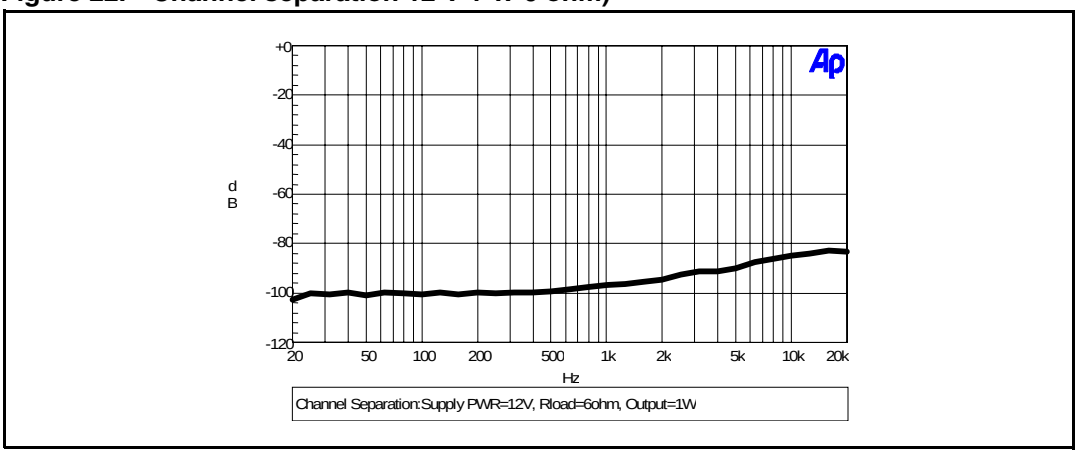


Figure 23. Channel separation 12 V 1 W 8 ohm)

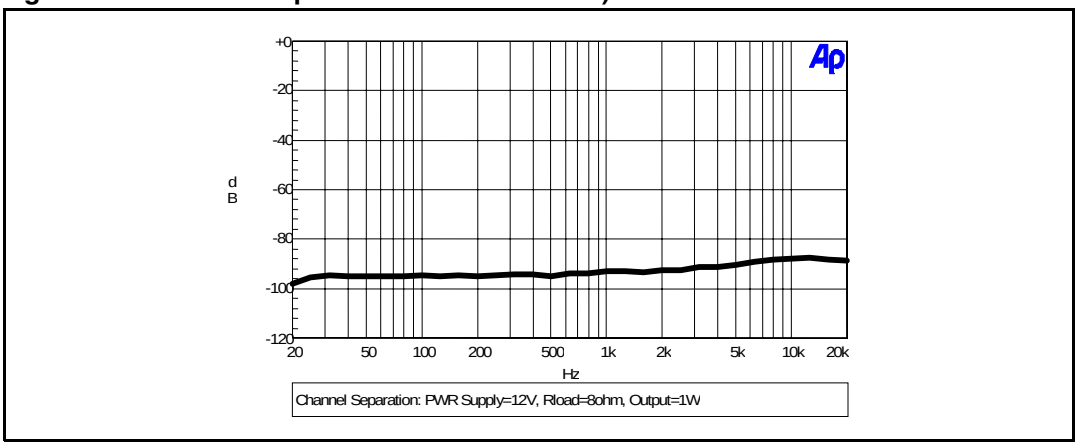


Figure 24. FFT 0 dBFs 1 KHz 12 V 4 ohm

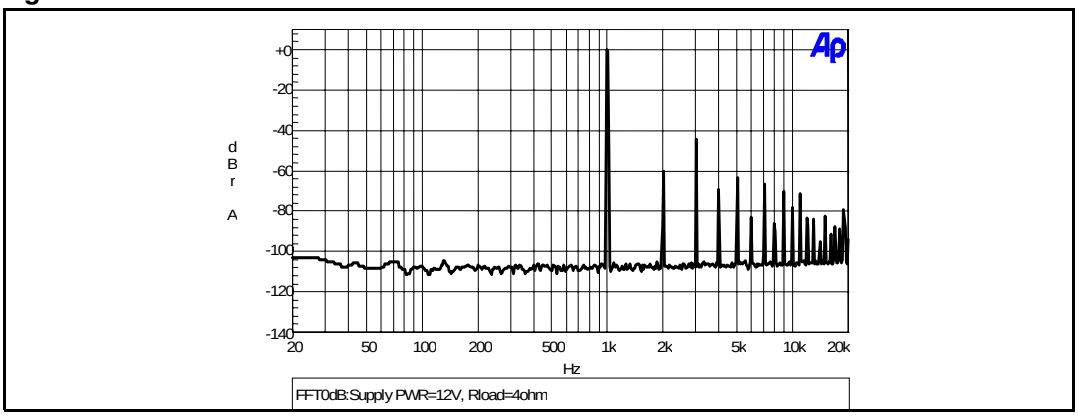


Figure 25. FFT -60 dBFs 1 KHz 12 V 4 ohm

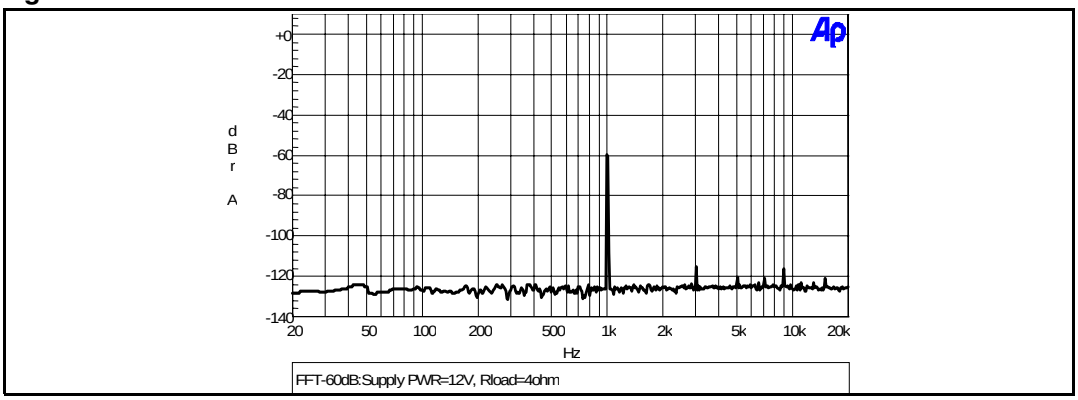


Figure 26. FFT 0 dBFs 1 KHz 12 V 6 ohm

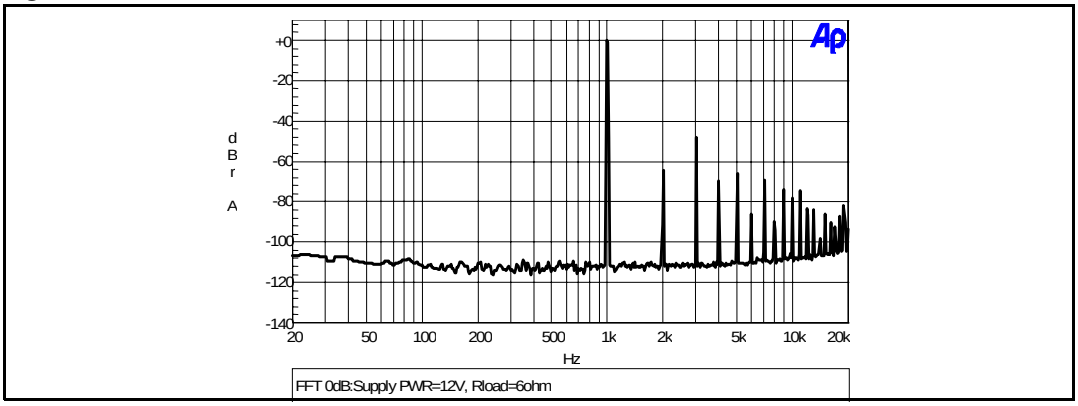


Figure 27. FFT -60 dBFs 1 KHz 12 V 6 ohm

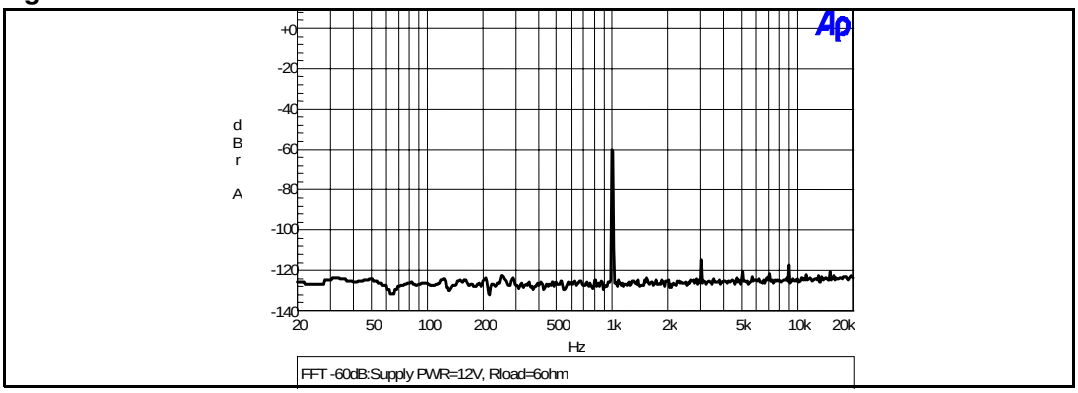


Figure 28. FFT 0 dBFs 1 KHz 12 V 8 ohm

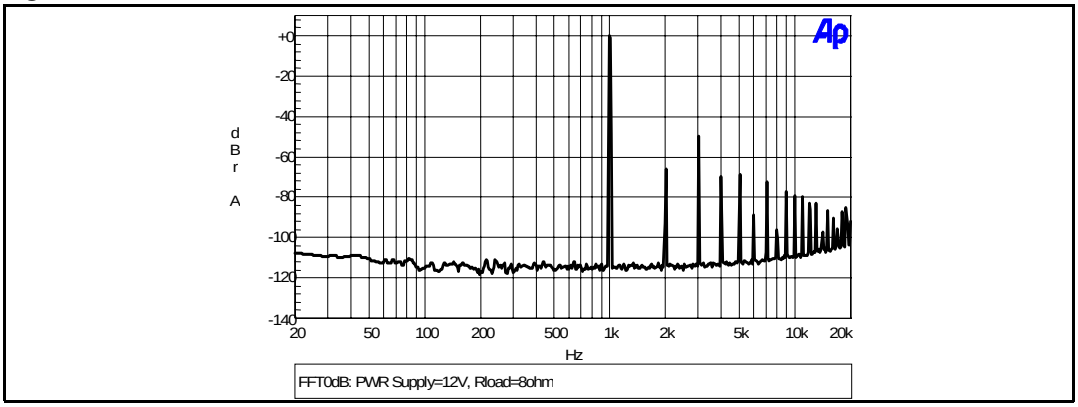


Figure 29. FFT -60 dBFs 1 KHz 12 V 8 ohm

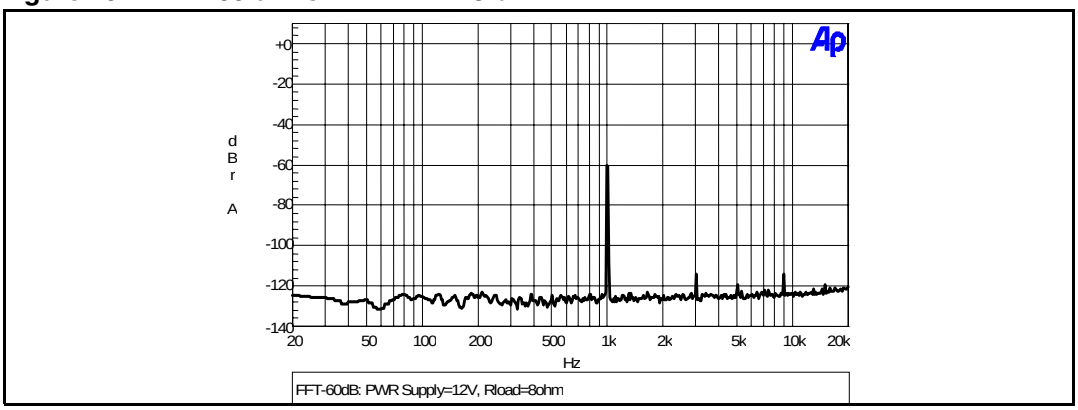


Figure 30. THD versus Freq 12 V Vcc 4 ohm

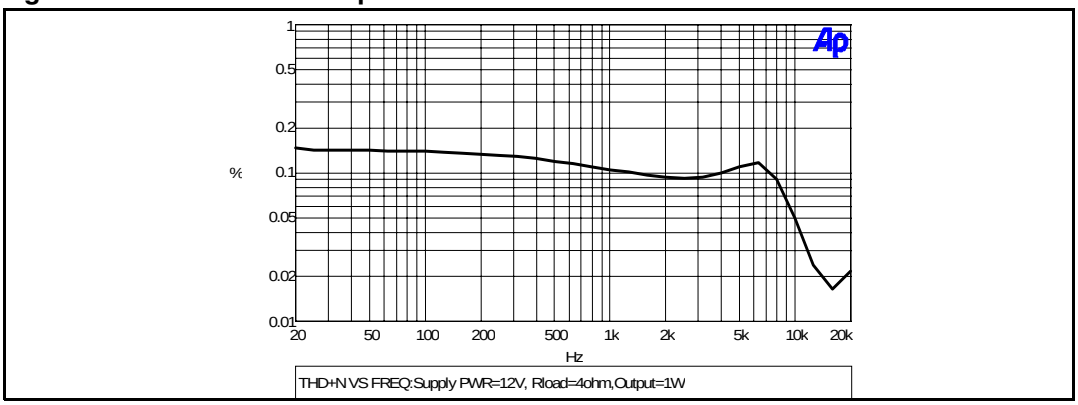


Figure 31. THD+N versus Freq 12 V 6 ohm

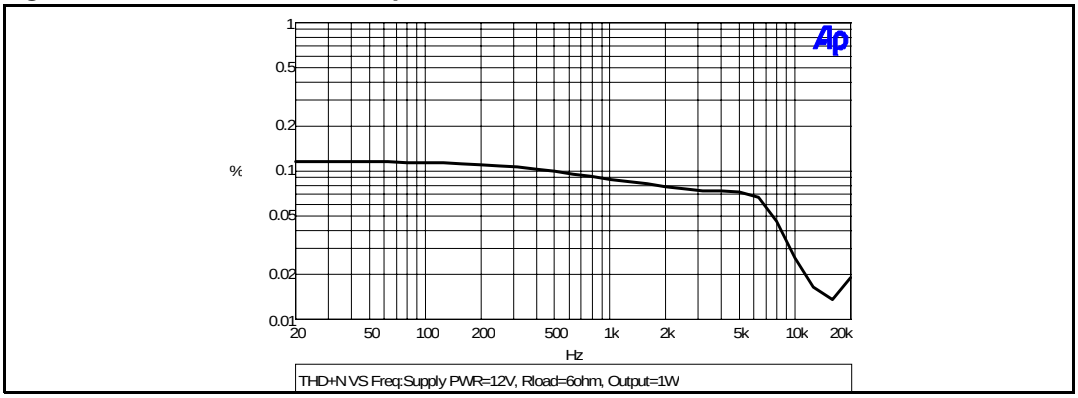


Figure 32. THD+N versus Freq 12 V 8 ohm

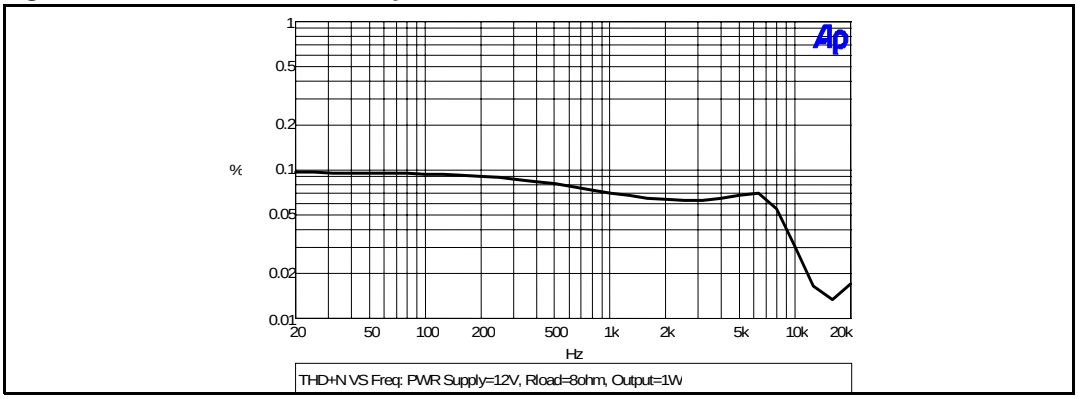


Figure 33. Channel separation 18 V 1 W 4 ohm

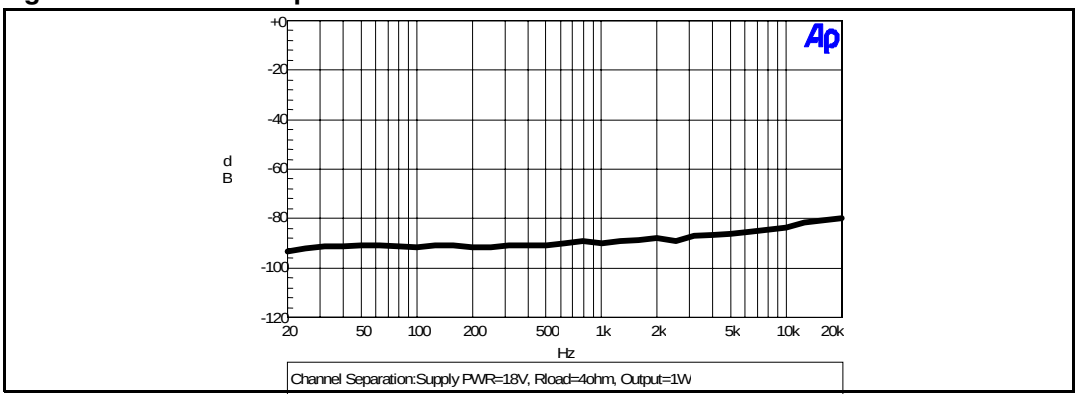


Figure 34. Channel separation 18 V 1 W 6 ohm

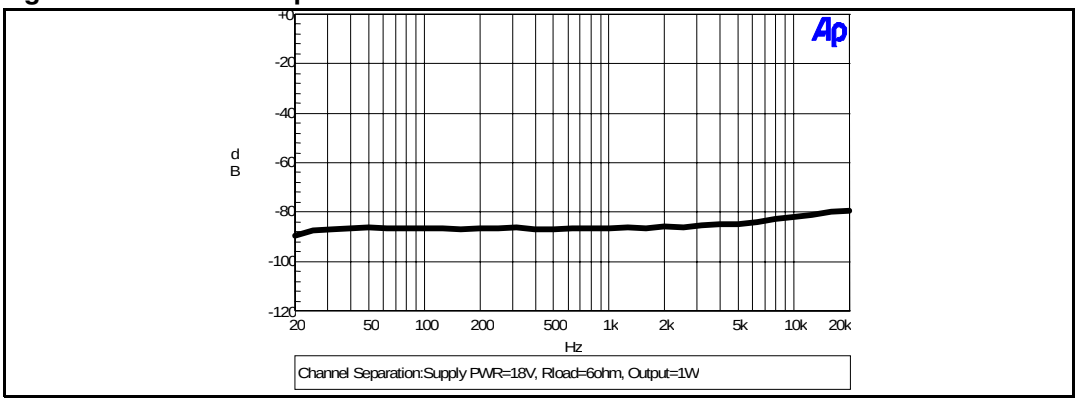


Figure 35. Channel separation 18 V 1 W 8 ohm

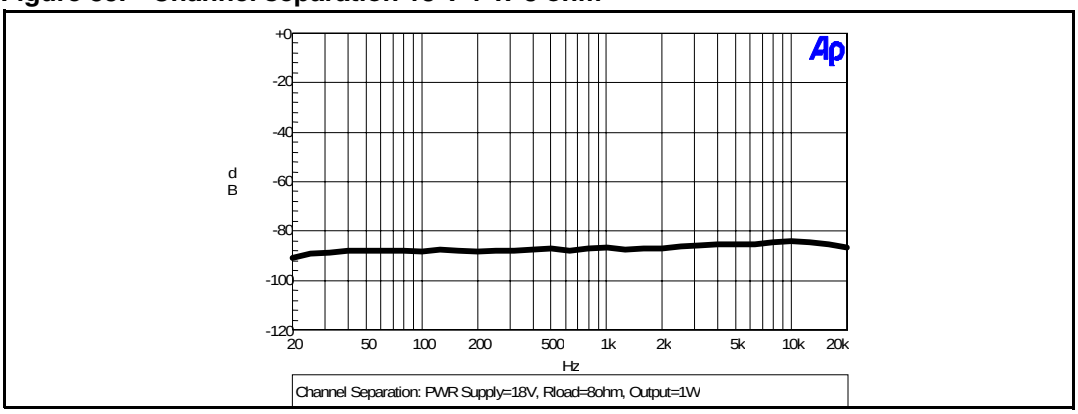


Figure 36. FFT 0 dBFs 1 KHz 18 V 4 ohm

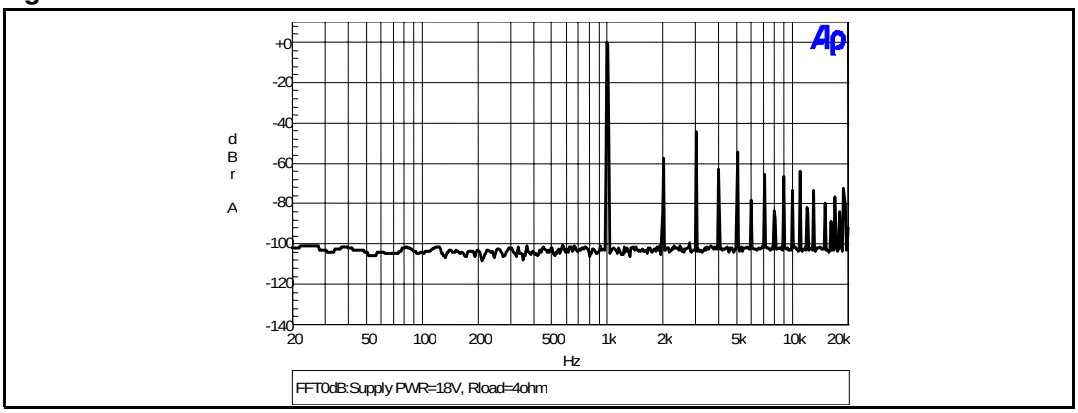


Figure 37. FFT -60 dBFs 1 KHz 18 V 4 ohm

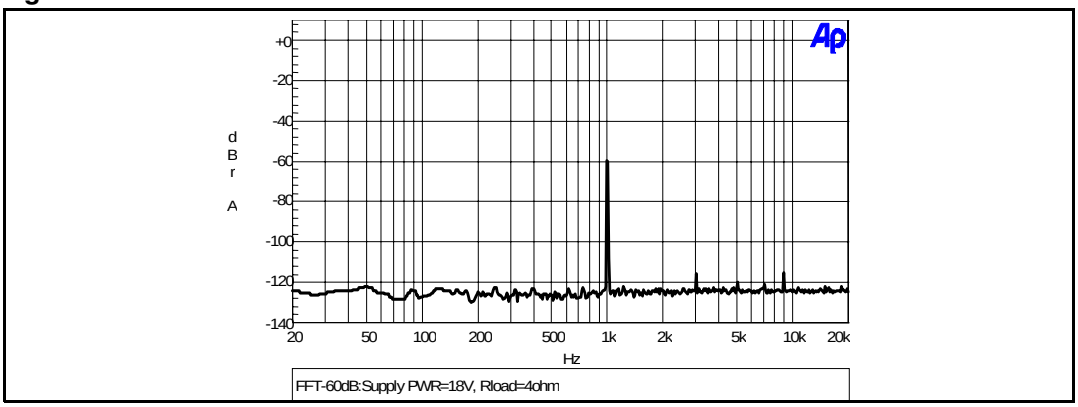


Figure 38. FFT 0 dBFs 1 KHz 18 V 6 ohm

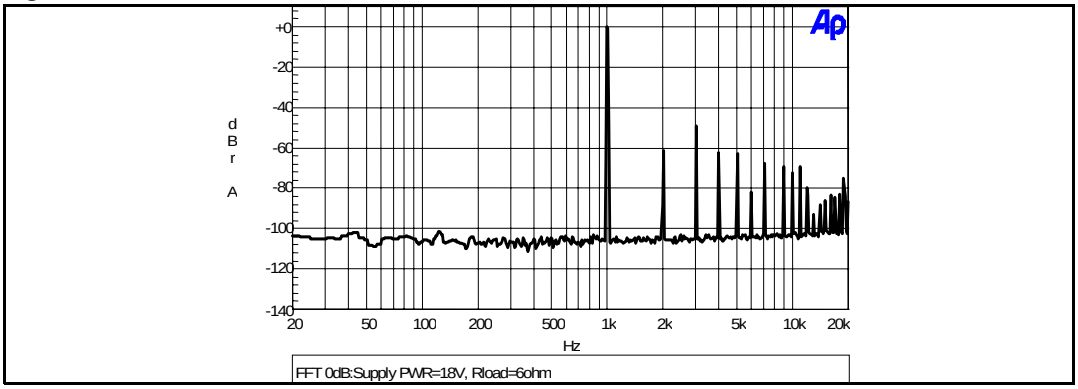


Figure 39. FFT -60 dBFs 1 KHz 18 V 6 ohm

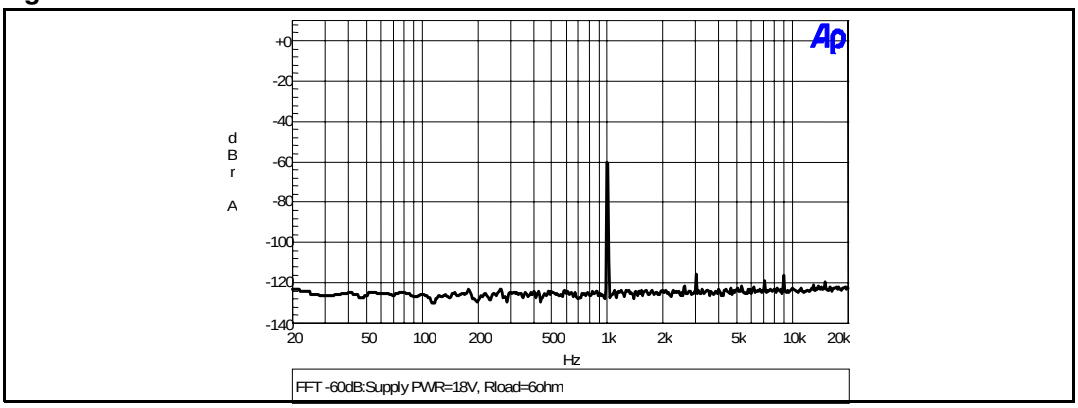


Figure 40. FFT 0 dBFs 1 KHz 18 V 8 ohm

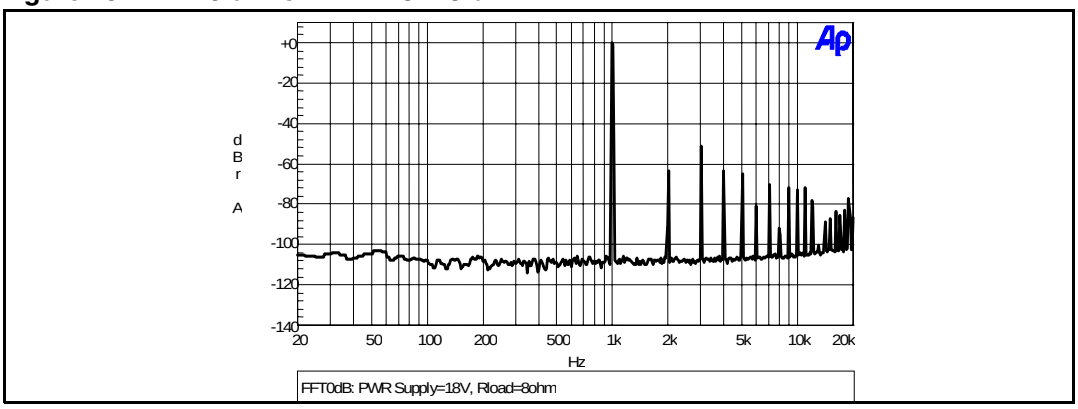


Figure 41. FFT -60 dBFs 1 KHz 18 V 8 ohm

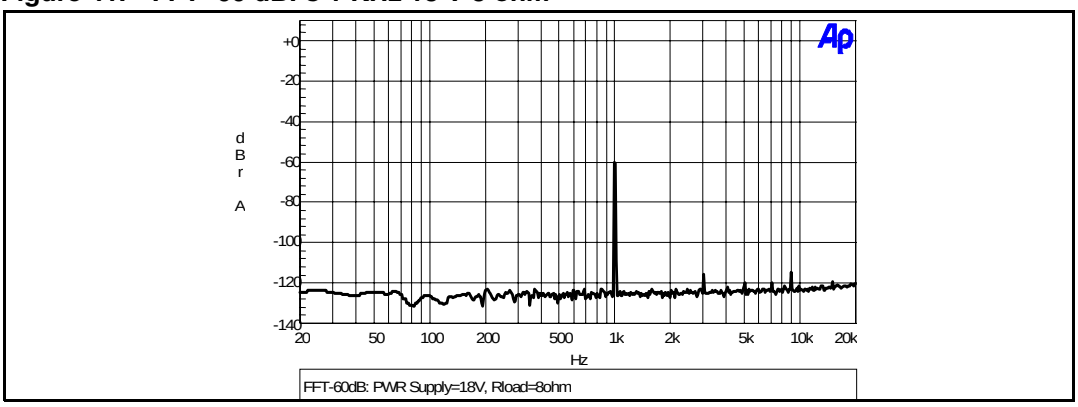


Figure 42. THD versus Freq. 18 V Vcc 4 ohm

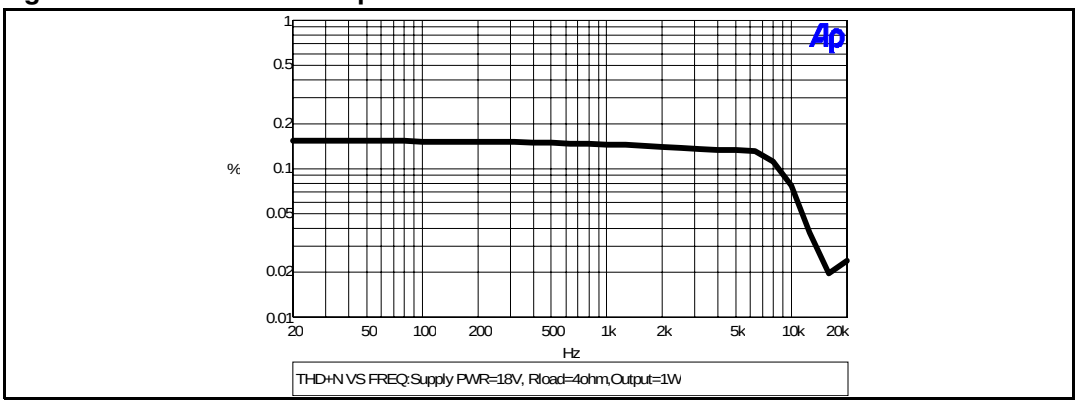


Figure 43. THD versus Freq. 18 V Vcc 6 ohm

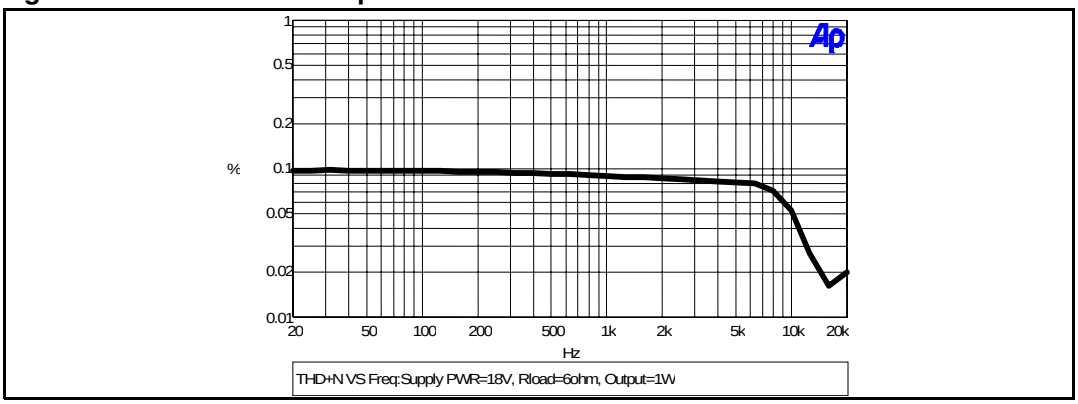


Figure 44. THD versus Freq. 18 V Vcc 8 ohm

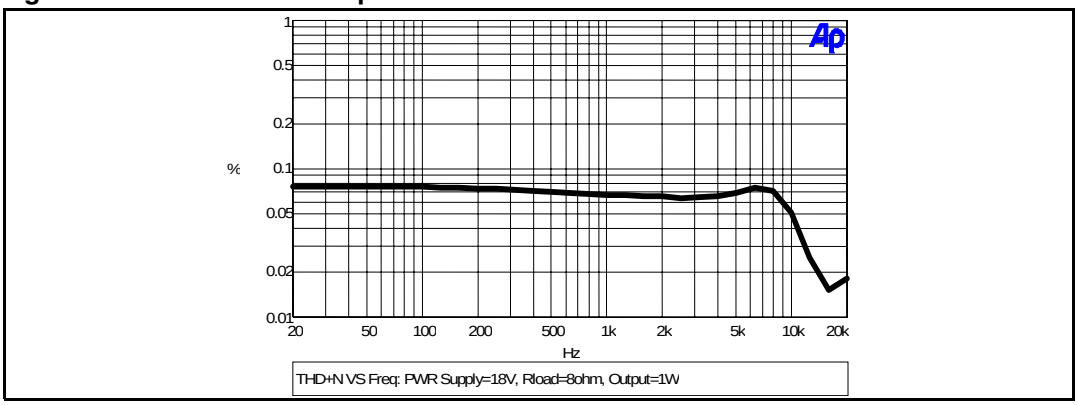


Figure 45. THD versus PWR 4 ohm load

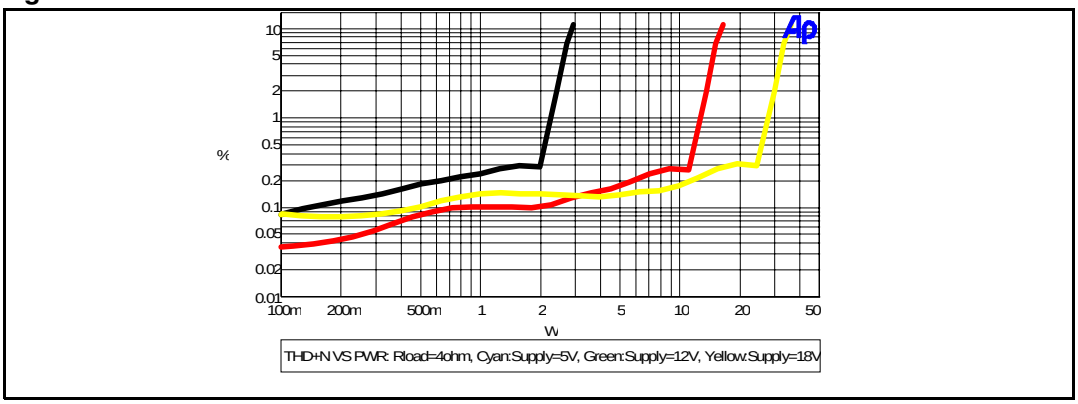


Figure 46. THD versus PWR 6 ohm load

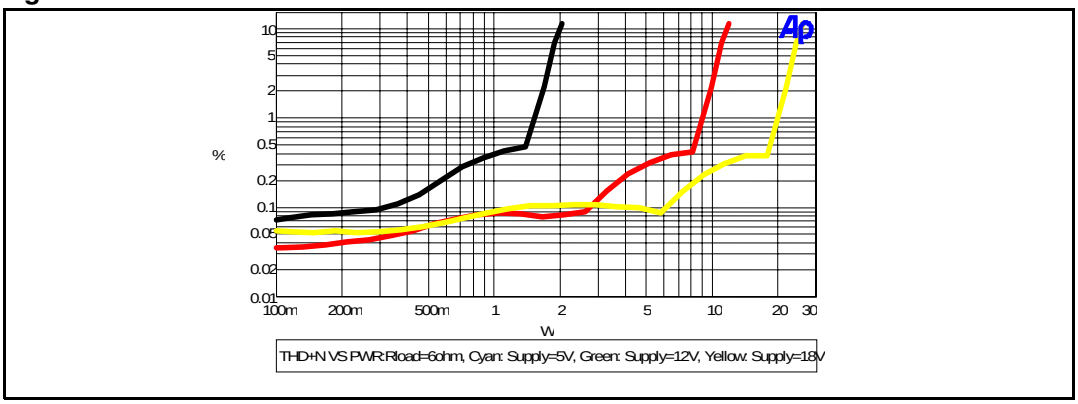
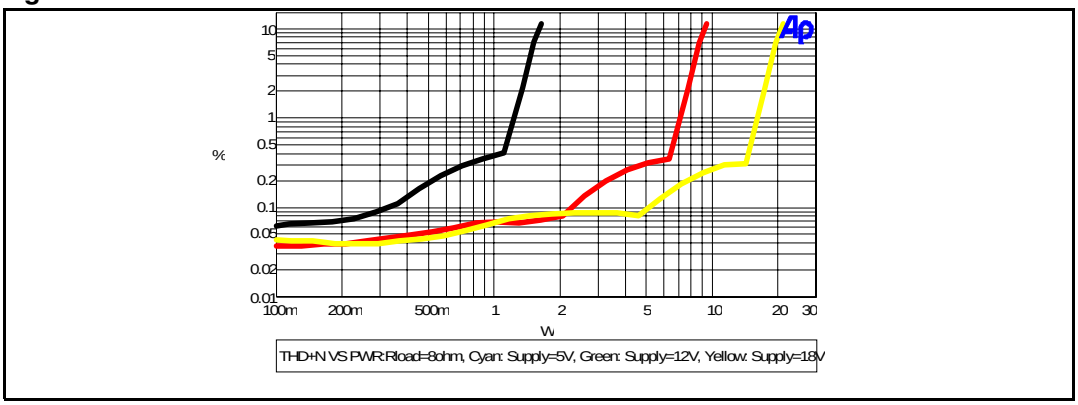


Figure 47. THD versus PWR 8 ohm load



4 Design guideline for PCB schematic and layout

4.1 Schematic

4.1.1 Main driver for components selection

- Absolute maximum rate: 20 V.
- Bypass capacitor 100 nF in parallel to 1 µF for each power Vcc branch. Preferable dielectric is X7R.
- Vdd and ground for PLL filter separate of the power supply.
- Coil saturation current compatible with the peak current of the application.

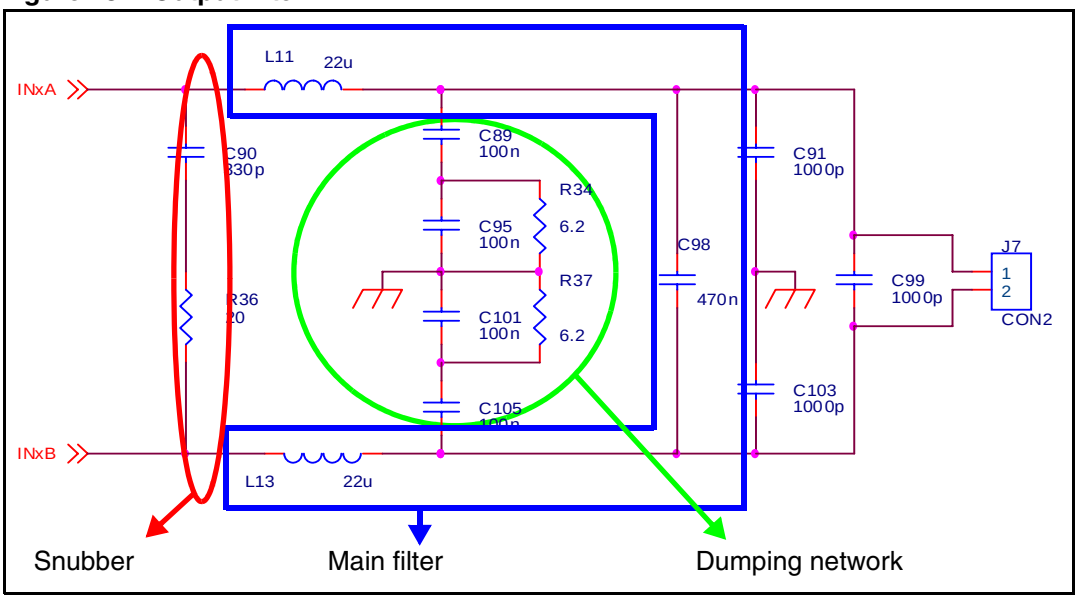
4.2 Decoupling capacitors

There are two different ways to use the decoupling capacitors:

- shared among the channels: the best practise layout route must be used for the board,
- one decoupling system per channel: it is mandatory that the decoupling capacitor must be as close as possible to the IC pins.

4.2.1 Output filter

Figure 48. Output filter



- The key function of a snubber network is to absorb energy from the reactance in the power circuit. The purpose of the snubber RC network is in order to avoid the high pulse energy (such as spikes) in the power circuit which can be dangerous to the system. When using the snubber network, the energy is be transferred to and from the snubber network, ensuring the system can work safely.

- The purpose of the main filter is to remove frequency higher than audible range of 20 KHz. The main filter uses the Butterworth formula to define the cut off frequency, which must be higher than 20 KHz, otherwise the frequency response is affected.
- The purpose of the dumping network is to avoid high frequency oscillation on the output circuit. After using the dumping network the THD can be improved, and can also avoid the inductive copper on the PCB route when the system is working in high frequency with PWM or PCM.

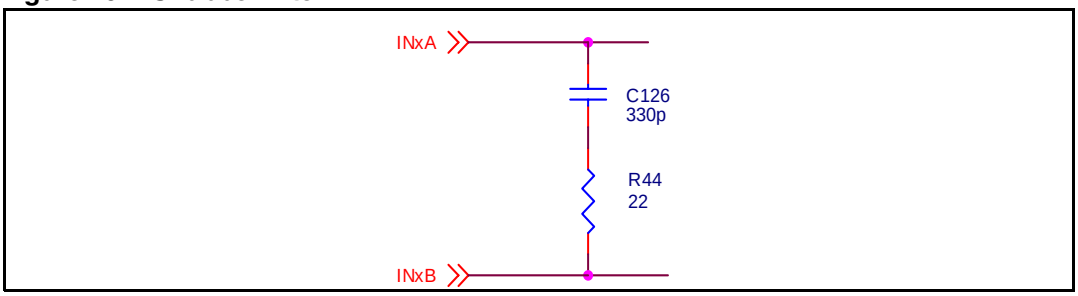
Snubber filter

The snubber circuit must be optimized for the application. Starting values are 330 pF in series to 22 ohm. The power can be defined by the following formula which considers the power supply, frequency and capacitor value:

P=C*f*(2*V)^2

This power is dissipated in series resistance.

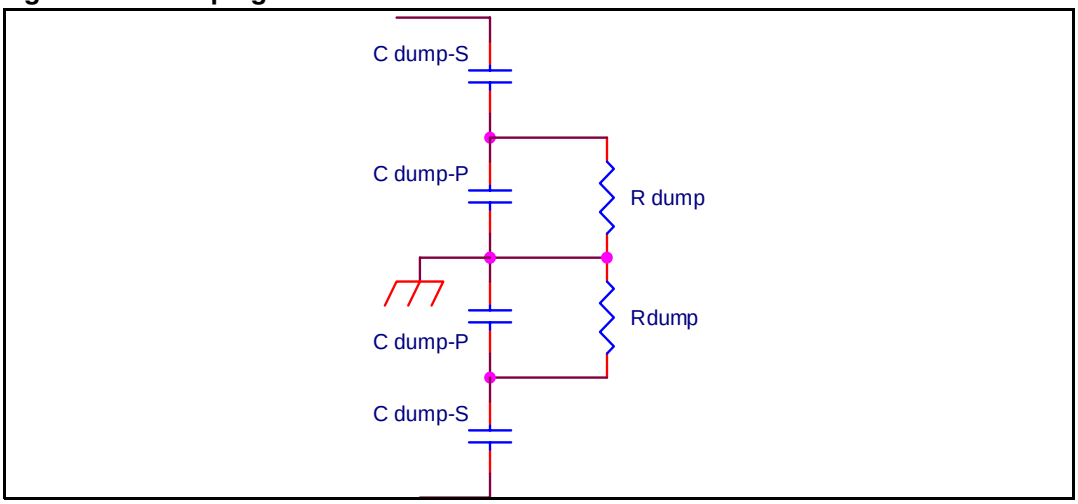
Figure 49. Snubber filter



Dumping network

The C-R-C is a dumping network. It is mainly intended for high inductive loads.

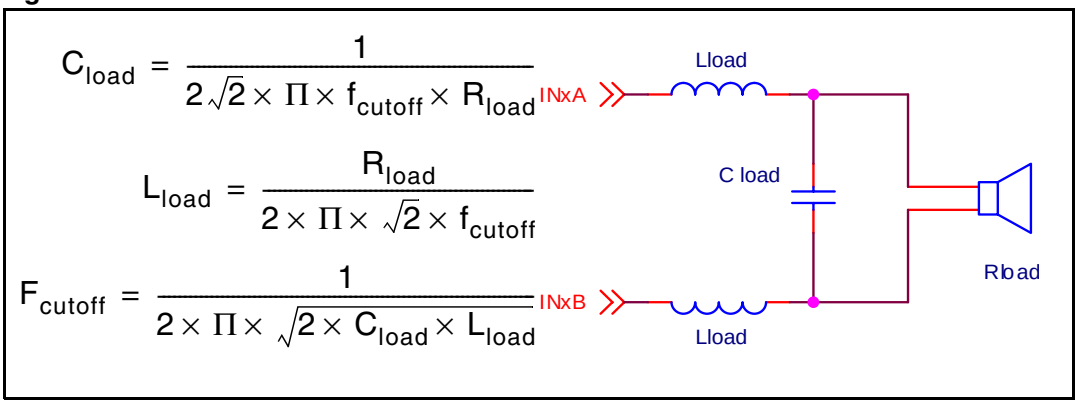
Figure 50. Dumping filter



Main filter

The main filter is an L and C based Butterworth filter. The cut-off frequency must be chosen between the upper limit of the audio band (20 KHz) and the carrier frequency (384 KHz).

Figure 51. Main filter

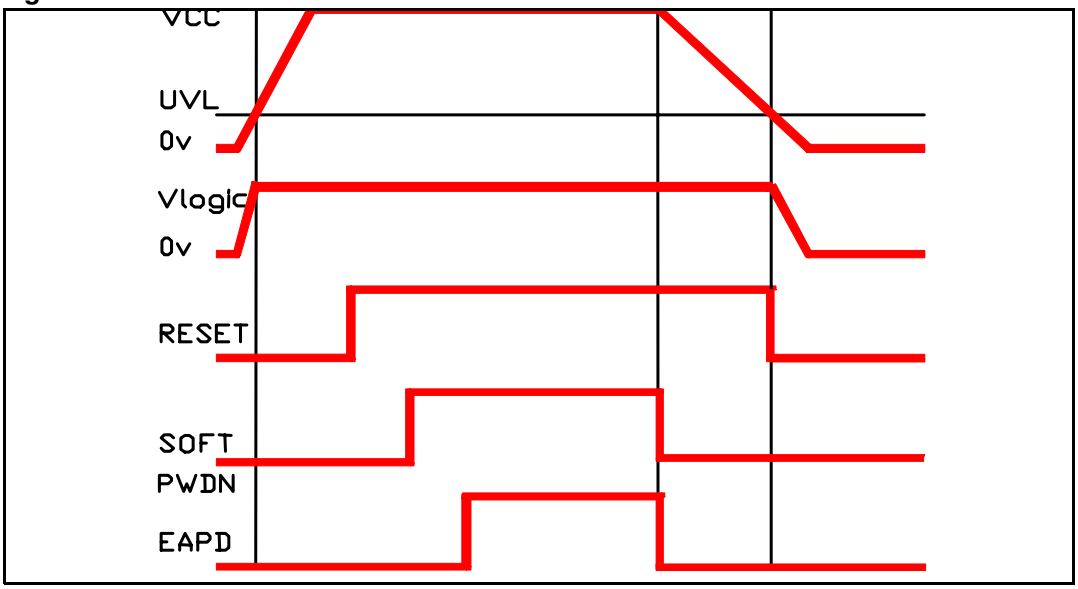


Recommended values

Rload	8 ohm	4 ohm
Lload	22 µH	10 µH
Cload	470 nF	1 µH
C dump-S	100 nF	220 nF
C dump-P	220 nF	220 nF
R dump	6.2	2.7

Recommended power up and power down sequence

Figure 52. Main filter



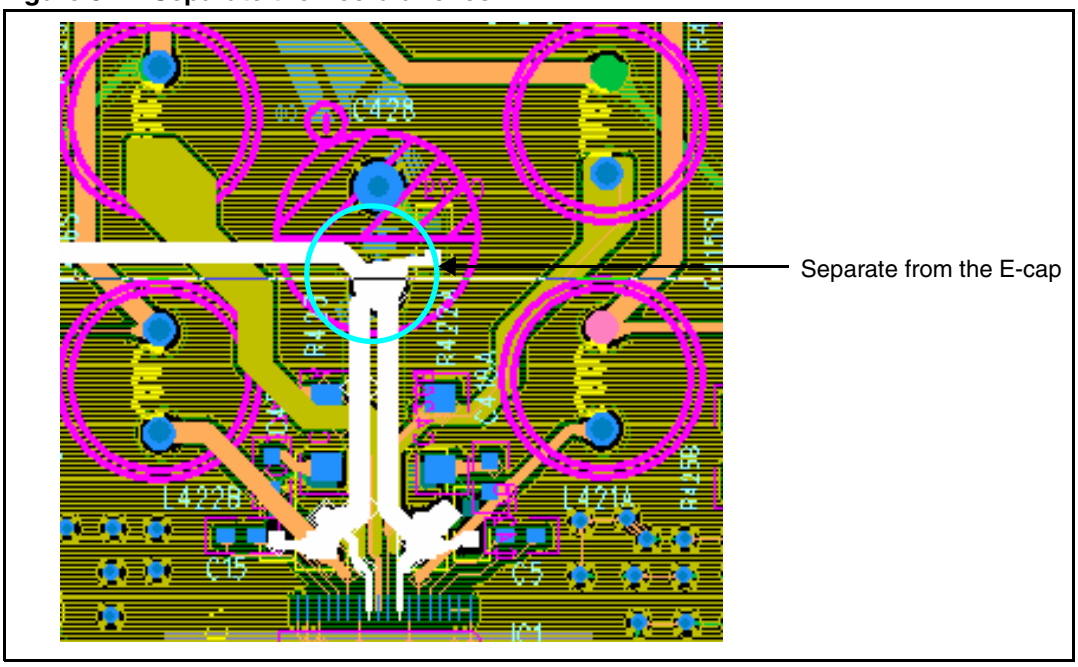
4.3 Layout

1. Solder snubber network as close as possible to the IC related pin.

Figure 53. Snubber network

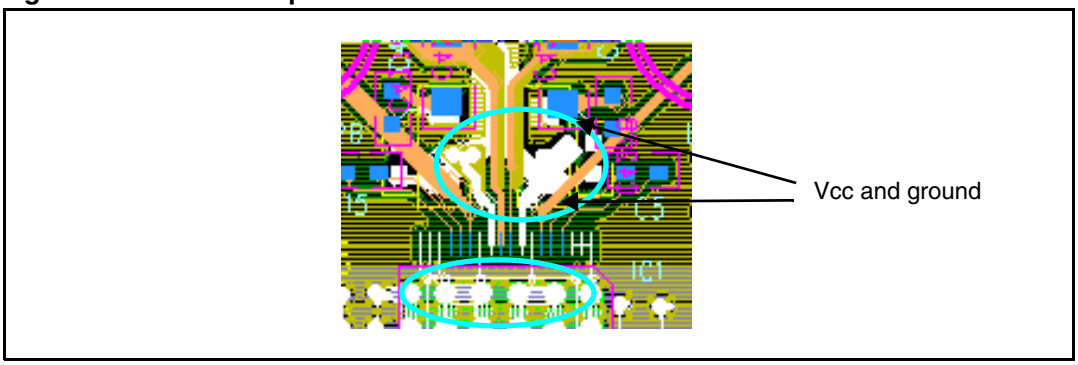
2. Use electrolytic capacitor first to separate the Vcc branches.

Figure 54. Separate the Vcc branches



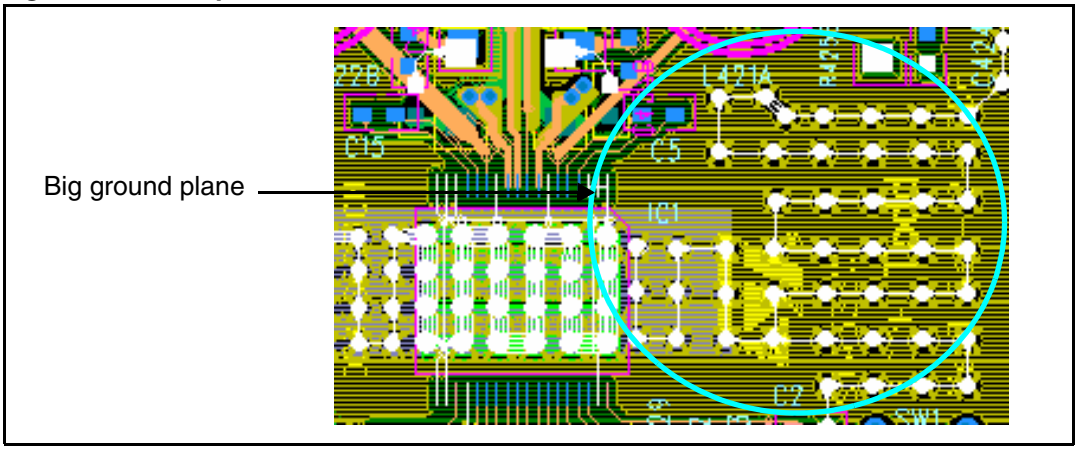
3. Minimize the path between Vcc pins and ground pin in order to avoid inductive paths.

Figure 55. Minimized paths between Vcc and GND



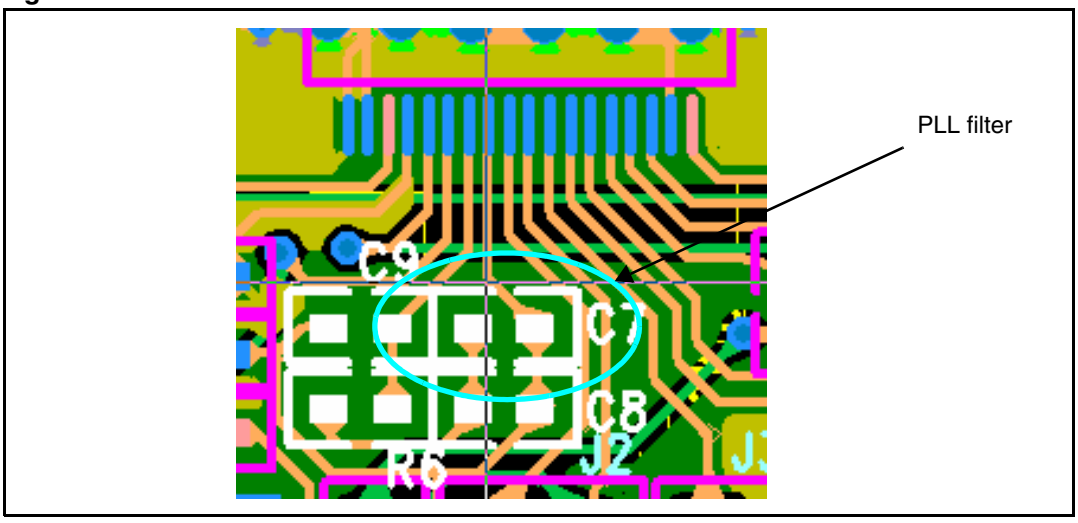
4. To dissipate the thermal with a ground plane.

Figure 56. Dissipate thermal



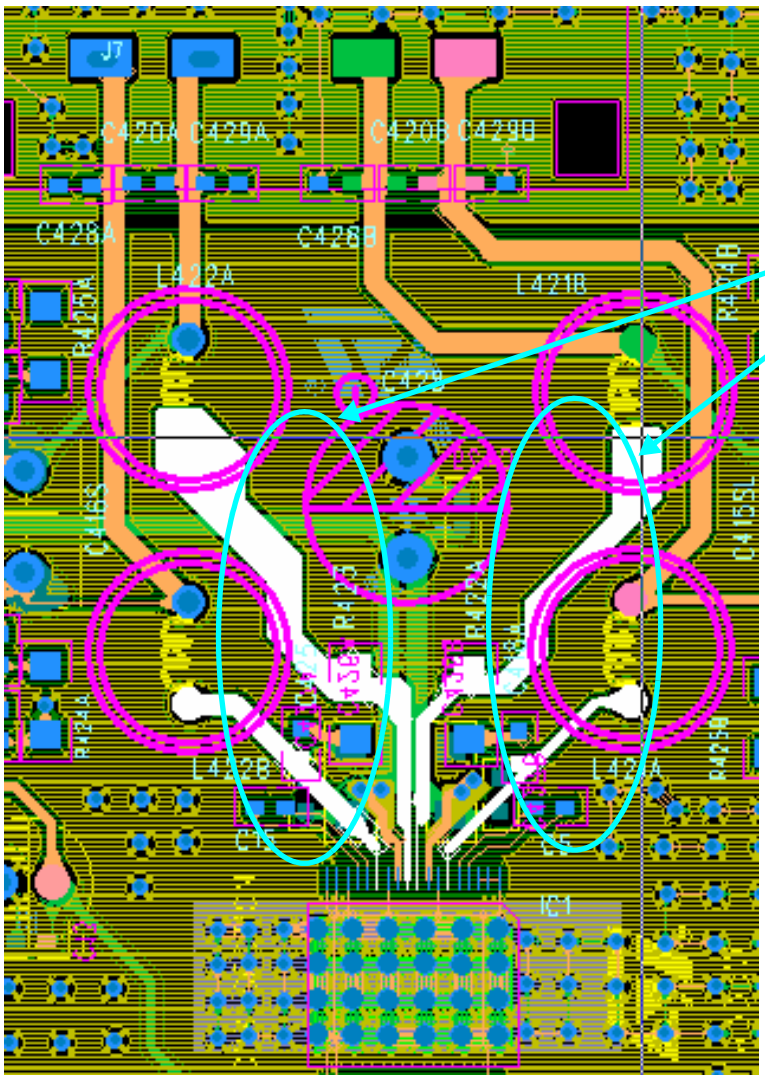
5. Solder PLL filter as close as possible to the FILT pin.

Figure 57. PLL filter



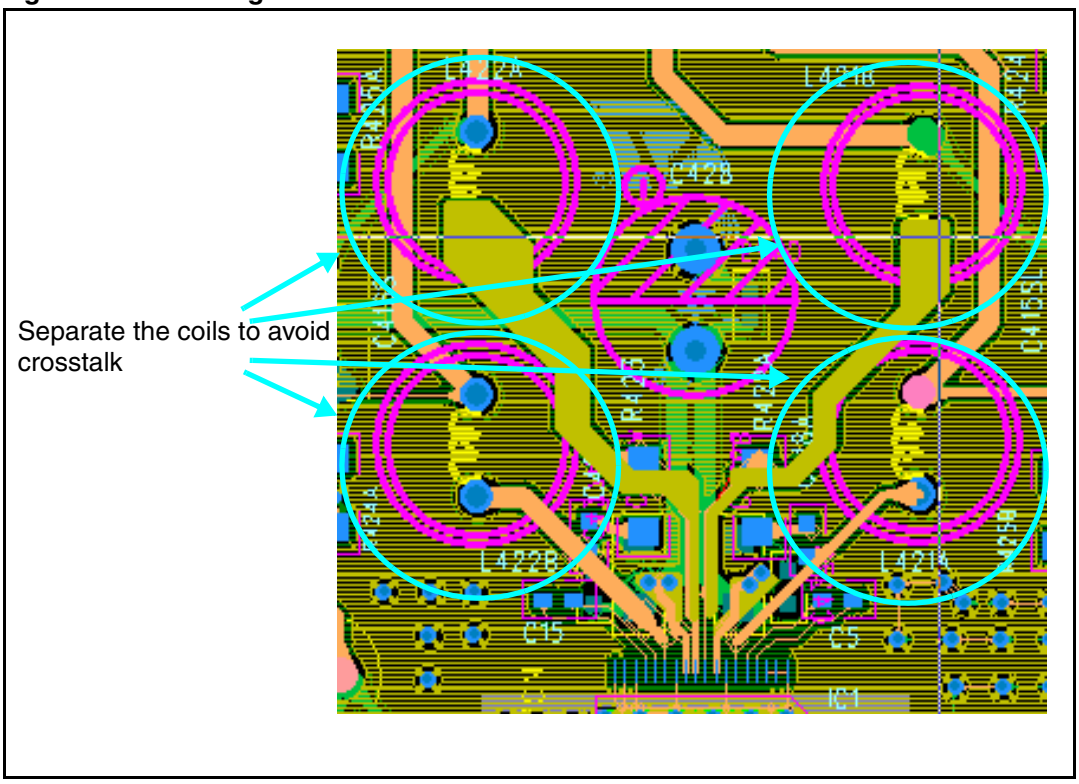
6. For differential application create symmetrical paths for the output stage.

Figure 58. Symmetrical paths for output stage



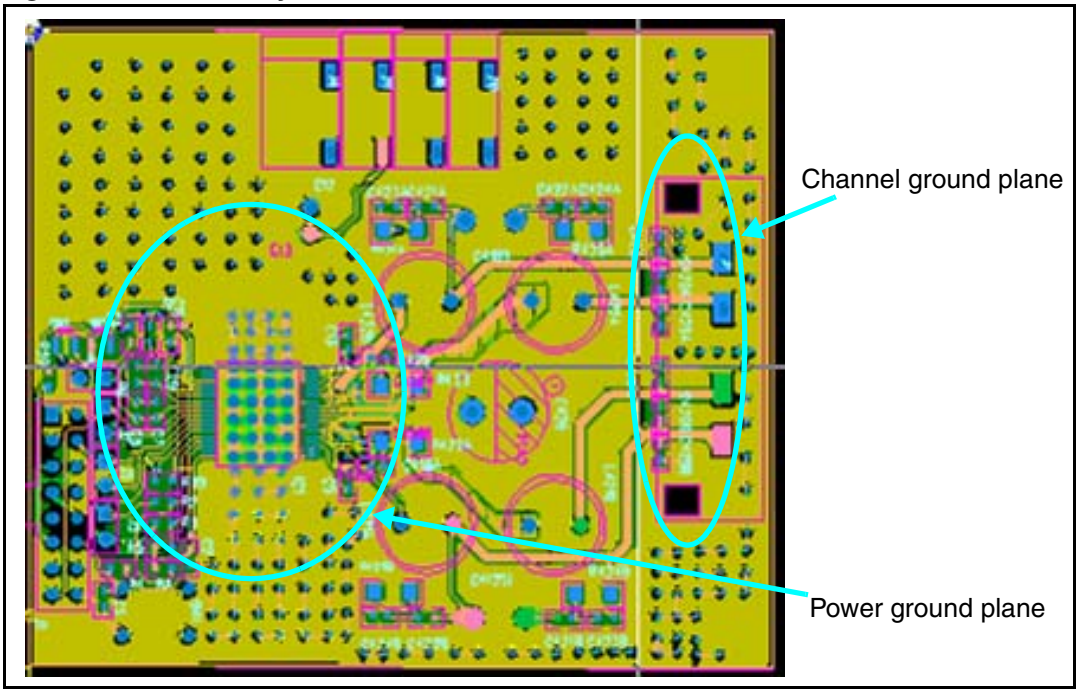
7. Separate the coil and the neighboring coil are vertical to avoid crosstalk.

Figure 59. Avoiding crosstalk



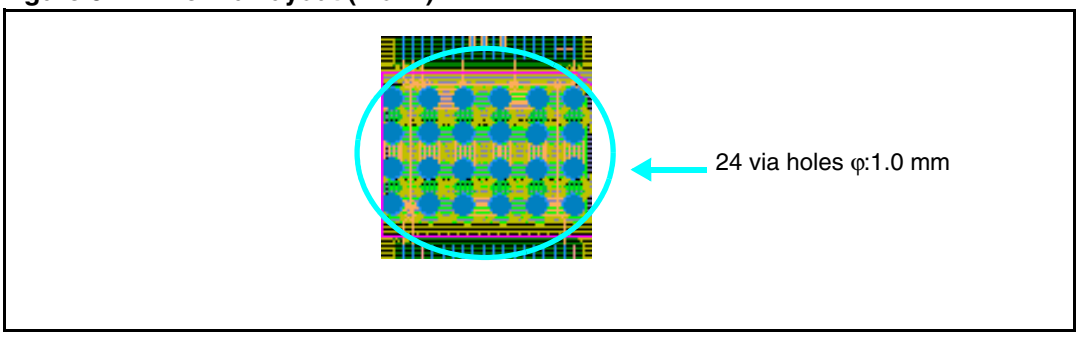
8. Consider ground layout. To avoid interference between ground power and small signal ground, it is necessary to divide the grounding as shown in *Figure 60*.

Figure 60. Ground layout



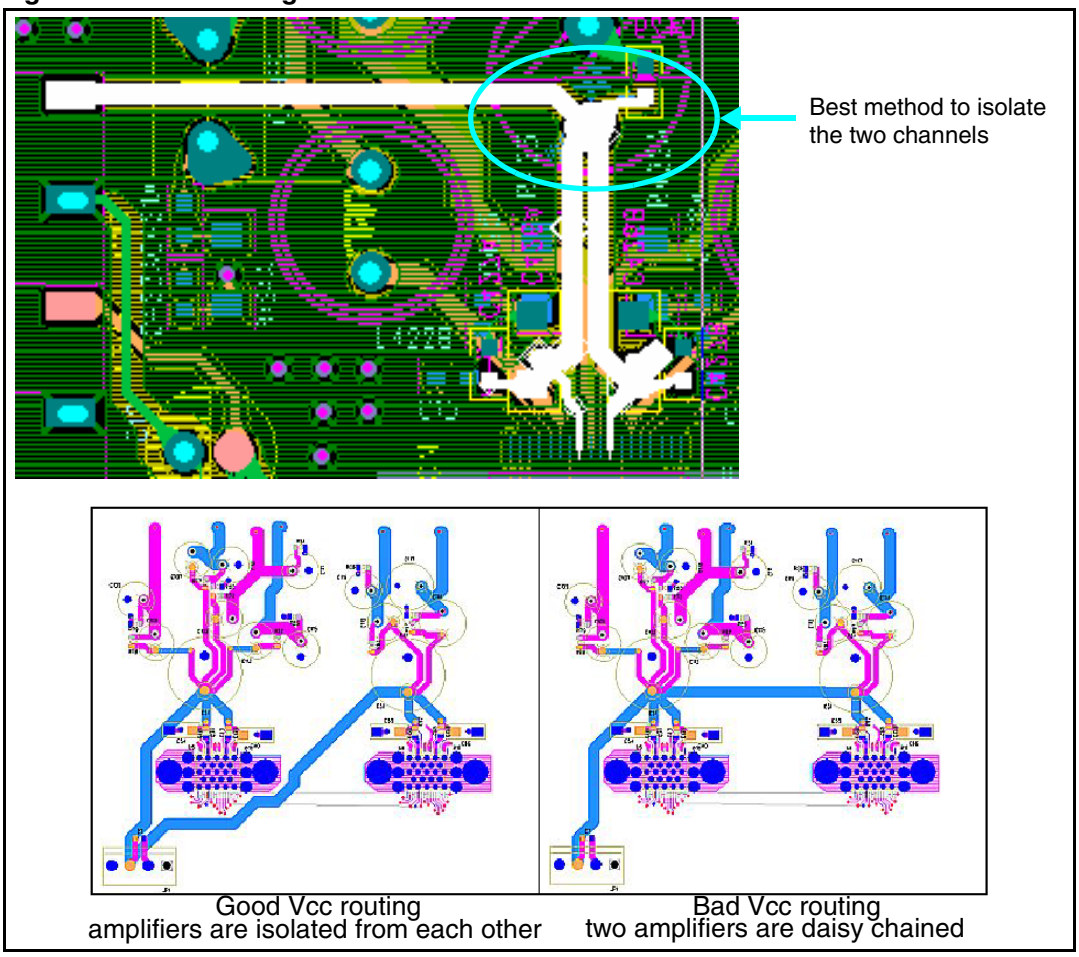
9. Thermal layout with big ground (for thermal and soldering holes).
The thermal resistance junction at the bottom of the STA333W to the ambient obtainable with a ground copper area of 4 x 4 cm and with 24 via holes (see *Figure 61*).

Figure 61. Thermal layout (2 of 2)



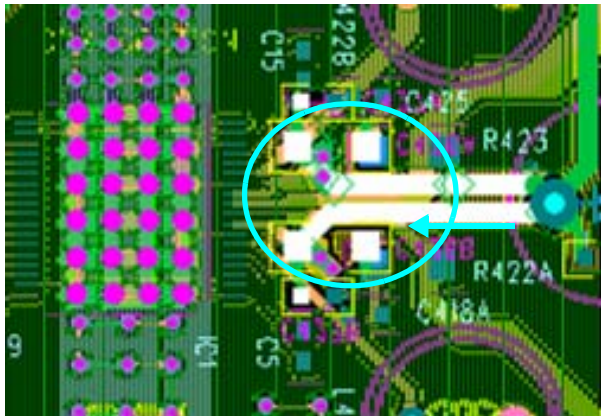
10. VCC routing.
The best route for the Vcc supply is one which avoids interference between different signals (for example, part A is idle whilst part B is working at full load).

Figure 62. Vcc routing



11. Vcc filter for high frequency.
The PWM system works with a fast switch (frequency of 340 KHz approximately) which means the copper wire works as a coil. In order to avoid this, a ceramic capacitor should be used to balance resistance. It is a mandatory requirement that ceramic capacitors are placed as close as possible to the related pins. The distance between the capacitor and their respective pins should be less then 5 mm in order to minimize inductive coil effect generated by the copper wire.

Figure 63. Vcc filter



Vcc capacitor filter as close to the r elated pins as possible.
The ceramic capacitors on the bottom of the PCB close to the IC due to SMD mounting limitations.

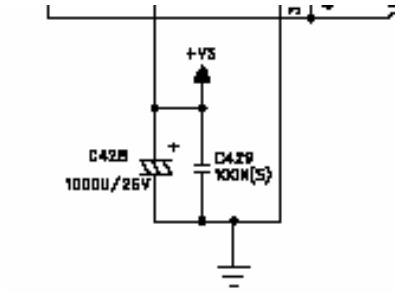
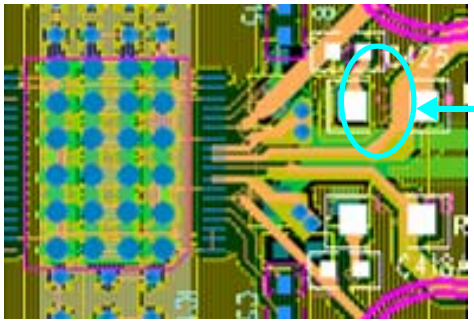


Figure 64.

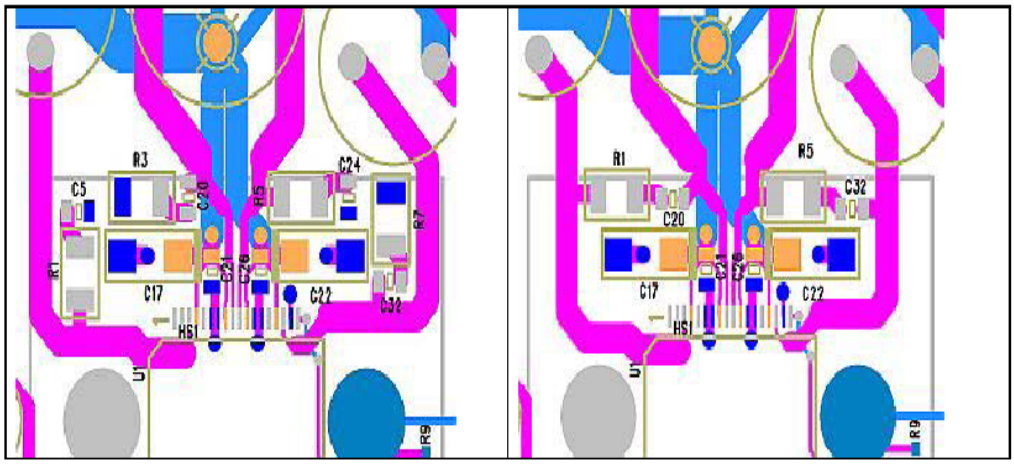
12. Snubber filters for high frequency spike protection on the PWM.

Figure 65. Snubber filter placement



Place snubber circuit as close as possible to the appropriate IC pins, and the - and + for each channel.

Figure 66. Examples of snubber filter placement



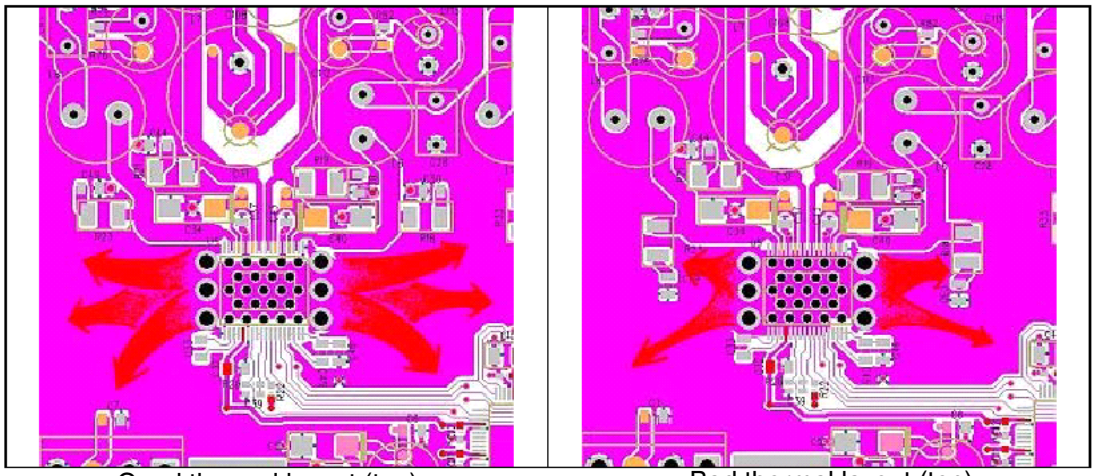
Good common mode snubber placement Good differential snubber placement

Caution: A spike can occur if there > 3 mm distance between the snubber network and the pins. This can cause damage to the IC. Therefore the distance must be kept below 3 mm.

13. Thermal layout

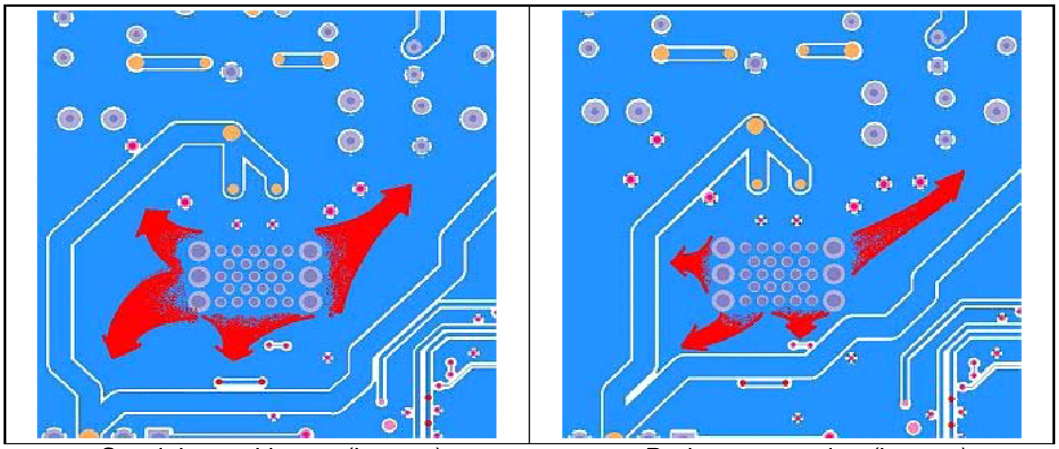
Note: The thermal pad must be connected to ground in order to properly set the IC references. It is necessary to allow the heat to flow freely to all sides of the board including top and bottom. For optimum heat dissipation it is recommended that the PCB has some solder via holes.

Figure 67. Output routing



Good thermal layout (top)
heat can flow freely to the sides

Bad thermal layout (top)
heat flow cut off by the snubbers



Good thermal layout (bottom)
plenty of copper area

Bad output routing (bottom)
little copper area on 3 sides

5 Revision history

Table 2. Document revision history

Date	Revision	Changes
07-Dec-2006	1.0	Initial release.