AN2639

Application note

Soldering recommendations and package information for lead-free ECOPACK2 MCUs and MPUs

Introduction

STMicroelectronics MCUs and MPUs support various types of lead-free ECOPACK2 packages to meet customer requirements.

The mounting technologies are surface mount technology (SMT), and through hole technology (THT). Besides the available mounting technology, the choice is often driven by technical and economic concerns. This application note describes the various package types used, introduces the different mounting technologies, and gives soldering recommendations.

1 Lead-free packages at STMicroelectronics

STMicroelectronics is fully committed to environment protection and sustainable development started a voluntary program in 1997 for removing polluting and hazardous substances from all devices. In 2000, a strategic program, named ECOPACK2 has been officially launched to develop and implement solutions leading to environment-friendly packaging and to progressively ban lead and other heavy metals from our manufacturing lines. ECOPACK2 is a registered trademark of STMicroelectronics.

STMicroelectronics ECOPACK2 products are RoHS compliant with the directive 2011/65/EU.

For more detailed information, go to *https://www.st.com*.

Note: RoHS stands for "Restriction of the use of certain hazardous substances". It is specified by the directive 2011/65/EU of the European Parliament and of the Council of 8th June 2011 on the restriction of the use of certain hazardous substances in electrical and electronic equipment. This directive is the recast of the RoHS Directive 2002/95/EC of the European Parliament and of the Council of 27th January 2003 on the Restriction of the use of certain Hazardous Substances in Electrical and Electronic Equipment.

2 Packages overview

The different packages available at STMicroelectronics are described in Table 1.

Table 1. Package types

Larger package portfolios can be proposed upon request.

Surface mount technology	Through hole technology
Package	Package
SOIC	PDIP.3
QFP	PDIP.4
QFN/DFN	-
BGA	-
LGA	-
WLCSP	-

Through hole technology (THT) and surface mount technology (SMT) imply different soldering technologies leading to different constraints.

In THT, the package body is exposed to relatively low temperatures (< 150 °C) because the lead extremities are only dipped in the soldering alloy, whereas in SMT the whole package body is exposed to a very high temperature (from 245 °C to 260 °C) during reflow soldering process.

In addition, molding compounds used for integrated circuit encapsulation absorb moisture from the ambient medium. During rapid heating in the solder reflow process (see Section 4.1: Soldering methods for more details), this absorbed moisture can vaporize, generating pressure at lead frame pad/silicon to plastic interfaces in the package, with a risk of package cracking and potential degradation of device reliability.

3 SMD presentation

Unlike through hole technology where leads are inserted into the printed circuit board, an SMD (surface mount device) package is attached directly onto mounting pads of the substrate. SMT is extensively used in electronic applications because it has the following advantages:

- Packages are smaller and support higher pin counts
- Packages are light and compact, thus reducing system sizes
- Mounting can be done on either side of the PCB
- No cost for drilling holes into the PCB

Surface mount technology also comes along with a few disadvantages:

- Increased sensitivity to soldering heat because of their thinner dimensions
- Soldering conditions harder to determine (use of finer structures and higher pin count)

3.1 Handling SMDs

Though the intrinsic reliability of SMD packages is now excellent, the use of inappropriate techniques or unsuitable tools during mechanical handling can affect the long-term reliability of the device, or even destroy it.

When handling an SMD package, it is strongly recommended to use adapted tools such as vacuum pipes to avoid touching the pins as much as possible. Manual handling could affect lead coplanarity and cause lead contamination or scratches that could generate solderability problems. it is not allowed to increase the spacing between two consecutive pins.

4 Soldering

4.1 Soldering methods

There are three main soldering methods (which are detailed in Figure 1. Soldering method descriptions):

- Single-sided reflow soldering
- Double-sided reflow soldering
- Wave soldering (for THT devices)

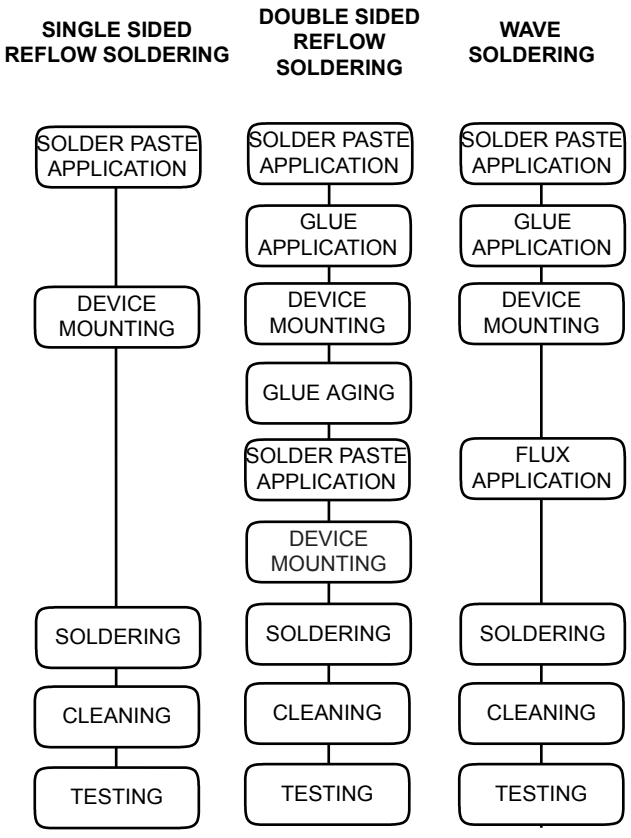
4.1.1 Bending leads

In all processes, it is important to avoid straining the package and particularly the area where the leads enter the encapsulating resin. If the package/lead interface is strained, the resistance to humidity and thermal stress is compromised, affecting device reliability.

4.1.2 Insertion

When mounting devices on a printed circuit board the golden rule is, again, to avoid stress. In particular, adhere to the specified pin spacing of the device: do not try to bend the leads to fit nonstandard hole spacing.

Figure 1. Soldering method descriptions



4.2 Soldering recommendations

The following recommendations must be followed for soldering each package type (see Table 2).

Table 2. Package/soldering process compatibility

Reflow soldering with DIP and wave soldering with BGA, VFQFPN, UFQFPN, WFQFPN, and WLCSP are strictly impossible due to the lead/ball configuration.

Package	Reflow processing process		Wave soldering process	
	Process	Reliability	Process	Reliability
SOIC	OK	OK	Feasible	(1)
QFP	OK	OK	Under customer responsibility (2)	(1)
BGA	OK	OK	Impossible	N/A
LGA	OK	OK	Impossible	N/A
QFN/DFN	OK	OK	Impossible	N/A
WLCSP	OK	OK	Impossible	N/A

1. *Wave soldering with SMT packages is not qualified by STMicroelectronics. SMT package qualification performed as a standard by STMicroelectronics only includes infrared reflow soldering.*
   *JEDEC JESD22A111 recommends that wave soldering of SMT packages is evaluated by the **user** because the stress induced inside the package may generate internal structural damage and closely depends on soldering process parameters.*
2. *Wave soldering with VFQFPN, UFQFPN, and WFQFPN is not recommended because it is difficult to avoid solder bridges when leads pass through the double wave.*

4.3 Compatibility with leaded soldering process

Lead-free packages can be assembled using a leaded soldering process.

4.4 Reflow soldering conditions

The greater danger during reflow soldering is overheating. If an integrated circuit is exposed to high temperature for an excessive period of time, it may be damaged and its reliability reduced.

It is also important to use suitable fluxes for the soldering baths to avoid deterioration of the leads or package resin. Residual flux between the leads or in contact with the resin must be removed to guarantee long-term reliability. The solvent used to remove excess flux should be chosen with care. It is particulary true for trichloroethylene (CHCl: CCl2). Base solvents should be avoided because the residue could corrode the encapsulating resin.

High-quality low-defect soldering requires identifying the optimum temperature profile for reflowing the solder paste, thus optimizing the process. The heating and cooling rise rates must be compatible with the solder paste and components.

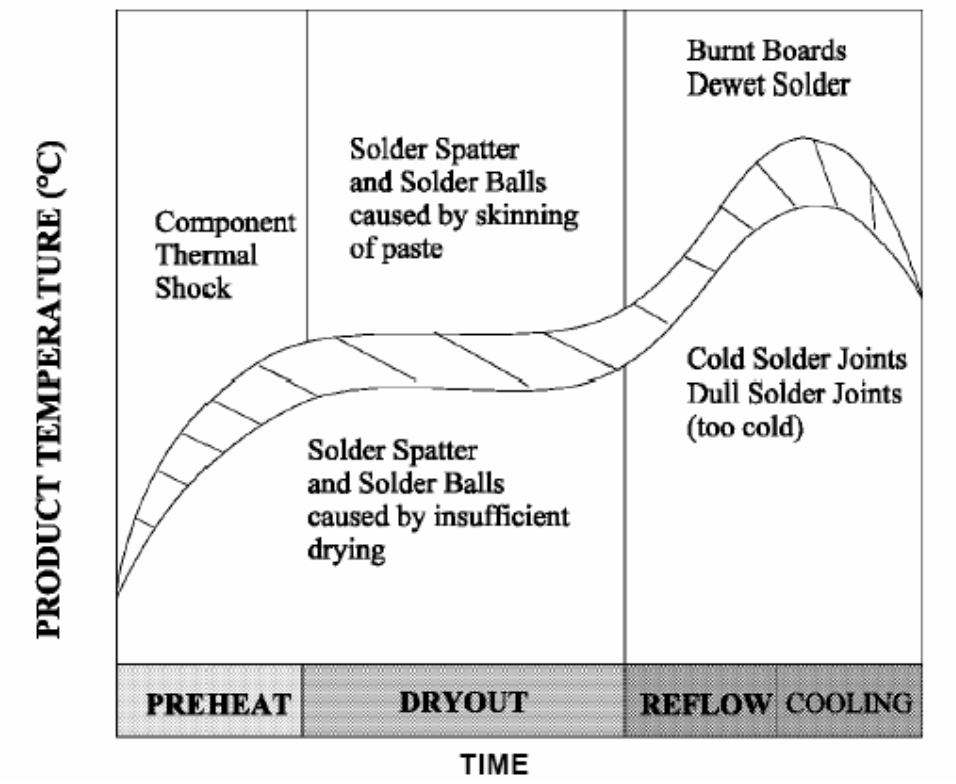
A typical profile consists of a preheat, dry out, and reflow sections.

The most critical point in the preheat section is to minimize the temperature rise rate to less than 2°C/second, to minimize thermal shock on the semiconductor components.

The dry out section is used primarily to ensure that the solder paste is fully dried before hitting reflow temperatures.

Solder reflow is accomplished in the reflow zone, where the solder paste is elevated to a temperature greater than the melting solder point. Melting temperature must be exceeded by approximately 20°C to ensure quality reflow.

Figure 2. **Typical reflow soldering profile**



Note: STMicroelectronics cannot guarantee the state of the product after reflow soldering while it is powered on, because the product is not qualified or characterized at such temperatures (above the absolute maximum ratings). The product can go into an unknown state, and long-term reliability may be impacted.

It is strongly recommended to change the PCB architecture to avoid product bias during reflow.

If it is not possible, it is recommended to perform a power-on reset by driving the VBAT pin low for more than 100 ms while V_{DD} is below the PDR threshold (1.60 V), in order to put the product in a determinate state.

After the SMT soldering process, when the parts arrive at the first test station, the first action done on the tester is to short the VBAT pin to ground for a certain period of time.

4.4.1 Convection reflow for SOIC packages

There are no special requirements necessary when reflowing SOIC components. As with all SMT components, it is important that profiles be checked on all new board designs. In addition, if there are multiple packages on the board, the profile must be checked at different locations on the board. The solder paste manufacturer's temperature profile should be used to optimize flux activity and minimize the voiding. The recommended lead-free reflow profile is illustrated on Figure 3. Typical lead-free reflow profile for SOIC and Table 3. SOIC recommended profile parameters (lead-free mounting).

Figure 3. **Typical lead-free reflow profile for SOIC**

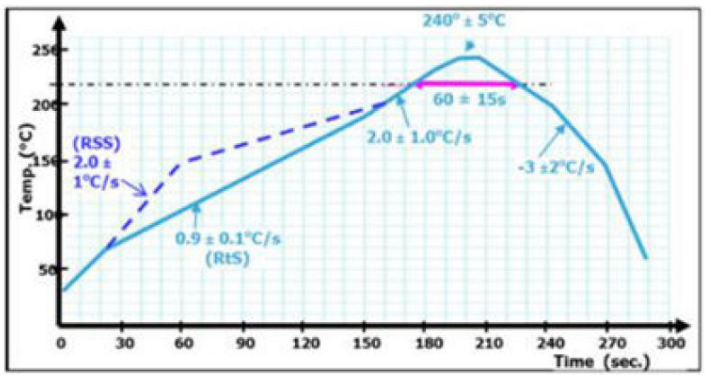


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Table 3. **SOIC recommended profile parameters (lead-free mounting)**

Profile	Ramp to spike	Ramp-soak-Spike
Temperature gradient in preheat	Temp. : 70°C to 150°C 0.8°C/sec to 1.0°C/sec	Temp. : 70°C to 150°C 1.0°C/sec to 3.0°C/sec
Soak/Dwell (refer to solder paste supplier recommendation)	N/A or Temp. : 150°C to 200°C: 40 to 80s	Soak Temp. : 150°C to 200°C: 40 to 100s
Temperature gradient in preheat	Temp. : 200°C to 225°C 1.0°C/sec to 3.0°C/sec	Temp. : 200°C to 225°C 1.0°C/sec to 3.0°C/sec
Peak temperature	235°C to 245°C	
Duration above 220°C	45 to 75 seconds	
Temperature gradient in cooling	-1°C to -5°C	
Time from 50 to 220°C	150 to 230 seconds	

Note: Proposed reflow profile and peak temperature are to be considered as suggestion only.

4.4.2 Convection reflow for QFP packages

There are no special requirements necessary when reflowing QFP components. As with all SMT components, it is important that profiles be checked on all new board designs. In addition, if there are multiple packages on the board, the profile must be checked at different locations on the board. The solder paste manufacturer's temperature profile should be used to optimize flux activity and minimize the voiding. The recommended lead-free reflow profile as illustrated on Figure 4. Typical lead-free reflow profile for QFP and Table 4. QFP recommended profile parameters (lead-free mounting).

Figure 4. **Typical lead-free reflow profile for QFP**

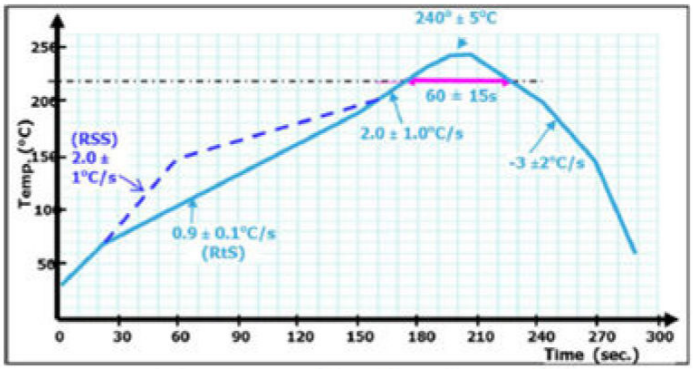

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Table 4. QFP recommended profile parameters (lead-free mounting)

Profile	Ramp to spike	Ramp-soak-Spike
Temperature gradient in preheat	Temp. : 70°C to 150°C 0.8°C/sec to 1.0°C/sec	Temp. : 70°C to 150°C 1.0°C/sec to 3.0°C/sec
Soak/Dwell (refer to solder paste supplier recommendation)	N/A or Temp. : 150°C to 200°C: 40 to 80s	Soak Temp. : 150°C to 200°C: 40 to 100s
Temperature gradient in preheat	Temp. : 200°C to 225°C 1.0°C/sec to 3.0°C/sec	Temp. : 200°C to 225°C 1.0°C/sec to 3.0°C/sec
Peak temperature	235°C to 245°C	
Duration above 220°C	45 to 75 seconds	
Temperature gradient in cooling	-1°C to -5°C	
Time from 50 to 220°C	150 to 230 seconds	

Note: Proposed reflow profile and peak temperature are to be considered as suggestion only.

4.4.3 Convection Reflow for QFN/DFN packages

There are no special requirements necessary when reflowing QFN components. As with all SMT components, it is important that profiles be checked on all new board designs. In addition, if there are multiple packages on the board, the profile must be checked at different locations on the board. The solder paste manufacturer's temperature profile should be used to optimize flux activity and minimize the voiding. The recommended lead-free reflow profile as illustrated on Figure 5. Typical lead-free reflow profile for QFN/DFN and Table 5. QFN/DFN recommended profile parameters (lead-free mounting).

Figure 5. Typical lead-free reflow profile for QFN/DFN

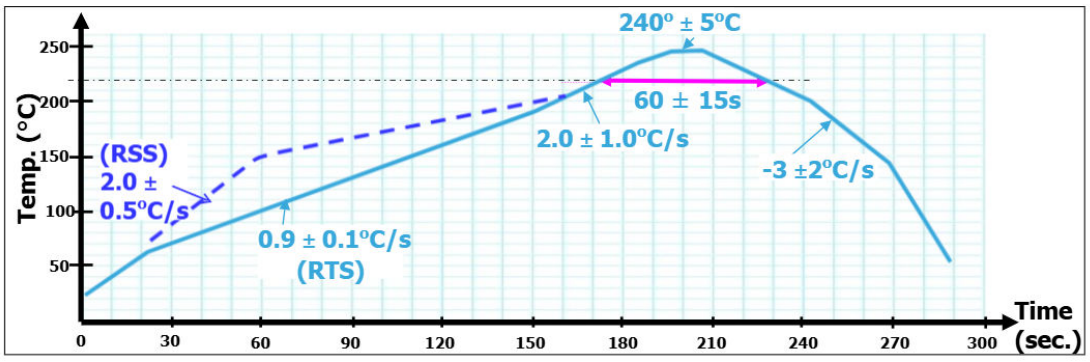

Table 5. QFN/DFN recommended profile parameters (lead-free mounting)

Profile	Ramp to spike	Ramp-soak-Spike
Temperature gradient in preheat	Temp. : 70°C to 150°C 0.8°C/sec to 1.0°C/sec	Temp. : 70°C to 150°C 1.0°C/sec to 3.0°C/sec
Soak/Dwell (refer to solder paste supplier recommendation)	N/A or Temp. : 150°C to 200°C: 40 to 80s	Soak Temp. : 150°C to 200°C: 40 to 100s
Temperature gradient in preheat	Temp. : 200°C to 225°C 1.0°C/sec to 3.0°C/sec	Temp. : 200°C to 225°C 1.0°C/sec to 3.0°C/sec
Peak temperature	235°C to 245°C	
Duration above 220°C	45 to 75 seconds	
Temperature gradient in cooling	-1°C to -5°C	

Profile	Ramp to spike	Ramp-soak-Spike
Time from 50 to 220°C	150 to 230 seconds	

Note: Proposed reflow profile and peak temperature are to be considered as suggestion only.

4.4.4 Convection reflow for BGA packages

There are no special requirements necessary when reflowing BGA components. As with all other SMTcomponents, it is important that soldering profiles be checked on all new board designs. In addition, if there are multiple packages on the board, the profile must be checked at different locations on the board. The solders paste manufacturer's recommended profile should be considered and used to optimize flux activity and minimize the voiding. The recommended Lead-free reflow profile is illustrated on Figure 6. Typical lead-free reflow profile for BGA and its typical parameters in Table 6. Typical lead-free reflow profile parameters for BGA.

- Ramp-to-Spike profile is recommended for Pb-free assembly with better wetting and less thermal exposure than traditional Ramp-Soak-Spike profile.
- Avoid temperature plateau around melting temperature for better accuracy
- Perform reflow optimization for actual board/panel and refer to solder paste supplier's recommendation

Figure 6. Typical lead-free reflow profile for BGA

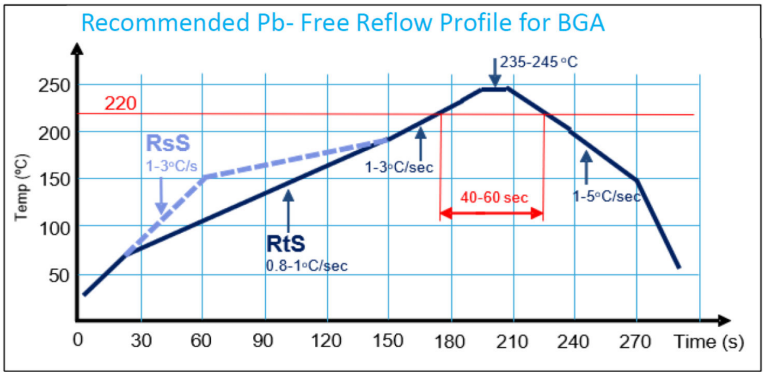

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Table 6. Typical lead-free reflow profile parameters for BGA

Profile	Ramp to spike	Ramp-soak-Spike
Temperature gradient in preheat	Temp. : 70°C to 150°C 0.9 ± 0.1°C/sec	Temp. : 70°C to 150°C 2.0 ± 1.0°C/sec
Soak/Dwell (refer to solder paste supplier recommendation)	N/A or Temp. : 150°C to 200°C: 60 ± 20 sec	Soak Temp. : 150°C to 200°C: 70 ± 30 sec
Temperature gradient in preheat (in pre-reflow)	Temp. : 200°C to 225°C 2 ± 1°C/sec	Temp. : 200°C to 225°C 2 ± 1°C/sec
Peak temperature (in reflow)	235°C to 245°C	
Duration above 220°C	45 to 60 seconds	
Temperature gradient in cooling	-1°C to -5°C	
Time from 50 to 220°C	150 to 230 seconds	

Note: Proposed reflow profile and peak temperature are to be considered as suggestion only.

4.4.5 Convection reflow for LGA packages

There are no special requirements necessary when reflowing LGA components. As with all SMT components, it is important that profiles be checked on all new board designs. In addition, if there are multiple packages on the board, the profile must be checked at different locations on the board. The solder paste manufacturer's temperature profile should be used to optimize flux activity and minimize the voiding. The recommended lead-free reflow profile as illustrated on Figure 7. Typical lead-free reflow profile for LGA and its typical parameters in Table 7. Typical lead-free reflow profile parameters for LGA:

Figure 7. Typical lead-free reflow profile for LGA

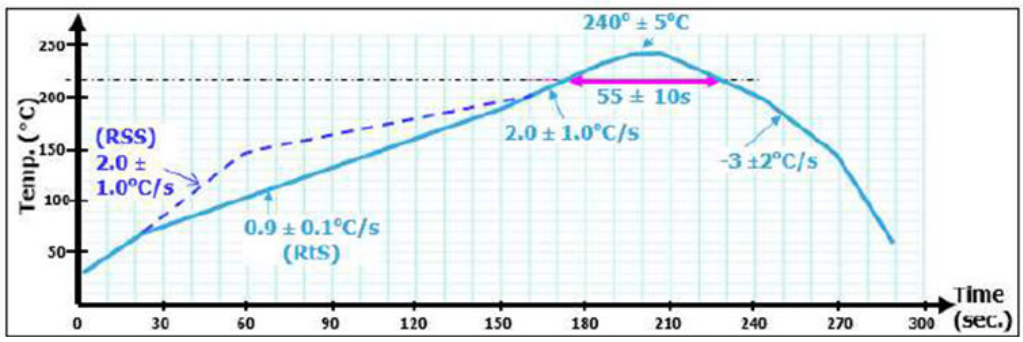

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Table 7. Typical lead-free reflow profile parameters for LGA

Profile	Ramp to spike	Ramp-soak-Spike
Temperature gradient in preheat	Temp. : 70°C to 150°C 0.9 ± 0.1°C/sec	Temp. : 70°C to 150°C 2.0 ± 0.5°C/sec
Soak/Dwell (*refer to solder paste supplier recommendation)	N/A or Temp. : 150°C to 200°C: 60 ± 20 sec	Soak Temp. : 150°C to 200°C: *70 ± 30 sec
Temperature gradient in pre-reflow	Temp. : 200°C to 225°C 2 ± 1°C/sec	
Peak temperature (in reflow)	240 ± 5°C	
Duration above 220°C	55 ± 10 seconds	
Temperature gradient in cooling	-3 ± 2°C/sec	
Time from 50 to 220°C	150 to 230 seconds	

Note: Proposed reflow profile and peak temperature are to be considered as suggestion only.

4.4.6 Convection reflow for WLCSP packages

There are no special requirements necessary when reflowing WLCSP components. As with all SMT components, it is important that profiles be checked on all new board designs. In addition, if there are multiple packages on the board, the profile must be checked at different locations on the board. The solder paste manufacturer's temperature profile should be used to optimize flux activity and minimize the voiding

The recommended lead-free reflow profile as illustrated on Figure 8. Typical lead-free reflow profile for WLCSP and its typical parameters in Table 8. Typical lead-free reflow profile parameters for WLCSP:

Figure 8. **Typical lead-free reflow profile for WLCSP**

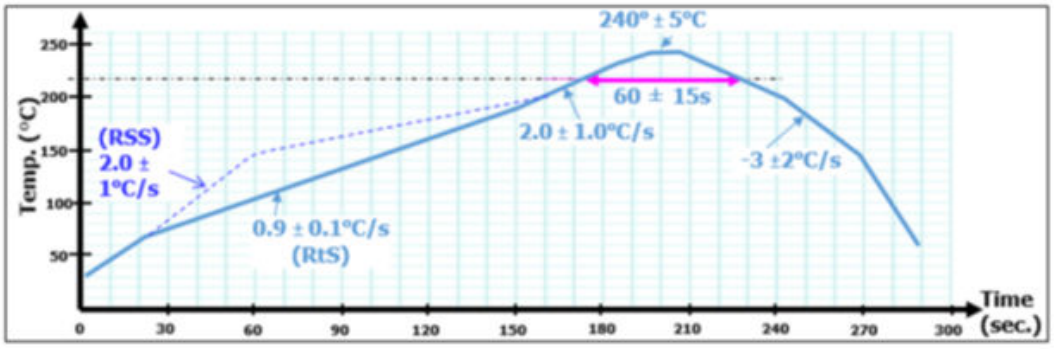

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Table 8. **Typical lead-free reflow profile parameters for WLCSP**

Profile	Ramp to spike	Ramp-soak-Spike
Temperature gradient in preheat	Temp. : 70°C to 150°C 0.9 ± 0.1°C/sec	Temp. : 70°C to 150°C 2.0 ± 0.5°C/sec
Soak/Dwell (*refer to solder paste supplier recommendation)	N/A or Temp. : 150°C to 200°C: 60 ± 20 sec	Soak Temp. : 150°C to 200°C: *70 ± 30 sec
Temperature gradient (in pre-reflow)	Temp. : 200°C to 225°C 2 ± 1°C/sec	
Peak temperature (in reflow)	240 ± 5°C	
Duration above 220°C	60 ± 15 seconds	
Temperature gradient in cooling	-3 ± 2°C/sec	
Time from 50 to 220°C	150 to 230 seconds	

Note: Proposed reflow profile and peak temperature are to be considered as suggestion only.

5 SMD gluability

It is strongly recommended to follow glue application specifications from the glue supplier, and to use 100% glue polymerization for optimal glue efficiency.

Figure 9. Recommended profiles for glue polymerization using regular oven and linear flow oven

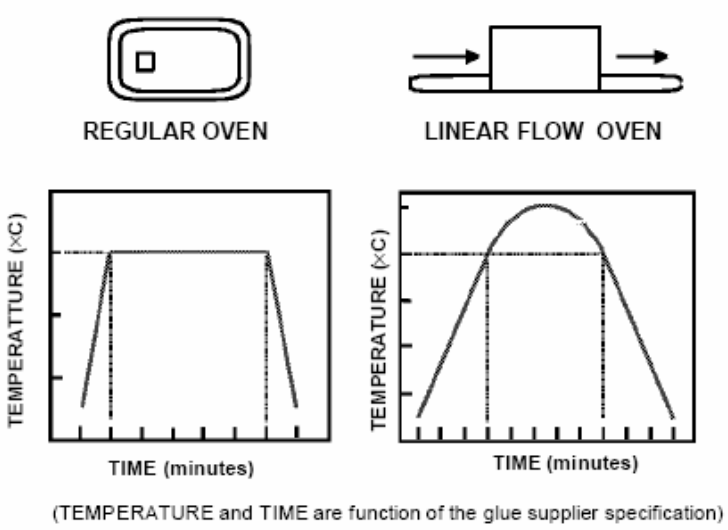
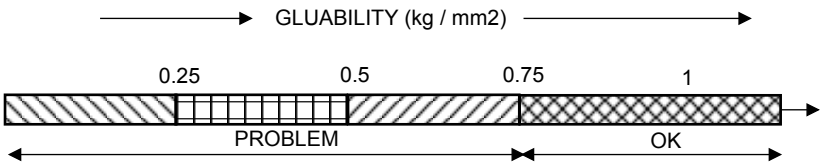


Figure 10. Gluability evaluation with a shear test



Various tests have shown that the glue shear test specification limit conforms to the IPC SM817 standard (0.75 kg/mm^2 minimum). Customer complaints usually happen when values are below 0.5 kg/mm^2. It has been verified that below 0.25 kg/mm^2 components fall from PCB during handling. General capability in plastic SMD is greater than 1 kg/mm^2.

6 Dry packing

The quality and reliability of SMDs after soldering depend heavily on moisture absorption during storage. A specific packing called dry pack was implemented for defined conditions at the delivery. Time and environment modify the amount of humidity absorbed. Moisture sensitive SMDs (SOP, PQFP, BGA, VFQFPN, UFQFPN, and WLCSP) are dry packed to protect them from moisture absorption during shipment / storage and then to reduce failure risks mainly due to popcorn effect.

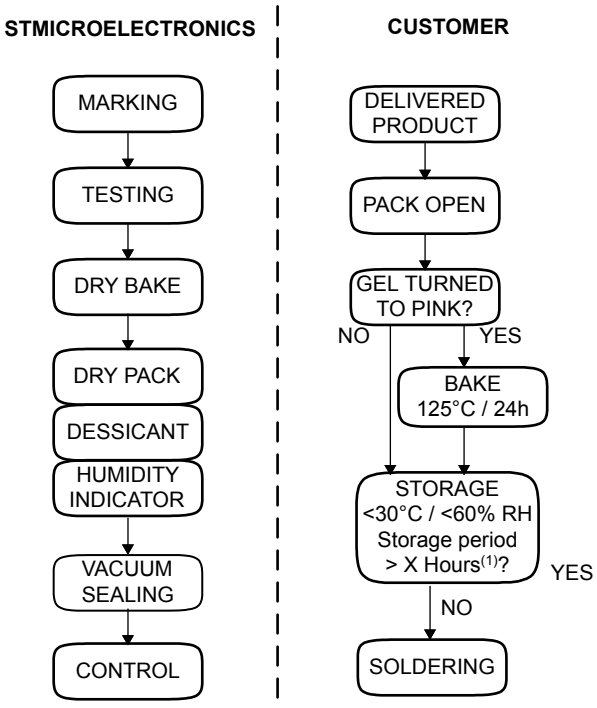
6.1 Pop-corn effect

Pop-corn effect is the cracking of the package during the soldering cycle. It has got a growing importance due to the trends towards larger die size in integrated circuits. This phenomenon is mainly caused by the moisture absorbed by the epoxy molding. When the package is exposed to high temperatures, as in most SMT soldering processes, the water at the interface between plastic and die pad vaporizes suddenly, generating high internal pressure. Cracks may occur in the molding compound depending on the absorbed moisture level, soldering temperature and time, die size, package structure and molding compound characteristics.

SMD products are contained in tubes, trays, or tapes, and are then vacuum-sealed in a hermetic bag.

Opening the package stops the ideal conditions and starts the influence of the normal environment. Figure 11 shows the recommended handling flow.

Figure 11. Recommended flow to control package moisture absorption



1. *X depends on the MSL (Moisture Sensitivity Level). See JEDEC standard J-STD-033D.*

It is recommended to store parts in dry pack in dry boxes (that is, cabinets under nitrogen atmosphere). See Table 9 for the recommended environmental conditions for storage when no dry boxes are available.

Table 9. Environmental conditions

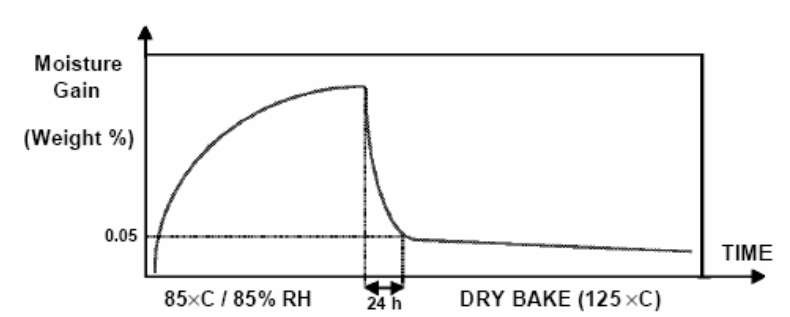
Condition	Recommended value
Temperature	5 → 30 °C
Humidity	60% RH max

Dust should also be minimized. There should be no vibration or shock, which could distort the packing container. To avoid excess weight packing, containers should not be stacked on top of each other.

6.2 Dry pack opening

After opening a dry pack, soldering should be done within 24 hours for optimal results. Otherwise, refer to MSL (Moisture Sensitivity Level) related floor life. SMD products stored over the specified storage period need to be baked at 125 °C for 24 hours (under nitrogen atmosphere). Devices packed in tubes or in tapes must be transferred to metal tubes before baking whereas trays can be baked.

Figure 12. Moisture absorption/drying curve



Revision history

Table 10. **Document revision history**

Date	Revision	Changes
16-Oct-2007	1	Initial release.
26-May-2009	2	Modified t_L and t_{Pin} in Table 3. JEDEC standard lead-free reflow profile (according to J-STD-020D). Updated Figure 6. Recommended flow to control package moisture absorption.
22-May-2013	3	Updated Table 1. Package types and Table 2. Package/soldering process compatibility. Added UFQFPN and WLCSP packages in Section 6: Dry packing. Document converted to new template and disclaimer updated.
07-Jul-2014	4	Updated RoHS directive and related note in Section 1: Lead-free packages at STMicroelectronics.
17-May-2016	5	Updated maximum temperature during soldering in Section 2: Packages overview. Removed reference to application note AN2034 in Section 4.3: Compatibility with leaded soldering process. Updated humidity recommended value unit in Table 4. Environmental conditions.
27-Mar-2018	6	Table 2. Package/soldering process compatibility: • updated note 1. changed process for QFP packages
10-Oct-2019	7	Updated Section Introduction, title of Section 2: Packages overview, Table 1. Package types, Table 3. JEDEC standard lead-free reflow profile (according to J-STD-020D).
05-Nov-2024	8	Replaced ECOPACK by ECOPACK2. Removed PLCC package from the whole document. Updated Table 1. Package types and Table 2. Package/soldering process compatibility. Updated Section 4.4: Reflow soldering conditions..
03-Apr-2025	9	Added note on product state after reflow after Section 4.4: Reflow soldering conditions.
09-Jul-2026	10	Updated: • Section 2: Packages overview • Section 4.2: Soldering recommendations • Section 4.4: Reflow soldering conditions • Figure 11. Recommended flow to control package moisture absorption • Section 6.2: Dry pack opening Added: • Section 4.4.1: Convection reflow for SOIC packages • Section 4.4.2: Convection reflow for QFP packages • Section 4.4.3: Convection Reflow for QFN/DFN packages • Section 4.4.4: Convection reflow for BGA packages • Section 4.4.5: Convection reflow for LGA packages • Section 4.4.6: Convection reflow for WLCSP packages

Contents

List of tables

List of figures