AN2744
Application note

ST7538Q power line FSK transceiver dual channel reference design for AMR

Introduction

The ST7538Q dual channel reference design is a practical tool to start the activity of designing an automatic meter reading (AMR) node based on the ST7538Q power line FSK transceiver.

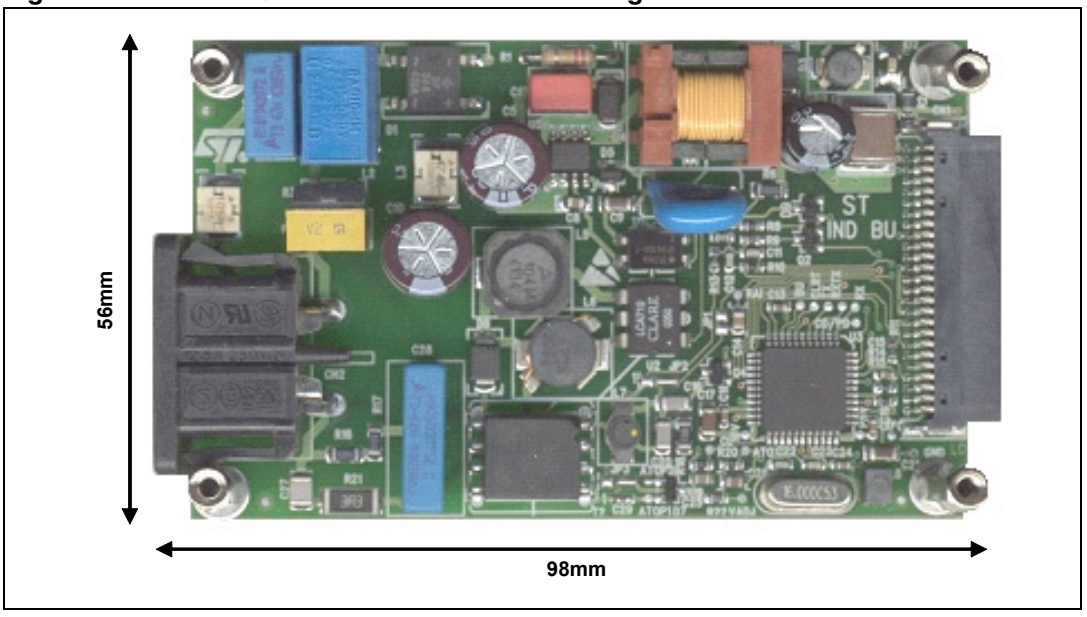
With this reference design, it is possible to evaluate the features of the ST7538Q and its transmitting and receiving performances in an actual communication on the power line network.

The ST7538Q reference design can be considered as composed of three main sections:

- power supply section, specifically designed to coexist with power line communication and to operate from a wide-range input mains voltage
- modem and crystal oscillator section
- dual channel line coupling interface section

The dual channel line coupling interface allows the ST7538Q FSK transceiver to transmit and receive on the mains using two different carrier frequencies: 72 kHz and 86 kHz, both within the frequency band A specified by the European CENELEC EN50065 standard for AMR applications.

Figure 1. ST7538Q dual channel reference design board with outline dimensions



As it can be seen from the picture above, a special effort has been made to develop a compact reference design board, oriented to practical applications.

Note: The information provided in this application note refers to the EVALST7538DUAL reference design board.

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1 Electrical characteristics

Table 1. Electrical characteristics of the ST7538Q dual channel reference design

Parameter	Value			Notes
	Min.	Typ.	Max.	
Operating condition				
Ambient operating temperature			85 °C	If junction temperature exceeds 180 °C the device shuts down
Transceiver section				
Selectable channel frequencies: 72 kHz (CH1), 86 kHz (CH2)				
Transmitting specifications (Tx Mode)				
Transmitting output voltage level		2 V_{RMS}	2.25 V_{RMS}	R20 = 3.9 kΩ, R22=2.2 kΩ – see *Table 2*
Transmitting output current limit		325 mA_{RMS}		R19 = 2 kΩ – see *Figure 2*
Second harmonic distortion			-55 dB	Loaded with CISPR 16-1 network
Third harmonic distortion			-61 dB	Loaded with CISPR 16-1 network
50 Hz attenuation		100 dB		
Receiving specifications (Rx Mode)				
Minimum detectable Rx signal		53 $dB/\mu V_{RMS}$		BER<10^{-3}, negligible noise
Auxiliary supply				
5 V linear regulator (VDC) output voltage	-5%	5.05 V	+5%	ST7538Q internally generated
5 V linear regulator (VDC) current capability			100 mA	
Power supply section				
AC mains voltage range	85 V		265 V	
Mains frequency		50-60 Hz		
Output voltage	-10%	10 V	+10%	Green LED ON
Output voltage ripple			1%	I_{OUT} = 600 mA, V_{IN}=85 V_{AC}
Output current			600 mA	
Output power			5.6 W	
Efficiency at P_{OUT} = 3.5 W		70%		
Nominal transformer isolation(1)		4 kV		Primary to secondary/ secondary to auxiliary
Number of holdup cycles		0		

Table 1. Electrical characteristics of the ST7538Q dual channel reference design (continued)

Parameter	Value			Notes
Input power	100 mW			
Switching frequency	-10%	60 kHz	+10%	Transceiver section in Tx mode

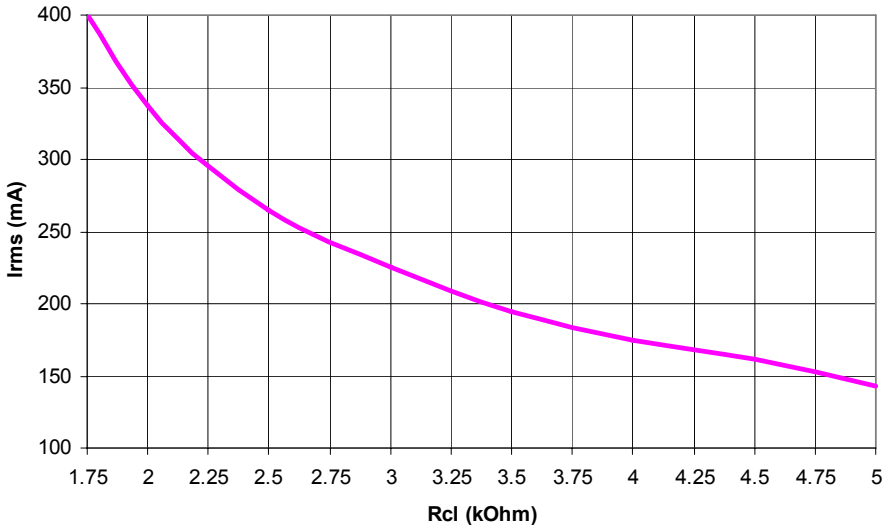
1. ST does not guarantee transformer isolation. ST assumes no responsibility for the consequences that may result from that risk.

Table 2. Output signal level setting through V_{SENSE} partitioning - typical values

V_{OUT} [V_{RMS}]	V_{OUT} [dBuV_{RMS}]	(R_7 + R_8) / R_8	R_7 [kΩ]	R_8 [kΩ]
1.000	120	1.25	0.910	2.2
1.125	121	1.4	1.3	2.2
1.250	122	1.6	2.2	2.2
1.500	124	2.0	2.7	2.2
1.800	125	2.25	3.3	2.2
2.000	126	2.5	3.9	2.2
2.250 (*Note 1*)	127	2.8	4.7	2.2
2.500 (*Note 1*)	128	3.15	6.8	2.2
3.000 (*Note 1*)	130	4.0	7.5	2.2

Note: 1 EN50065-1 normative compliance is not guaranteed with a signal level at mains output greater than 2 V_{RMS}

Figure 2. Typical curve for output current limit vs. R_{CL} value



2 Safety precautions

The board must be used only by expert technicians. Due to the high voltage (220 V ac) present on the parts which are not isolated, special care should be taken with regard to people's safety.

There is no protection against high voltage accidental human contact.

After disconnection of the board from the mains, none of the live parts should be touched immediately because of the energized capacitors.

It is mandatory to use a mains insulation transformer to perform any tests on the high voltage sections (see circuit sections highlighted in *Figure 7* and *Figure 8*) in which test instruments like spectrum analyzers or oscilloscopes are used.

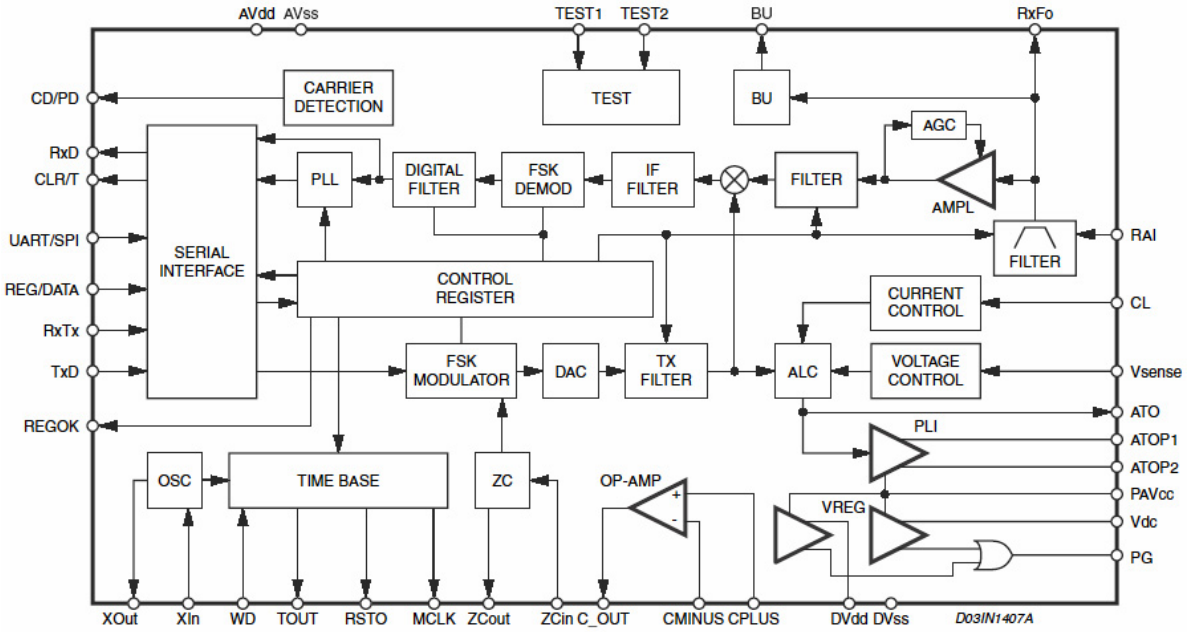
Do not connect any oscilloscope probes to high voltage sections in order to avoid damaging instruments and demonstration tools.

Warning: ST assumes no responsibility for any consequences which may result from the improper use of this tool.

3 ST7538Q FSK power line transceiver description

The ST7538Q transceiver performs a half-duplex communication over the power line network using frequency shift keying (FSK) modulation. It operates from a 7.5 to 12.5 V single supply voltage (PAV_{CC}) and integrates a differential-output power line interface (PLI) stage and two linear regulators providing 5 V (VDC) and 3.3 V (DV_{DD}).

Figure 3. ST7538Q transceiver block diagram



The ST7538Q can be programmed to communicate using eight different frequency channels (60, 66, 72, 76, 82.05, 86, 110 and 132.5 kHz), four baud rates (600, 1200, 2400 and 4800 symbols per second) and two frequency deviations (1 and 0.5).

Many auxiliary functions are integrated. The transmission section includes automatic control on PLI output voltage and current, programmable time-out function and thermal shutdown. The reception section includes automatic input level control, carrier/preamble detection and band-in-use signaling.

Additional features are included, such as watchdog timer, zero-crossing detector, internal oscillator and a general purpose op-amp.

The serial interface (configurable as UART or SPI) allows interfacing to a host microcontroller, intended to manage the communication protocol. A reset output (RSTO) and a programmable 4-8-16 MHz clock (MCLK) can be provided to the microcontroller to simplify the application.

Communication on the power line can be either synchronous or asynchronous with the data clock (CLR/T) provided by the transceiver at the programmed baud rate.

When in transmission mode (i.e. RxTx line at low level), the ST7538Q transceiver samples the data on the TxD line, generating an FSK modulated signal on the ATO pin. The same

signal is fed into the differential power amplifier to get four times the voltage swing and a current capability up to 370 mA rms.

When in reception mode (i.e. RxTx line at high level), an incoming signal at the RAI line is demodulated and converted to a digital bit stream on the RxD pin.

The internal control register, which contains the operating parameters of the ST7538Q transceiver, can be programmed only using the SPI interface. The control register settings include the header recognition and frame length count functions, which can be used to apply byte and frame synchronization to the received messages.

4 Evaluation tools description

The complete evaluation environment for the ST7538Q power line communication consists of:

- 1 PC using the "ST7538 power line modem demonstration kit" software tool
- 1 EVALCOMMBOARD hosting an ST7 microcontroller
- 1 ST7538Q dual channel reference design board (EVALST7538DUAL)

The correct procedure for connecting the EVALST7538DUAL and the EVALCOMMBOARD is as follows:

1. Connect the EVALST7538DUAL and the EVALCOMMBOARD together
2. Connect the ac cable to the EVALST7538DUAL and the USB cable to the EVALCOMMBOARD
3. Connect the EVALST7538DUAL to the mains supply
4. Connect the EVALCOMMBOARD to the PC via USB cable

Warning: Follow the connection procedure to avoid damaging the boards!

Figure 4. Complete evaluation system including a PC, an EVALCOMMBOARD and the EVALST7538DUAL board

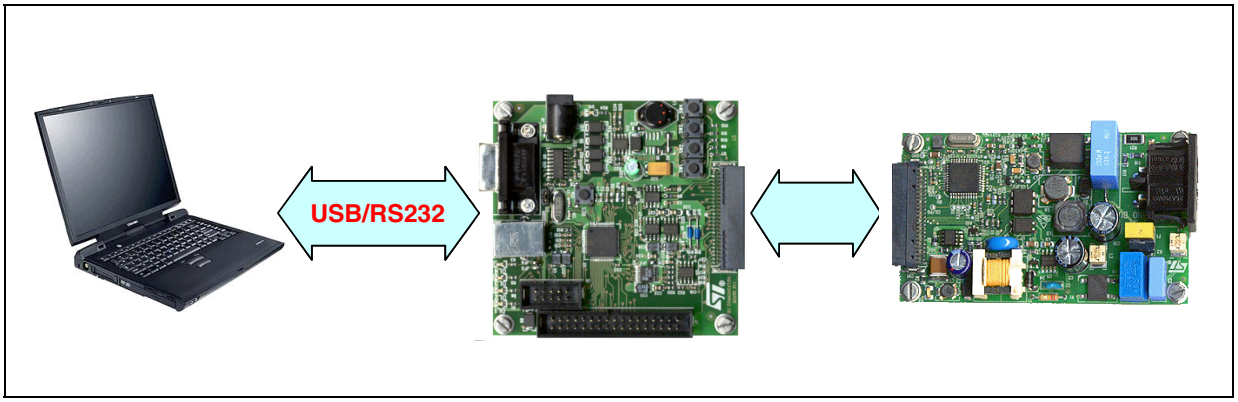
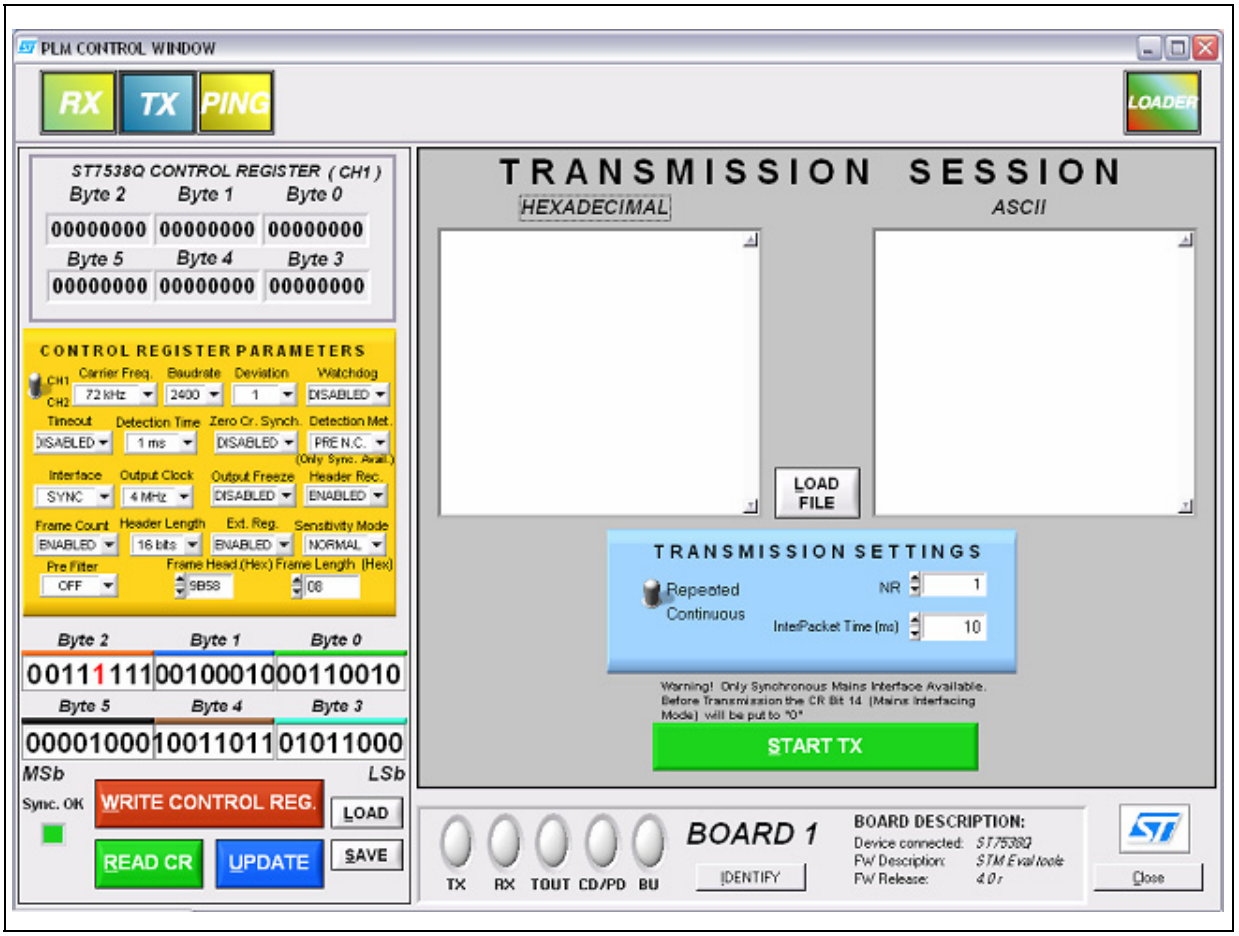


Figure 5. Power line modem demonstration kit with transmission session window



This complete communication node, controlled by the ST7538Q power line modem demonstration kit, implements real communication at bit level, simply sending or receiving a user-defined bit stream.

It is possible to establish a half-duplex communication between two of these communication nodes connected to each other. For better evaluating communication performances, the ST7538Q power line modem demo kit software tool has some particular features, including:

- **Frame synchronization**: a frame synchronization header can be added to the transmitted data to set up a simple protocol, intended to test the capability of the system to correctly receive the exact bit sequence as it has been transmitted. This feature can be enabled in the Rx panel of the ST7538Q power line modem demonstration kit. A bit synchronization can be introduced as a simpler feature by enabling the preamble detection method in the control register panel and then inserting at least one "0101" or "1010" sequence at the beginning of the bit stream to be transmitted.
- **Ping session**: a master-slave communication with automatic statistics calculation can be useful to test a point-to-point or a point-to-multipoint power line communication network, thus providing a method to evaluate reachability of each node in the network.

For further details about the ST7538Q power line modem demonstration kit tool, please refer to user manual UM0241 "ST7538 power line modem demonstration kit graphical user interface".

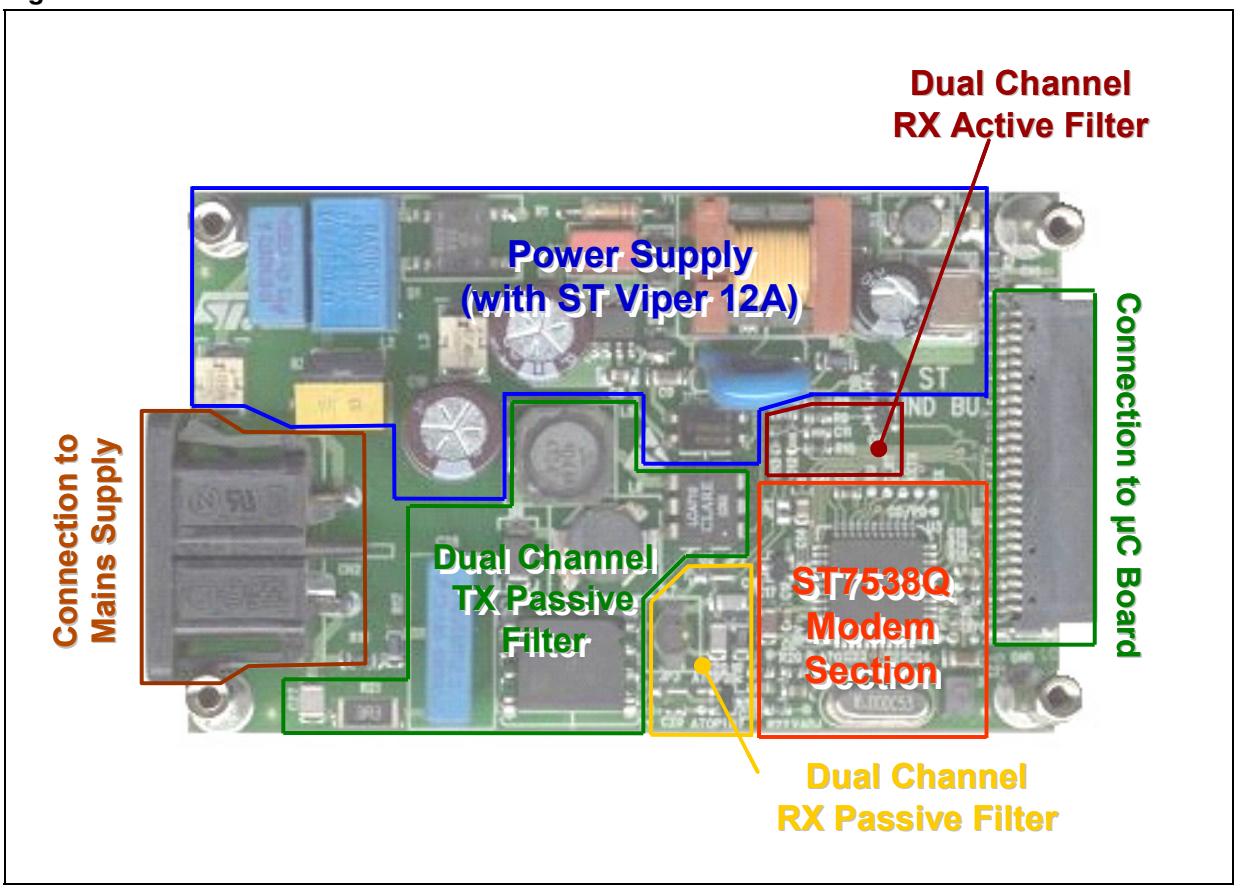
5 Board description

The ST7538Q dual channel reference design is composed of the following sections:

- power supply section, based on ST's VIPer12A-E IC
- ST7538Q modem and crystal oscillator section
- line coupling interface section, with three subsections:
  - dual channel transmission passive filter
  - dual channel reception passive filter
  - dual channel reception active filter

The board has also two connectors, which allow the user to plug the mains supply on one side of the board and the IBU communication board on the other side.

Figure 6. Scheme of the various sections of the board



The schematics of the whole reference design are given in the following pages. *Figure 7* shows the modem and coupling interface circuits, while *Figure 8* represents the power supply circuit. In both schematics, high voltage regions are highlighted.

Table 3 lists the components used to develop the reference design board. All parts have been selected to give optimal performances.

The layout of the printed circuit is shown in *Appendix A* - *Figure 50* and *Figure 51*.

Figure 7. Modem and coupling interface schematic

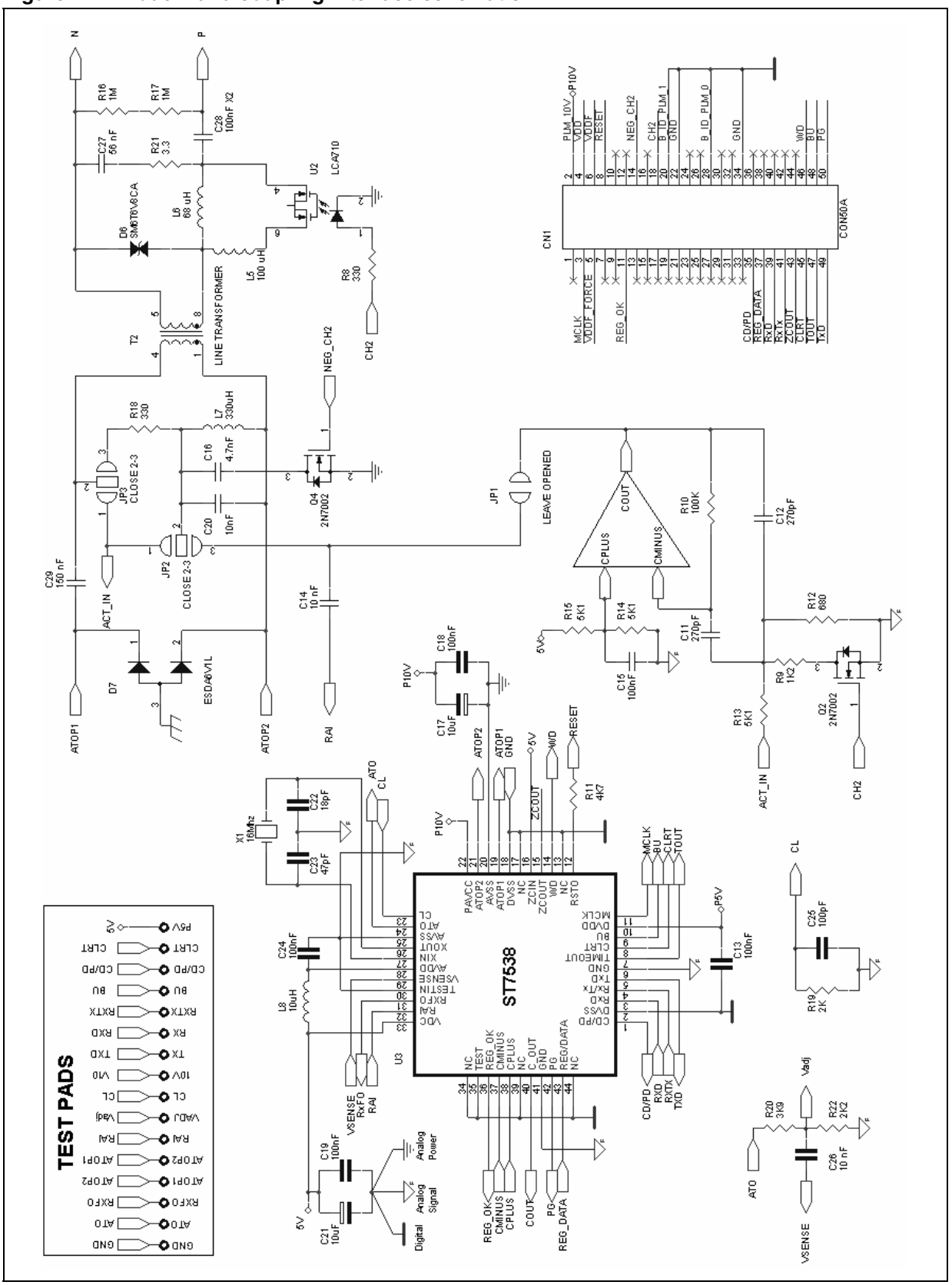


Figure 8. Power supply schematic

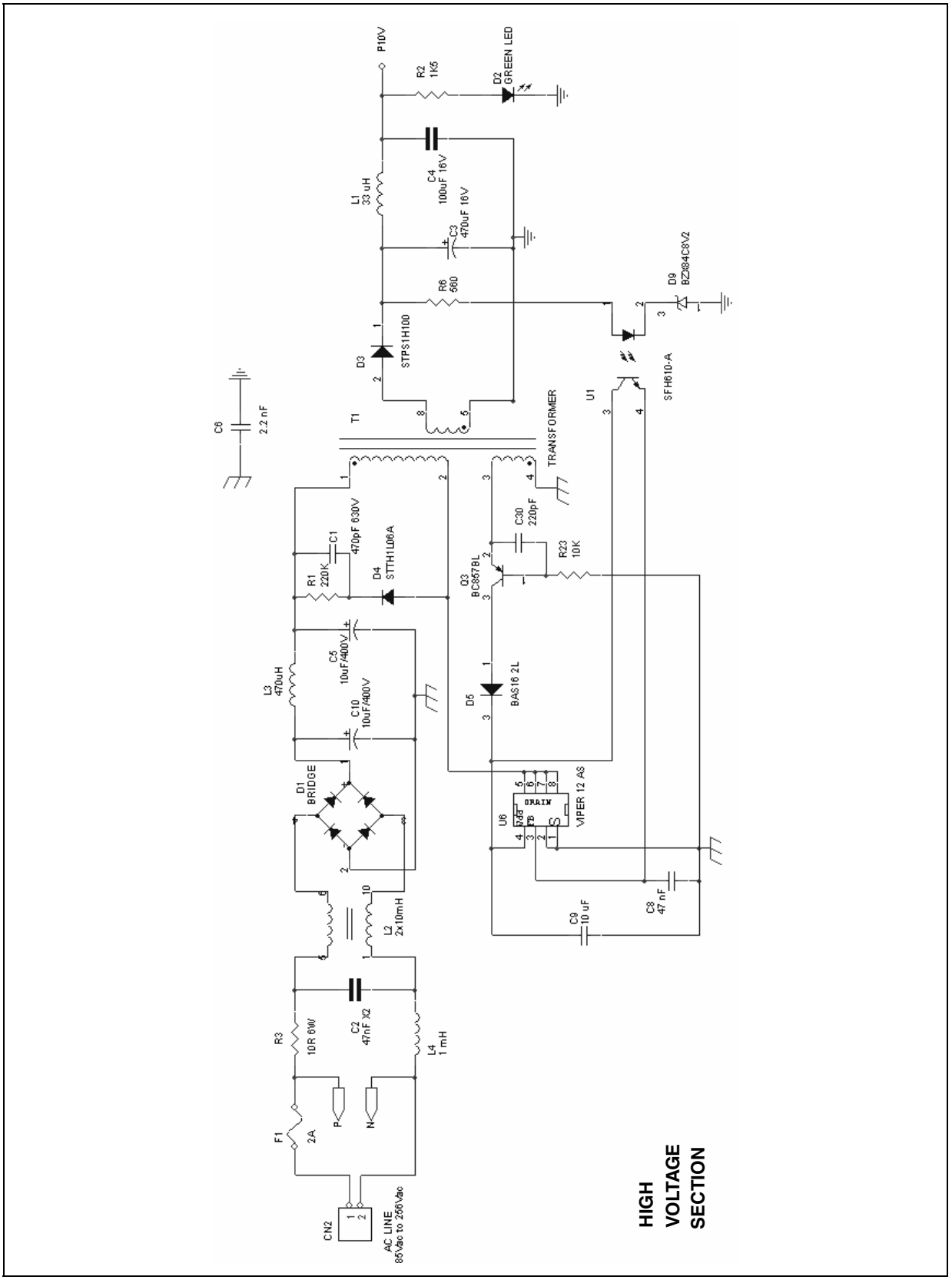


Table 3. Bill of materials

Item	Q.ty	Reference	Value	Description
1	16	ATOP1, ATOP2, P5 V, 10 V, VADJ, TX, RXTX, RXFO, RX, RAI, GND, CLRT, CL, CD/PD, BU, ATO	Test point	
2	1	CN1	CON50A	50-pin female connector
3	1	CN2	Header 2	Mains supply connector
4	1	C1	470 pF 630 V	EVOX-RIFA PFR5-471J630L4
5	1	C2	47 nF X2	Epcos B32921-A2473K
6	1	C3	470 µF 16 V electrolytic	Rubycon YK / Yageo SE-K / Nichicon VK
7	1	C4	100 µF 16 V	TDK CKG57DX7R-1C107M
8	2	C5,C10	10 µF 400 V electrolytic	Yageo SE-K / Nichicon VK
9	1	C6	2.2 nF Y2	TDK CD12E2GA222MYNS
10	1	C8	47 nF	
11	3	C9,C17,C21	10 µF	TDK C3216X7R-1C106M
12	2	C11,C12	270 pF	
13	5	C13,C15,C18,C19,C24	100 nF	
14	2	C14,C26	10 nF	
15	1	C16	4.7 nF	
16	1	C20	10 nF	
17	1	C22	18 pF	
18	1	C23	47 pF	
19	1	C25	100 pF	
20	1	C27	56 nF 50 V	
21	1	C28	100 nF X2 10%	Epcos B32922-A2104K
22	1	C29	150 nF	
23	1	C30	220 pF	
24	1	D1	DF06S	600 V - 1.5 A bridge rectifier
25	1	D2	Green LED	
26	1	D3	STPS1H100	
27	1	D4	STTH1L06A	
28	1	D5	BAS16 2L	BAS21 also suitable
29	1	D6	SM6T6V8CA	6.8 V bidirectional Transil™ diode
30	1	D7	ESDA6V1L	6.1 V ESD Transil™ diode
31	1	D9	BZX84C8V2	8.2 V Zener diode
32	1	F1	FUSE	2 A time-lag (T)

Table 3. Bill of materials (continued)

Item	Qty	Reference	Value	Description
33	1	JP1	Jumper	Leave open
34	2	JP2, JP3	Jumper	Close 2-3
35	1	L1	33 µH	Epcos B82462-A4333K
36	1	L2	2x10 mH - 0.3 A	Radiohm 42V15-0307
37	1	L3	470 µH	Epcos B82442-A1474K
38	1	L4	1 mH	Epcos B82442-H1105K
39	1	L5	100 µH 10%	Würth 744-775-210K / Epcos B82464-A4104K
40	1	L6	68 µH 10%	Würth 744-775-168K / Epcos B82464-A4683K
41	1	L7	330 µH 10%	Würth 744-774-233K
42	1	L8	10 µH	Epcos B82432-T1103K
43	2	Q2, Q4	2N7002	
44	1	Q3	BC857BL	
45	1	R1	220 kΩ	
46	1	R2	1K5	
47	1	R3	10R 1 W	Metal oxide - radial
48	1	R6	560	
49	2	R8, R18	330	
50	1	R9	1K2	
51	1	R10	100 kΩ	
52	1	R11	4K7	
53	1	R12	680	
54	3	R13, R14, R15	5K1	
55	2	R16, R17	1M	
56	1	R19	2 kΩ	
57	1	R20	3K9	
58	1	R21	3R3	
59	1	R22	2K2	
60	1	R23	10 kΩ	
61	1	T1	SMPS transformer	TDK SRW12.6ES-ExxH013 / Würth S06-100-057
62	1	T2	Line transformer	VAC T60403-K5024-X044 / Radiohm 69H14-2101
63	1	U1	SFH610-A	Optoswitch
64	1	U2	LCA710	Optoswitch - 3750 V isolation
65	1	U3	ST7538Q	Power line transceiver
66	1	U6	VIPer12AS-E	SMPS controller / switch
67	1	X1	16 Mhz	Jauch Q 16.0-SS2-16-30/50-FU

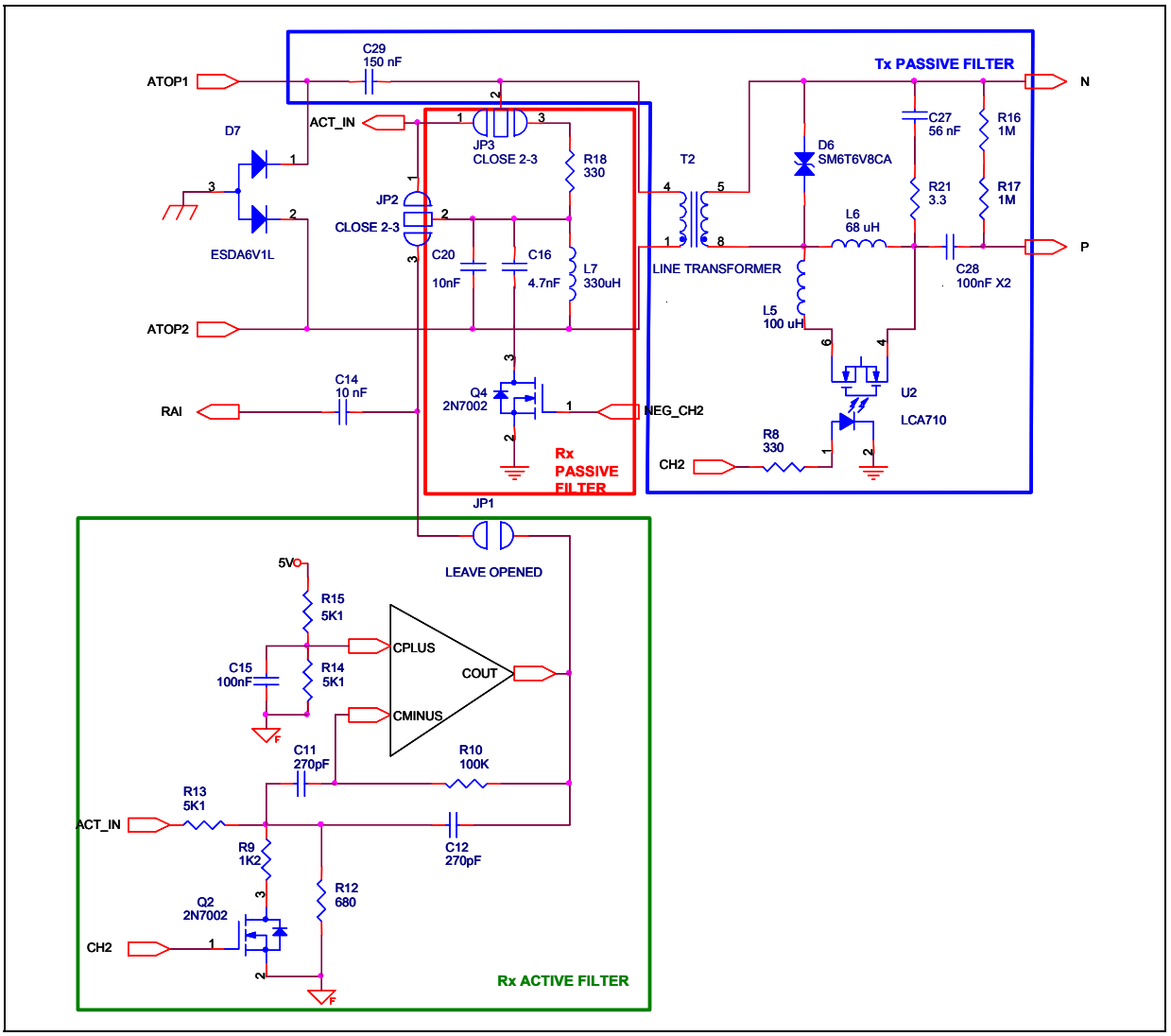
Table 4. ST parts on the ST7538Q dual channel reference design board

Value	Description
ST7538Q	Power line transceiver
VIPer12AS-E	SMPS controller / switch
STTH1L06A	Ultrafast diode
STPS1H100	Schottky diode
SM6T6V8CA	6.8 V bidirectional Transil™ diode
ESDA6V1L	6.1 V ESD Transil™ diode

5.1 Line coupling interface

The line coupling interface is composed of three different filters: the dual channel Tx passive filter, the dual channel Rx passive filter and the dual channel Rx active filter. The coupling interface structure is represented in *Figure 9*.

Figure 9. Schematic of Rx and Tx filters



All three filters are described in *Section 5.1.2*, *Section 5.1.3* and *Section 5.1.3*. For each filter, calculations and measured frequency responses are given.

The filters are quite sensitive to the components' value tolerance. Actual components used in the ST7538Q dual channel reference design have the following tolerances:

- +/- 10% for coils and for the X2 capacitor
- +/- 1% for SMD resistors
- +/- 5% for SMD ceramic capacitors

To evaluate sensitivity to the tolerances indicated above, the following sections include simulated responses of the filters with Montecarlo statistical analysis. Statistical simulation helps to understand the relationship between tolerance of components' value and variations

on frequency response of the filters. In simulation curves, the ideal response is drawn in blue, while red curves indicate statistical variations generated through simulation.

5.1.1 Dual channel selection

To obtain a dual channel interface, each filter is tunable via software command. The ST7538Q dual channel reference design has two available channel frequencies, 72 and 86 kHz.

The channel can be simply changed by including or excluding one passive component per each filter: an inductor for the Tx filter, a capacitor for the Rx passive filter and a resistor for the Rx active filter.

5.1.2 Dual channel Tx passive filter

The dual channel Tx passive filter is made of the following parts: DC-decoupling capacitor C29, line transformer T2, inductors L5 and L6 and X2 safety capacitor C28, plus a shunt branch made of R21 and C27.

The center frequency for the series resonance is calculated with good approximation as:

Equation 1

$$f_C = \frac{1}{2\pi \cdot \sqrt{L_P \cdot C_P}}$$

where C_P = C29(C27+C28)/(C27+C28+C29) and L_P is equal to: L6 for 72 kHz channel, L6 // L5 for 86 kHz channel. To guarantee adequate filtering action on signal harmonics, it is required to set the center frequency at a value lower than the one of the channel frequency. See *Figure 10* and *Figure 11* to check the resulting measured frequency response.

L5 and L6 have been accurately chosen to have high saturation current (> 1 A) and low equivalent series resistance (< 0.5 Ω), to limit distortion and insertion losses.

R21 is intended to damp resonance, to better control filtering action and getting desired rejection on transmitted signal harmonics.

Resonance shape is also affected by the ratio between the two capacitors C27 and C28. C27 must be smaller than C28 (in this case, about half the value of C28) to get lower insertion losses when the line impedance is very low.

To optimize the coupling efficiency, particular attention must be paid to the line transformer. The required characteristics are listed in *Table 5*.

In order to have a good power transfer and to minimize the insertion losses, it's recommended to choose a transformer with a primary (magnetizing) inductance greater than 1mH and a series resistance lower than 0.5 Ω.

Another important parameter is the leakage inductance. If it has a relevant value (10 to 50 µH), this can be used to design the coupling filter without adding series inductance (L5, L6). The drawback is that this parameter is usually affected by poor accuracy which can lead to a drift on the filter response and then to bad coupling.

Consequently, a low leakage inductance value (<1 µH) has been chosen. The series inductance is fixed through discrete components, resulting in a greater accuracy.

The last parameter specified in the table, the 4 kV insulation voltage requirement, is described and codified by the EN50065-4-2 CENELEC document.

Table 5. Line coupling transformer specifications

Parameter	Value
Turn Ratio	1:1
Magnetizing Inductance	> 1 mH
Leakage Inductance	< 1 µH
DC total resistance	< 0.5 Ω
DC saturation current	> 2 mA
Interwinding capacitance	< 50 pF
Withstanding Voltage	4 kV

Figure 10 and *Figure 11* show the measured response of the filter for both channels, loaded with the CISPR reference network and with 5 Ω impedance. When loaded with the CISPR network, the Tx passive filter gives an almost flat gain of nearly 3.5 dB around the transmission carrier frequency. Applying a heavier load makes the frequency response sharper and the gain at carrier frequency lower. This effect leads to a loss of about 7-8 dB with a 5 Ω load for both channels.

Figure 10. Measured frequency response of the Tx passive filter for 72 kHz channel (typical)

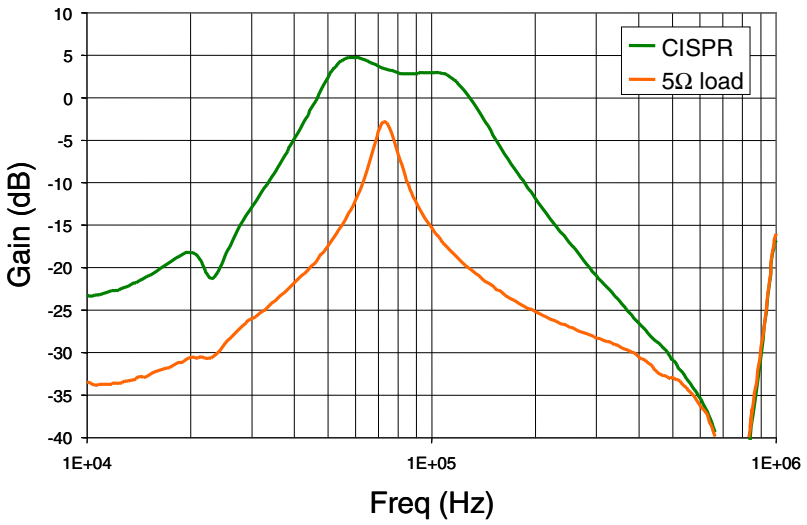
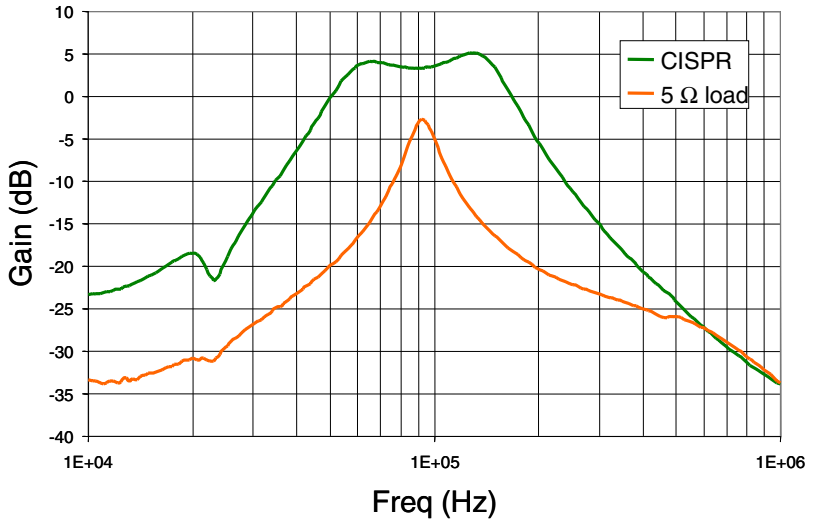


Figure 11. Measured frequency response of the Tx passive filter for 86 kHz channel (typical)



Simulations of the filter for both frequency channels, given in *Figure 12* and *Figure 13*, show limited effect by the components' tolerance.

Figure 12. Simulated frequency response of the Tx passive filter for 72 kHz channel with tolerance effect

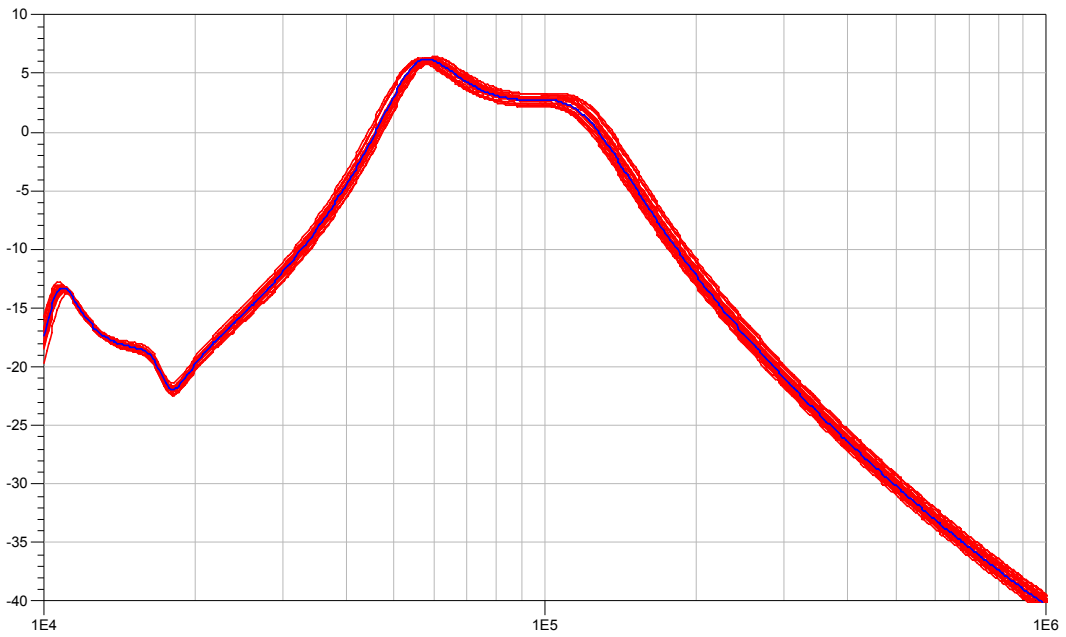
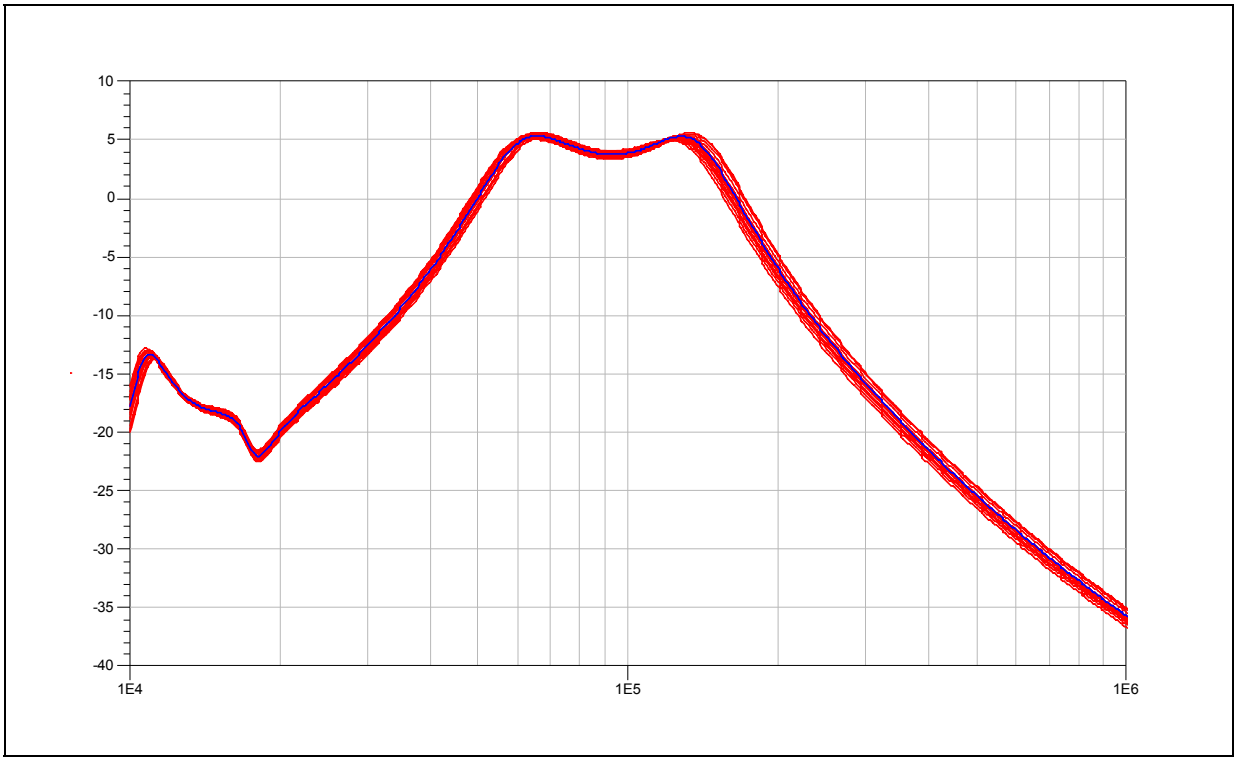


Figure 13. Simulated frequency response of the Tx passive filter for 86 kHz channel with tolerance effect



5.1.3 Dual channel Rx passive filter

The dual channel Rx passive filter is made of a resistor in series with a parallel L-C resonant circuit. The transfer function of the filter can be written as:

Equation 2

$$R(s) = \frac{\frac{s \cdot L_7 + R_L}{R_{18} \cdot L_7 \cdot C_P}}{s^2 + \frac{R_{18} \cdot R_L \cdot C_P + L_7}{R_{18} \cdot L_7 \cdot C_P} \cdot s + \frac{R_{18} + R_L}{R_{18} \cdot L_7 \cdot C_P}}$$

where R_L is the dc series resistance of the inductor L7 (in the worst case, 2 Ω) and C_P is the equivalent capacitance for the two channels: C16 + C20 for 72 kHz, only C20 for 86 kHz.

The center frequency and the quality factor of the filter can be expressed as:

Equation 3

$$fc = \frac{1}{2\pi} \cdot \omega_C = \frac{1}{2\pi} \sqrt{\frac{R_{18} + R_L}{R_{18} \cdot L_7 \cdot C_P}} \cong \frac{1}{2\pi\sqrt{L_7 \cdot C_P}}$$

The simplification done in *Equation 3* is possible because $R_{18} >> R_L$. It's evident that the quality factor, and then the filter selectivity, depends not only on the value of R_{18}, but also on R_L. A higher R_L means a lower steepness of the resonance, while a higher R_{18} gives a

higher selectivity. The values of the actual components give a Q of about 2.2 for the 72 kHz channel and 1.8 for the 86 kHz channel.

The value of R_L impacts more obviously on insertion losses. To evaluate the relationship between R_L and the losses on received signal, the following simplified expression of $|R_{(s)}|$ at $f = f_c$ can be used:

Equation 4

$$\left|R(j \cdot 2\pi f_C)\right| \cong Q \cdot \frac{\omega_C \cdot L_7}{R_{18}} = \frac{1}{1 + R_L \cdot R_{18} \cdot \frac{C_P}{L_7}}$$

With the chosen components, this formula gives a loss always lower than 1 dB. The same calculation gives unitary transfer if R_L is set to zero.

Looking at the first way to express the module of the transfer function, it can be noticed that a higher Q can help to keep the losses small. A high Q would bring to a higher sensitivity of the filter to tolerance of the components.

Figure 14 and *Figure 15* show the measured frequency response of the Rx passive filter for the two channels. The filter has an attenuation of about 5 dB at center frequency. This loss is mostly due to the Tx filter topology, in particular to the R21-C27 branch that is in parallel to the Rx path.

Figure 14. Measured frequency response of the Rx passive filter for 72 kHz channel (typical)

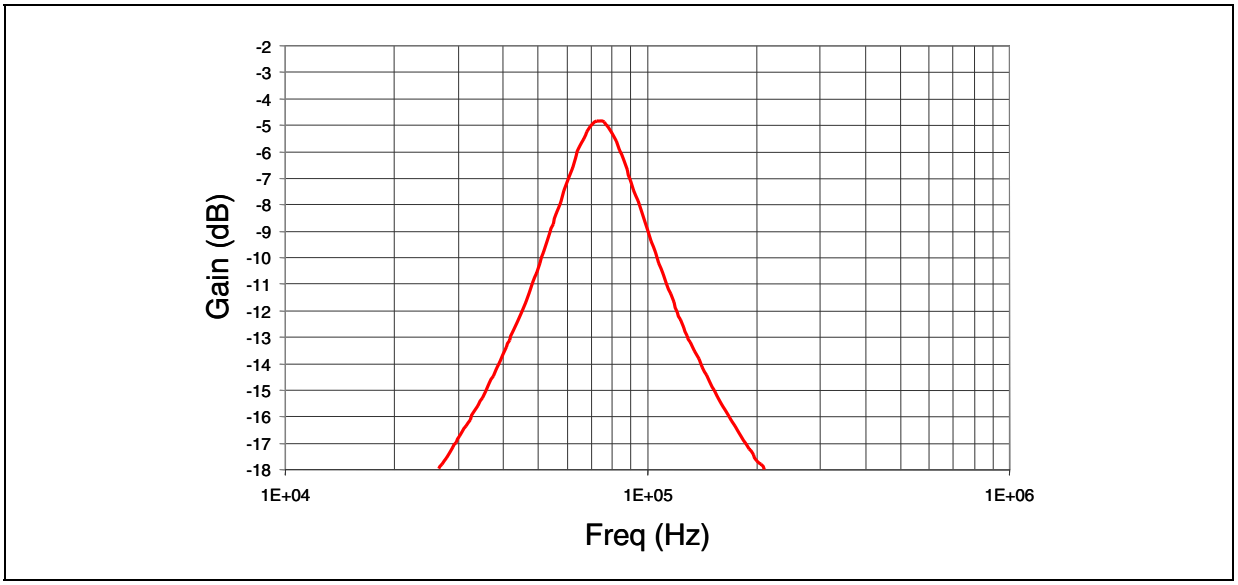
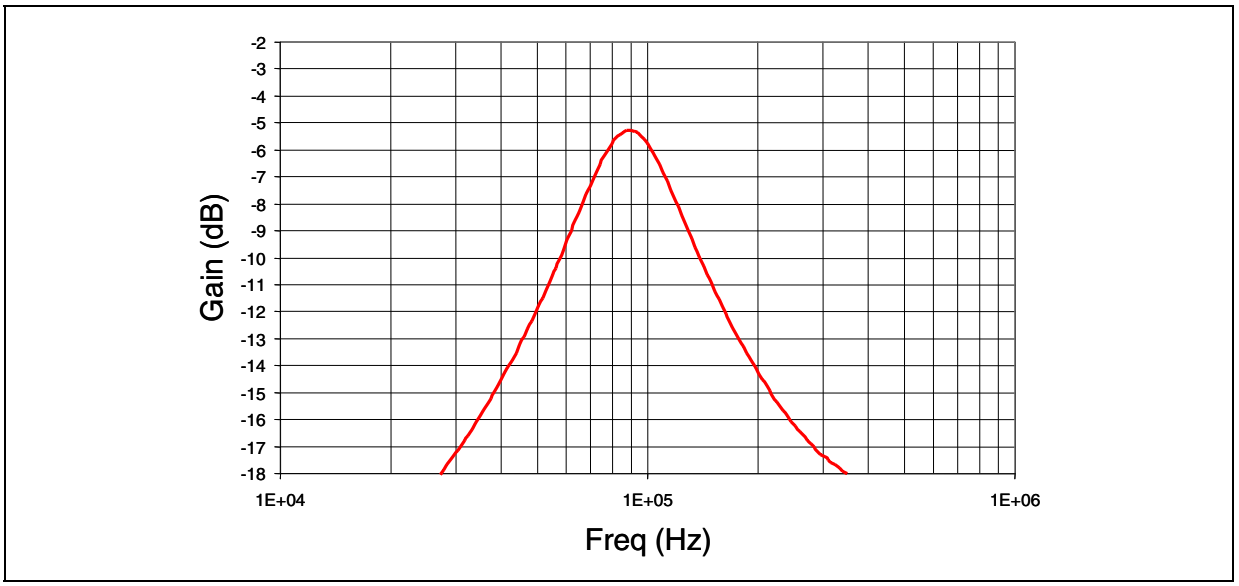


Figure 15. Measured frequency response of the Rx passive filter for 86 kHz channel (typical)



It can be observed from the simulation curves of *Figure 16* and *Figure 17* a maximum loss at center frequency of 1 dB due to the spread of the components' value.

Figure 16. Simulated frequency response of the Rx passive filter for 72 kHz channel with tolerance effect

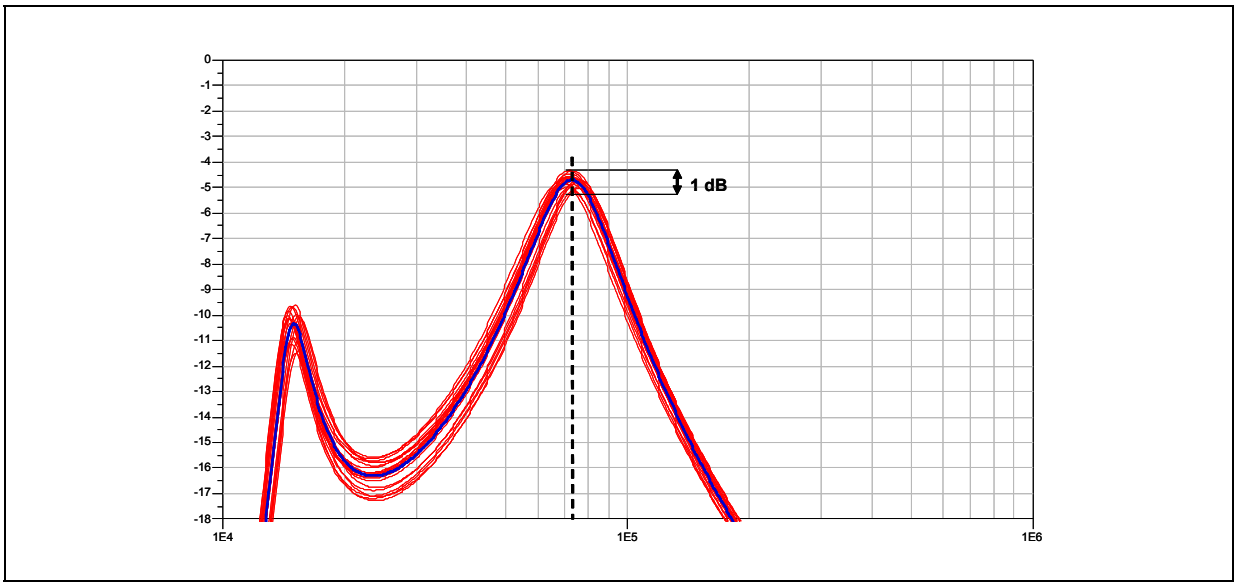
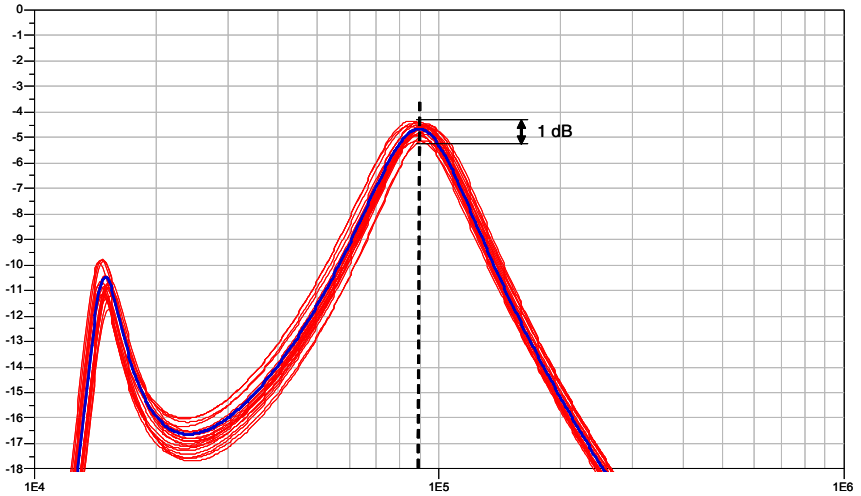


Figure 17. Simulated frequency response of the Rx passive filter for 86 kHz channel with tolerance effect



5.1.4 Dual channel Rx active filter

An active filtering is suitable for receiving a highly attenuated signal. Without the gain of an active filter, it could be impossible to detect a signal lower than the ST7538Q receiving sensitivity even filtering the noise around it. Therefore, the choice of the Rx filter depends mostly on the attenuation introduced by the network and then on the point of insertion of the power line communication node.

It is possible to choose the received signal path on the board by configuring the three jumpers shown in *Figure 9* (JP1, JP2 and JP3) in different ways. The Rx path can include only the passive filter, only the active filter, both of them or even none (no filtering).

Figure 18 and *Figure 19* show the measured transfer function of the Rx active filter for both channels. The curves show a 10 dB gain at center frequency and a -3 dB bandwidth of about 20 kHz.

Figure 18. Measured frequency response of the Rx active filter for 72 kHz channel (typical)

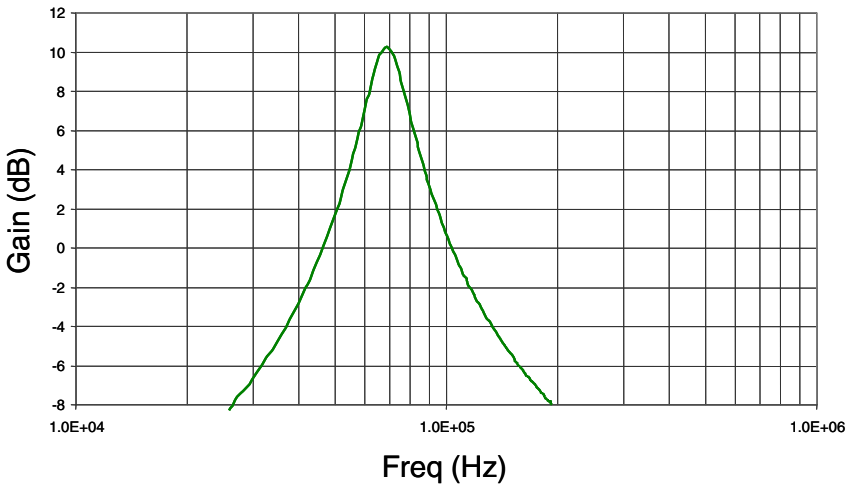


Figure 19. Measured frequency response of the Rx active filter for 86 kHz channel (typical)

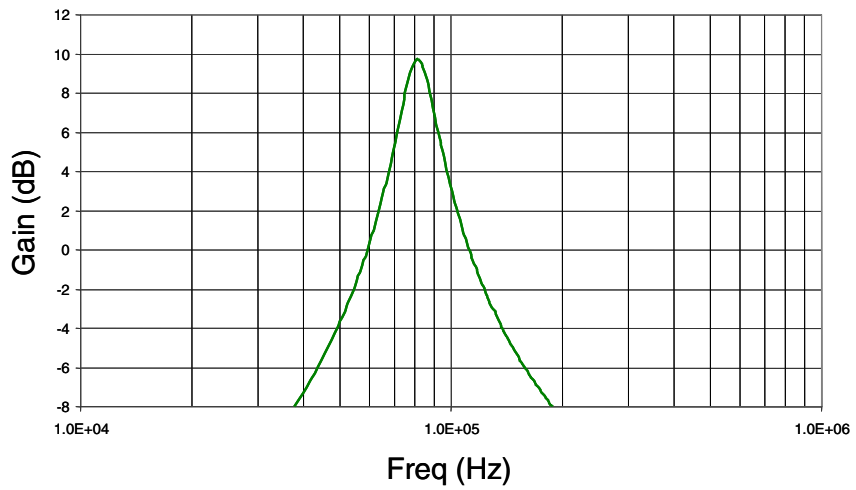


Figure 20 and *Figure 21* show the simulation results with Montecarlo analysis. The gain variation at center frequency is less than 2 dB.

Figure 20. Simulated frequency response of the Rx active filter for 72 kHz channel with tolerance effect

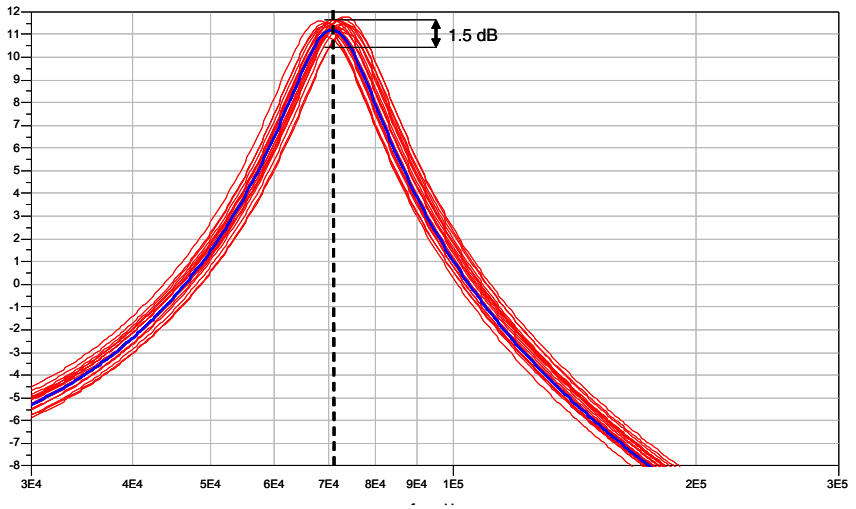
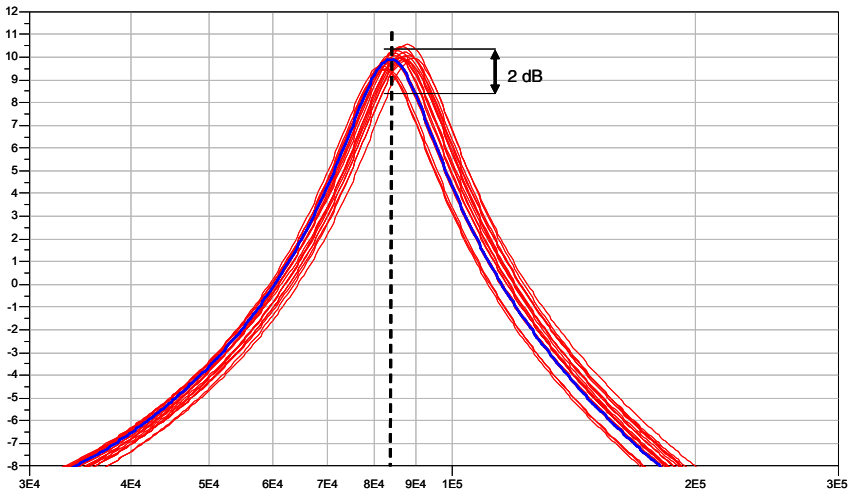


Figure 21. Simulated frequency response of the Rx active filter for 86 kHz channel with tolerance effect



5.1.5 Input impedance

The input impedance of a power line communication node is another critical point. *Figure 22* through *25* show the curves of input impedance magnitude vs. frequency in both Tx and Rx mode for the two channels.

The impedance magnitude values prove that the ST7538Q dual channel reference design board is compliant with EN50065-7 normative, which sets the following minimum impedance constraints for this kind of equipment:

– Tx mode: free in the range 3 to 95 kHz, 3 Ω from 95 to 148.5 kHz
– Rx mode: 10 Ω from 3 to 9 kHz, 50 Ω between 9 and 95 kHz only inside signal 20 dB-bandwidth (free for frequencies outside signal bandwidth), 5 Ω from 95 to 148.5 kHz

Figure 22. Measured input impedance magnitude of the coupling interface in Rx mode for the 72 kHz channel (typical curve)

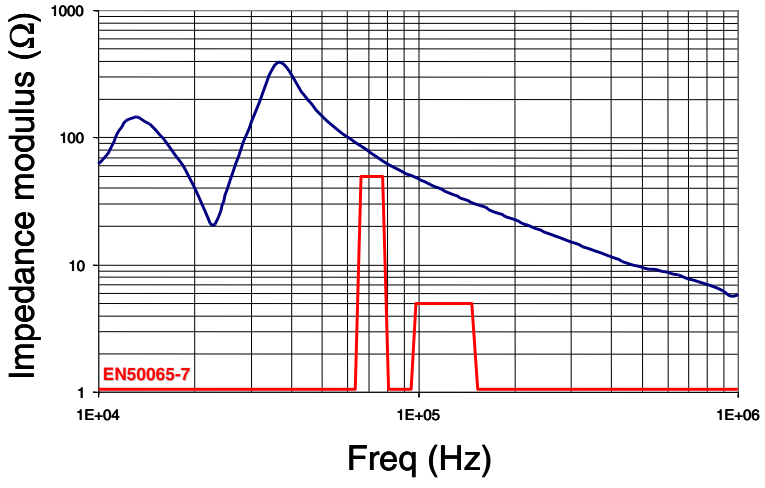


Figure 23. Measured input impedance magnitude of the coupling interface in Rx mode for the 86 kHz channel (typical curve)

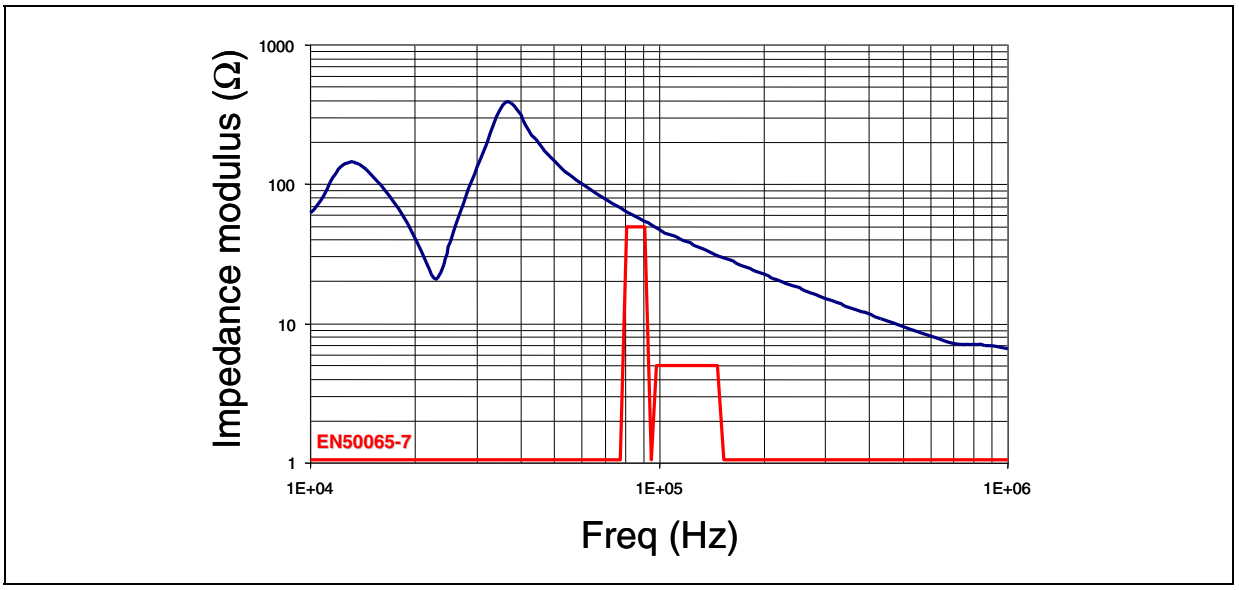


Figure 24. Measured input impedance magnitude of the coupling interface in Tx mode for the 72 kHz channel (typical curve)

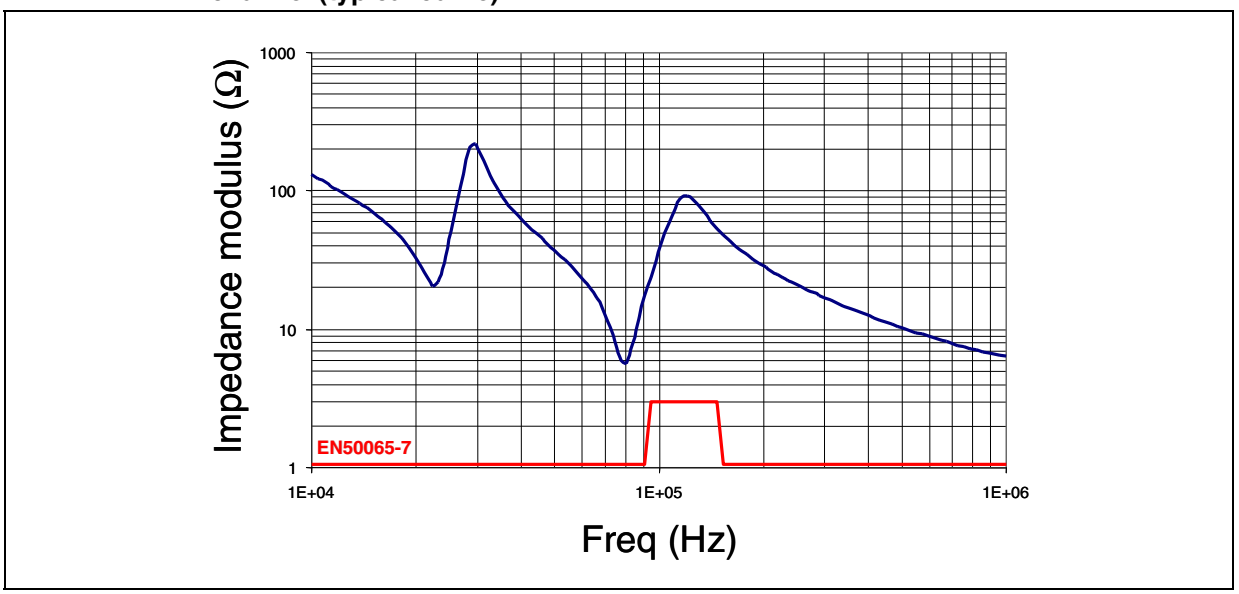
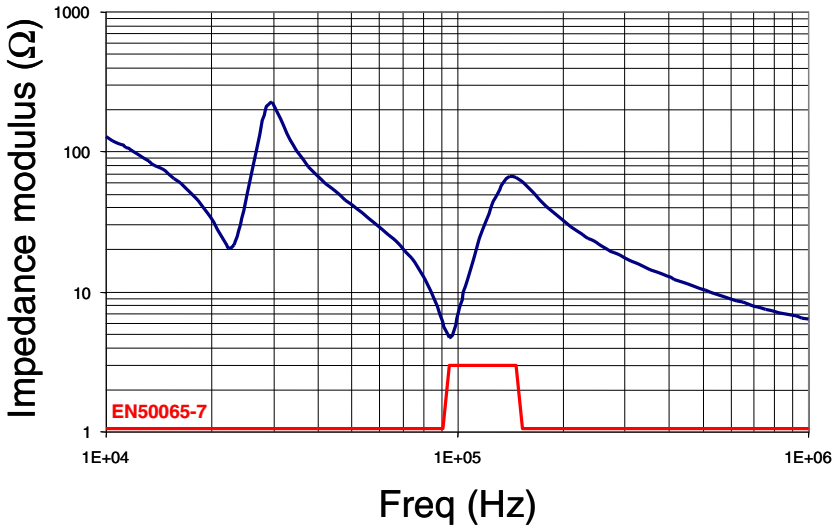


Figure 25. Measured input impedance magnitude of the coupling interface in Tx mode for the 86 kHz channel (typical curve)



5.2 Conducted disturbances

5.2.1 Conducted emissions

The EN50065-1 standard describes test setup and procedures for this kind of test.

The measures have been done with 220 VAC mains voltage. The test pattern consists of a continuous transmission of a fixed tone at a frequency of 70.8 kHz (72 kHz center frequency minus half the FSK frequency deviation, in this case 2400 Hz) which corresponds to a symbol "1".

The output signal measured at the artificial network has a value of 120 dBµV rms, which means a 2 V rms signal on the mains output of the board.

The spectrum analyzer performs a peak measure instead of a quasi-peak measure. For continuous sinusoidal signals, the two types of measurement give the same result.

Figure 26. Conducted disturbance test setup

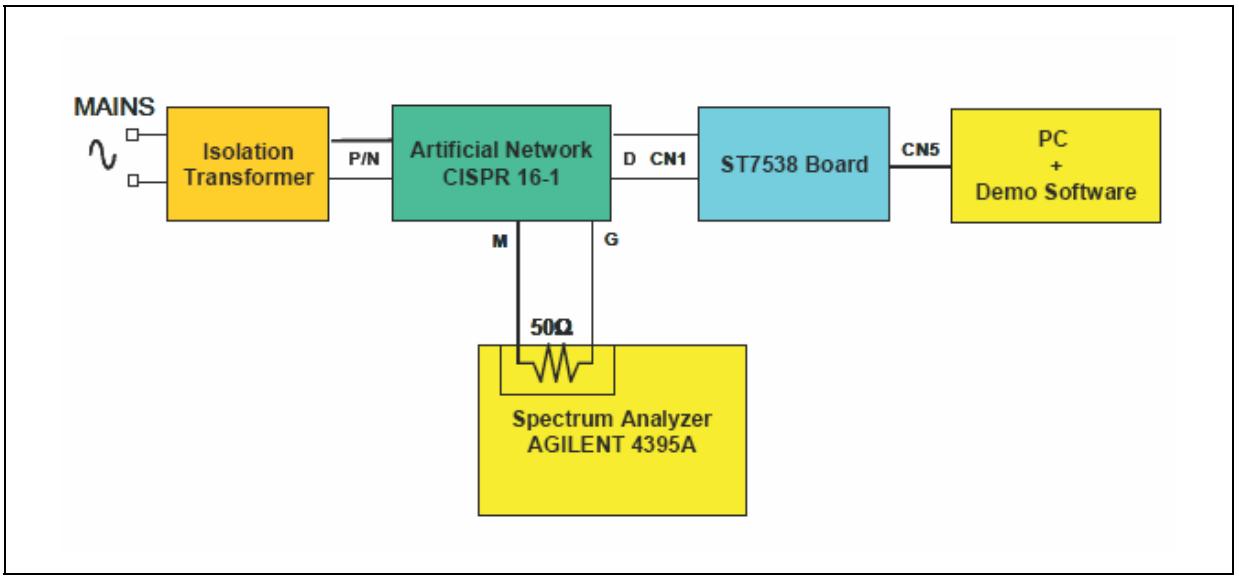


Figure 27 and *Figure 28* show the results for the output spectrum measurement. The EN50065-1 disturbance limits mask is traced in red. It may be compared with the typical output spectrum of the ST7538Q dual channel reference design board for each channel.

Figure 27. Output spectrum (typical) at 72 kHz channel, mains 220 V_{AC}, fixed transmitted tone = "1"

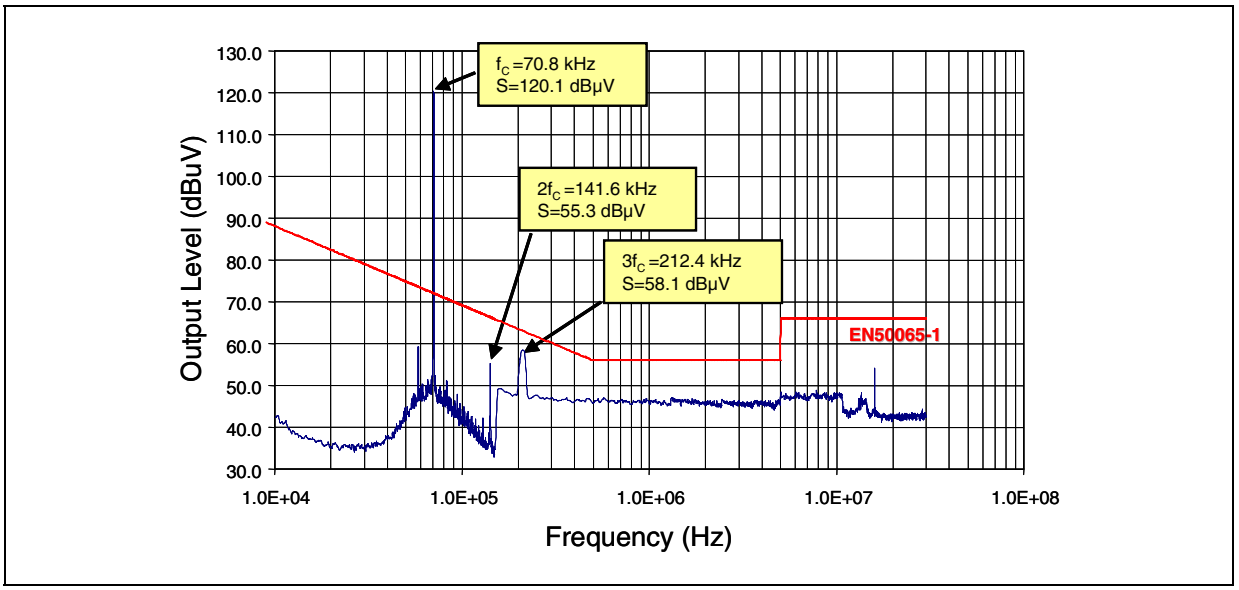
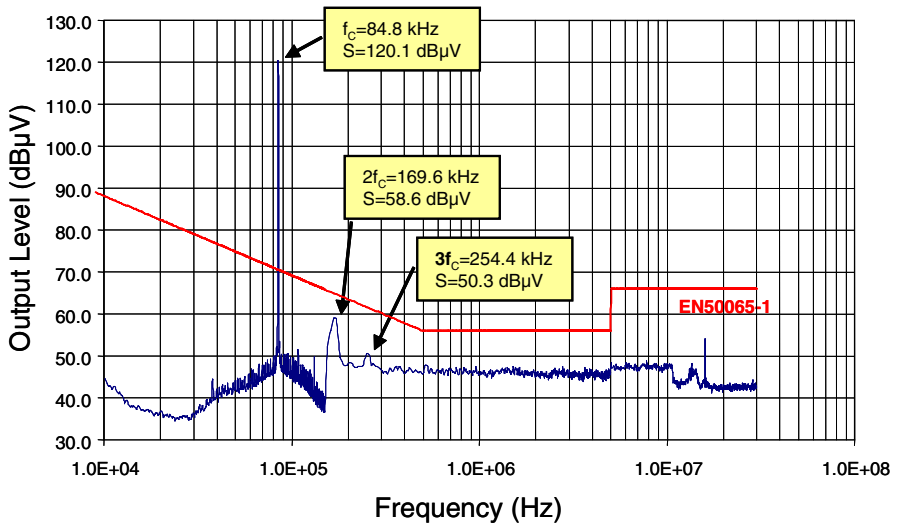


Figure 28. Output spectrum (typical) at 86 kHz channel, mains 220 V_{AC}, fixed transmitted tone = "1"



5.2.2 Noise immunity

The tests on immunity against white noise and narrowband conducted interferences are based on two ST7540 reference design boards performing a simplex (unidirectional) communication. The first board transmits a given bit sequence, while the receiving board passes the received bit stream to a PC bit error rate (BER) tester software, which evaluates the percentage of correctly received bits.

The noise (white noise or sinusoidal interferer) is produced by a waveform generator and injected into the artificial network through an AC-coupling circuit. *Figure 29* illustrates the test environment used for noise immunity tests.

Figure 29. Narrowband conducted interference test setup

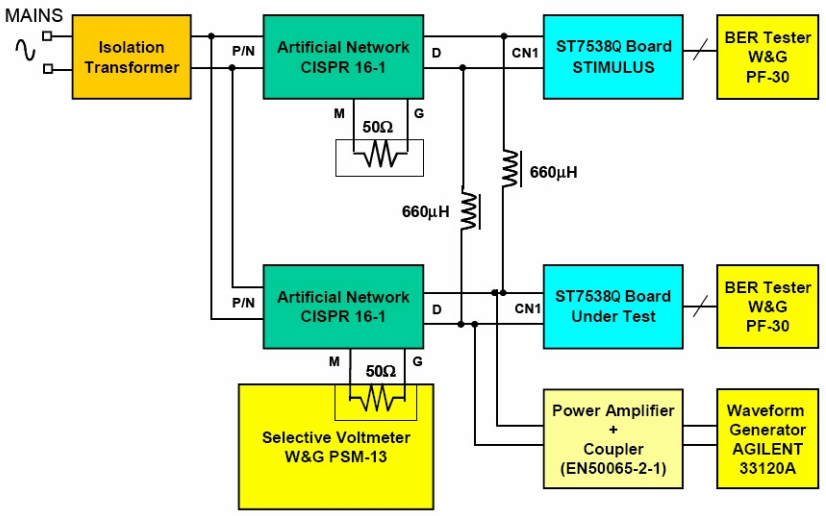


Table 6 gives the parameters for setting the test conditions.

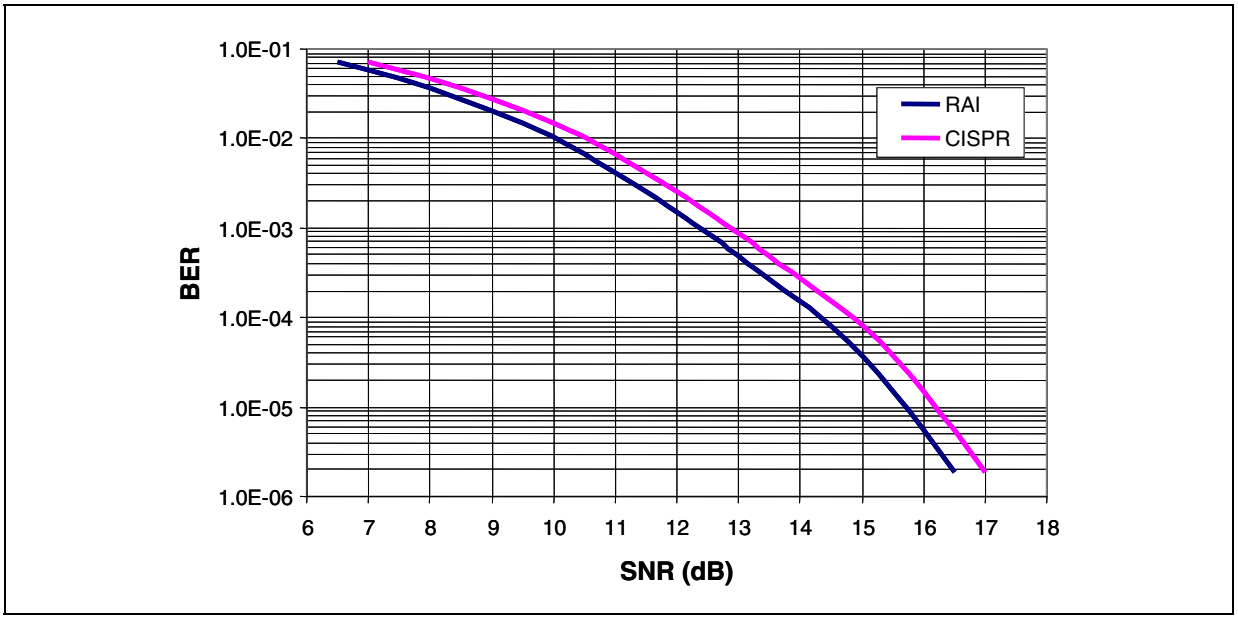
The received signal and noise level are measured with a spectrum analyzer at both the ST7538Q RAI pin and the measurement port of the CISPR artificial network. To obtain the right value, the noise level is measured in absence of the transmitted signal. The 3 kHz resolution bandwidth of the spectrum analyzer has been chosen to fit the spectrum of the transmitted FSK signal at 2400 baud.

Table 6. Noise immunity test settings

Parameter	Value
Received signal at RAI pin	78 dBµV rms
Frequency	72 kHz
Baud rate	2400
Deviation	1
Detection method	Carrier with conditioning
Detection time	3 ms
Sensitivity	High
Input filter	Off
Transmitted sequence	AACC h
S.A. resolution BW	3 kHz

Figure 30 represents the measured BER vs. SNR curve at both RAI pin and measurement port of the CISPR network in presence of white noise. It may be noted that a BER of 10^{-3} corresponds to a value of SNR which is a little higher than 12 dB, as it can be expected for a non-ideal FSK demodulator. The curve of *Figure 30* is valid for both 72 and 86 kHz channels.

Figure 30. Measured BER vs. SNR curve (typical), white noise



For narrowband interference tests, two types of interfering noise have been used: a pure sinusoidal tone and an amplitude-modulated signal, (modulating signal 1 kHz, modulation depth 80%). In these tests, the amplitude of the noise tone (or the carrier, in case of modulated interferer) is varied until the measured BER reaches 10^{-3} (one error every 1000 transmitted bits).

Figure 31 shows the measured SNR vs. frequency curves for both pure sinusoidal tone and AM modulated interferer, with a fixed BER of 10^{-3}.

Figure 31. Measured SNR vs. frequency curves (typical) at BER=10^{-3} - 72 kHz channel

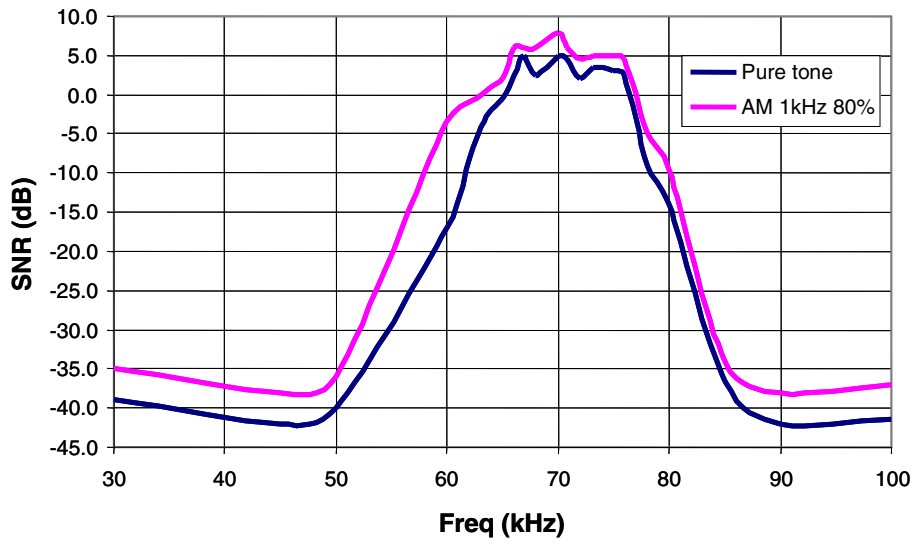
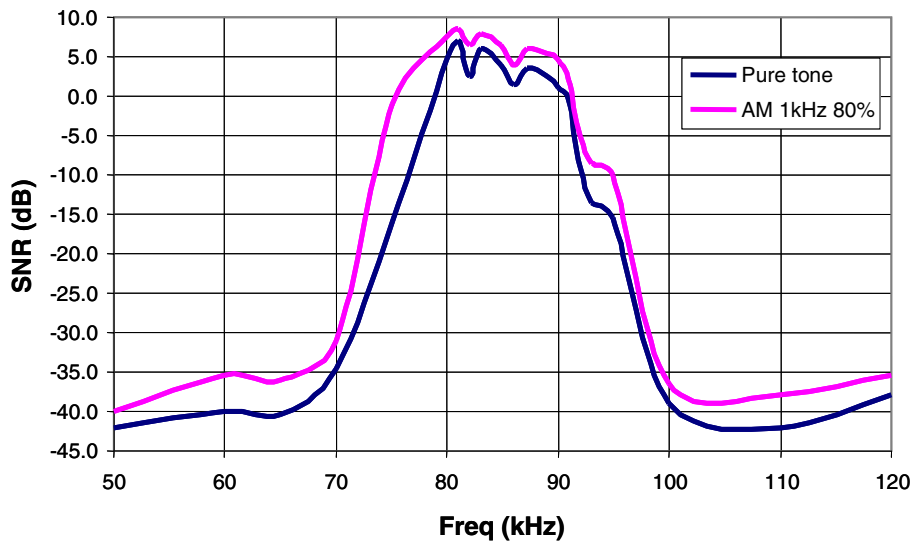


Figure 32. Measured SNR vs. frequency curves (typical) at BER=10^{-3} - 86 kHz channel



5.3 Thermal design

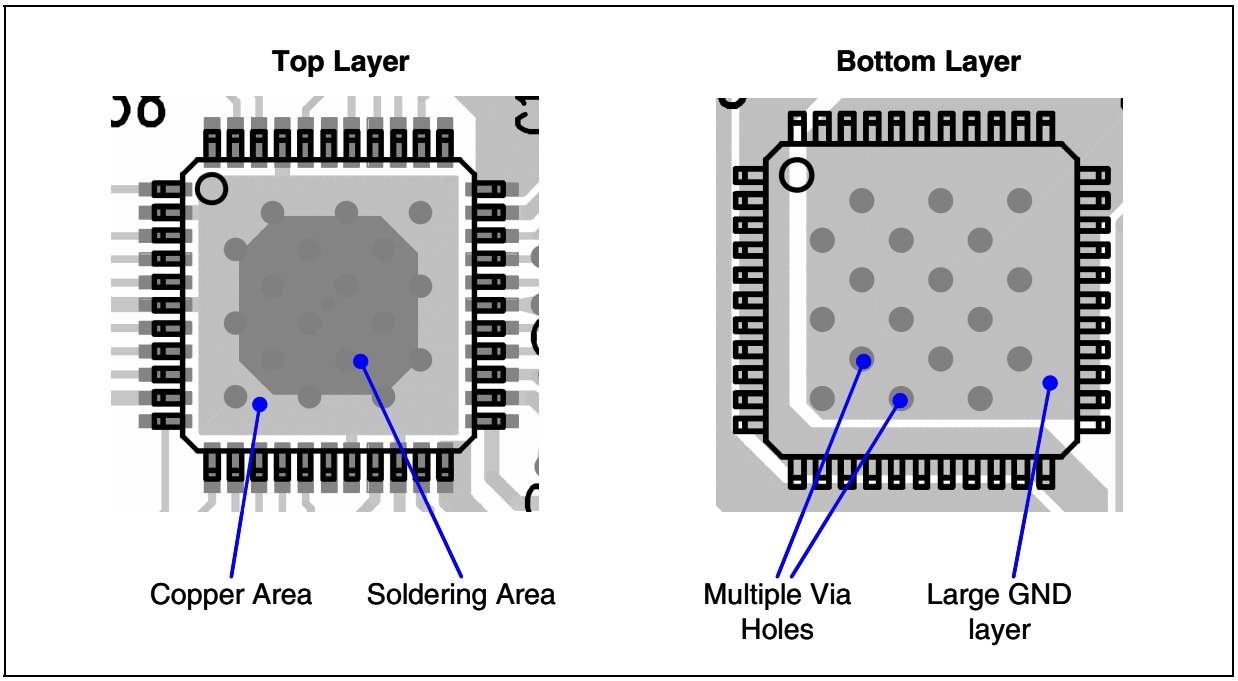
All heat dissipation is based on the heat exchange between the ST7538Q IC, the PCB and the environment.

A large PCB copper area under the device is recommended in order to achieve a better heat transfer from the IC to the environment, see *Figure 33*.

The metallic slug under the ST7538Q (the exposed pad of the PwTQFP44 package) must be properly soldered to the ground copper area on the PCB top side, as recommended in the datasheet. For the ST7538Q dual channel reference design, the dissipating area is nearly 1.5 cm².

The larger ground layer on the bottom side should be connected to the top side area through multiple via holes.

Figure 33. PCB copper dissipating area for the ST7538Q dual channel reference design



Even if the ST7538Q has an integrated thermal shutdown circuitry, turning off the power stage if the die temperature (T_J) surpasses 170 °C, it is recommended that T_J does not exceed 125 °C to guarantee a safe condition for IC operation.

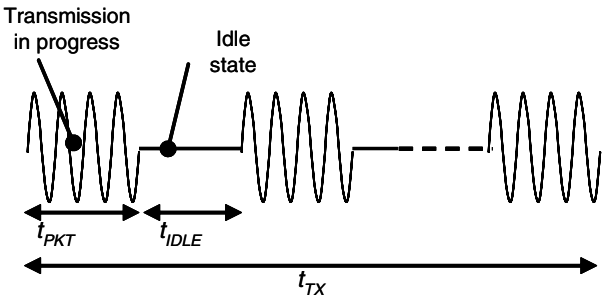
The relationship between the junction temperature T_J and the power dissipation during transmission PD is described by the following formula:

$T_J(t_{TX}, d) = T_A - P_D \cdot \theta_{JA}(t_{TX}, d)$

where T_A is the ambient temperature (from -45 to +85 °C) and θ_{JA} is the junction-to-ambient thermal impedance of the ST7538Q IC.

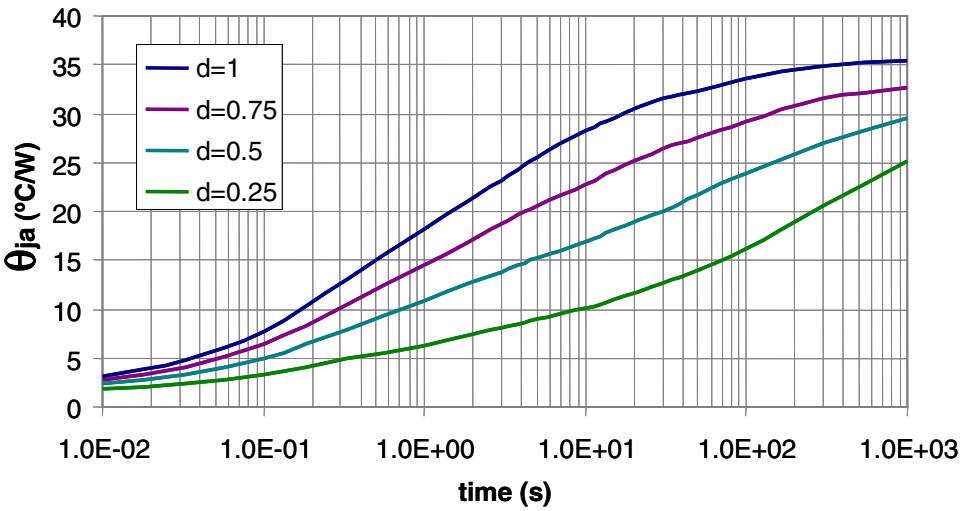
The value of the thermal impedance depends on the length of the transmission (t_{TX}) and on the duty cycle $d = t_{PKT}/(t_{PKT}+t_{IDLE})$, assuming a packet-fragmented transmission as depicted in *Figure 34*.

Figure 34. Packet-fragmented transmission



When soldered to a proper copper area on the PCB, according to the suggestions previously given, the IC is characterized by a steady-state thermal impedance of about 35 °C/W. Nevertheless, as shown in *Figure 35*, the steady-state value is reached after a transient whose duration depends on the duty cycle (d) of the transmission. In other words, a higher P_D can be sustained if the transmission time is less than the transient completion time and if the duty cycle of the transmission is lower than 100%.

Figure 35. Thermal impedance typical curve for the ST7538Q mounted on the reference design board



Actual dissipated power P_D can be calculated as:

$P_D = P_{IN} - P_{OUT}$

where $P_{IN} = V_{CC} \times I_{CC}$ and $P_{OUT} = V_{OUTrms} \times I_{OUTrms}$.

The value of V_{CC} can be inferred from the I_{CC} value according to the load regulation curve of the power supply, shown in *Figure 44 on page 45* in *Section 5.7*. Considering the power consumption by receiving circuitry and linear regulators negligible for thermal analysis purposes, the current absorption from the power supply (I_{CC}) results are nearly equal to the PLI output current to the load (I_{OUTrms}), so P_D can be expressed as:

$P_D = (V_{CC} - V_{OUTrms}) \times I_{OUTrms}$

Therefore, once the output voltage is fixed by the V_{SENSE} partitioning, the required P_D can be calculated as a function of the load current (I_{OUTrms}). The resulting value can be compared with the dissipation limit imposed by the θ_{JA} value, as a function of t_{TX} and duty cycle, to keep the junction temperature below the 125 °C limit.

5.4 Oscillator section

The ST7538Q crystal oscillator circuitry is based on a MOS amplifier working in inverter configuration. This circuitry requires a crystal having a maximum load capacitance of 16 pF and a maximum ESR of 40 Ω.

It is very important to keep the crystal oscillator and the load capacitors as close as possible to the device.

The resonant circuit must be far away from noise sources such as:

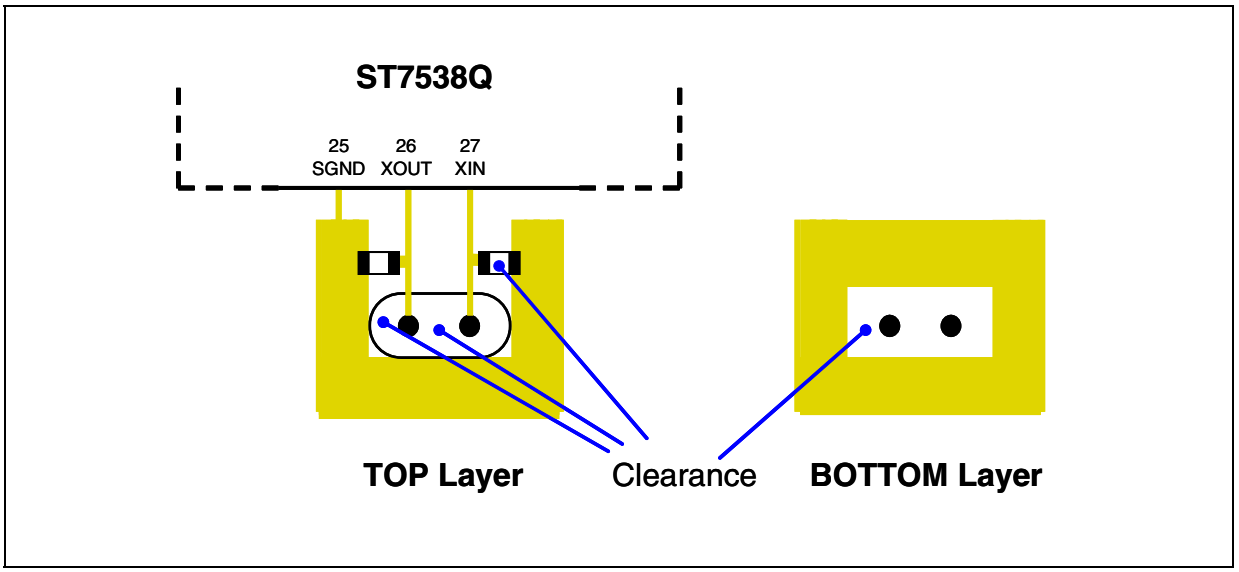
- power supply circuitry
- burst and surge protections
- mains coupling circuits
- any PCB track or via carrying a signal

To properly shield and separate the oscillator section from the rest of the board, it is recommended to use a ground plane, on both sides of the PCB, filling all the area below the crystal oscillator and its load capacitors. No tracks or via holes, except for the crystal connections, should cross the ground plane.

It is also recommended to use a large clearance on the oscillator-related tracks, to minimize humidity problems, see *Figure 36*.

Connecting the case to ground is also a good practice to reduce the effect of radiated signals on the oscillator.

Figure 36. A recommended oscillator section layout for noise shielding



5.5 Surge and burst protection

The specific structure of the coupling interface circuit of the application is a weak point against high voltage disturbances that can come from the external environment. In fact an efficient coupling circuit with low insertion losses realizes consequently a very low impedance path from the mains to the power line interface of the device.

For this reason it's recommended to add some specific protections on the mains coupling path, in order to prevent high energy disturbances coming from the mains from damaging the internal power circuitry of the ST7538Q.

The possible environments for this kind of application can be both indoor and outdoor: residential, commercial and light-industrial locations. To verify the immunity of the system to environmental electrical phenomena, a series of immunity specification standards and tests must be applied to the power line application.

The requirements for ac-connected ports include EN610000-4-4 (electric fast transients), EN610000-4-5 (surges), EN610000-4-6 (RF out-of-band disturbances), EN610000-4-11 (voltage dips). All these tests are listed in the EN50065-2-3 document (part 7, immunity specifications).

In particular, surge tests are specified as both common and differential mode at level +/- 4 kV, with pulse shape 1.2 x 50 µs. Fast transient burst tests are specified at level +/- 2 kV, with pulse shape 5 x 50 ns and pulse frequency 5 kHz.

Figure 37 and *Figure 38* illustrate the protection criteria implemented in the ST7538Q reference design.

Figure 37 shows the protection against common mode disturbances. The ESD Transil™ protection diodes are able to absorb quickly fast transient disturbances starting from their 6.1 V threshold voltage.

Figure 38 describes the protection intervention in case of differential mode disturbances. A differential voltage higher than 6.8 V is shorted by the bidirectional power Transil™, which is the most robust protection and also the one that is able to absorb most of the energy of any incoming disturbance.

Figure 37. Common mode disturbances protection

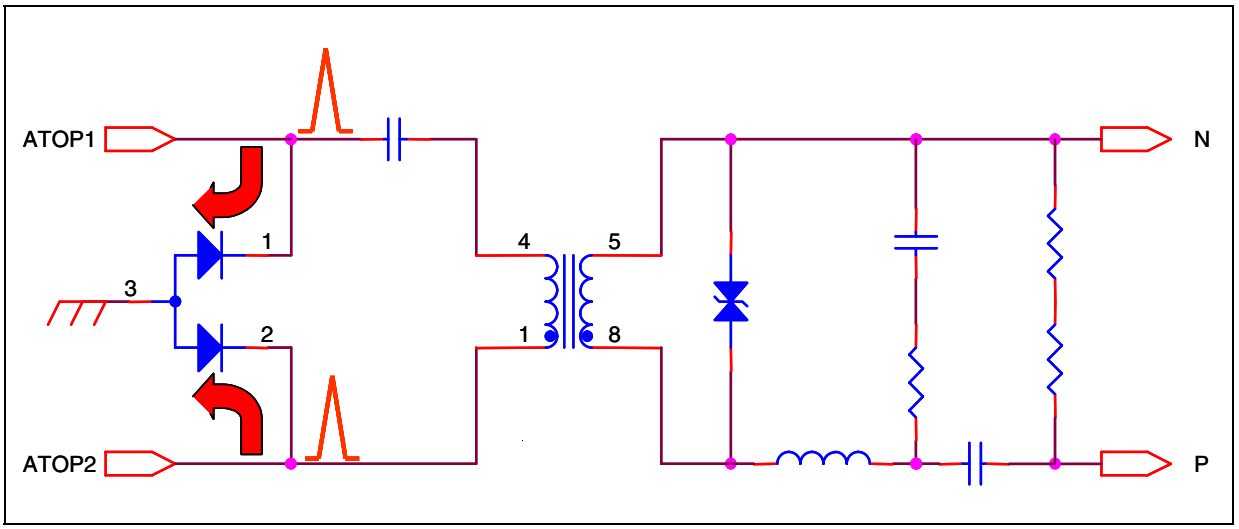
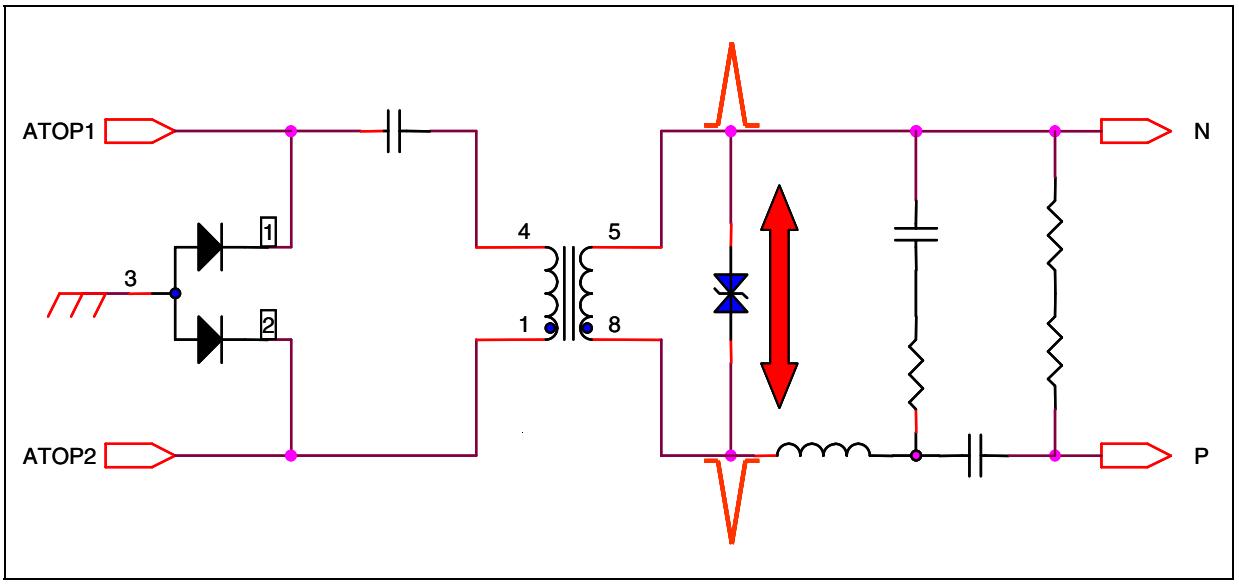


Figure 38. Differential mode disturbances protection



5.6 50-pin connector for communication board

The ST7538Q transceiver requires external digital control to perform communication. This is done through an ST7 microcontroller which is accommodated on the IBU communication board (see *Section 4*).

The communication with the ST7 microcontroller involves several signals, which can be gathered into 3 groups: digital signals, analog signals and power connections. The signals for each group are listed in *Table 7*, *Table 8* and *Table 9*.

Beside the ST7538Q input and output signals, the link to the IBU communication board includes:

– A 2-bit (B_ID_PLM_1 and B_ID_PLM_0) Board Identification Code, which identifies the hosted power line transceiver. The "00" HW binary configuration makes the microcontroller able to recognize the ST7538Q reference design board.

– A VDDF_FORCE signal that forces the microcontroller to refer digital interface levels to VDDF (VDD) supply voltage provided by the ST7538Q reference design board. This way both the modem and the microcontroller communicate on the same digital levels.

Figure 39. Scheme of the communication board connector

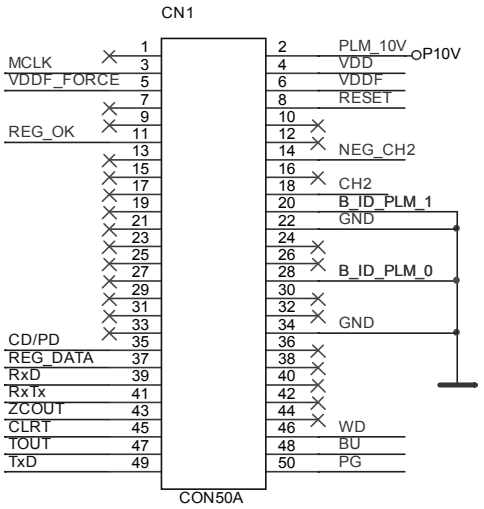


Table 7. 50-pin connector digital signals

Pin n°	Signal name	Description	Generated by
3	MCLK	Oscillator output (programmable)	ST7538Q
8	RESET	Reset Out for microcontroller	ST7538Q
11	REGOK	Register OK signal	ST7538Q
14	NEG_CH2	Secondary channel select (active low)	µC
18	CH2	Secondary channel select (active high)	µC
35	CD/PD	Carrier or preamble detected signal	ST7538Q
37	REG/DATA	Register or Data access	µC
39	RxD	Serial Data Out	ST7538Q
41	RxTx	Reception or Transmission select signal	µC
43	ZCOUT	Zero-crossing detection output	ST7538Q
45	CLR/T	Serial Data Clock	ST7538Q
46	WD	Watchdog counter reset	µC
47	TOUT	Timeout / Thermal Protection event signal	ST7538Q
48	BU	Band in Use detection signal	ST7538Q
49	TxD	Serial Data Input	µC
50	PG	Power good signal	ST7538Q

Table 8. 50-pin connector control signals

Pin n°	Signal name	Description	Generated by
20	B_ID_PLM_1	Board ID for PLM Applications (MSB)	PLC Board
28	B_ID_PLM_0	Board ID for PLM Applications (LSB)	PLC Board
5	VDDF_FORCE	Force µC digital level to VDDF	PLC Board

Table 9. 50-pin connector power connections

Pin n°	Signal name	Description	Generated by
2	PLM_10V	10V power supply	PLC Board
4	VDD	3.3V/5V power supply	ST7538Q
6	VDDF	Digital power supply	ST7538Q
22,34	GND	Ground	-

5.7 Power supply

The ST7538Q dual channel reference design includes a specifically designed switching mode power supply circuit, based on ST's VIPer12AS-E device.

VIPer12AS-E is a smart power device with current mode PWM controller, startup circuit and protections integrated in a monolithic chip using VIPower M0 technology. It includes a 27 Ω Mosfet with 730 V breakdown voltage and a 400 mA peak drain current limitation. The switching frequency is internally fixed to 60 kHz, in order to provide a good compromise between EMI performances and magnetic parts dimensioning.

The internal control circuit offers the following benefits:

- large input voltage range on VDD pin accommodates changes in supply voltage

- automatic burst mode in low load condition

- overload and short circuit protection in hiccup mode

The power supply is designed in isolated flyback configuration with secondary regulation by means of an optocoupler and a Zener diode, considering the requested output tolerance for the specified application.

The main specifications are listed in *Table 10*

Table 10. SMPS specifications

Parameter	Value
Input voltage range, V_{IN}	85-265 V_{AC}
Output voltage, V_{OUT}	10V±10%
Peak output current, $I_{OUT(MAX)}$	600 mA

In the input stage, an EMI filter is implemented (C2, L2, C10, L3, C5) for both differential and common mode noise, in order to fit the requested standard.

The blocking diode D4 and the clamping network (R1-C1) clamp the peak of the leakage inductance voltage spike, assuring reliable operation of the VIPer12AS-E. D4 must be not only very fast-recovery but also very fast turn-on type to avoid additional drain overvoltage. The clamp capacitor C1 must be low-loss type (with polypropylene or polystyrene film dielectric) to reduce power dissipation and prevent overheating, since it is charged with high peak currents by the energy stored in the leakage inductance.

Also a leading edge blanking (LEB) circuit for leakage inductance spikes filtering has been implemented (Q3 - C30 - R23). It blanks the spike appearing at the leading edges of the voltage generated by the self-supply winding, greatly improving the behavior in short-circuit.

The output rectifiers have been selected considering the maximum reverse voltage and the RMS secondary current. A STPS1H100 Power Schottky rectifier has been chosen for this purpose.

A LC filter has been added on the output (made of L1 and C4) in order to filter the high frequency ripple without increasing the output capacitors size or quality.

The transformer used for this application has three windings, since one of them is needed to supply the VIPer12AS-E. The primary inductance has been chosen at 2.7 mH and the reflected voltage has been set to 80 V.

A layer type has been chosen, with EF12.6 or E13/7/4 core. The characteristics are listed in *Table 11*.

Table 11. SMPS transformer specifications

Parameter	Value
Core Geometry	SRW12.6ES or E13/7/4
Primary Inductance	2.7 mH±10%
Leakage Inductance	180 µH max
N_P	224 turns – 0.1mm
N_{AUX}	39 turns – 0.1mm
N_{SEC}	31 turns – 0.2mm (TEX-E wire)
Withstanding Voltage	4 kV_{RMS}

In the following pictures some significant waveforms are represented. *Figure 40* and *Figure 41* show typical waveforms in both open load and full load conditions.

An important behavior in any SMPS is the protection against output short circuit. All tests have been done by shorting the SMPS output at maximum input voltage. The results are shown in *Figure 42*.

The main parameters are the drain-source voltage (V_{DS}), the output current (I_{OUT}) and the supply voltage (V_{DD}).

The output current is an important parameter to be checked during shorts. Although the output current peaks are quite high, the mean value is very low, thus preventing component melting for excessive dissipation. In this way, the output rectifier, transformer windings and PCB traces won't be overstressed. This assures system reliability against long-term shorts.

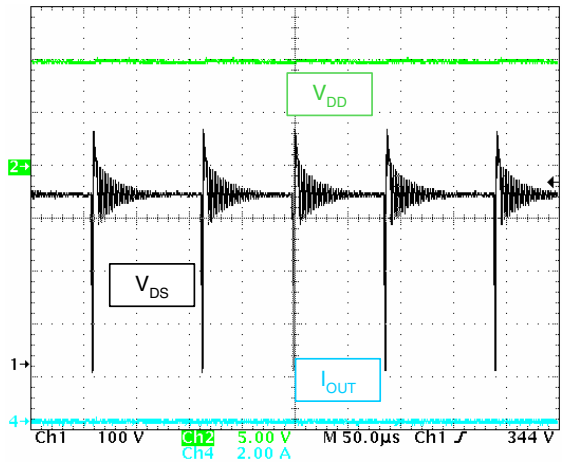
Besides, in case of device overheating, the integrated thermal protection stops the device operation until the device temperature falls.

The startup phase could also be critical for the SMPS as output overshoot occurs if the circuit is not properly designed. Care must be taken in designing a proper clamp network in order to prevent voltage spikes due to leakage inductance from exceeding the breakdown voltage of the device (730 V minimum value).

The startup transient is shown in *Figure 43*. Note that the maximum drain-source voltage doesn't exceed the minimum breakdown voltage BVDSS, with a reasonable safety margin.

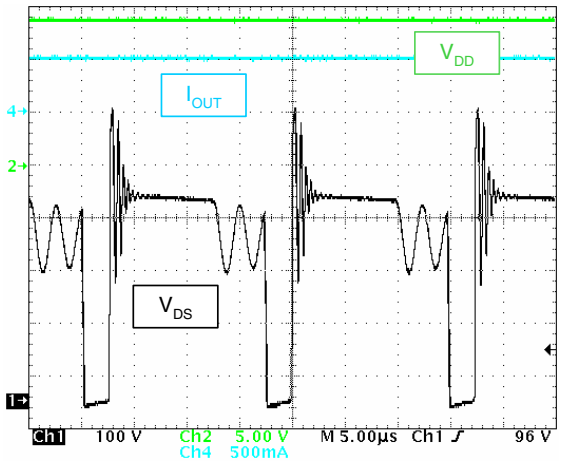
Finally, load regulation is presented in *Figure 42* and *Figure 43* for different load conditions. The voltage ranges from 10 V to 9.3 V, within the requested tolerance.

Figure 40. Typical waveforms at 230 V_{AC}: open load



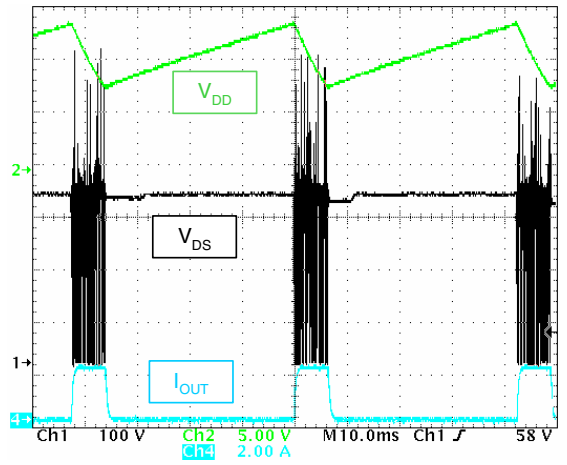
Ch1 Freq - 9.62kHz; Ch2 Mean - 9.90V

Figure 41. Typical waveforms at 230 V_{AC}: full load



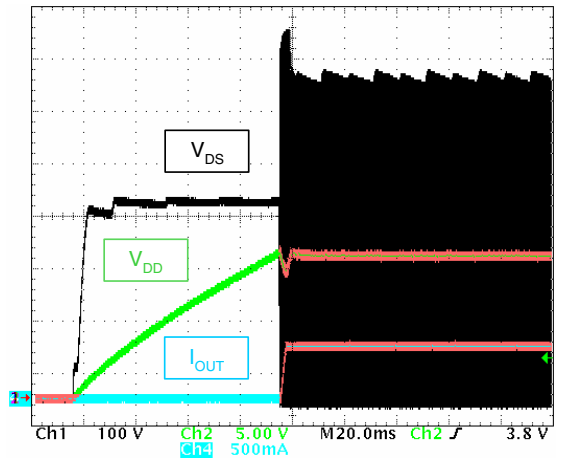
Ch1 Freq - 57.71kHz; Ch2 Mean - 13.79V; Ch4 Max - 503mA

Figure 42. Typical waveforms at 265 V_{AC}: short-circuit



Ch2 Freq - 23.50Hz; Ch4 Max - 2.08A; Ch4 Mean - 383mA

Figure 43. Typical waveforms at 265 V_{AC}: startup



Ch1 Max - 702V; Ch2 Mean - 19.72V; Ch4 Max - 500mA

Figure 44. Load regulation

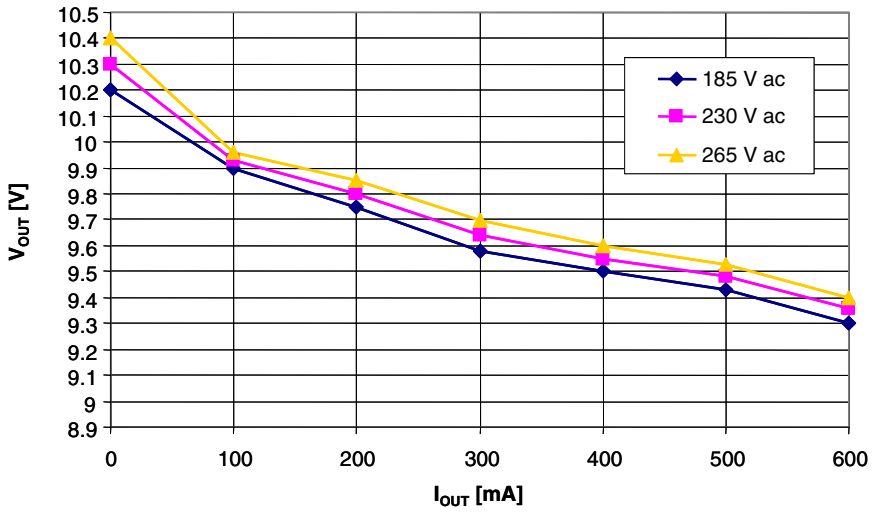
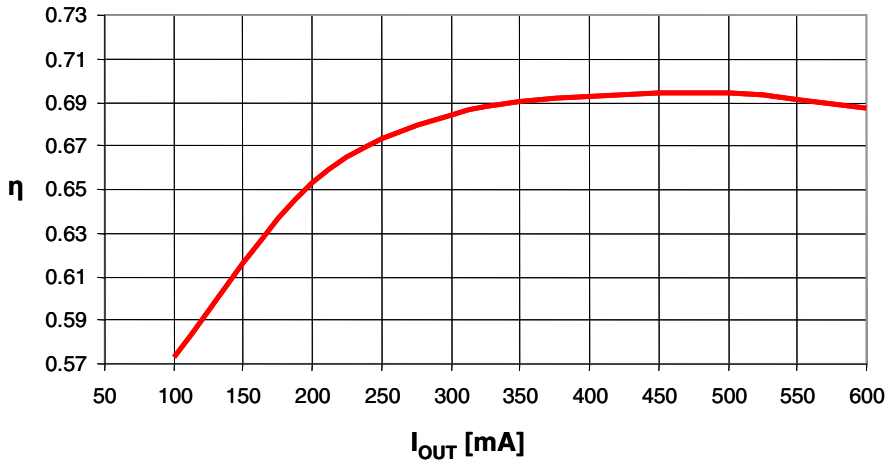


Figure 44 shows the efficiency vs. output current curve. Minimum efficiency occurs at low load condition, as expected from any SMPS. This is not an issue for our application, since low efficiency corresponds also to low power consumption and thus to low dissipation.

On the other hand, at full load condition the efficiency is reduced because of the losses due to R1 (series input resistor limiting in-rush current) and to the filtering on both primary and secondary side. Filtering is more important than efficiency because a power line communication appliance has very restrictive electromagnetic disturbance limits and it's also highly sensitive to noise coming from the power supply.

Figure 45. SMPS efficiency curve



6 Performance and ping tests

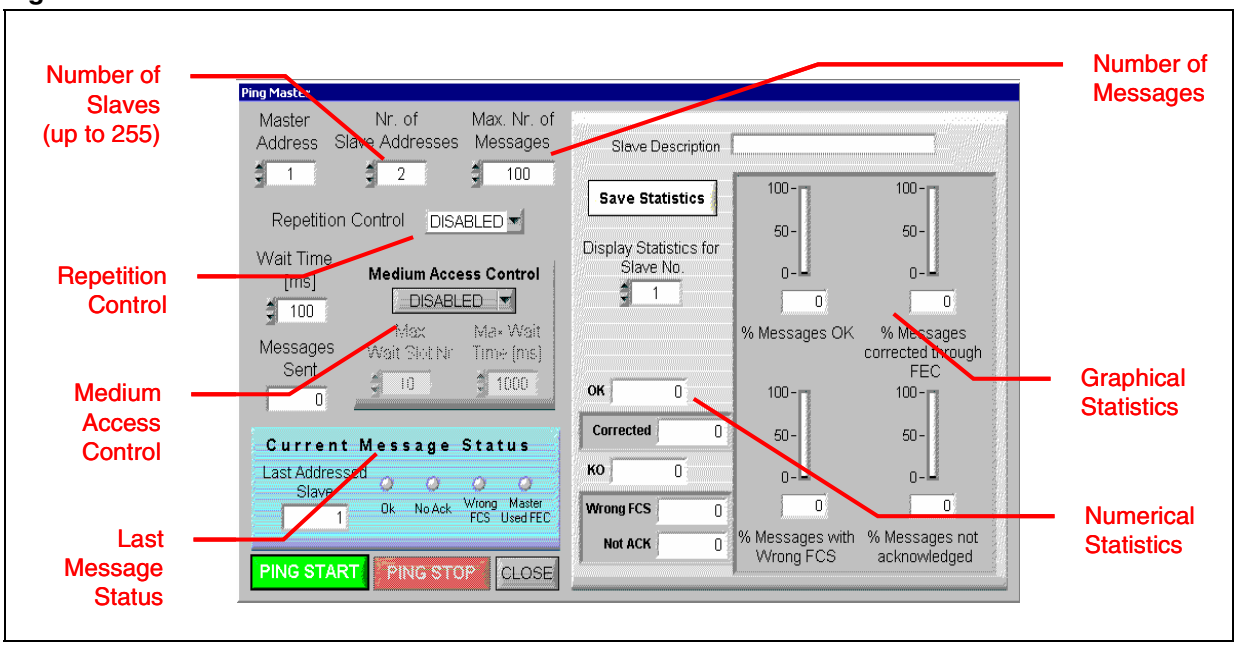
Our evaluation environment includes a ping test embedded into the demonstration software and the communication board firmware. This feature allows to perform in-field communication tests and to evaluate reachability of PLC network nodes.

A ping session is based on a master board sending to one or more slave boards a sequence of messages. If the messages are correctly received by the slave boards, they are resent one by one to the master.

The PC.connected to the master keeps statistics of the messages sent and correctly received by the slave boards, making it possible to get a numerical evaluation of the reachability of each node corresponding to a slave.

Figure 46 represents the ping window of the demonstration software tool for the master node. The main characteristics of this tool are indicated in red.

Figure 46. Demonstration software window for the master board



Special controls are included in the ping test:

- Repetition control: repetition can be used to improve reliability of the communication. When enabled, if a message is not responded by a slave, it will be re-sent up to three times before sending a new message.
- Medium access control: defines what type of medium access has to be used. Choices are "none", "BU" or "PD". In the last two cases, messages are sent to slave only if BU or CD/PD lines of the ST7538Q modem are not active. If PD setting is selected, content of the ST7538Q internal control register is changed to select "Preamble" as the detection method.

For further details about the ST7538Q demonstration software tool, please refer to UM0241 "ST7538 Power Line Modem DEMO KIT GUI - User Guide".

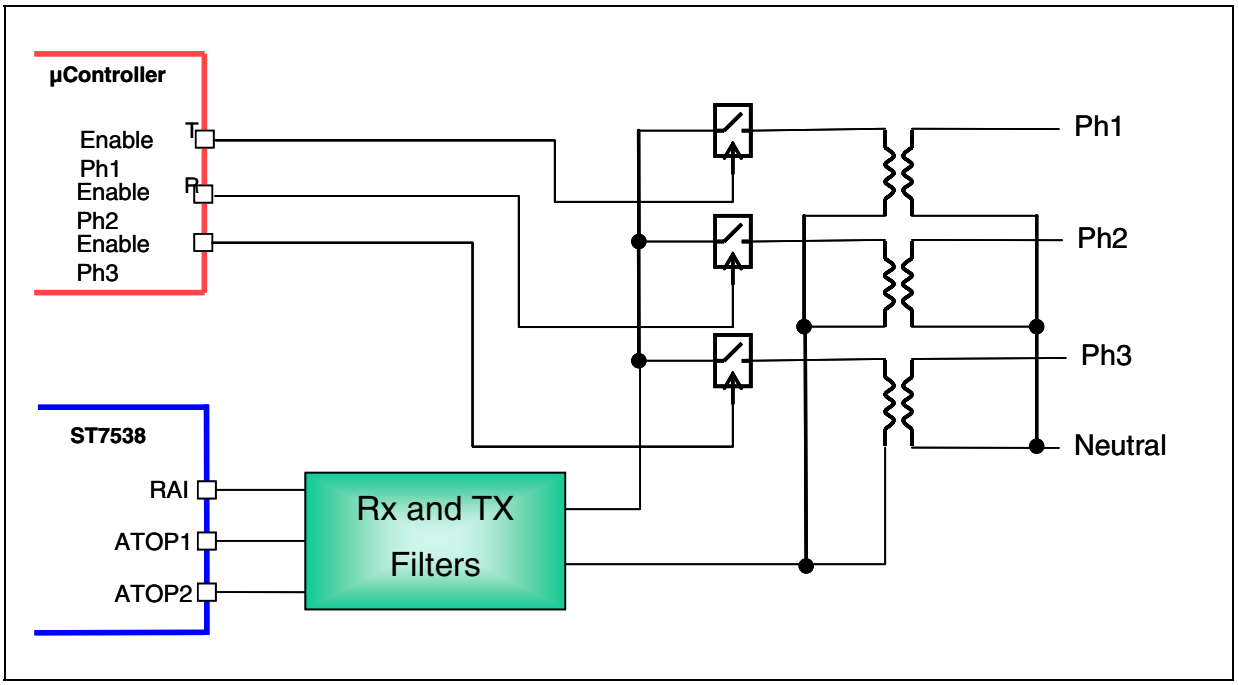
7 Application ideas

7.1 Three-phase architecture

The ST7538Q modem can be used to communicate on a three-phase network. A microcontroller should switch communication between the three phases, since the modem can transmit/receive over only one phase at a time.

In the example scheme of *Figure 47*, the microcontroller uses three output lines as enable signals for three switches (typically opto-switches), one for each phase line. For the modem, there is no difference with respect to single-phase communication.

Figure 47. Scheme of principle for three-phase architecture



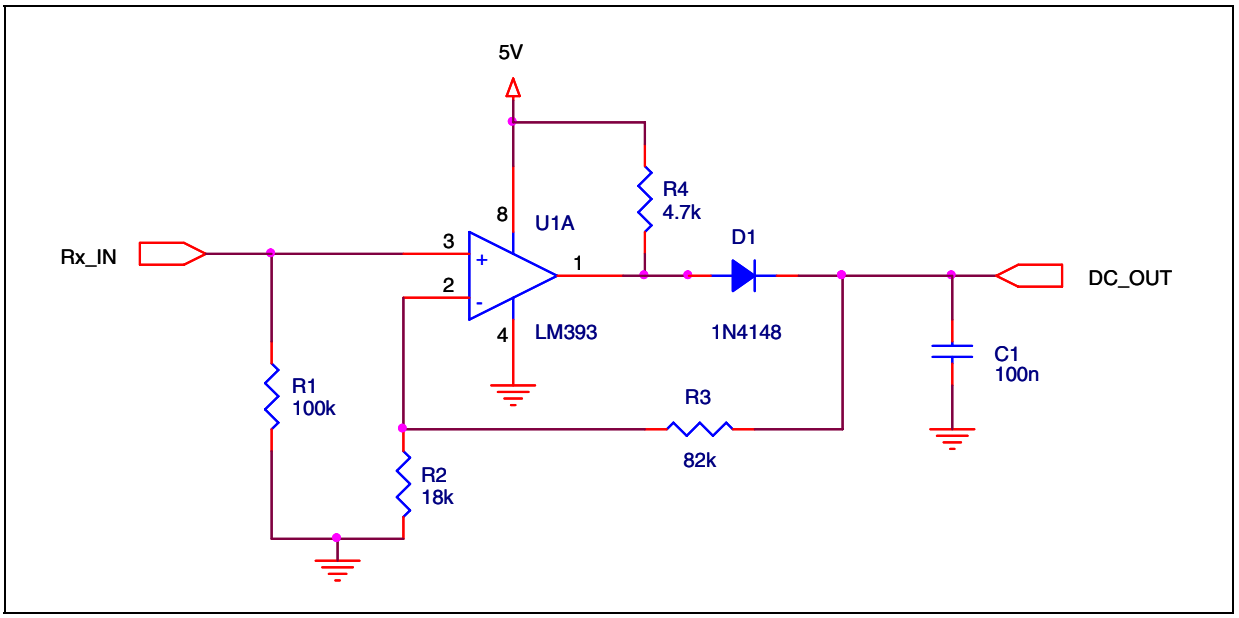
7.2 Received signal strength indication (RSSI)

In many application fields, measuring the strength of the incoming signal is useful to:

1. evaluate the SNR (signal-to-noise ratio) at the node
2. choose the best routing through the network (if repeaters are allowed)

A possible received signal strength indicator (RSSI) implementation is the one depicted in *Figure 48*, where a peak detector is used to measure the amplitude of the incoming signal.

Figure 48. Peak detector electrical schematic

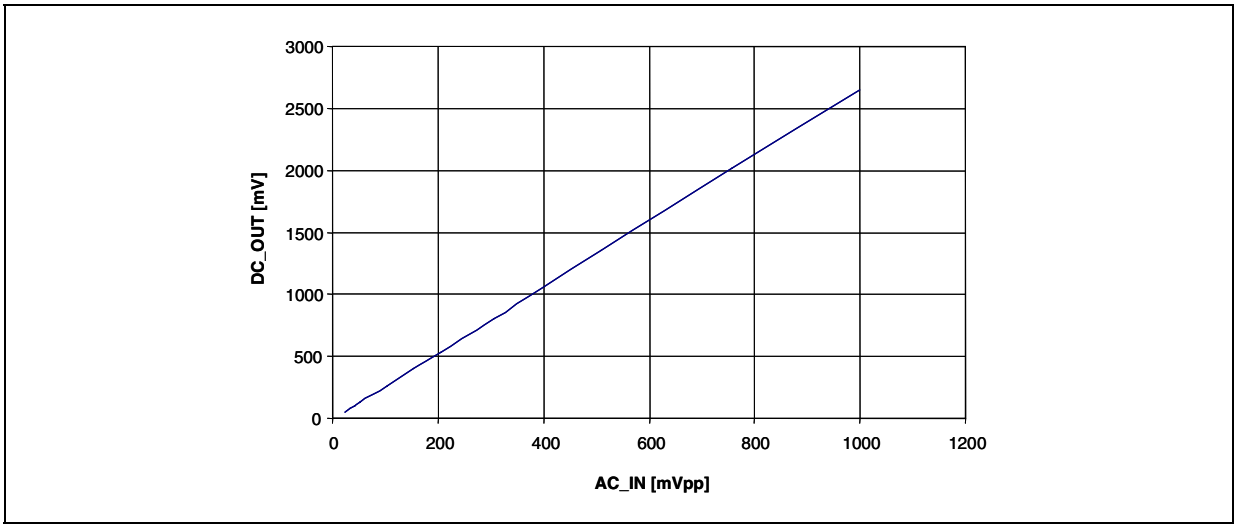


The schematic above is based on a simple diode-capacitor (D1-C1) circuit improved with an LM393 comparator so that:

- The comparator eliminates the diode reverse voltage
- The feedback network (R3/R2) introduces a gain of 4 to improve the performance against low amplitude signals

In the end this circuit gives on DC_OUT line a DC voltage proportional to the AC peak to peak level at the input. *Figure 49* shows the measured behavior of this circuit with a given pure sinusoidal waveform at the input. The DC_OUT signal shall be converted by the application microcontroller through an integrated A/D converter.

Figure 49. Measured DC_OUT vs. AC_IN peak detector performance



7.3 110-132.5 kHz dual channel coupling circuit

In this paragraph the dual channel application circuit for CENELEC band B and C is suggested. The 110 and 132.5 kHz channel frequencies of the ST7538Q transceiver are suitable for home automation applications and in general for applications not subject to the European AMR regulations.

Table 12 gives the values for changing a few components to obtain a dual channel line coupling interface at 110 kHz (CH1) and 132.5 kHz (CH2)

Table 12. List of components to be modified for the 110-132.5 kHz dual channel coupling

Reference	Value
L5	47 µH
L6	22 µH
L7	220 µH
C16	2.2 nF
C20	6.8 nF
C27	82 nF
C29	220 nF
R18	390 Ω
R21	6.8 Ω

8 Troubleshooting

In this section the most frequently asked questions are described.

1. **PROBLEM**: the ST7538Q reference design board doesn't work at all.

What to check:

a) Check that the AC mains supply cable is well connected to CN2.

b) Check if the green LED D2 is on.

c) Check voltage on the 10 V test point near the ST7538Q. The value must be 9 to 11 V.

2. **PROBLEM**: the ST7538Q reference design board is not responding.

What to check:

a) Check the VDC 5 V voltage output. Spurious voltage spikes can cause dips on the VDC line. This could force a shutdown of the Tx circuitry if the VDC voltage goes below 1.5 V. The solution is to force a power-off by mains disconnection.

b) Verify if MCLK selected frequency is present to check whether the ST7538Q is working.

c) Verify the connection between the reference design board and the communication board and between the communication board and the PC.

3. **PROBLEM**: the ST7538Q reference design board does not transmit.

What to check:

a) Check the voltage on ATOP1 and ATOP2 test points with the oscilloscope ground probe connected to the AVSS signal ground. Programmed carrier frequency must be present on both lines.

b) Check that programmed board channel (CH1/CH2) is matching the carrier frequency selected through the control register panel of the reference design software window.

c) Check that there is no short-circuit impedance on the mains at the selected transmitting channel.

d) Check CL voltage. CL voltage fixes the current limiting threshold. It has to be lower than 1.9 V, otherwise the IC is put in current limit mode.

If current limit mode is forced on the transceiver, check the value of R19 feedback resistor and if there are any short circuits in the transmission path on the board.

4. **PROBLEM**: the ST7538Q reference design board transmits only for a short while.

What to check:

a) Check transmission time-out setting. It has to be disabled for continuous transmission.

b) Check if continuous or single sequence transmission is selected in the Tx panel of the reference design software window. Select continuous mode to be able to force a lasting transmission.

c) Check if zero-crossing function is enabled. If yes, verify the ZCOUT synchronization bit.

d) Check that there is no short-circuit impedance on the mains at the selected transmitting channel.

5. **PROBLEM**: the ST7538Q reference design board does not receive.

What to check:

a) Check if JP2 and JP3 are closed. Please refer to *Section 5.1* for receiving path configuration.

b) Check if carrier frequency is present on RAI pin voltage with the oscilloscope ground probe connected to the AVSS signal ground pin.

c) Check that programmed board channel (CH1/CH2) is matching the carrier frequency selected through the control register panel of the reference design software window.

d) Check preamble detection setting on the control register panel of the reference design software window.

e) Check if data are present on RxD pin.

6. **PROBLEM**: During a ping test or a transmission test, the ST7538Q reference design board shows a high bit error rate.

Note: This point refers to a half-duplex communication involving two ST7538Q reference design boards communicating with each other.

What to check:

a) Check that both reference design boards are programmed to transmit/receive on the same carrier frequency.

b) Check on both reference design boards that programmed board channel (CH1/CH2) is matching the carrier frequency selected through the control register panel of the reference design software window.

c) Check preamble detection setting on the control register panel of the reference design software window.

d) Check if data are present on RxD pin.

9 List of normative references

EN50065: Signaling on low voltage electrical installations in the frequency range 3 kHz to 148.5 kHz

- Part 1: General requirements, frequency bands and electromagnetic disturbances
- Part 2-1: Immunity requirements
- Part 4-2: Low voltage decoupling filters - Safety requirements
- Part 7: Equipment impedance

Appendix A Board layout

Figure 50. PCB layout - top view

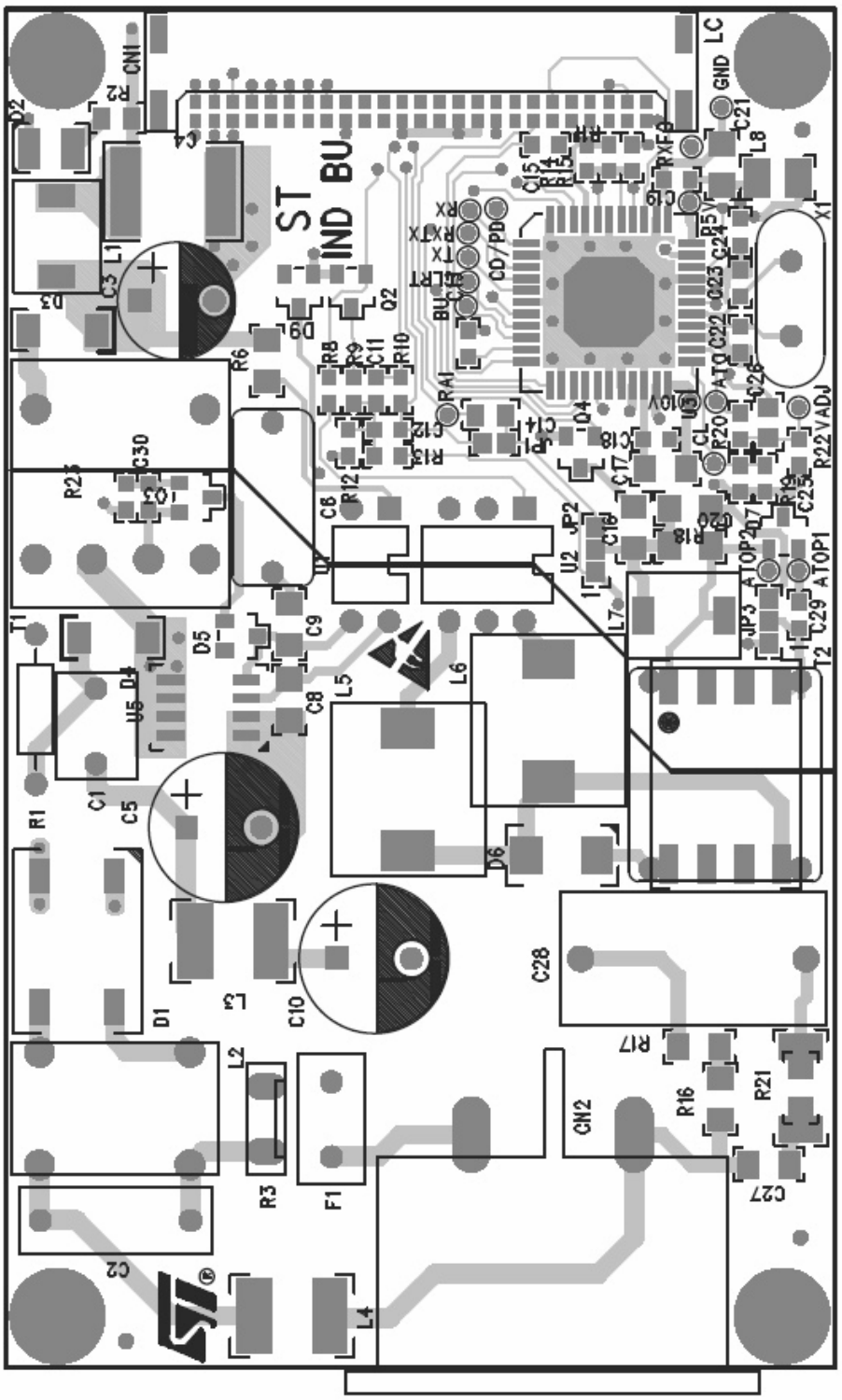
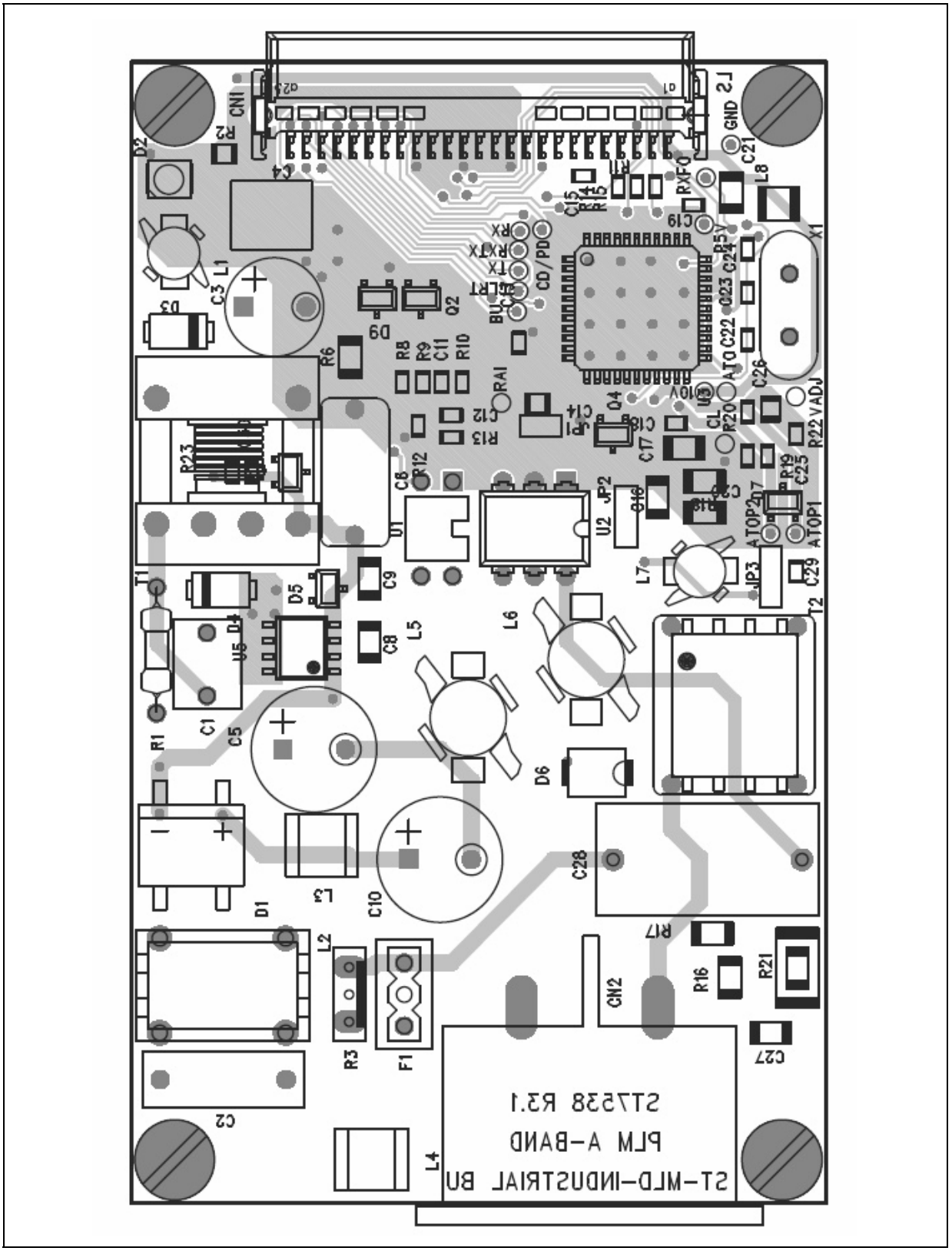


Figure 51. PCB layout - bottom view



10 Revision history

Table 13. Document revision history

Date	Revision	Changes
30-Apr-2008	1	Initial release.

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