



Introduction

This application note describes a low cost solution for directly driving QVGA TFT-LCD using any STM32F10xxx microcontroller, which is not equipped with an on-chip LCD controller. The powerful STM32F10xxx devices have an embedded FSMC (flexible static memory controller) which can be used together with the on-chip DMA controller to implement a direct drive for TFT-LCDs. This low cost solution is ideal for applications such as digital photo frames, stand-alone information displays and static advertisement panels.

The application note describes how to use the STM32F10xx as LCD controller to drive a QVGA 3.5" TFT panel interfaced with the FSMC. The optimization that can be achieved with this solution means that only 1% of CPU load is needed to display static images.

A firmware demonstration has been developed and tested on a CT05350DW0000T QVGA 3.5" LCD module with a resolution of 320x240 pixels.

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1 STM32 QVGA TFT-LCD direct drive

The STM32 microcontrollers have an embedded Flexible Static Memory Controller (FSMC) to interface with external memories such as NAND, NOR, SRAM and PSRAM memories. The microcontroller also has a large number of general-purpose I/O port pins which together with the FSMC can act as a cost-effective TFT-LCD controller for low-end displays:

- The 16-bit data bus of the FSMC peripheral can easily be interfaced with the 565 RGB format lines of a TFT-LCD panel (in 565 RGB format, 5 bits are for red, 6 bits for green and 5 bits for blue).
- An external memory can be used as the image source as well as a frame buffer for the TFT-LCD refresh.
- The general-purpose I/O pins can provide the synchronization logic for the LCD.

1.1 STM32 QVGA TFT-LCD direct drive principle

Controller-less TFT-LCD panels have different data-line configurations, for example 16-bit, 18-bit or 24-bit RGB lines. A TFT-LCD with a 16-bit data interface offers 565 format for each pixel.

The TFT-LCD panel displays are managed as row and column structures. Vertical scanning controls row data output and horizontal scanning controls column data output.

Apart from different data line configurations, other data display management signals are common to all TFT-LCD panels:

- The frame synchronization signal (VSYNC) manages vertical scanning and acts as an image (frame) update strobe.
- The line synchronization signal (HSYNC) manages horizontal line scanning and acts as line display strobe.
- Synchronization signals along with pixel data clock (DCLK) perform data output to TFT RGB data lines.
- The DCLK simply acts as the data valid signal for the TFT. The TFT considers data as input only on the DCLK edge. DCLK valid edge (rising/falling) is mentioned in the TFT datasheet.

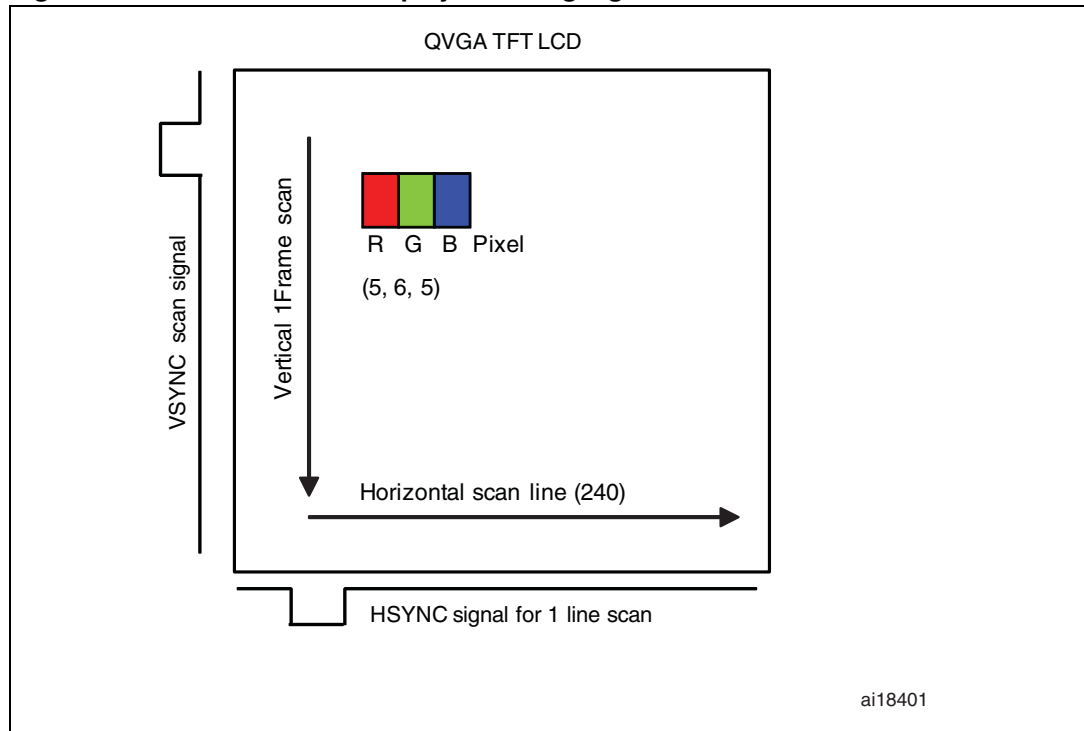
The horizontal scanning builds one line for display and the vertical scanning builds a complete frame. The vertical and horizontal scanning of the image is carried out in a continuous manner for multiple frames per second.

The TFT also needs a TFT-enable signal that acts simply as a chip-enable signal and TFT reset signal.

The TFT signals must be synchronized in accordance with the display timing constraints to ensure that the display has a continuous visual effect.

Figure 1 shows the horizontal and vertical scanning signals.

Figure 1. QVGA TFT-LCD display scanning signals



The FSMC bus data width is 16-bit. Hence, if the TFT-LCD panel has 24-bit RGB lines, the MSBs of the LCD RGB data lines can be interfaced in 565 format.

Images must be displayed on the TFT-LCD continuously, this is easily managed by the STM32 microcontroller.

Figure 2 shows the TFT synchronization signals waveform.

Figure 2. Frame synchronization signal waveform

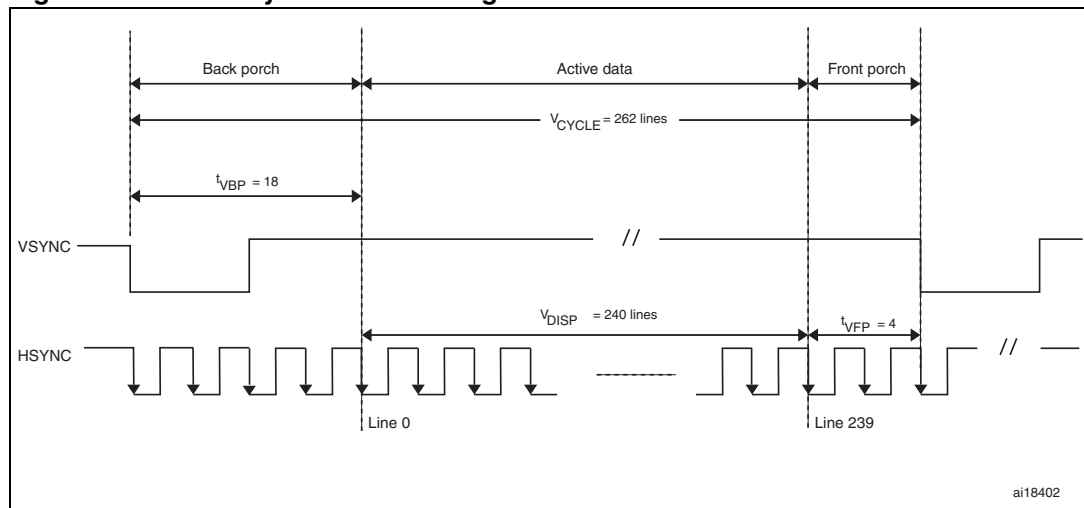
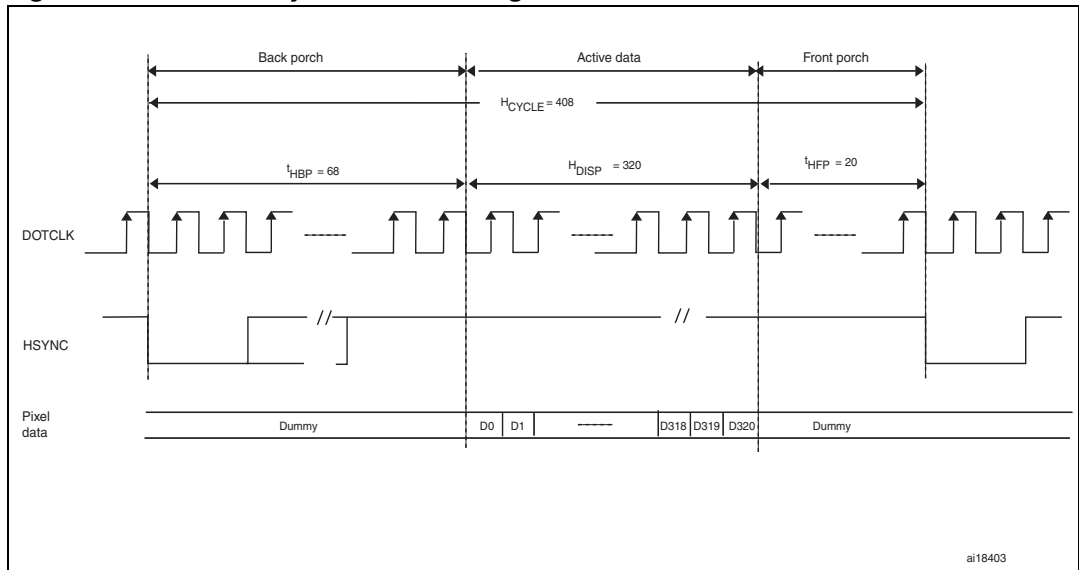


Figure 3. TFT Line synchronization signal waveform

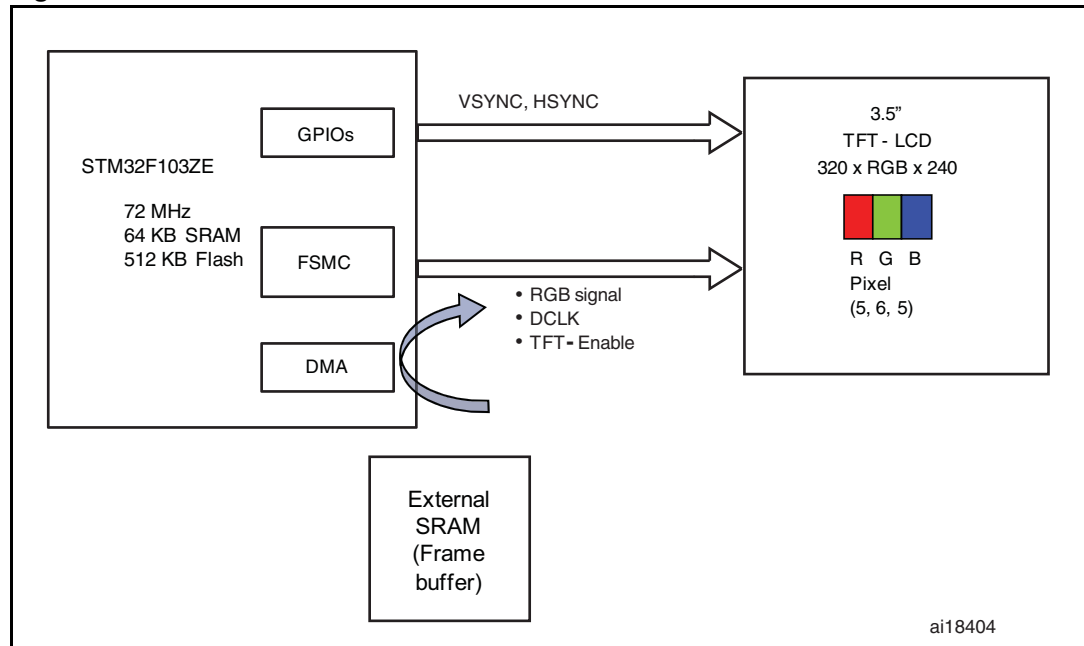


2 STM32 QVGA TFT-LCD drive implementation

The STM32-based TFT-LCD drive is implemented using the FSMC 16-bit data bus. The STM32 has two internal DMA controllers that are used to boost the display performance, thereby enabling an increased display frame rate.

An external SRAM memory is used as frame buffer to allow a continuous image-refresh process which can be controlled by a timer.

Figure 4. STM32 TFT-LCD Drive



2.1 QVGA TFT-LCD signal interfacing with STM32F10xx FSMC

The TFT-LCD synchronization signals VSYNC and HSYNC are managed through STM32 GPIOs.

The FSMC memory interface Write-enable signal is used in inverted configuration as a DCLK (pixel clock) for the TFT, and the FSMC chip-select signal acts as a TFT-enable signal.

When data is transferred to the FSMC bus, the chip-select is first asserted low to enable the TFT-LCD. Then the write-enable signal is asserted low to allow 16-bit data transfer to the TFT RGB line on its low level which results in a single pixel display:

- TFT-Enable: FSMC chip select (pin PG12)
- VSYNC: GPIO - pin PA8
- HSYNC: GPIO - pin PC6
- DCLK: FSMC WE in inverted mode - pin PD5
- Data Bus: FSMC[D0:D15]
- SPI1: used for LCD configuration

2.2 Image format and resolution

The 16-bit data bus of the STM32 FSMC can drive a controller-less 24-bit LCD module. With only 16 data lines on the FSMC memory bus, the interface is a 565-format RGB. The remaining lines of the QVGA TFT-LCD are left open. The images are loaded in external SRAM memory in 565 format to avoid conversion overhead for the STM32.

From a performance perspective, converted image availability in memory offers the benefit of fast data transfer to the TFT interface. So, a faster image refresh rate can be supported.

- Pixel data size = 16 bit = 2 bytes
- Image memory size for QVGA TFT = $320 \times 240 \times 2 = 153600$ Bytes

2.3 Image source

The 565 format images are programmed in NOR memory.

In a first step, two images are transferred from NOR to external on-Board SRAM. External SRAM acts as frame refresh buffer for TFT-LCD.

To implement an animated banner display, the SRAM frame buffers are updated during run mode with new images from NOR memory. This approach is used to maintain the exact working model of the TFT-LCD controller.

The on-board NOR memory contains the programmed images which are to be used for display on the LCD. SRAM Double buffer management allows the source data to be updated in run mode.

2.4 STM32 QVGA LCD-TFT direct drive flow

To achieve a static image view on a controllerless TFT, the image frame has to be refreshed at a rate of at least 15 fps. Vertical and horizontal scanning of one frame are performed as per the TFT-LCD module specifications.

A QVGA-LCD module single-frame display needs 320x240 pixels of data.

240 horizontal lines (each of 320 pixels) are scanned vertically on the TFT to display one frame.

Along with data scanning, dummy data writes are required for the TFT to reach the required horizontal and vertical front and back-porch values. These values are available the TFT datasheet.

Dummy data writes are composed of writing zero data to the TFT RGB lines.

- DMA1_Channel1 is used for back porch data transfer
- DMA1_Channel2 is used for active data transfer
- DMA1_Channel3 is used for front porch data transfer

The FSMC is configured in asynchronous mode and operates in Mode1 which is the default mode selected when configuring the SRAM memory type.

Figure 5 and *Figure 6* show the FSMC asynchronous read and write transactions in SRAM mode1 for one 16-bit data pixel.

Figure 5. Mode 1 - SRAM read accesses

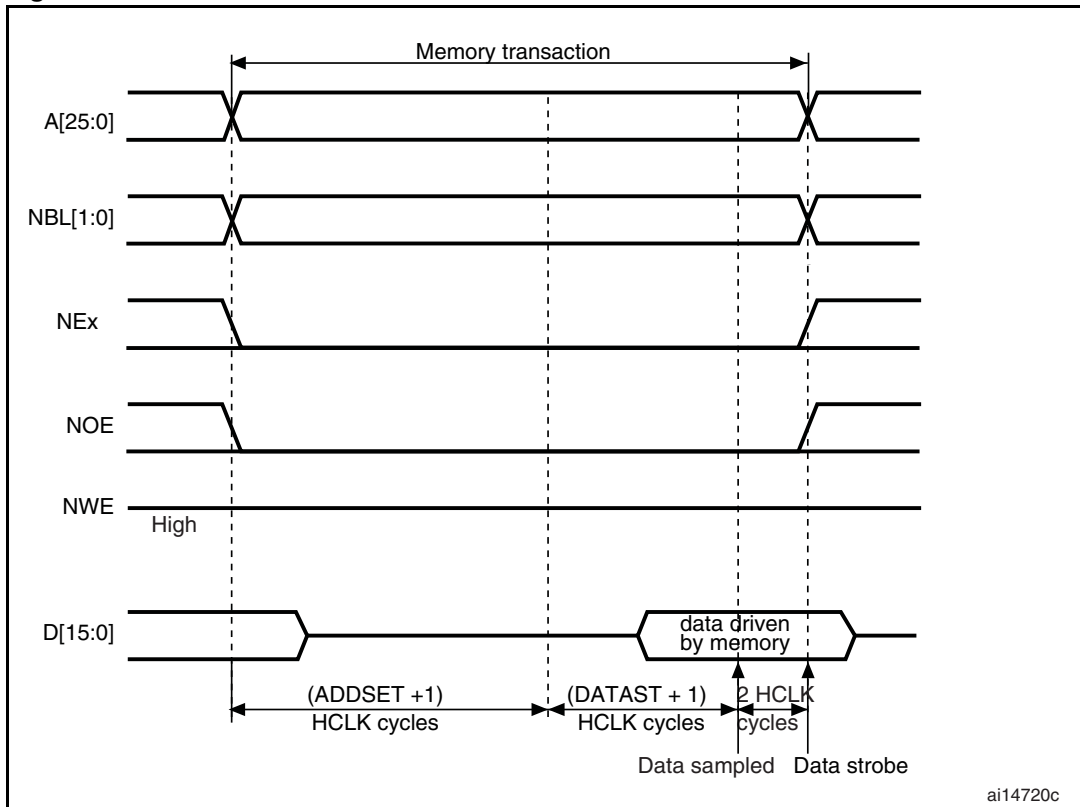
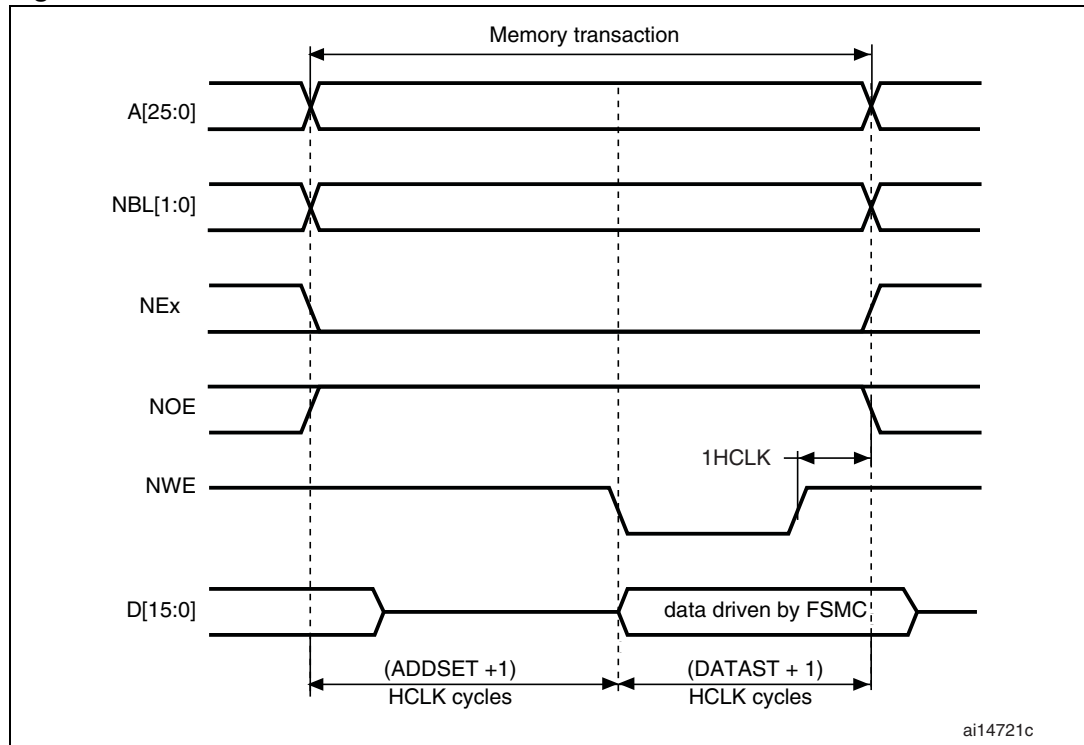


Figure 6. Mode1- SRAM write accesses



The DMA channels are used to refresh images on the TFT-LCD. This offloads the CPU from data transfer tasks.

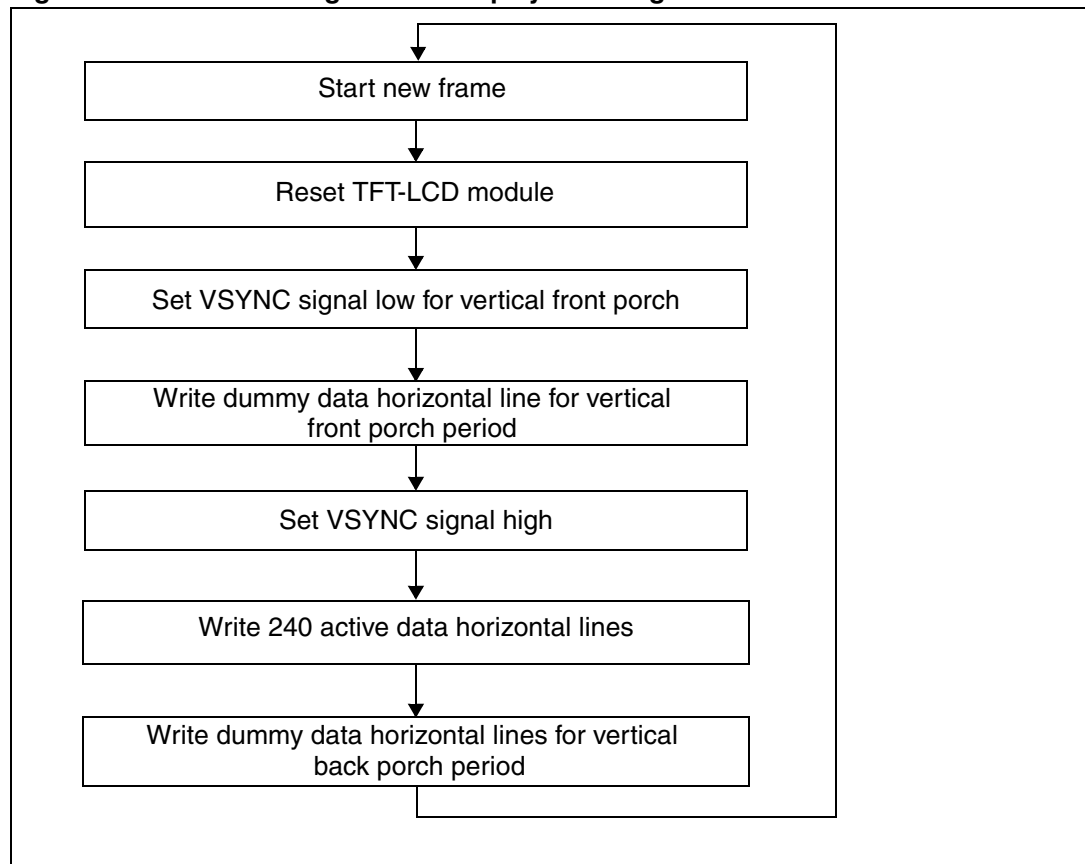
The DMA is configured with external SRAM memory as the source and the LCD as the destination. DMA transfer complete interrupts are used to toggle the VSYNC and HSYNC synchronisation signals for a new frame transfer. A timer (TIM3) is used to control the display frame rate.

When the DMA writes data on the FSMC bus, the FSMC generates the TFT-enable signal, TFT DCLK, and data are written to the TFT RGB lines.

In this way, the STM32 manages the complete image display for controller-less TFT LCD modules.

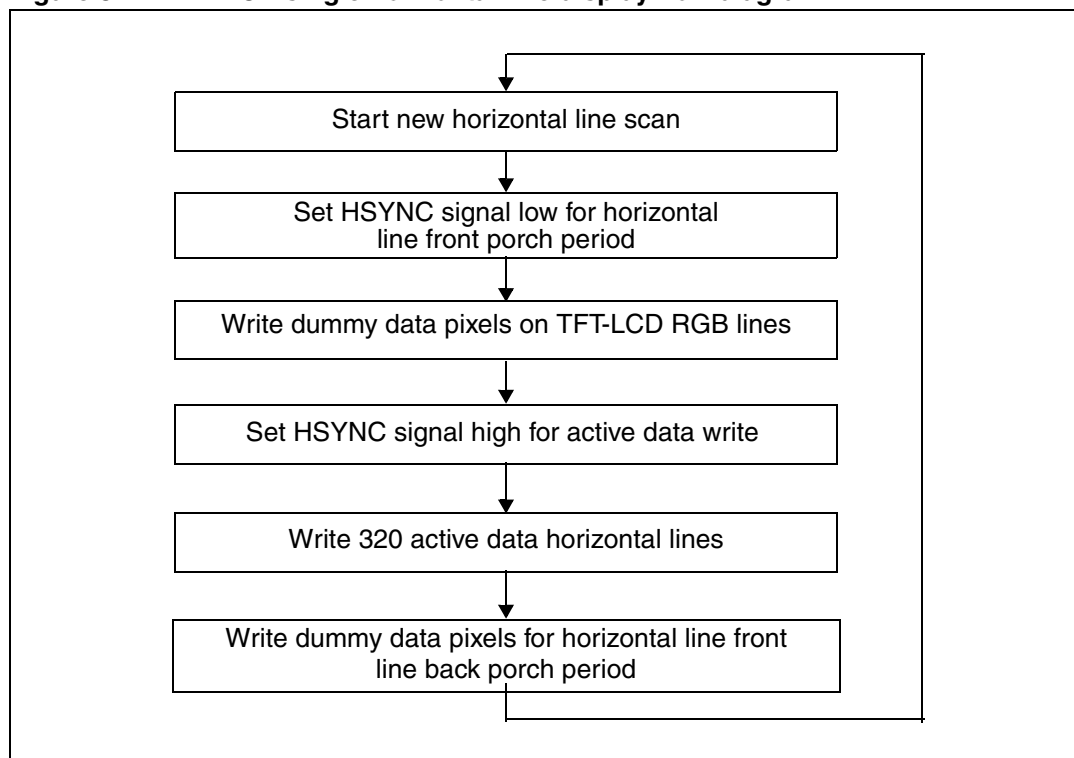
Figure 7 and *Figure 7* show the TFT- LCD single-frame and horizontal-line display flow diagram.

Figure 7. TFT- LCD single-frame display flow diagram



Note: Refer to the TFT-LCD datasheet for the vertical front porch and back porch period values.

Figure 8. TFT- LCD single horizontal-line display flow diagram



Note: Refer to the TFT-LCD datasheet for the horizontal front porch and back porch period values

2.4.1 Display modes

Two display modes are provided and can be selected.

STM32 slide-show display mode

In this mode, two static images in the SRAM buffers are displayed on the TFT-LCD after a fixed time interval. The user can configure more than 2 images as well as change the Frame buffer address location. In this mode, up to 40 frames per second can be displayed.

Table 1. STM32 slide-show display: CPU load & frame rate

Parameter	Value
DCLK (pixel clock)	3.6 MHz
Maximum frame rate	40 Hz
CPU load	1%

STM32 banner display mode

In this mode, image buffers in SRAM are dynamically updated from NOR Flash memory to show an image animation. For updating the image, two DMA channels are used.

Table 2. STM32 slide-show display: CPU load & frame rate

Parameter	Value
DCLK (pixel clock)	3.6 MHz
Maximum frame rate	19 Hz
CPU load	51%

The frame rate in Banner display mode is lower due to the SRAM frame buffer dynamic update for the animation. The Frame buffer update is made after the display of one complete frame display.

Note: The frame rate and CPU load measurements were done with high speed optimization using EWARM Toolchain V5.5. The CPU frequency is 72 MHz.

2.5 TFT-LCD backlight control

In both display modes, the TFT backlight is also controlled via a Timer and an ADC channel.

The timer (TIM4) is configured to generate 1 KHz PWM signal output on PB6 and can be used as a PWM enable signal for the TFT backlight controller. The TFT-LCD backlight control is implemented by varying the duty cycle of the PWM enable signal by rotating the RV1 potentiometer installed on the MB672 STM3210E-EVAL evaluation board.

For more details on the potentiometer hardware, please refer to the MB672 STM3210E-EVAL evaluation board user manual.

3 Hardware reference design

The STEVAL-CCM002V1 evaluation board intended to be used as a daughter board for MB672 STM3210E-EVAL Evaluation board. The STEVAL-CCM002V1 board has a QVGA TFT 3.5" (CT05350DW0000T (thin-film-transistor liquid crystal display)).

The table below provides description of the CT05350DW0000T TFT signals when interfacing with STM32F103ZET6.

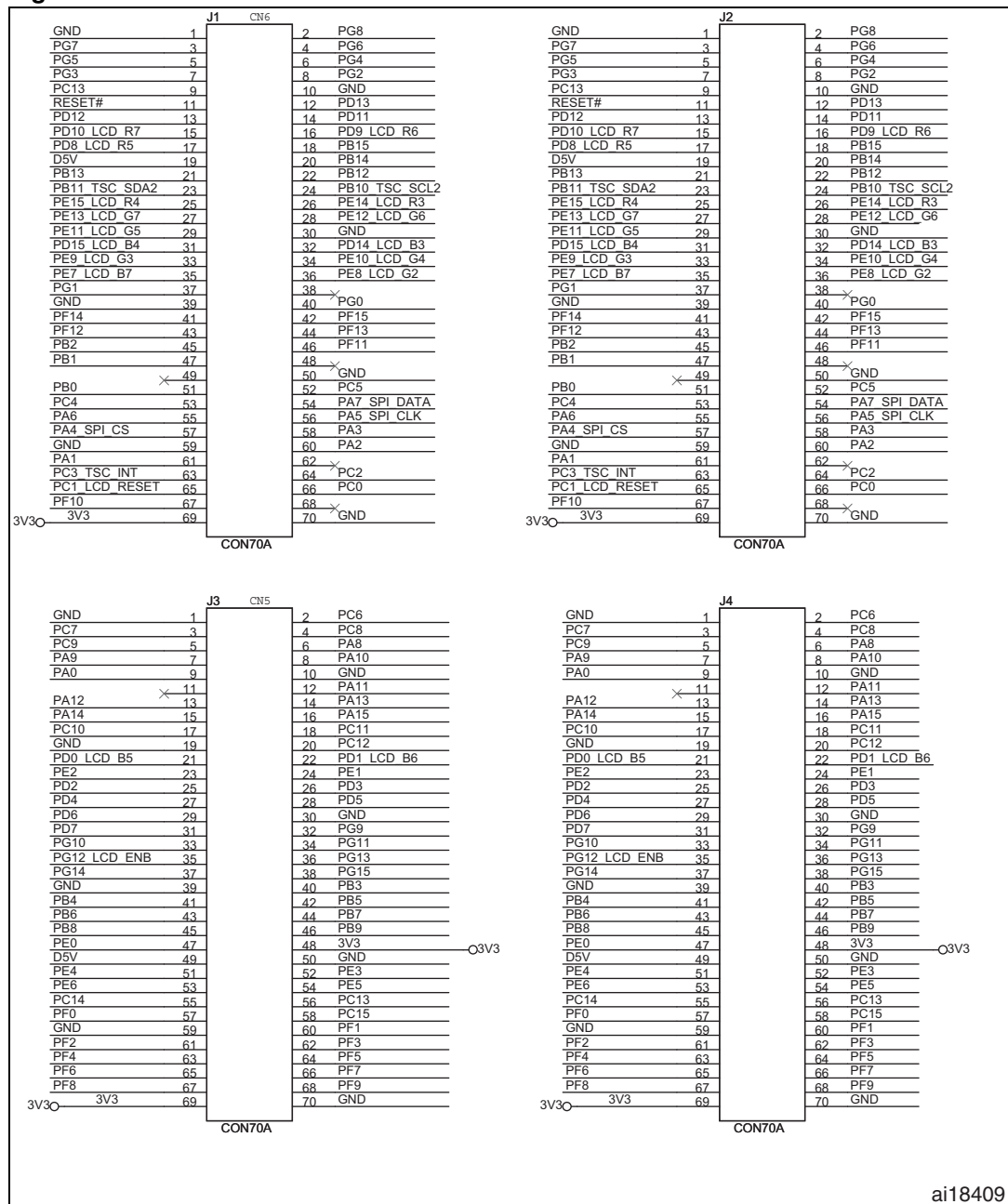
Table 3. STM32F103ZET6 signal interface with CT05350DW0000T LCD

LCD signal	STM32F103ZET6 signal	Description
LCD Reset	GPIO- PC1	Used to reset TFT-LCD
LCD X1,X2,Y1,Y2	Connected to STMPE811 touchscreen controller device	LCD touch screen signals
LCD B0-LCD B2	Do not connect	LCD blue data lines [0-2]
LCD B3-LCD B7	FSMC[D0..D4]	LCD blue data lines [3-7]
LCD G0-LCD G1	Do not connect	LCD green data lines [0-1]
LCD G2-LCD G7	FSMC[D5..D10]	LCD green data lines [2-7]
LCD R0-LCD R2	Do not connect	LCD red data lines [0-2]
LCD R3-LCD R7	FSMC[D11..D15]	LCD red data lines [3-7]
LCD HSYNC	GPIO- PC6	LCD horizontal synchronization signal
LCD VSYNC	GPIO- PA8	LCD vertical synchronization signal
LCD DCLK	FSMC NWE Inverted	LCD pixel clock signal
LCD SPI CS	SPI1_CS - PA4	LCD SPI chip select signal
LCD SPI CLK	SPI1_CLK - PA5	LCD SPI clock signal
LCD SPI DATA	SPI1_MOSI -PA7	LCD SPI data signal
LCD ENABLE	FSMC NE4	LCD chip select signal

Please refer to User manual UM0921 for a complete description of the STEVAL-CCM002V1 daughter board.

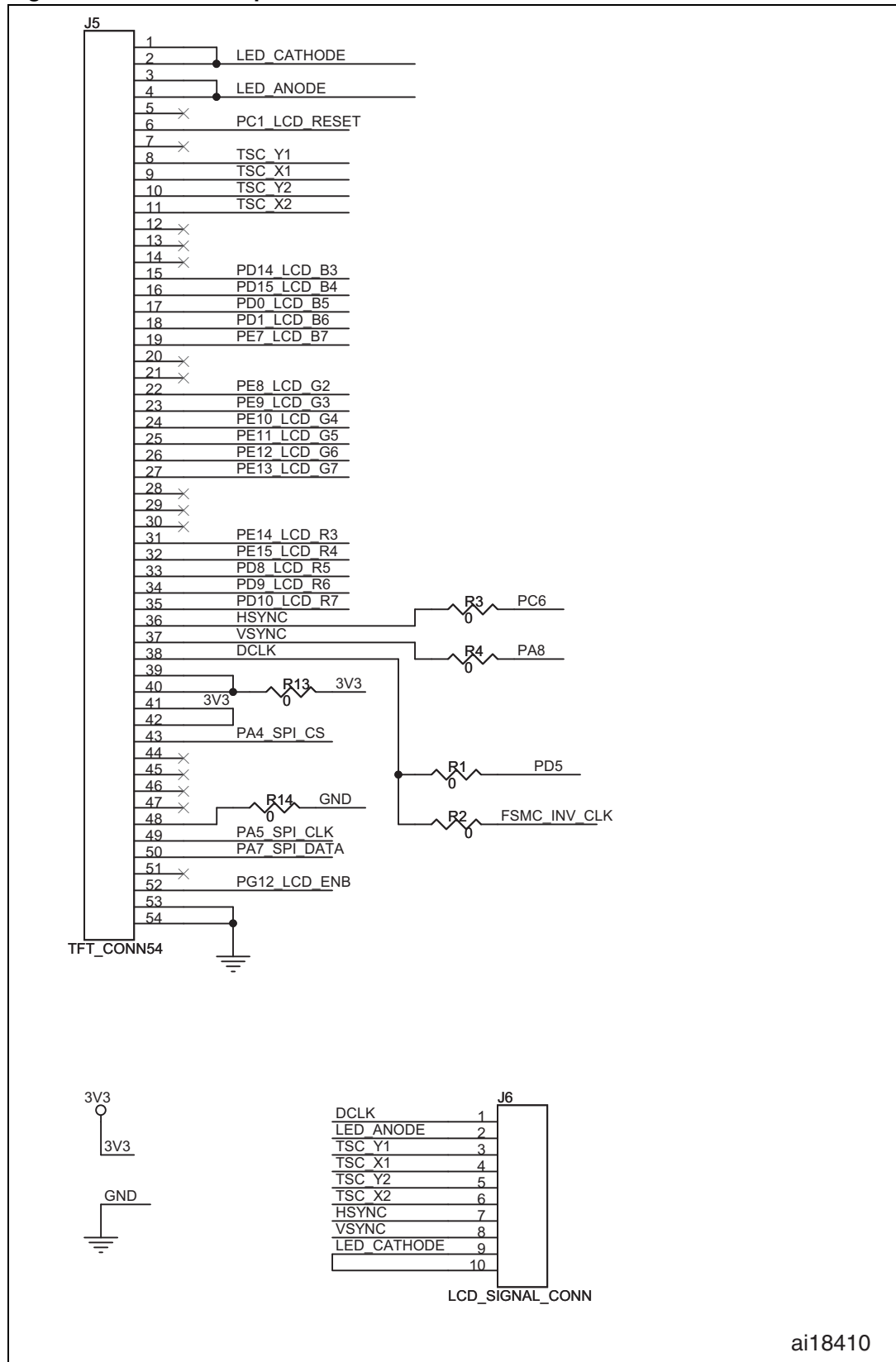
The daughter board order code is: STEVAL-CCM002V1.

Figure 9. STM3210E- EVAL board connector for TFT-LCD



ai18409

Figure 10. TFT-LCD 54 pin connector



ai18410

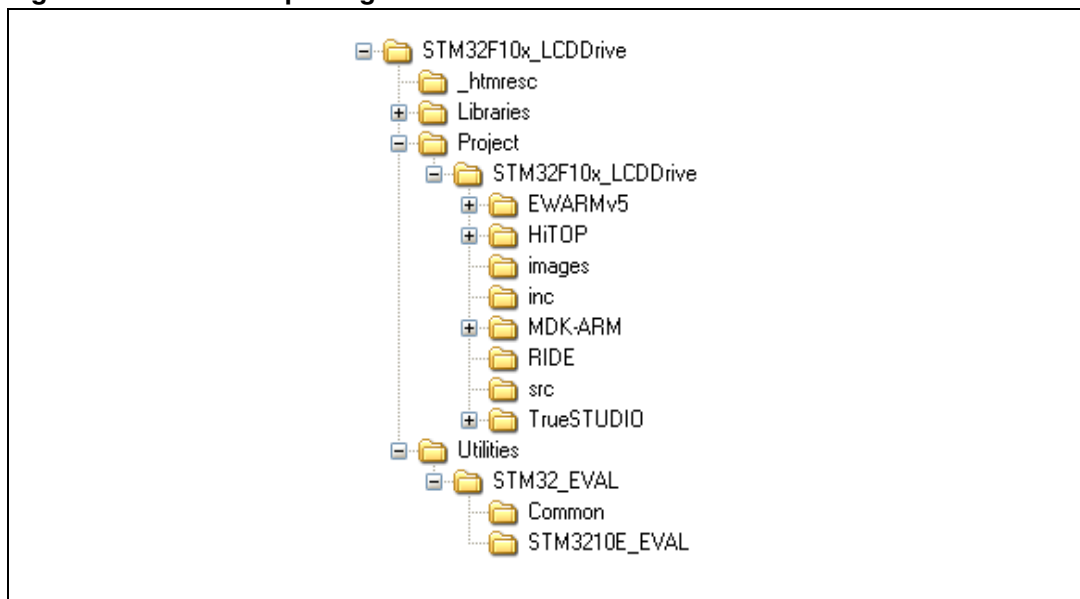
4 Firmware package

The firmware associated to this application note consists of a demonstration of a direct drive TFT (CT05350DW0000T) using the STM32F103ZE device. The source code example is based on the STM32F10xxx standard peripheral library V3.3.0.

The user may build any similar application using the same library and driver, and different interfacing firmware/hardware.

The firmware package installation folders are shown in [Figure 11](#).

Figure 11. Firmware package architecture



Libraries

The Libraries folder contains all the subdirectories and files that make up the core of the STM32F10xxx Standard Peripheral library V3.3.1:

CMSIS

- CM3\CoreSupport: contains the Cortex-M3 files
- CM3\DeviceSupport\ST\STM32F10x: contains the STM32F10x CMSIS layers files.

STM32F10x_StdPeriph_Driver

- inc subfolder: contains the Standard Peripheral library header files
- src subfolder: contains the Standard Peripheral library source files

Project

STM3210x-LCDDrive

Images: contains the Image.dfu file of the bitmap images.

EWARMv5: contains preconfigured projects for the EWARM toolchain

ARM-MDK: contains preconfigured projects for the RVMDK toolchain

HiTOP: contains preconfigured projects for the HiTOP toolchain

RIDE: contains preconfigured projects for the RIDE toolchain

TrueSTUDIO: contains preconfigured projects for the attolic toolchain

- **inc** subfolder: contains the TFT-LCD driver and the demonstration heard files:
 - lcd_driver.h: contains the prototypes of the basic functions to drive a controller-less TFT-LCD. It includes also the TFT-LCD configurable parameters following the TFT specification.
 - backlight_control.h: contains the prototypes of the basic functions used to control the TFT backlight.
 - main.h: this file contains prototypes for the main.c file
 - stm32f10x_it.h: contains the headers of the interrupt handler.
 - stm32f10x_conf.h: the microcontroller library configuration file

- **src** subfolder: contains the TFT-LCD driver and the demonstration source files:
 - lcd_driver.c: it contains basic routines to drive a controller-less QVGA TFT-LCD including the FSMC, GPIO pins and DMA configurations
 - backlight_control.c: contains the basic functions used to control the TFT-LCD backlight.
 - mainc.c: initializes the TFT-LCD Drive demonstration
 - stm32f10x_it.c: contains all the peripheral interrupt service routines used in the LCD driver and provides templates for all exception handlers.

Utilities

STM3210E-EVAL: contains the STM3210E-EVAL board-related drivers

4.1 Firmware installation

The firmware associated with this application note is built for the STM3210E- EVAL Evaluation board and the STEVAL-CCM002V1 daughter board.

After successful hardware setup and firmware programming, a bitmap image starts displaying on the TFT-LCD on the STEVAL-CCM002V1 evaluation board.

Banner display mode is selected by default.

Push the Key button connected to PB3 on the STM3210E-EVAL Evaluation board to switch to slide show display mode.

Demonstration Images

16-bit Bitmap images are copied by the firmware from NOR memory to on-board external SRAM during firmware initialization. Then the image is refreshed on the TFT-LCD from external SRAM only.

These images are programmed by default in the NOR memory the MB672 STM3210E-EVAL Evaluation board. If the images are not available in NOR memory, they can be easily programmed in the NOR memory using USB DFU firmware. For more details on board and NOR programming, refer the UM0549 user manual available on www.st.com.

The USB DFU firmware and DFU image file are available for download from the STMicroelectronics website: www.st.com.

4.2 How to configure the QVGA TFT-LCD parameters

The LCD driver can be customized to support other types of QVGA LCDs. The QVGA LCD parameters that can be updated are the front porch, back porch period or frame rate frequency as well as the I/O pins used for VSYNC and HSYNC, TFT power control and backlight.

These configurable parameters are defined in the `lcd_driver.h` and `backlight_control.h` header files.

The TFT LCD driver can be easily ported to other hardware. [Table 4](#) describes the configurable TFT-LCD parameters.

Table 4. QVGA TFT-LCD driver configurable parameters

QVGA TFT-LCD parameters	Description
<code>#define LCD_FRAME_FRONT_PORCH</code>	Frame Front Porch value
<code>#define LCD_FRAME_BACK_PORCH</code>	Frame Back Porch value
<code>#define LCD_LINE_FRONT_PORCH</code>	Line Front Porch value
<code>#define LCD_LINE_BACK_PORCH</code>	Line Back Porch value
<code>#define SRAM_IMAGE1_ADDR</code>	Address of first image in frame buffer
<code>#define SRAM_IMAGE2_ADDR</code>	Address of second image in frame buffer
<code>#define FRAME_RATE</code>	Frame rate frequency value (can be 40 Hz or 19 Hz)
<code>#define SLIDESHOW_TIME_GAP</code>	Slide show time value in second
<code>#define TFT_VSYNC_GPIO_PIN</code>	GPIO Pin:GPIO_Pin_8
<code>#define TFT_VSYNC_GPIO_PORT</code>	GPIO Port: GPIOA
<code>#define TFT_HSYNC_GPIO_PIN</code>	GPIO Pin: GPIO_Pin_6
<code>#define TFT_HSYNC_GPIO_PORT</code>	GPIO Port: GPIOC
<code>#define LCD_BL_GPIO_PIN</code>	GPIO Pin: GPIO_Pin_6
<code>#define LCD_BL_GPIO_PORT</code>	GPIO Port: GPIOB

5 Conclusion

The versatile capabilities of the STM32 peripherals have been put to good use in this case, with the objective of simplifying and lowering the cost of a TFT-LCD based application. The STM32 with its powerful DMA controller and highly flexible FSMC peripheral combine to offer a cost-effective solution for driving a QVGA TFT-LCD with a CPU load of only 1% for static image display.

6 Revision history

Table 5. Document revision history

Date	Revision	Changes
16-Jul-2010	1	Initial release.

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