AN3322
Application note

Watt-hour meter based on the STM32F101 microcontroller

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Introduction

This document describes, in detail, the hardware and software implementation of a watt-hour meter using the STM32F101 microcontroller. This cost effective watt-hour meter uses shunt with an operational amplifier as a current sensor, an embedded 12-bit ADC for current and voltage measurement, GPIO for LCD management, and a lot of other peripherals for communication, tamper detection, keyboard, and power disconnection. Powerful architecture of the STM32™ microcontroller allows sampling at 1 Msps. The high sampling rate makes it possible to use methods for ADC resolution enhancement.

Main features

- Metrological parts
  - Microcontroller and external op amp only
  - Compliant with EN 50470-1:2006 Class B, precision better than 1%
  - Starting current 20 mA, nominal current 5 A, maximum current 100 A
  - Reads the voltage and the current signal up to the 21st harmonic
  - Shunt as a current sensor. CT and Rogowski coil is optional
- Additional parts included in reference design
  - LCD driven directly by microcontroller
  - Keyboard driven directly by microcontroller
  - An extra external EEPROM for user data
  - Bi-stable relay, IR communication, serial communication
  - Backup battery, complete power meter power management

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1 Watt-hour meter using the STM32

The following sections describe the necessary feasibility study, theory and computation for the STM32 power meter implementation. The system design, STM32 parameter evaluation, ADC feature enhancement, and international standards are also covered here.

1.1 STM32 ADC parameters

The most important part of the power meter and its microcontroller used in metering applications is the embedded ADC. Its parameters are the key to deciding if the requirements for precision of the implemented meter can be fulfilled (international standards mentioned in these sections). The first step is to evaluate the parameters given in the ADC specifications:

Table 1. STM32 ADC parameter specifications

Symbol	Parameter	Test conditions	Typ.	Max.	Unit
ET	Total unadjusted error	f_{PCLK2} = 24 MHz, f_{ADC} = 12 MHz, R_{AIN} < 10 kΩ, V_{DDA} = 3 to 3.6 V, T_A = 25 °C, Measurements made after ADC calibration, V_{REF+} = V_{DDA}	±1.3	±2	LSB
EO	Offset error		±1	±1.5	
EG	Gain error		±0.5	±1.5	
ED	Differential linearity error		±0.7	±1	
EL	Integral linearity error		±0.8	±1.5	

For the given STM32 ADC, the specifications and tests show:

Equation 1

Integral non-linearity error is $E_{INL}^{12-bit} = 0{,}8LSB_{12-bit}$.

Equation 2

The resolution of the 12-bit ADC is $\frac{1}{2^{12}}$ = 0.02% of the full scale ADC range.

Equation 3

If $E_{INL}^{12-bit} < 1LSB$, then the *accuracy* = *resolution* of given ADC.

Equation 4

The accuracy of the 12-bit ADC is $\frac{1}{2^{12}}$ = 0.02% of the full scale ADC range.

1.2 Requirements for meter in Class B

The European standard defining the requirements for electricity metering equipment should be the source of constraints and limits for the design presented in this application note. EN 50470-1:2006 and EN 50470-3:2006 are referenced in this case. All the computation is directed to the precision of Class B.

Definitions of the power meter parameters (according to EN 50407-1:2006)

RMS values indicated

I - current - the electrical current flowing through the meter.

I_{st} - starting current - the lowest value of the current at which the meter is declared to register active electrical energy at unity power factor.

I_{min} - minimum current - the lowest value of the current at which the European standard specifies accuracy requirements. At and above I_{min}, up to I_{tr}, relaxed accuracy requirements apply.

I_{tr} - transitional current - the value of the current at, and above which, up to I_{max}, full accuracy requirements of the European standard apply.

I_{ref} - reference current - for direct meters, 10 times the transitional current. (This value is the same as the basic current, I_b defined in the EN 62052-11, chapter 3.5.1.2.) For current transformer operated meters, 20 times the transitional current. (The value is the same as rated current I_n.)

I_{max} - maximum current - the highest value of current at which the meter purports to meet the accuracy requirements of this European standard (EN 62052-11, chapter 3.5.2.).

I_{tr} - can be chosen (for Class B) from the set of values: 0.5, 1, 1.5 and 2 A

Example 1

Example of one setup for a meter

I_{tr} - chosen 0.5 A

I_{st} = 0.04 I_{tr} = 20 mA

I_{min} = 0.5 I_{tr} = 250 mA

I_{max} > 50 I_{tr}, I_{max} > 25 A

Figure 1 shows the prescribed precision in given current intervals.

Figure 1. Requirements for Class B power meter precision, three ranges

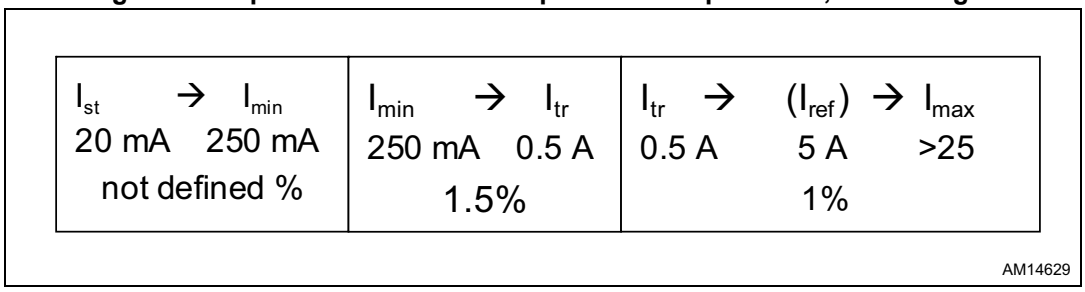
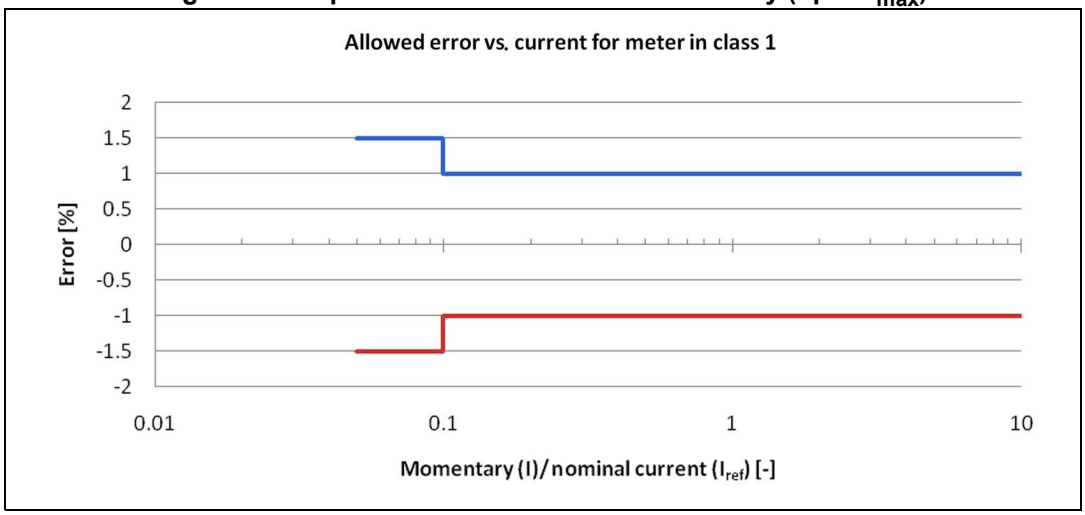


Figure 2. Template used to check meter accuracy (up to I_{max})



1.3 STM32 ADC dynamic measurement range

The precision and resolution of the ADC determines the dynamic range of measured voltage and current. This section analyses whether the given ADC is capable of covering, with its precision and resolution, the whole range for requested maximum current and voltage.

The input current and voltage are scaled to the full scale of the STM32 ADC:

- By a voltage divider for voltage measurement
- By a shunt and external operational amplifier for a low current measurement
- By a shunt and external operational amplifier for a high current measurement.

1.3.1 Voltage measurement

One voltage channel, nominal voltage 230 V RMS is used

$U_{peak\text{-}to\text{-}peak}$ = 230 x $\sqrt{}$2 x 2 x 120% = 780 V (120% means a safety margin)

Resolution for 780 V: $U_{LSB:peak\text{-}to\text{-}peak}$ = 780 V x 0.02% = 0.16 V

Resolution for 230 V: $U_{LSB:RMS}$ = 230 V x 0.02% = 0.055 V_{RMS}

Value 0.02% represents resolution and precision of the ADC and is defined in *Section 1.1: STM32 ADC parameters*.

The range where it is necessary to take care of the precision is between 80% to 115% (extended operating range) of the nominal voltage:

U_{MAX} = 230 V_{RMS} x 115% = 253 V_{RMS}

U_{MIN} = 230 V_{RMS} x 80% = 184 V_{RMS}

For the lowest and highest voltage value the precision of the voltage measurement is:

Error of U_{MAX} = 0.055 V_{RMS} / 184 V_{RMS} = 0.030%

Error U_{MIN} = 0.055 V_{RMS}/ 253 V_{RMS} = 0.022%

Error values are much lower than prescribed by standards: 1% >> 0.030%.

1.3.2 There are two current ranges in the meter

Low gain range (LG): for 100 A range a resolution and accuracy with the 12-bit ADC are:

I_{max} = 100 x 2 x 1.414 = 300 $A_{peak-peak}$

Resolution in A for maximum value: 300A x 0.02% = 60 mA

Resolution in A for RMS value: 100 A_{RMS} x 0.02% = 20 mA_{RMS}

Minimal error of measurement of current about:

- Starting current: I_{st}: 20 mA_{RMS} / 20 mA_{RMS} = 100% (no precision prescribed)
- Minimum current: I_{min}: 20 mA_{RMS} / 250 mA_{RMS} = 8% (1,5% prescribed)
- Transition current: I_{tr}: 20 mA_{RMS} / 500 mA_{RMS} = 4% (1% prescribed)
- Reference current: I_{ref}: 20 mA_{RMS} / 5 A_{RMS} = 0.4% (1% prescribed)
- Maximum current: I_{max}: 20 mA_{RMS} / 100 A_{RMS} = 0.02% (1% prescribed).

Error values are lower than prescribed standards in case of I_{ref} and I_{max}. Lower currents I_{min} and I_{tr} cannot be measured within this LG range.

High gain range (HG): for 10 A range a resolution and accuracy with the 12-bit ADC are:

I_{max} = 10 x 2 x 1.414 = 28 $A_{peak-peak}$

Resolution in A for maximum value: 28 A x 0.02% = 5.8 mA

Resolution in A for RMS value: 10 A_{RMS}x 0.02% = 2.4 mA_{RMS}

Minimal error of measurement of current about:

- Starting current: I_{st}: 2.4 mA_{RMS} / 20 mA_{RMS} = 12% (no precision prescribed)
- Minimum current: I_{min}: 2.4 mA_{RMS} / 0.5 A_{RMS} = 0.48% (1,5% prescribed)
- Transition current: I_{tr}: 2.4 mA_{RMS} / 1 A_{RMS}= 0.24% (1% prescribed)
- Reference current: I_{ref}: 2.4 mA_{RMS} / 5 A_{RMS} = 0.048% (1% prescribed)
- Maximum current: I_{max}: 2.4 mA_{RMS} / 10 A_{RMS} = 0.024% (1% prescribed).

Error values are lower than prescribed standards in the case of I_{st}, I_{min}, I_{tr}, and I_{ref}. Higher current I_{max} cannot be measured within this HG range due to ADC saturation.

From the analysis performed in this section it can be seen that a system using one range for voltage and two ranges for current measurement can fulfill requirements for the prescribed precision of the system.

1.4 Error sources on the STM32 meter

There are a lot of sources of error when measuring current and voltage. They can be compensated in mostly all cases.

1. ADC linearity: it limits total accuracy compensated by ADC symmetry, see *Section 1.5*.
2. Temperature: external voltage reference keeps ADC conversion stable.
3. Op amp and ADC offsets: they are removed by AC coupling, calibration and digital filtering.
4. ADC gain: it is compensated by calibration of the meter.
5. Thermal noise present on the STM32 meter PCB board: see *Section 1.6*.
6. Crosstalk between subsequent channel measurement: compensation is discussed in *Section 1.7*.
7. Linearity of op amps: it is present, not compensated. Selection of a good op amp is made.
8. Phase shift between channels; the compensation is shown in *Section 2.7*.

1.5 Linearity of STM32 ADC and its INL reduction

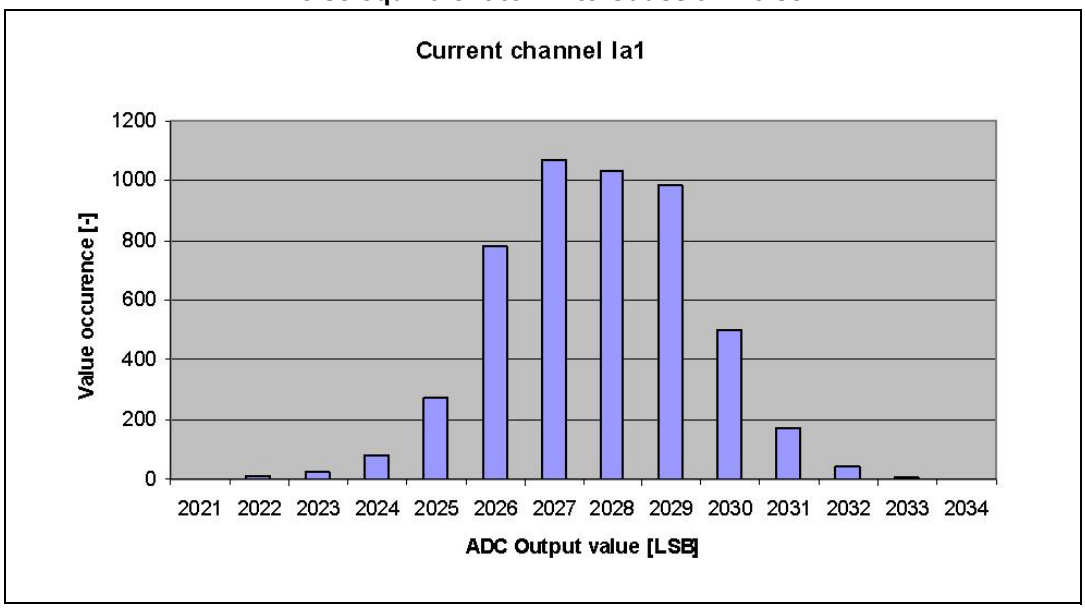
Increasing the ADC resolution does not result in higher accuracy since the techniques for obtaining higher resolution can reduce DNL (differential non-linearity) but not INL (integral non-linearity), see *Section 1.9: ADC enhancement by oversampling technique*.

The linearity can be enhanced (INL reduction) from 0.7 to 0.17 LSB by the application of a simple technique to the HW and SW design. Good knowledge of the ADC is assumed for this technique, described in a separate document supplied on request.

1.6 Thermal noise present on STM32 meter platform

The number of effective bits of a given ADC depends on the presence of noise in the system, namely on the PCB and microcontroller itself. If the noise is white Gaussian noise (or similar), the number of effective bits can be recovered by oversampling and decimation mentioned in *Section 1.9*. *Figure 3* brings a direct noise measurement of the system. The single voltage level was connected to an input of the ADC on the STM32 power meter board and a thousand samples were collected. *Figure 3* shows a histogram of the values taken.

Figure 3. Typical thermal noise present on STM32 meter platform. Histogram shows noise equivalent to white Gaussian noise



Measured thermal noise (overall on the board) degrades the ADC resolution and accuracy by 2 to 5 LSB. This means that the number of effective bits drops from 12 to less than 10. To recover from this situation it is necessary to use techniques for NOEB (number of effective bits) enhancement, see *Section 1.9*. Using oversampling requires, in some cases, the addition of the dithering signal. According to the noise level found in this system, it is not necessary to add the dithering signal. It's addition does not bring any enhancement in the performance.

1.7 Crosstalk between subsequent multiplexed channels

When reading more channels subsequently with maximum speed, values sampled from the subsequent channel may be influenced by the reading of the previous channel. This is called crosstalk between subsequent multiplexed channels.

It is caused by the balance of external impedance and capacitance of a signal source and an internal impedance and capacitance of the sample and hold circuit in the given ADC. The longer the sample and hold phase, the lower the correlation between subsequent samples.

The technique to overcome this phenomenon presented in this section is based on reading every channel in the sequence twice and only the second value is taken as the valid one. The error is reduced from 0.07% of ADC full range to less than 0.0001%.

The total conversion time is calculated as follows:

Equation 5

T_{conv} = sampling time + 12.5 cycles

Example 2

With an ADCCLK = 14 MHz and a sampling time of 1.5 cycles:

T_{conv_14MHz} = 1.5 + 12.5 = 14 cycles = 1 µs

Example 3

With the setting used in this application ADCCLK = 9 MHz and a sampling time of 1.5 cycles:

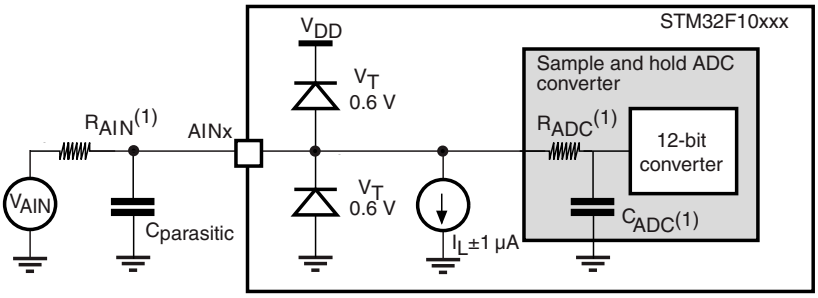
T_{conv_9MHz} = 1.5 + 12.5 = 14 cycles = 1.56 µs

$T_{Sampling\_time}$ = (1.5 cycles / 14 cycles) x 1.56 µs = 167 ns

Table 2. STM32 ADC input characteristics specifications

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
RADC	Sampling switch resistance				1	kΩ
CADC	Internal sample and hold capacitor				12	pF

Figure 4. Internal and external analog input pin capacitors and resistors



Equation 6

R_{129} = 820 Ω and R_{137} = 820 Ω (resistors between an output of op amp and an ADC input)

$R_{AIN} = R_{129} = R_{137}$ = 820 Ω

R_{OpAmp} = 80 Ω

$\tau = RC = (R_{ADC} + R_{AIN}) + R_{OpAm}p)\ C$ = 1900 Ω x 12 pF = 22.8 ns

Error % = 100 x exp. [-1 x ($T_{Sampling\_time}$/ τ)]

Table 3. Crosstalk between subsequent multiplexed channels

Number of the same channel readings [-]	T_{conv} [cycle / µs]	$T_{Sampling\_time}$ [ns]	Error [%]
1	1.5 / 1.55	167	0.07
2	3.0 / 3.10	334	0.00
3	4.5 / 4.65	501	0.00
4	6.0 / 6.20	668	0.00

From *Table 3* it is recommended to use every second value sampled on the same channel. This approach renders an error caused by this phenomenon negligible.

1.8 Power and energy measurement by STM32 embedded ADC

This section gives a complete overview of the whole hardware and firmware of the STM32 power meter design. *Figure 5* shows a block diagram of the firmware, *Figure 6* and *Figure 7* show the physical realization of the current and voltage path.

Figure 5. Complete block diagram of the algorithm used in STM32 power meter

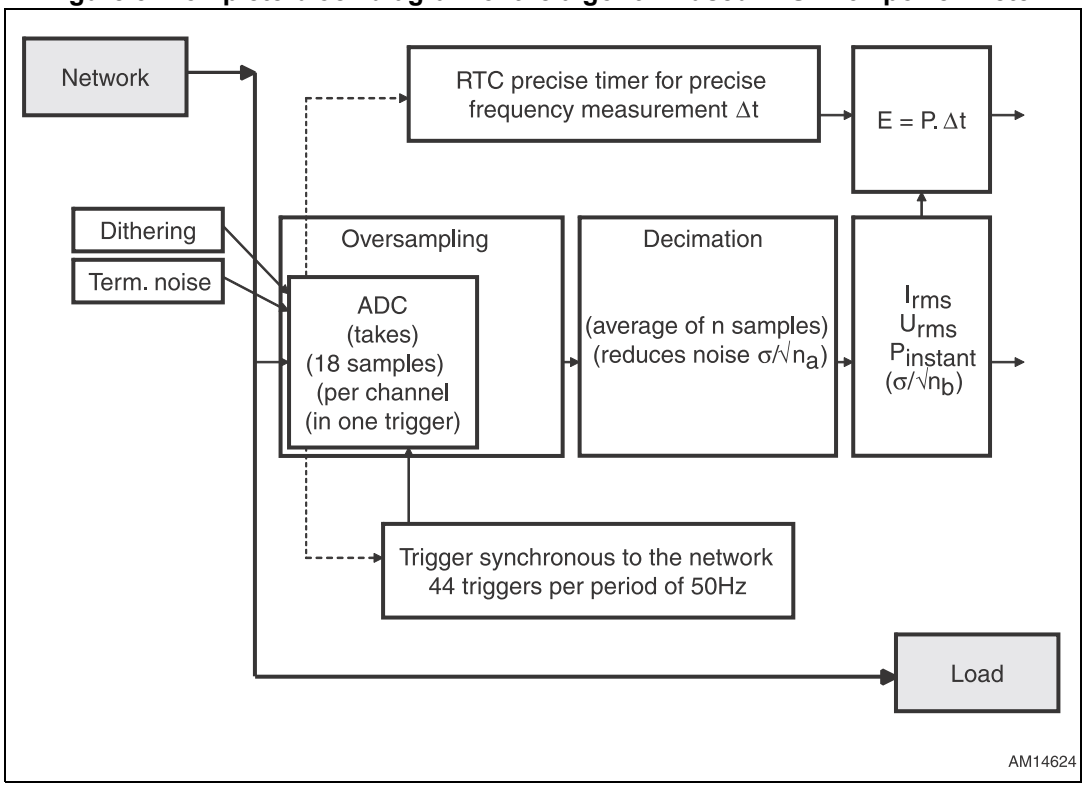
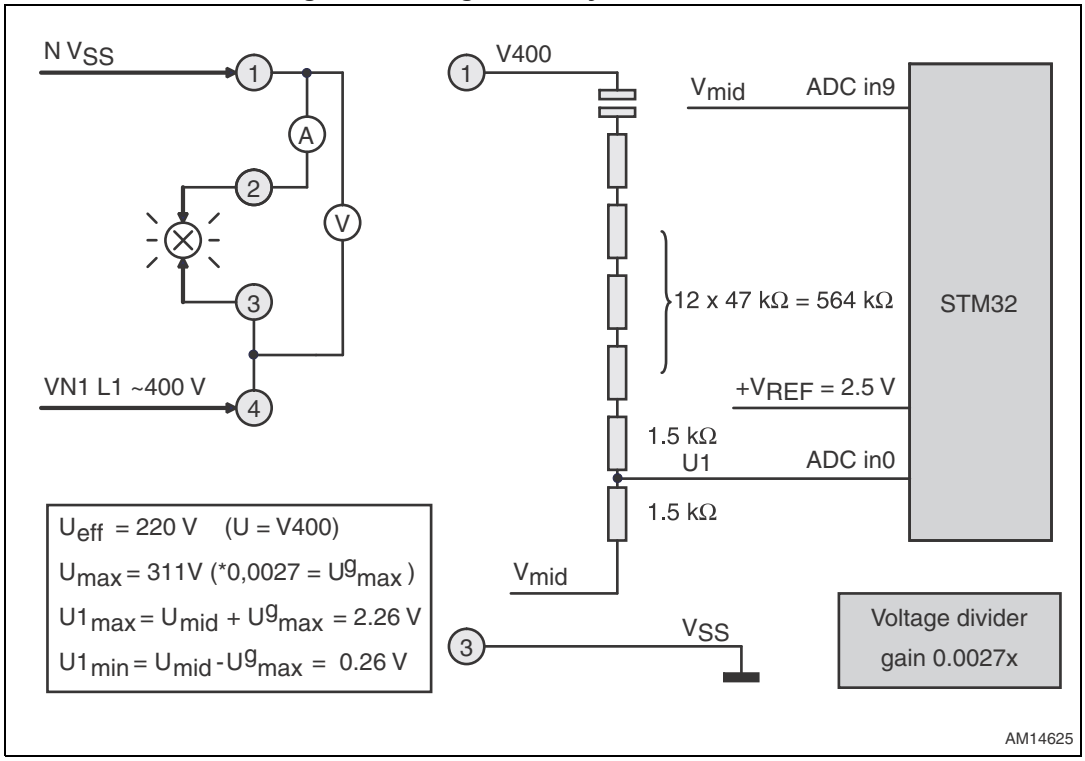


Figure 5 shows the algorithm flow measurement.

- A fast measurement of the current and voltage with injected noise from surrounding environment triggered by network synchronized timer
- Decimation of measured samples
- RMS values computation
- Use of a precise RTC clock source for energy computation.

Figure 6 shows the connectors of the power meter (circles with the numbers 1, 2, 3, and 4) and its connection to the network and load on the left side and voltage and current measurement circuit on the right side. Voltage circuitry depicted in this image shows that the voltage divider consists of resistors and a capacitor and it is referenced to U_m (V_{mid}) voltage, which is half of $+V_{REF}$ (2.5 V). The voltage divider has a gain of 0.0027. U_m (V_{mid}) voltage is also measured by the system.

Figure 6. Voltage circuitry of STM32 meter

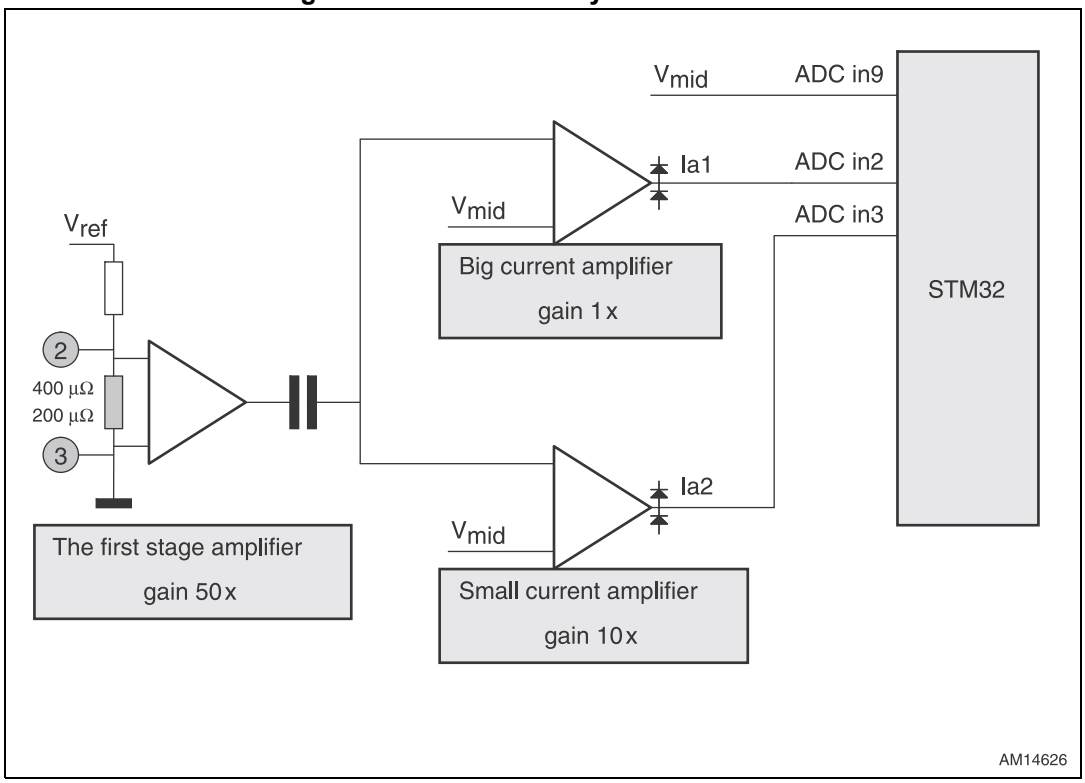


A current circuit is depicted in *Figure 7*. The circuit consists of two stages:

- The first stage which amplifies 50 times the voltage across the shunt connected to the current terminals (circles with numbers 2 and 3)
- The second stage which amplifies the signal coming from the first stage.

The second stage has two paths with different gain: 1 and 10. Both the second stage outputs (for gain of 1 and for gain of 10) are connected to the STM32 ADC (ADC in2 and ADC in3).

Figure 7. Current circuitry of STM32 meter



The introduction of two parallel paths within the second stage with the different gain allows the user to measure with higher resolution at the low current part of the measured current range. Even with the two range measurements, an ADC enhancement must be employed in order to cover both ranges with desired precision. *Section 1.9* describes, in detail, a technique for ADC enhancement.

1.9 ADC enhancement by oversampling technique

In order to reach the required precision and resolution of the system, it is necessary to maintain the number of effective bits (NOEB) higher than that offered by the embedded ADC. After the improvement of the linearity and INL reduction in *Section 1.5*, it is possible to increase the number of effective bits from 10 bits (see *Section 1.6: Thermal noise present on STM32 meter platform*) up to the 14 bits necessary to reach the required precision of the whole system. The theory and implementation of the resolution enhancement by oversampling is described in a separate document supplied on request.

1.10 Output values

This section and its subsections theoretically compute output values as U_{RMS}, I_{RMS}, P (instant power), E (energy) and pulse output. These values must be calibrated later on by a gain and an offset constant in order to compensate an imprecision in the analog circuitry.

Some reference values and constants are defined

ADC reference circuit TL431 gives a voltage of 2.5 V

U_{ADCref} = 2.5 V

DC offset value U_{mid} is delivered from U_{ADCref}: using voltage divider R116, R117, and R120

$U_{mid} = U_{ADCref}$ x R116||R117 / (R116||R117 + R120) = 2.5 x 0.498 = 1.245 V

One LSB of the 12-bit ADC is equal to:

$LSB_{12\text{-}bit}$ = 2.5 V / 4096 = 0.00061 V [V / LSB]

Conversion constant from I to U for R_{SHUNT} = 400 µΩ is:

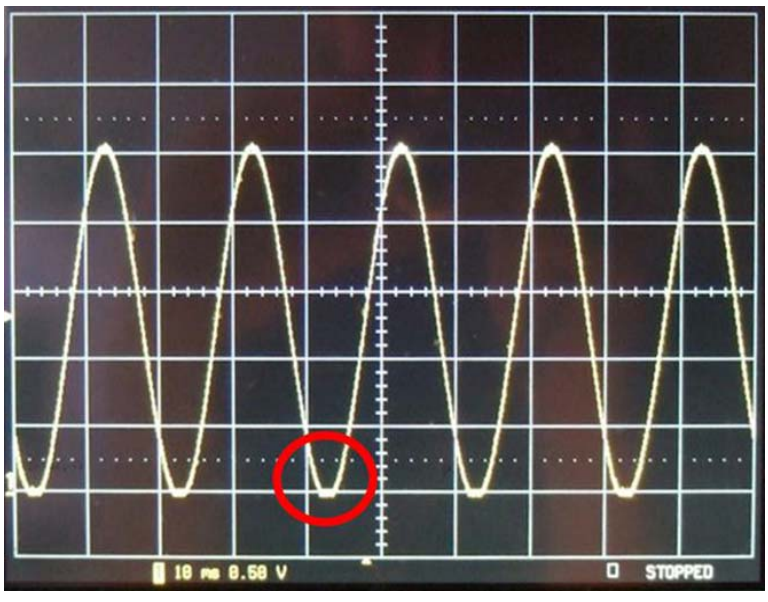
$SHUNT_{400}$ = 2500 [1/Ω] (1 / U_{out}/I_{IN} = R x I/I = R_{SHUNT}T = 0.0004)

Conversion constant from I to U for R_{SHUNT} = 200 µΩ is:

$SHUNT_{200}$ = 5000 [1/Ω] (1 / U_{out}/I_{IN} = R x I/I = R_{SHUNT} = 0.0002)

Figure 8 shows experimental measurements of the maximum output signal from an operational amplifier used in the current analog circuitry. It can be seen that the signal with peak value (amplitude of the sinus signal with DC value in the middle) higher than 1.245 V is clamped due to the limitation given by U_{mid}, U_{ADCref}.

Figure 8. Current circuitry of STM32 meter, op amp saturation marked by red circle



1.10.1 RMS voltage

The voltage analog circuitry is described in detail in this section. Main phase voltage is reduced by a voltage divider directly connected to the phase voltage. The voltage divider consists of a parallel and serial connection of these components:

$L_1 + R_1 + C_1||C_2 + 12 \times R_2$ and R_{14}

The output voltage from the voltage divider is given by the VOLTDIVIDER that is computed from:

Equation 7

$$R_{all} = R_1 + 12 \times R_2 + R_{14} = 100\ R + 12 \times 47\ k\Omega + 1.5\ k\Omega = 565.6\ k\Omega$$

Equation 8

Voltage division is: VOLTDIVIDER = $\frac{R_{14}}{R_{all}} = \frac{1{,}5k\Omega}{565{,}6k\Omega} = 0{,}002652$ [-]

VOLTDIVIDER constant means that the input voltage is divided by number 377.

Voltage represented in volts is computed by:

Equation 9

U_{LSB} in LSB - actual output of ADC channel

U_V in volts - output from METER

$U_V = C_U \times U_{LSB}$

The calibration constant for the voltage circuitry consists of:

Equation 10

C_U = VOLTDIVIDER x $LSB_{12\text{-}BIT}$ x V_IMPRECISION

where $LSB_{12\text{-}BIT}$ is defined in *Section 1.1: STM32 ADC parameters*, *V_IMPRECISION* is the imprecision and tolerance of the components used in analog circuitry, mainly resistors and soldering.

Since we want the smallest value to be 1 µV, we must multiply everything by 1.000.000 additionally. This also helps to maintain the preservation of the precision.

In order to save the microcontroller computational power and to keep precision as high as possible, it is beneficial to avoid division operation during all the computations during a period and do it as the last step after every period computation.

According to *Section 1.9: ADC enhancement by oversampling technique*, during oversampling, the sum of 18 samples from ADC results as the V_{SUM} value representing measured voltage with higher precision.

Computation of the voltage RMS value takes 44 V_{SUM} values. They may only be squared, then summed, and finally they can be divided by common decimation and RMS constant.

A standard computation of the decimation and RMS value computation

Equation 11

$V(i) = 1/18 \times SUM [U(i)]$

$U_{RMS} = \sqrt{} 1/44 \text{ sqrt } [V(i)]^2$

Computation with delayed division saving the computational power and the precision

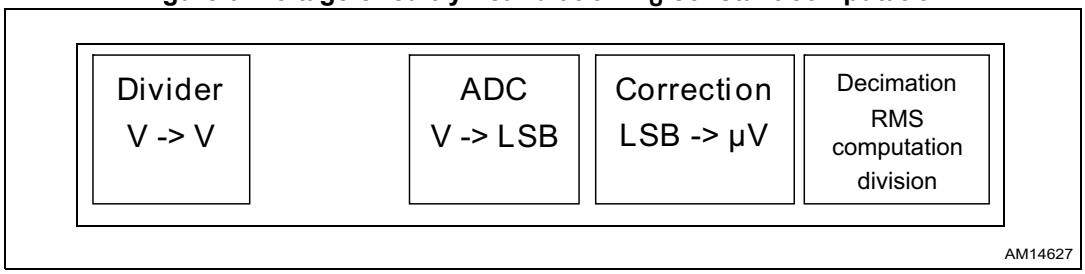
Equation 12

$V_{SUM} = SUM [U(i)]$

$U_{RMS} = 1/\div 44 \times 1/\div 18 \times \text{sqrt } (SUM \{SUM [U(i)] (y)\}^2)$

The final value must be divided by 28.1424 (or 28142 if the values are in millivolts) or multiplied by 0.035533 (or 0.000035533 if the values are in millivolts).

Figure 9. Voltage circuitry - calibration C_U constant computation



1.10.2 RMS current - high gained

Current analog circuitry is described in detail in this section. Main phase current is measured as a voltage on small resistance - shunt. The shunt (R142) converting current to the voltage to be measured has a value of:

1. 200 µΩ
2. 400 µΩ

The voltage from the shunt is amplified by the first stage of the current amplification with a gain of 50. For current that needs further gain, an additional gain of 10 is added.
If a path with the additional multiplication 10 is used, all the variables have index HG (high gain). The complete gain is 50 x 10 = 500 times. The value obtained after the amplification must be multiplied by $OPAMPGAIN_{HG}$ in order to get the original value.

Equation 13

$OPAMPGAIN_{HG} = 0.002$

$I_A^{HG} = C_I^{HG} \times I_{LSB}^{HG}$

where I_{LSB} is the value in LSB from ADC and I_A is the current in amperes.

$C_I^{HG} = SHUNT_{400} \times OPAMPGAIN_{HG} \times LSB_{12\text{-}BIT} \times HG\_IMPRECISION [A / LSB]$

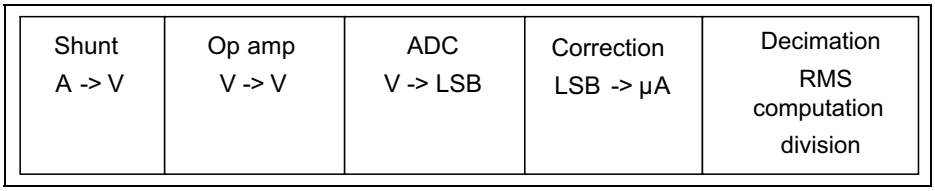
Where $SHUNT_{400}$ and $LSB_{12\text{-}BIT}$ were defined in *Section 1.1: STM32 ADC parameters*. *HG_IMPRECISION* is the imprecision and tolerance of the components used in the HG path of analog circuitry; mainly resistors and soldering.

Since we want the smallest value to be 1 µA, we must multiply everything by 1.000.000 additionally.

No decimation, shifts or division are performed during computation in order to preserve precision and reduce microcontroller computation. The correct multiplication or division is done at the end of the whole computational chain.

The final value must be divided by 28.1424 (or 28142 if the values are in milliamperes) or multiplied by 0.035533 (or 0.000035533 if the values are in milliamperes).

Figure 10. Current circuitry - calibration C_I constant computation



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1.10.3 RMS current - low gained

The basic gain of the current input is 50. There is an additional gain of 1. If the path with the additional multiplication 1 is used, all the variables have index LG (low gain). The complete gain is:

Equation 14

$OPAMPGAIN_{LG} = 0.02$

$I_A^{LG} = C_I^{LG} \times I_{LSB}^{LG}$ [A] = [A/LSB] x [LSB]

where I_{LSB} is the value in LSB from ADC and I_A is the current in amperes.

Equation 15

$C_I^{LG} = SHUNT_{400} \times OPAMPGAIN_{LG} \times LSB_{12\text{-}BIT} \times LG\_IMPRECISION$

where $SHUNT_{400}$ and $LSB_{12\text{-}BIT}$ were defined in *Section 1.1: STM32 ADC parameters*. *LG_IMPRECISION* is the imprecision and tolerance of the components used in the LG path of analog circuitry; mainly resistors and soldering.

The final computation is described in *Section 1.10.4: Power*, *Section 1.10.5: Energy*, and *Section 1.10.6: Pulse output*.

1.10.4 Power

Instant power is computed by:

Equation 16

$p = i(t) \times u(t)$

$P_W = (C_I \times C_U) \times I_{IN} \times U_{IN}$

$P_W = C_P \times I_{IN} \times U_{IN}$

Even the C_P is theoretically equal to (C_I x C_U); C_P is set during the calibration process as a constant between a supplied instant power P_{Theor} and the instant power P_W measured by the STM32 power meter.

Equation 17

$$P_{Theor} = C_P \times P_W$$

The difference between C_P given by the calibration process and (C_I x C_U) is given by the phase shift that, even when carefully compensated, does still not have a negligible influence on the computation of the power.

The instant power over one period of mains P_W can be computed also from the energy E taken over one period of mains equal to 20 ms:

Equation 18

$$\Delta E = \Sigma u(t) \times i(t) \times \Delta t_s = \Delta t_s \times \Sigma u(t) \times i(t) = \frac{\Delta t}{44} \times (\Sigma u(t) \times i(t))$$

Equation 19

$$P_W = \frac{\Delta E}{\Delta t} = \frac{1}{\Delta t} \times \frac{\Delta t}{44} \times \Sigma u(t) \times i(t) = \frac{1}{44} \times \Sigma u(t) \times i(t)$$

where t_S is the sampling period for $u\ (t)$ and $i\ (t)$. t is the period of mains equal to 20 ms. In order to reach the desired precision in the pulse generation, P_W and all the energy values are computed in µW.

1.10.5 Energy

Energy is calculated as a product of current I_{IN}, voltage U_{IN}, time T_{timer} and power calibration constant C_P (T_{timer} - time in seconds).

Equation 20

$$E_{Wh} = C_P \times I_{IN} \times U_{IN} \times T_{timer}$$

In order to save the microcontroller computational power, the previously computed instant power P_W can be used to get energy.

Equation 21

$$E_{Wh} = P_W \times T_{timer}$$

Equation 22

$$\Delta E_{fragment} = \frac{1}{44} \times \Sigma u(t) \times i(t) \times \Delta t_s = \frac{1}{44} \times \Delta t_s \times \Sigma u(t) \times i(t) = \frac{1}{44} \times \frac{\Delta t}{44} \times \Sigma u(t) \times i(t) =$$

$$= \frac{1}{44} \times \frac{\Delta t}{44} \times \Sigma u(t) \times i(t)$$

Equation 23

$$\Delta E_{fragment} = \frac{1}{44} \times \Delta t \times P$$

To keep energy resolution up to 1 mW, we need power to be specified by 25 bits or more. In order to reach desired precision in the pulse generation, $E_{fragment}$ and all the energy values are computed in µWs.

1.10.6 Pulse output

In order to reduce jitter when generating the pulse output signal, the following algorithm is used:

- The energy is computed once per period of mains (i.e. every 0.02 s) E_{Wh}
- The energy computed is divided by 44. $E_{fragmentWh} = E_{Wh} / 44$
- This fragment is added to the accumulator every time the ADC is triggered (44 times per one period of mains) that is equal to 2.2 kHz
- Whenever the accumulator surpasses a certain level, E_{THR}, impulse threshold, the pulse LED is toggled and the E_{THR} is distracted from the accumulator
- In order to reach desired precision in the pulse generation, E_{THR} and all the energy values are computed in µWs.

The pulse constant (the number of pulses generated per consumed kWh) is set by the manufacturer.

Example 4

Impulse constant *K* is set by the manufacturer to:

K = 3200 impulses / kWh

Relation between joules and watts per second is the following:

W x s = J

W x h = 3600 J

kW x h = 3.600.000 J

1 kW x h = 3.600.000.000 µW x s

In order to be able to set correctly E_{THR}, it is necessary to know that 1 impulse means:

3200 impl. .....1 kWh

1 impl. .....X kWh

3200 impulses = 1 kWh = 3.600.000 J

The energy of one impulse E_{IMPL} is:

x = E_{IMPL} = 1 kWh / K [imp / impl/kWh] = 3.600.000.000 / K [µWs]

E_{IMPL} = 1125 J = 1125 Ws

E_{IMPL}= **1.125.000.000 µWs**

Because the LED is toggled by reaching the E_{THR} value (impulse-threshold), the generation of one complete pulse (rising and falling edge) requires two events (two times reaching E_{THR} within E_{IMPL} step). It is necessary to divide the threshold constant for 1impl E_{IMPL} by two:

E_{THR} = **E_{IMPL}/ 2 = 1.125.000.000 / 2 = 562.500.000 µWs**

2 Computational issues and compensation algorithms

This section deals with issues that can influence measurements and computation and were not mentioned in *Section 1.4: Error sources on the STM32 meter*. The topics covered in this section deal with coherent sampling, precise frequency measurement, proper zero crossing detection and phase shift correction. The correct approach used when dealing with this topic leads to the precision improvement and makes it possible to keep precision in the required range.

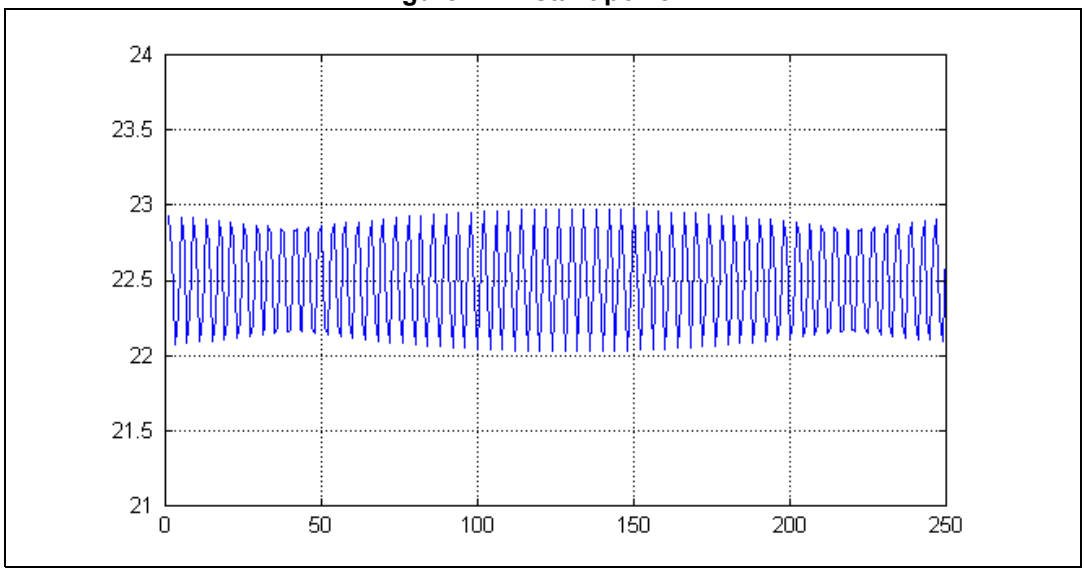
Coherent sampling is the sampling of the periodical signal where the number of the samples per period of the signal is still the same. The sampling time of the first sample is still in the same time position in relation to the phase of the sampled signal. The timing of the following samples is still the same and constant. In this case, 44 samples per period of the mains (50 Hz, period 20 ms) are always kept.

Non-coherent sampling is, on the contrary, the sampling of the periodical signal where the number of the sample per period of the signal is not the integer number. The sampling does not need to start in the same position in relation to the phase of the sampled signal. The timing of the subsequent samples can vary. For example, 44.76 samples per period of mains are acquired. It means that the sample rate is a bit higher than required in the case of coherent sampling.

2.1 Non-coherent sampling issues

If non-coherent sampling is present (it means no integer number of samples per period of mains is taken), it is possible to observe an additional disrupting signal in the graph of computed instant power from such sampled current and voltage. The additional disrupting signal consists of two frequencies: a high frequency F_H and a low frequency F_L.

Figure 11. Instant power(1)

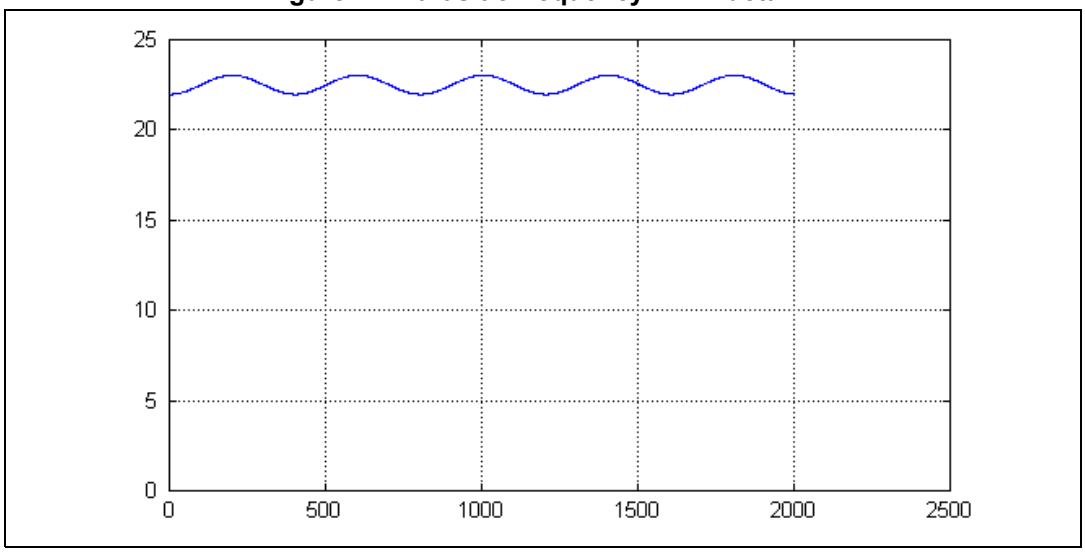


1. Y-axis: voltage, X-axis: cycles of mains/100 (50 Hz).

When using the non-coherent sampling, the measured period of the signal is not completely covered and every period and this coverage differs from period to period. The amount of the

power computed from these samples is not the same for every period of mains. This causes the parasitic signal with the frequency F_H. After some time (Tx) the coverage of the period is the same as it was at the beginning (in relation to the phase of the measured signal). This time Tx is the period of the frequency F_H.

Figure 12. Parasitic frequency FH in detail(1)



1. Y-axis: voltage, X-axis: cycles of 50 Hz.

In this example, the sampling of 44 samples per period is synchronized with a frequency of 49.93785 Hz. During every period of the mains, the last sample is displaced by time T_{diff_sample}.

Equation 24

$$T_{diff\_sample} = 1/50Hz - 1/49.93785Hz = 0.00002489\ s$$

In every cycle of the mains, all the samples are shifted by T_{diff_sample}. They again pass their initial position in the time T_{shift}.

Equation 25

$$T_{shift} = (1/\ 50\ Hz) / T_{diff\_sample} = 803.5\ cycles\ (of\ 50\ Hz)$$

Since the computed instant active power is a function with double the frequency of the input voltage and current (negative instant voltage and negative instant current again give instant positive power), the T_{shift} should be divided by two:

Equation 26

$$1/F_H = (803.5 / 2) * 0.020\ s = 8.035\ s$$

That the specific sample again passes its initial position does not mean that it is exactly in the same position. This happens after even more cycles of mains. This causes the fluctuation of the instant power by additional disruption of signal with F_L. The period of F_L is, in this example, 17,500 cycles of mains that is equal to 350 s (obtained by a simulation).

The jitter in instant power brings jitter to the accumulated energy value that brings the jitter to the LED pulse output generation.

In order to obtain correct instant power, during every period of the mains, or over a short period of time, it is necessary to provide coherent sampling.

2.2 Timer evaluation for coherent sampling triggering

In order to introduce coherent sampling into the system, it must be evaluated, if the timer and its resolution is precise enough to ensure precise outputs (instant power, RMS voltage and current). This section evaluates the quality of the synchronization with the network which is possible with the given system. It evaluates errors in respect to the distance from ideal synchronization to the network.

Sampling frequency for 44 samples per 20 ms (per one cycle of mains 50 Hz) results in the ADC sample time of 454.5 μs.

The STM32 timer used for synchronization with the network and for triggering of the ADC sampling is a 16-bit timer. This timer has a time stamp generation resolution: 27.777 ns when the STM32 is running on 36 MHz.

Precision of sampling frequency generation

One cycle of 50 Hz can be divided exactly into 720.000 steps when using the given timer.

The timer generates 16363 time stamp events within two subsequent sampling triggers out of 44.

The error of the trigger generation for one sample position is:

Equation 27

$$1 / 16363 = 0.000061 = 0.0061\% \sim 0.01\%$$

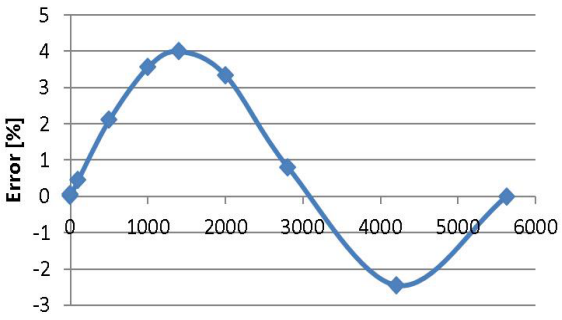
Experimental results in *Figure 13* show the influence of the sampling instant generation correctness on the instant power error.

Table 4. Precision vs. timer setting. Simulated on signal u (t) = sin (2 x pi x 50 x t)

Distance from ideal sampling (timer steps)	Sample time error (%)	URMS (V)	Error U_{RMS} (%)	P at 1 Ω (W)	Error P (%)
1	0.0089	0.707075	0.004	0.499956	0.009
10	0.0889	0.706794	0.044	0.499557	0.089
100	0.8889	0.703984	0.443	0.467189	0.881
500	4.4444	0.692307	2.093	0.479290	4.142
1000	8.8888	0.681974	3.554	0.465089	6.982
1406	12.4965	0.678874	3.993	0.460870	7.826
2812	24.9956	0.701548	0.786	0.492170	1.566
4218	37.4895	0.724468	-2.455	0.524853	-4.971
5625(1)	50.0000	0.707107	0.000	0.500000	0.000

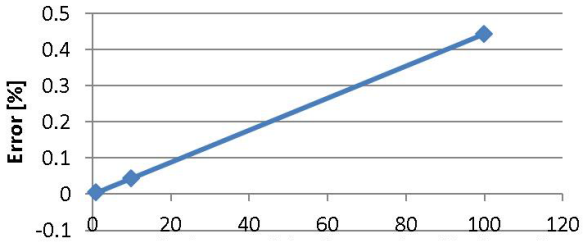
1. 5625 = 11250/2 is exactly half of the sampling period, so the error is zero. *Table 4* was computed for the same setting taking 64 samples per period instead of 44. For 44 samples per second, the errors indicated are even lower, see the text above *Table 4*.

Figure 13. Error of U_{RMS} vs. the timer error in timer ticks



Sample time precision (steps of 16-bit timer at the 36 MHz STM32 device)

Figure 14. Error of U_{RMS}(1)



Sample time precision (steps of 16-bit timer at the 36 MHz STM32 device)

1. Detail of *Figure 13* (zoom in x-axis).

Table 4 shows that the precision of the timer resolution is enough to make coherent sampling in order to reach the requirements for precision. There is no need for additional correction or approximation of the samples, unless the future requirements for the higher accuracy class of the meter appear. The system is always able to synchronize to the network frequency with the error of the three steps of the timer constants. This leads to the error of U_{RMS} three times 0.004% (according to *Table 4*) (that means an error U_{RMS} value of 0.012%). This is still ten times lower than other influences to the system that can affect overall precision.

2.3 Timer setting constraints for coherent sampling triggering

The automatic system that is implemented to synchronize sampling with the network (negative feedback introduced in *Section 2.4*) sets one parameter. This parameter is the reload constant of the timer for sampling triggering. Allowed values of this constant should be limited to an interval avoiding incorrect system behavior in case it is set to a very different value from the ideal one.

The limits of the timer reload constant are computed from variation of the STM32 microcontroller main system clock and from allowed variation of the network frequency prescribed by international standards.

Table 5. High speed internal (HSI) RC oscillator

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Unit
f_{HSI}	Frequency				8		MHz
ACC_{HSI}	Accuracy of the HSI oscillator	User-trimmed with the RCC_CR register				1	%
		Factory calibrated	T_A = –40 to 105 °C	–2		2.5	%
			T_A = –10 to 85 °C	–1.5		2.2	%
			T_A = 0 to 70 °C	–1.3		2	%
			T_A = 25 °C	–1.1		1.8	%

To set the correct limits, it is necessary to combine the maximum error of HSI and network frequency variation:

Max. HSI error = ± 3%

Max. 50 Hz variation = ± 2%

The max. deviation from correct frequency is ± 5%.

The mains signal is sampled 44 times per period of mains, this results in the sample frequency F_S:

Equation 28

F_S = 50 Hz x 44 samples = 2200 Hz

F_S equal to timer constant C_{Timer} that is derived from main system clock.

C_{Timer} = 36.000.000 Hz / 2200 Hz = 16363

The maximum and minimum values for the timer constant are:

$C_{Timer-MAX}$ = C_{Timer} x 105% = 17182

$C_{Timer-MIN}$ = C_{Timer} x 95% = 15545

The timer constant can be set from one border ($C_{Timer-MAX}$ or $C_{Timer-MIN}$) to the center value (C_{Timer}) after 818 steps when updating the constant by one every cycle of mains. That is 818 x 0,02 s = 16 seconds (correction is done every second period of the signal, so, in fact, the PLL takes 32 seconds to get from total border to center). This is too long, so it is necessary to implement faster iteration.

Section 2.4 shows a fast locking algorithm for synchronization with the mains.

2.4 Precise timer setting for coherent sampling

All the computation (RMS current, RMS voltage, instant power) and the conversion of the instant power into energy needs correct timing and the influence of the STM32 main clock must be taken in account.

The high speed internal RC oscillator (HSI) inaccuracy (over a long period) is not an issue, since the frequency is measured and updated every period of mains and the timer is set accordingly.

The meter should be able to measure and correct the mains frequency fluctuation of ± 2%; it means from 49 to 51 Hz according to the international standard. The HSI RC oscillator has a frequency fluctuation ± 3% (even the internal HSI can be calibrated by RTC to accuracy ± 1%) over the whole temperature range (the value ± 3% is used for computation as the worst case). If the combination of the maximum network frequency variation and maximum HSI frequency variation is ± 5%, it means from 47.5 to 52.5 Hz. The meter must be able to adapt to this variation and measure correctly in this range of values.

All the computation for precise timing is updated only when input voltage is higher than 50 V. A possible voltage drop over some periods can bring a frequency detection error. The international standards allow incorrect measurement during the period of the time when voltage is under 80% of its nominal value.

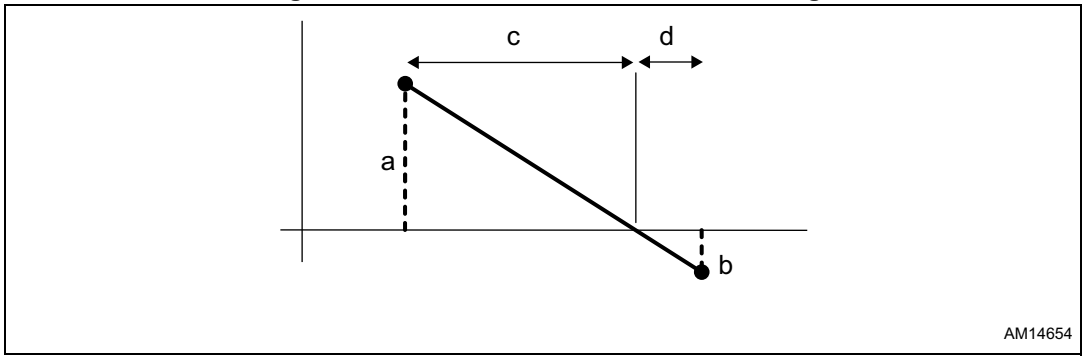
The algorithm for the precise timer setting uses the mains zero crossing information. In order to keep the whole number of the samples per period of the mains, the positive zero crossing of the mains must still appear in the same position in the sampled data array (for example: if we detect zero crossing at the 4^{th} sample out of 44, in the next period of mains the zero crossing must appear in the same position, it means the 4^{th} sample out of 44). The sample triggering timer constant must be updated to keep the zero crossing at the same sample index. The timer constant is updated only if the zero crossing is different from the previous one. If the difference is positive, the timer constant is updated by -1, if the difference is negative, the timer constant is updated by +1. This negative feedback locks the sampling frequency to the frequency of mains.

The sampling frequency difference represented by one sample (44 samples per period of 50 Hz) is 1.16 Hz (which is 2%). If the timer setting differs from mains by less than 2%, the difference in zero crossing position appears after many cycles of mains (the lower the difference, the more cycles there are). If we react only by adding or subtracting value 1 from the timer constant only when the difference is one whole sample, the frequency locking lasts for 225 steps (over the whole range - see the beginning of this section). More than 5 s is needed to stabilize the zero crossing sample index value to less than one between directly subsequent periods of mains. Furthermore, after that synchronization period, if the difference is lower than one whole sample index, the update of the timer is done after the difference appears over more periods and reaches one sample index. Typically, the lock-in time is about 30 seconds additionally.

Reduction of the necessary time for zero crossing stabilization (synchronizes the sampling with the mains frequency) can be done by introducing a sample index division in order to get finer and faster zero crossing stabilization. Using this technique, the lock-in algorithm needs 1-2 seconds to fully synchronize sampling with the network.

After detection of the zero crossing position *i*, the finer zero crossing is computed according to *Figure 15*, *Equation 29* and *Equation 30*.

Figure 15. Finer calculation of zero crossing



Equation 29

$$d_i = b_i / (\text{abs. } a_i + \text{abs. } b_i)$$

Equation 30

$$c + d = 1$$

where a_i is the amplitude of the signal prior to a zero crossing, and b_i is the amplitude of the signal after the zero crossing. The sub index position d_i computed is in the range from 0 to 1. The difference of the two subsequent zero crossings is $d_i - d_{i+1}$.

The value T_{update} that can be added or subtracted from the trigger timer reload constant must be an integer number bigger that one. The difference can be divided into 20 steps by the rounding of $T_{update} = [20 \times (d_i - d_{i+1})]$. This leads to a division of the position index of the zero crossing to 20 sub values.

The trigger timer reload constant is updated by this difference to stabilize the zero crossing in this finer position. This makes initial locking faster (by factor 20).

As described in *Section 2.6*, the signal used for zero crossing detection is filtered so that only fundamental frequency is preset. This avoids errors when computing the zero crossing position finer that one sample index.

2.5 Frequency measurement

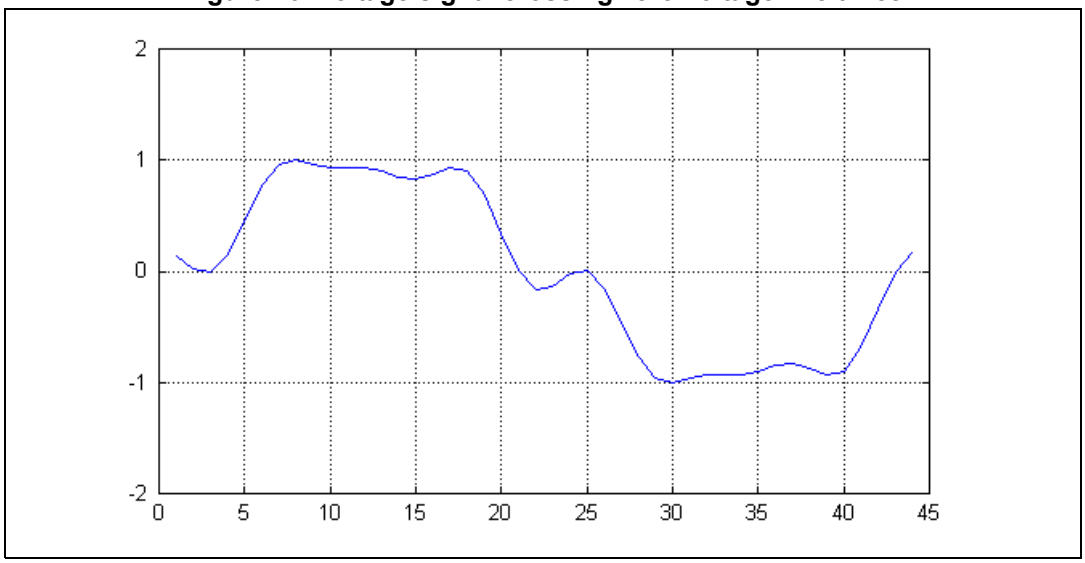
The frequency value is derived from the coherent sampling trigger period. The sampling trigger period is measured using a precise external low speed oscillator (LSE). From that value the frequency is computed.

In order to get a higher resolution of the measured frequency value, more values must be accumulated and averaged. The accumulation of ten values brings the resolution that is sufficient and can be displayed.

2.6 Filtering of input signal for proper zero crossing detection

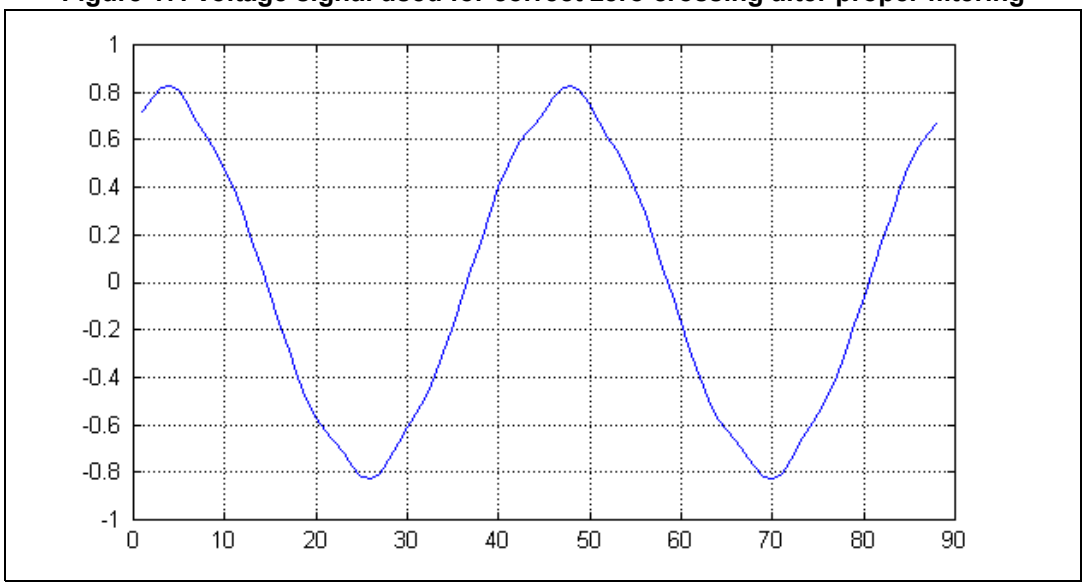
Proper detection of the zero crossing is the key parameter in order to measure and compute all the values correctly. Possible problems are caused when the voltage channel contains more harmonics and such a signal with these harmonics crosses the zero voltage line more times. *Figure 16* shows the voltage signal that is crossing the zero line twice. The same situation can be caused not only by higher harmonics but also by noise present in all the circuitry.

Figure 16. Voltage signal crossing zero voltage line twice



In order to avoid an incorrect zero crossing detection, a filter was introduced. The filter is the simple moving average. The length of the filter is 18. Since the number of the samples per period of mains is 44, the filter removes all the harmonics starting at 50 Hz with growing attenuation. *Figure 17* shows the signal after the filtering that allows for failure-less zero crossing detection.

Figure 17. Voltage signal used for correct zero crossing after proper filtering



Since the voltage signal with very low amplitude can lead to incorrect zero crossing detection, the zero crossing detection is not performed on the voltage signal with an amplitude lower that 50 V. The measured frequency and locking to the zero crossing is not updated in this case.

2.7 Phase shift correction

This section describes how to deal with phase shift in the analog circuitry of the STM32 power meter. The evaluation of the error caused by phase shift and the levels of its correction is computed in *Section 2.7.1*, *Section 2.7.2*, and *Section 2.7.3*.

2.7.1 Phase shift measured for the STM32 meter

The phase shift that needs to be compensated was measured directly in the STM32 meter. These values help to set the limits and resolution of the phase shift compensation method.

Figure 18. Zero crossing for green - U, blue - ILG, red- IHG

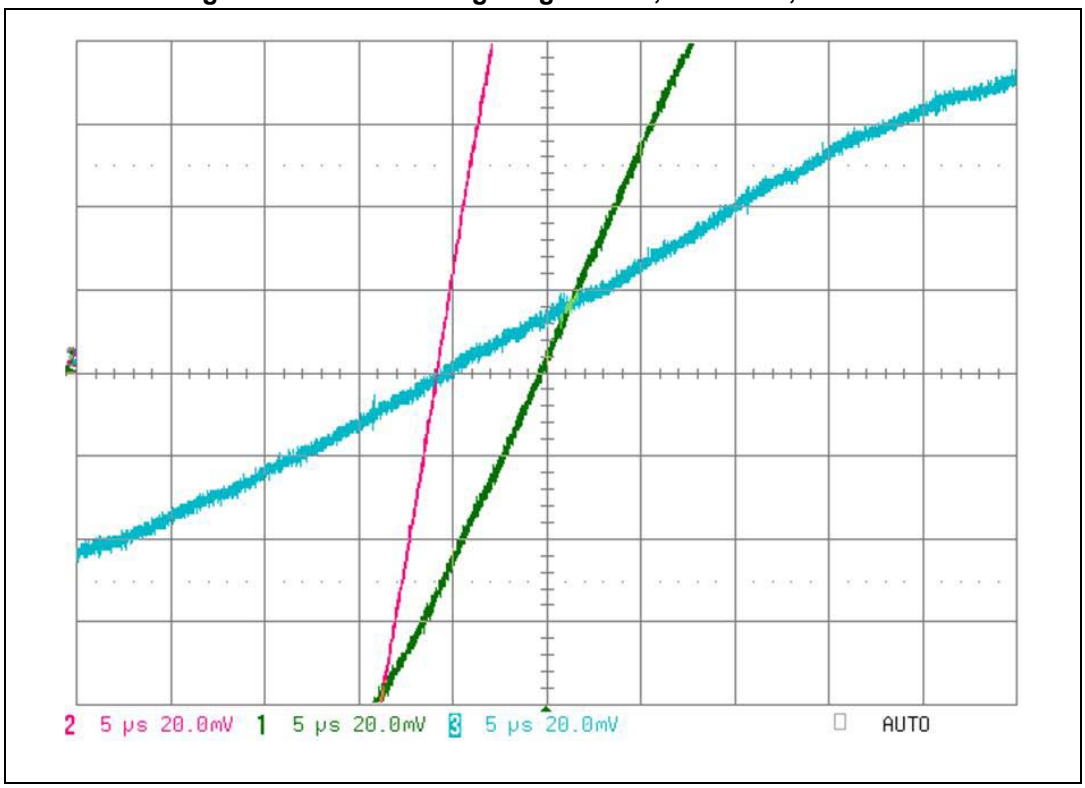


Figure 18 shows that there is a delay between voltage *U* and currents I_{LG} and I_{HG}. This delay between U and I_{LG} or between *U* and I_{HG} is in the same range for both ranges and it is 5 - 8 µs. This delay is mainly caused by the capacitance and inductance in the signal path of the input voltage divider (see *Section 2.10*).

2.7.2 Phase shift correction - error evaluation

The phase shift between voltage and current is also caused by non-simultaneous sampling of these values, see *Section 1.9*.

The voltage and I_L are shifted by two samples:

Equation 31

$T_{shift\_I\_L}$ ~ 2 samples ~3 µs ~ 0.05 deg.

The voltage and I_H are shifted by four samples:

Equation 32

$T_{shift\_I\_H}$ ~ 4 samples ~ 6 µs ~ 0.1 deg.

Table 6 shows what level of the phase shift correction is necessary to be reached in order to lower the error caused by the phase shift to an acceptable value. It can be seen that we need to correct the phase shift to a value lower than 0.1 deg. This value can be easily reached by the phase shift compensation filter introduced in *Section 2.7.3*, compensating with the step of 0.013 deg. The value 0.013 deg. allows negligible error of the instant power caused by the phase shift to be reached.

Table 6. Error of instant power caused by phase shift

Sampling time trigger shifted by [deg.]	Error of instant power [%] for PF = 1	Error of instant power [%] for PF = 0.5
0.01	0.000002	0.030232
0.02	0.000006	0.060466
0.05	0.000038	0.151200
0.1	0.000152	0.302500
0.2	0.000609	0.605200
0.5	0.003808	1.515300
1	0.015230	3.038100
2	0.060917	6.105700
5	0.380500	15.476300

Data from *Table 6* are depicted in *Figure 19*, *Figure 20*, and *Figure 21*.

Figure 19. Error of instant power for PF = 1 and PF = 0.5

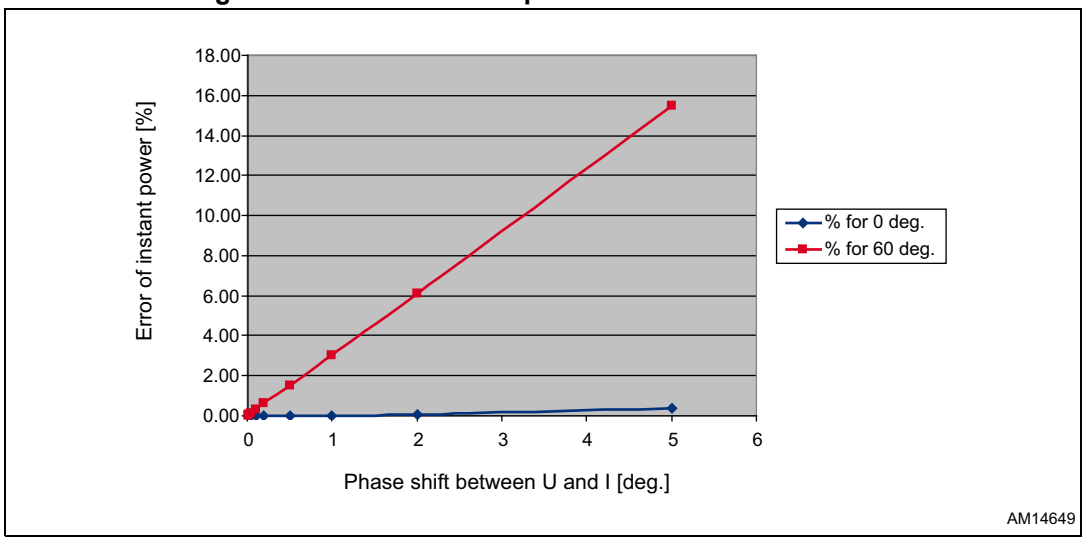


Figure 20. Error of instant power caused by phase shift for PF = 1

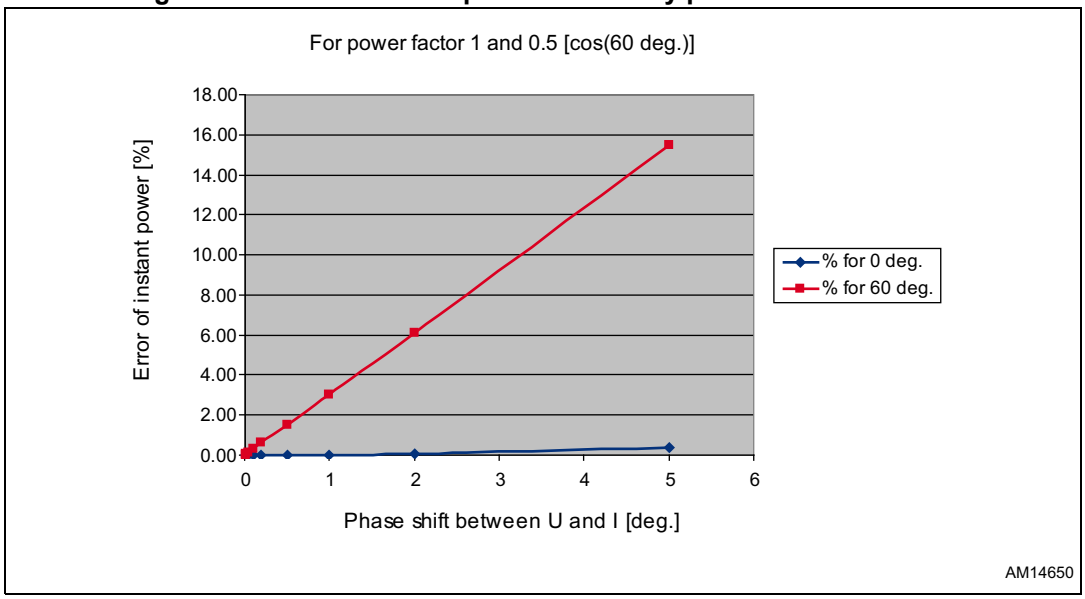
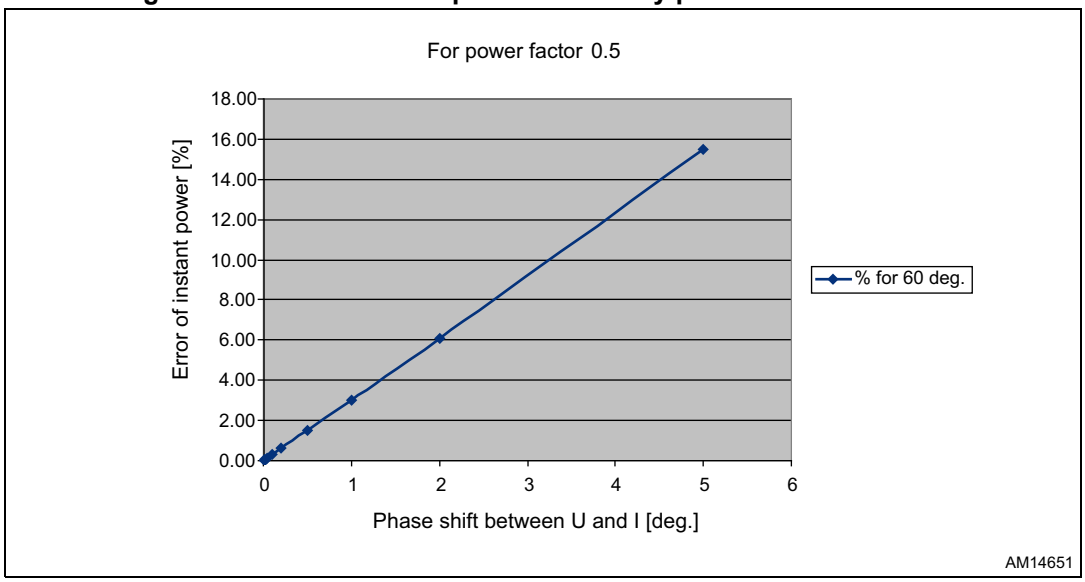


Figure 21. Error of instant power caused by phase shift for PF = 0.5



2.7.3 Phase shift correction - filter implementation

The phase shift in the time domain is not as simple as in the frequency domain or in a system where more ADC are employed for current and voltage measurements. In this HW implementation we need to use an approach that allows us effectively interpolate values of the voltage so that they are correctly aligned to current. This approach is described in a separate document supplied on request.

The phase compensation range that may be reached with this approach is:

With the step of 0.73 µs (0.013 deg.)

Maximum positive shift = -6.2 µs (0.11 deg.)

Maximum negative shift = +6.2 µs (0.11 deg.)

With the step of 0.77 µs (0.014 deg.)

Maximum positive shift = -12.4 µs (0.22 deg.)

Maximum negative shift = +12.4 µs(0.22 deg.)

When a higher value of the phase shift needs to be compensated, an extension to the method used is introduced.

2.8 Calibration procedure

Calibration (computation of the correction factor between measured and expected output) is a very important process and its correct performance results in the overall desired precision.

Even when the power meter measures the current and voltage with the maximum error 0.5%, we need to perform calibration on an even higher level of accuracy. If this is not done, calibrate the meter with the error of 0.5%, in the worst case (over the whole measured range) the maximum error may be an additional 0.5%, which results in an error of 1% (0.5 + 0.5) in total. This means that the measured value should be used for calibration after its error is the lowest possible. This happens after averaging the value over a longer period

of time. Calibration is performed, in this case, after the collection of data (RMS voltage, RMS current, instant active and reactive power) over 64 periods of mains (a bit more than one second or 50 Hz). If the error during the calibration process reduces to 0.1%, in the worst case there is an error of 0.6%, (0.1 + 0.5) in total over all the tests.

The calibration procedure consists of these steps:

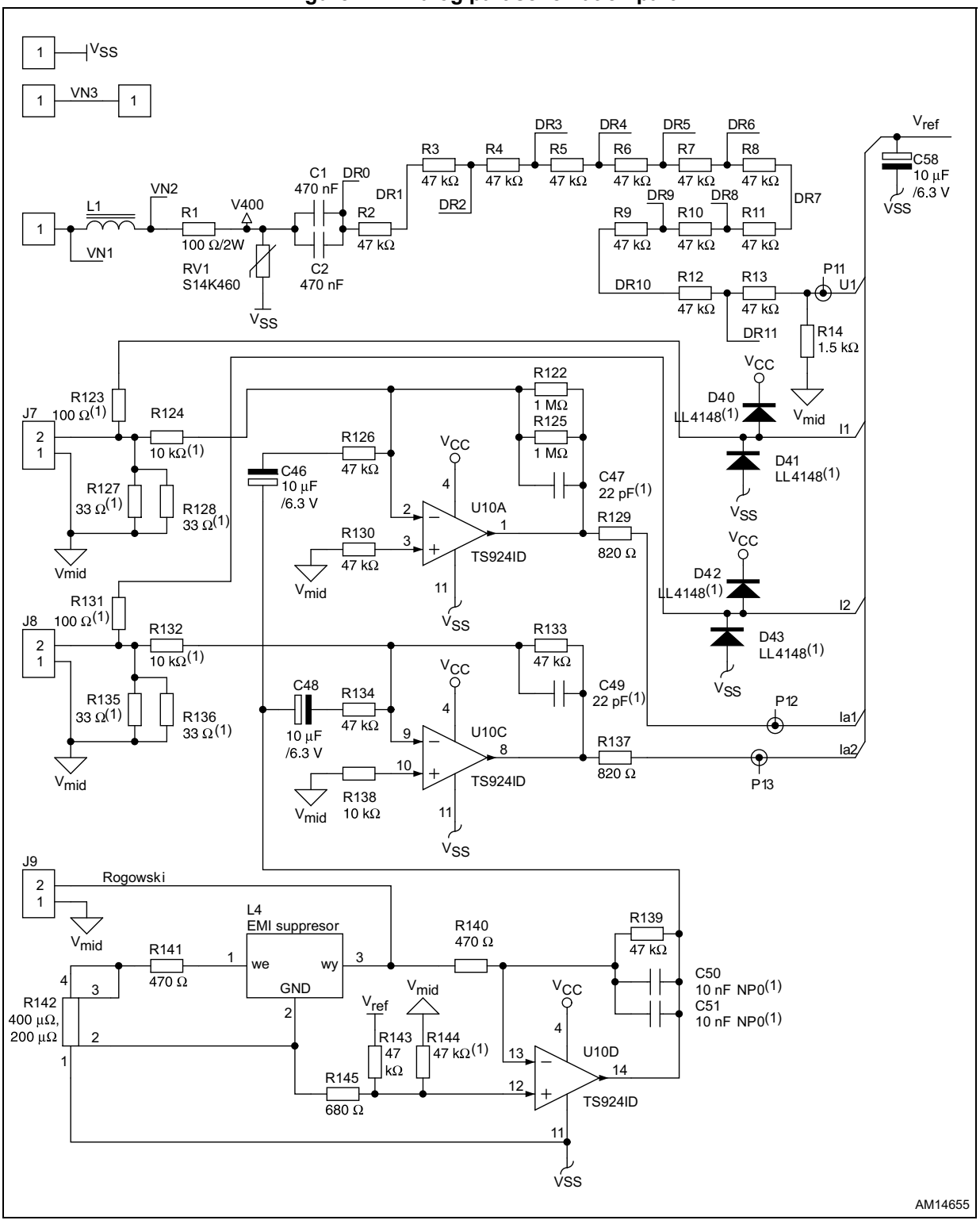
1. Connecting the STM32 meter to precise power supply.
2. Setting nominal current for lower range (5 A) current and nominal voltage (230 V).
3. After the power supply stabilizes (refer to the voltage and current source specifications), wait for an additional two seconds at least (in order to collect enough calibration data).
4. Pressing the button (number 4) on the meter keyboard.
5. Setting nominal current for higher meter range (40 A) and nominal voltage (230 V).
6. After the power supply stabilizes (refer to the voltage and current source specification), wait for an additional two seconds at least (in order to collect enough calibration data).
7. Pressing the button (number 4) on the meter keyboard.
8. After this procedure, all the calibrations are written into EEPROM and loaded after every power-up of the power meter.

2.9 Reactive and apparent power computation

The reactive power can be computed simply by $Q = \sqrt{S^2 + P^2}$ or by using a filtering method. Since the first method has its limitations, the filtering approach is introduced. This approach is described in a separate document supplied on request.

2.10 Analog part schematic - part 1

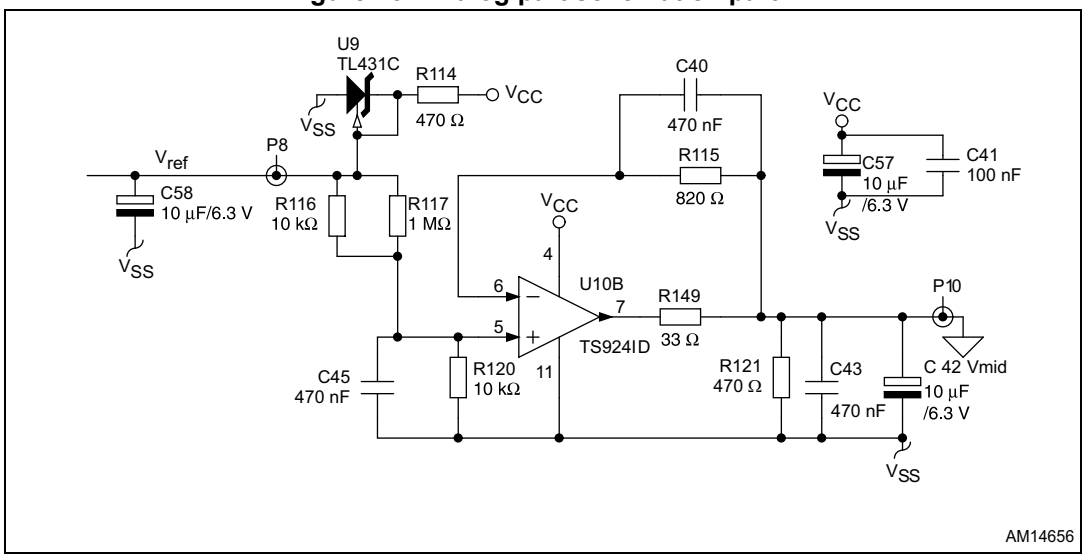
Figure 22. Analog part schematic - part 1



1. The component is optional and the user can fine tune its value according to their requirements.

2.11 Analog part schematic - part 2

Figure 23. Analog part schematic - part 2



3 References

Improving ADC Results Through Oversampling and Post-Processing of Data. (n.d.). Retrieved 2009, from Actel: www.actel.com/documents/Improve_ADC_WP.pdf.

AN2668 - application note.

4 Revision history

Table 7. Document revision history

Date	Revision	Changes
13-May-2013	1	Initial release.