

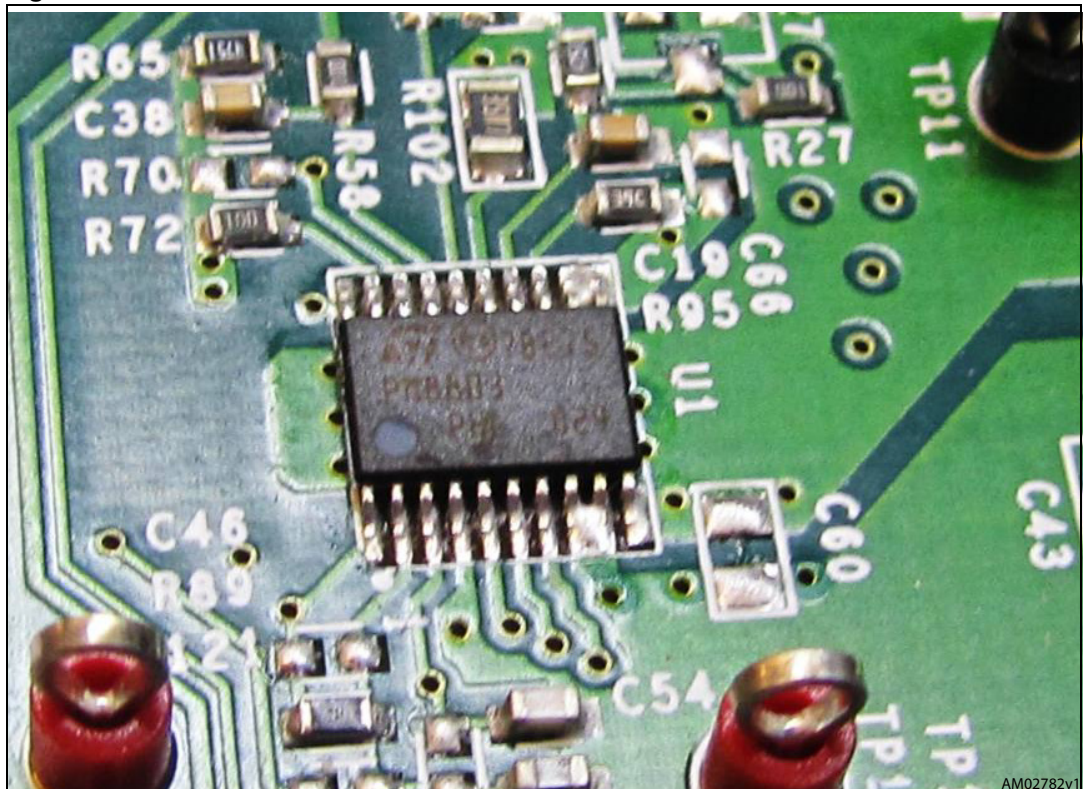
Introduction

This short document gives some practical indications for an optimal layout of a PoE converter based on the PM8803 PD + PWM controller; the focus is on the basic routing rules applicable for the device in this specific application. It is assumed that the user knows the power and EMI best practice guidelines for a DC-DC converter.

The EVALPM8803-FLY demonstration board layout is used as a practical example.

A suggested footprint for the HTSSOP20 package with exposed pad is also described.

Figure 1. Closed view of the PM8803 on EVALPM8803-FLY



1 PM8803 layout guideline

1.1 General guidelines for the PoE converter

The following general guidelines are valid for all the typical converter topologies used for PoE/PoE+ converters.

The length of the interconnections between the following groups of components belonging to the primary side of the converter must be kept as short as possible:

1. Input ceramic capacitors
2. Input side of the power transformer
3. Power MOSFET and sense resistors
4. Active clamp circuitry or snubber circuitry (if present)

The length of the interconnections between the following groups of components belonging to the secondary side of the isolation must be kept as short as possible:

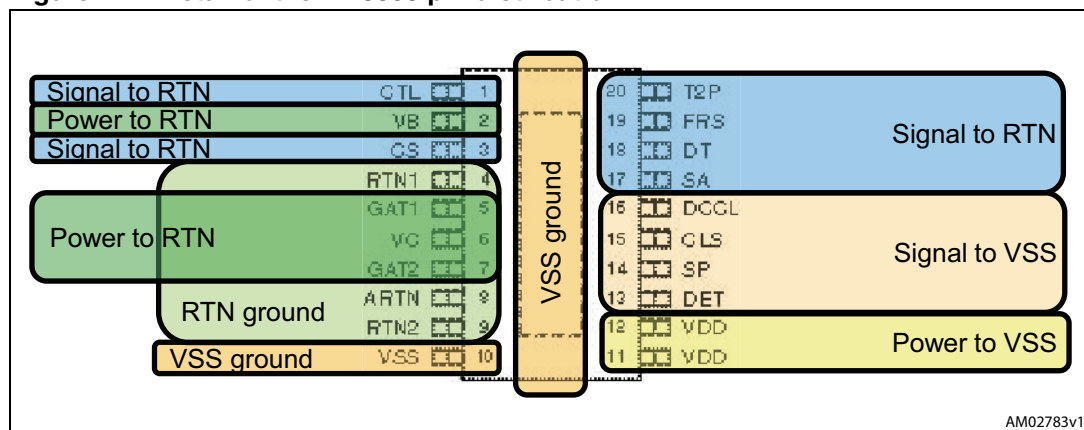
1. Secondary rectifier diode(s), or synchronous rectifier MOSFET(s) and associated driving circuitry
2. Output side of the power transformer
3. Output ceramic capacitors

Isolation/spacing, as required by applicable safety standards, must be assured between all the rails/traces/planes at 48 V and between the primary and secondary side of the converter.

1.2 Pin description of PM8803 device

Figure 2 gives an indication on how the PM8803 pins are distributed, while Table 1 provides a detailed description of each pin.

Figure 2. Detail of the PM8803 pin distribution



AM02783v1

Table 1. PM8803 pin descriptions

Pin#	Name	Type	Function
1	CTL	Signal to RTN	Input of the pulse width modulator. CTL pull-up to VB is provided by an external resistor which may be used to bias an optocoupler transistor.
2	VB	Power to RTN	5 V, up to 10 mA bias rail. This reference voltage can be used to bias an optocoupler transistor.
3	CS	Signal to RTN	Current sense input for current mode control and overcurrent protection. Current sensing is accomplished using a dedicated current sense comparator. If the CS pin voltage exceeds 0.5 V the GAT1 pin switches low for cycle-by-cycle current limiting. CS is internally held low for 60 ns after GAT1 switches high to blank leading edge current spikes.
4	RTN1	Ground RTN	Power ground for the GAT1 driver. This pin must be connected to RTN2 and ARTN.
5	GAT1	Power to RTN	Main gate driver output of the PWM controller. DC-DC converter gate driver output with 1 A peak sink-source current capability. (5 Ω typ. MOSFETs).
6	VC	Power to RTN	Output of the internal high voltage regulator. When the auxiliary transformer winding (if used) raises the voltage on this pin above the 8 V typ. regulation set point, the internal regulator shuts down, reducing the internal power dissipation. Filter this pin with a 1 μ F typ. connected to ground.
7	GAT2	Power to RTN	Secondary gate driver output. AUX gate driver output for active clamp or synchronous rectification designs. 1 A peak sink-source current capability (5 Ω typ. MOSFETs).
8	ARTN	Ground RTN	Analog PWM supply ground. RTN for sensitive analog circuitry including the SMPS current limit amplifier.
9	RTN2	Ground RTN	Power ground for the secondary gate driver. This pin is also connected to the drain of the internal current limiting Power MOSFET which closes VSS to the return path of the DC-DC converter. This pin must be connected to RTN1 and ARTN.
10	VSS	Ground VSS	System low potential input. Diode "OR'd" to the RJ45 connector and PSE's -48 V supply, it is the more negative input potential.
11	VDD	Power to VSS	System high potential input. The diode "OR" of several lines entering the PD, it is the most positive input potential.
12	VDD	Power to VSS	System high potential input. The diode "OR" of several lines entering the PD, it is the most positive input potential.
13	DET	Signal to VSS	Detection resistor pin. Connect the signature resistance between the DET pin and VDD. Current flows through the resistor only during the detection phase. This pin is 100 V rated with negligible resistance with respect to the external 24.9 k Ω .

Table 1. PM8803 pin descriptions (continued)

Pin#	Name	Type	Function
14	SP	Signal to VSS	Front auxiliary startup pin. Pulling up this pin to the auxiliary source changes the internal UVLO settings and allows PD to be powered with voltage lower than nominal PoE voltages. Default inrush and DC current protection are active. Use a resistor voltage divider from the auxiliary voltage to VSS to connect this low voltage rating pin. Connect this pin to VSS if not used.
15	CLS	Signal to VSS	Classification resistor pin. Connect the classification programming resistor from this pin to VSS.
16	DCCL	Signal to VSS	DC current limit. A resistor between this pin and VSS sets the current limit for the interface section of PM8803. It can be set to exceed the IEEE802.3at current limit. Leave the pin open for standard IEEE 802.3at applications.
17	SA	Signal to RTN	Rear auxiliary startup pin. Pulling up this pin gives high priority to an auxiliary power source like an external wall adapter. Use a resistor voltage divider from the auxiliary voltage to ARTN to connect this low voltage rating pin. Connect this pin to ARTN if not used.
18	DT	Signal to RTN	Delay time set. A resistor connected from this pin to ARTN sets the delay time between GAT1 and GAT2. This pin cannot be left open.
19	FRS	Signal to RTN	Switching frequency set. An external resistor connected from FRS to ARTN sets the oscillator frequency.
20	T2P	Signal to RTN	Successful 2-event classification indicator. T2P open drain signal assertion happens when powered by a PSE performing a 2-events classification. The T2P is an active low signal.
	EP	Ground VSS	Exposed pad. Connect this to a PCB copper plane to improve heat dissipation; must be electrically connected to VSS.

1.3 How to layout the PM8803 different ground pins

There are 4 different ground pins on the PM8803: VSS, RTN1, RTN2, and ARTN, plus the exposed pad.

The exposed pad of the PM8803 must be connected to VSS: design a fill area with at least 6 vias to VSS plane. Try, where possible, to increase the number of VSS power planes connected, at least below the PM8803 position, to improve the heat dissipation of the PM8803.

RTN1 and RTN2 are power ground pins for GAT1 and GAT2 drivers respectively. These pins are not internally connected together and therefore must be externally connected with a wide, short connection at the same point of the board power ground, which, in the following is called GND.

Use a wide power copper plane for such connections; avoid to use traces as much as possible.

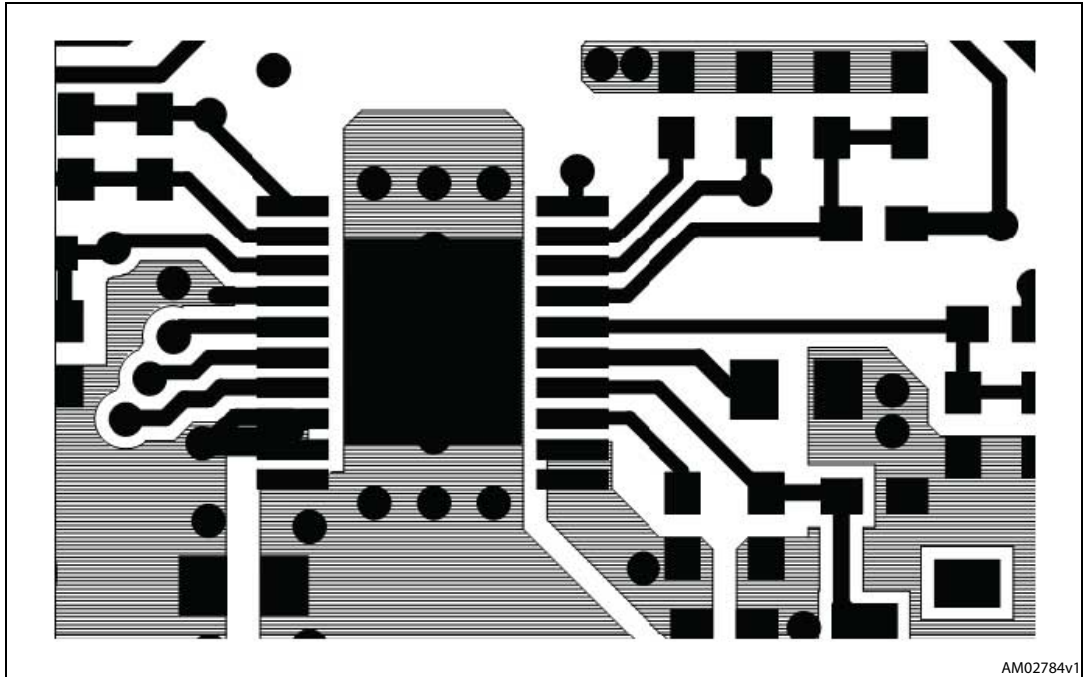
Board GND must be divided into power GND (to connect input caps, Rsense, PM8803 pin 4 and 9, SA auxiliary circuitry, isolation cap) and signal GND or ARTN (to connect the other components around the PM8803, the circuitry powered by VC voltage, and the IC pin 8). The signal GND must be connected to power GND in one point only, close to the PM8803 RTN pins 4 and 9.

Use large copper plane for the power GND, if possible foresee a layer completely dedicated to this.

ARTN can be a small copper plane or a wide trace connecting the several components referred to it.

On the secondary side keep separated the power path of the power secondary GND (output side of transformer, secondary rectifier, output capacitors) from the feedback network GND, which is connected only at the output capacitors side.

VSS is the low potential of PoE voltage; it can be routed with a wide trace, but close to the PM8803 as it must become a copper plane, in order to dissipate the heat transferred through the exposed pad of PM8803.

Figure 3. Detail of the device layout on the EVALPM8803-FLY demonstration board

1.4 Thermal aspects

Design the primary MOSFET area with at least 6-9 vias of connection to the internal copper area. Try, where possible, to increase the number of power planes connected, at least below the MOSFET position, to improve the heat dissipation.

Design the secondary rectifier area at least 6-9 vias of connection to the internal copper area. Try where possible to increase the number of power planes connected, at least below the diode position, to improve the heat dissipation.

A compromise on the thermal copper areas must be found between the need for a large area for thermal reasons and the need for a small copper area connected to switching devices, like Power MOSFETs and diodes, for EMI reasons.

Do not place other grounds or signals under the RJ45 and the data transformer area. Place any termination network on the bottom side.

1.5 In more detail

1. Place the transient voltage suppressor (TVS) close to the input common mode filter, if possible on the same side of the PCB
2. Place the PM8803 and all the related components close to each other; use both sides
3. Place all the feedback components close to each other, use both sides
4. Place the sense resistors close to the Power MOSFET, if possible on the same side
5. Place the input ceramic capacitors close to the input side of the power transformer, if possible on the same side
6. Place the primary snubber network close to the power transformer, on the bottom side
7. Place the rectifier diode or MOSFET close to the output side of the transformer, if possible on the same side
8. Place the secondary snubber network close to the rectifier diode or MOSFET, bottom side
9. Place the first ceramic capacitors close to the rectifier diode and the power transformer, on the copper areas, top side
10. Place the last ceramic capacitors close to the output of the power converter
11. Place the 100 nF input capacitor close to the VSS and GND pins
12. Place the decoupling capacitors for VC close to the PM8803 pin 6
13. Place the components for FRS, DT and DCCL pins in a quiet area, separated as much as possible from the other signals
14. Use traces of at least 20 mils for the following PM8803 pins: GAT1, GAT2, VC, CLS
15. Connect the PM8803 pins RTN1, RTN2, VSS, VDD to the relevant board copper areas
16. Use a wide path or copper area for SA auxiliary circuitry

2 EVALPM8803-FLY demonstration board layout

The layout of the PM8803 FLY demonstration board is shown as an example.

Even though not optimized for space, EVALPM8803-FLY is a good starting point for designing and laying out the PoE/PoE+ application with PM8803. In this demonstration kit, provision for multiple footprints for the key component (transformer, MOSFETs, diodes, gate driver transformer, optocoupler) have been made. Pictures of the various layers of the board are given below as an example to perform optimized layout for targeted applications.

Figure 4. Top layer

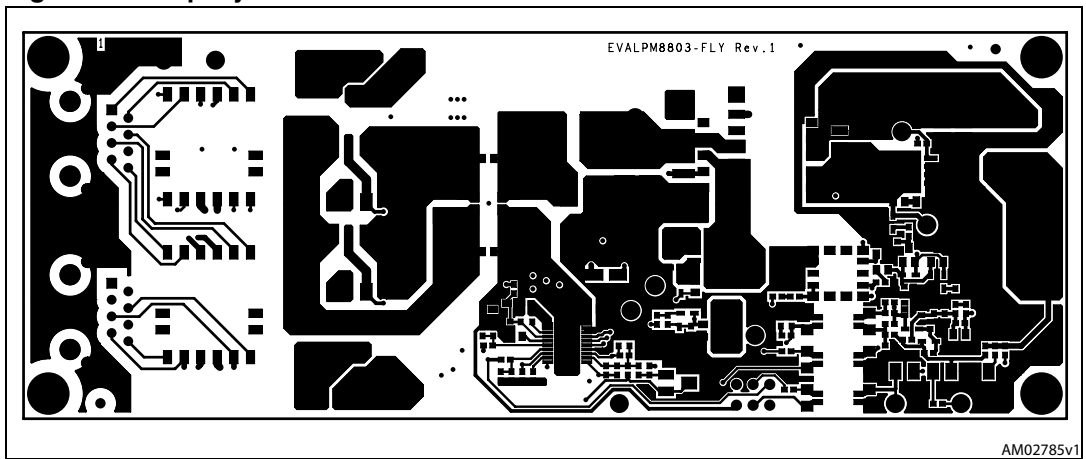


Figure 5. Inner layer 1

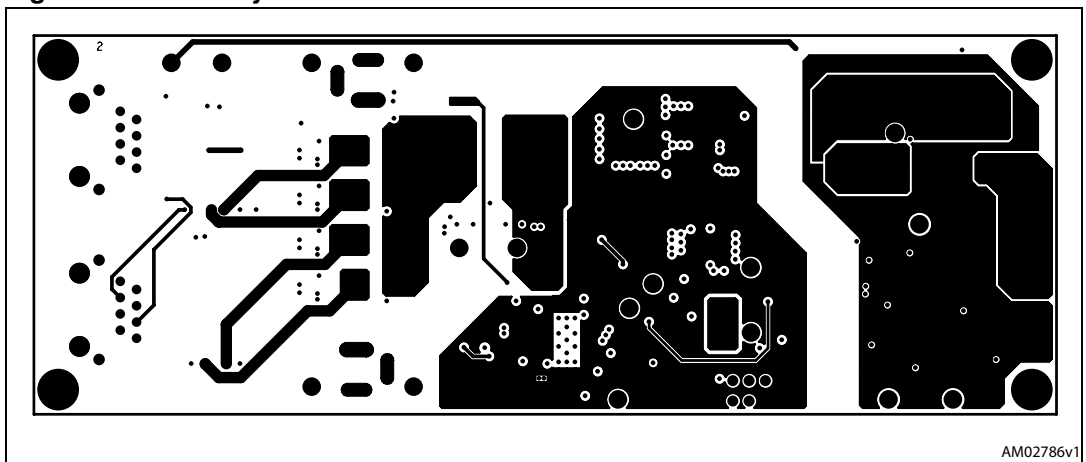


Figure 6. Inner layer 2

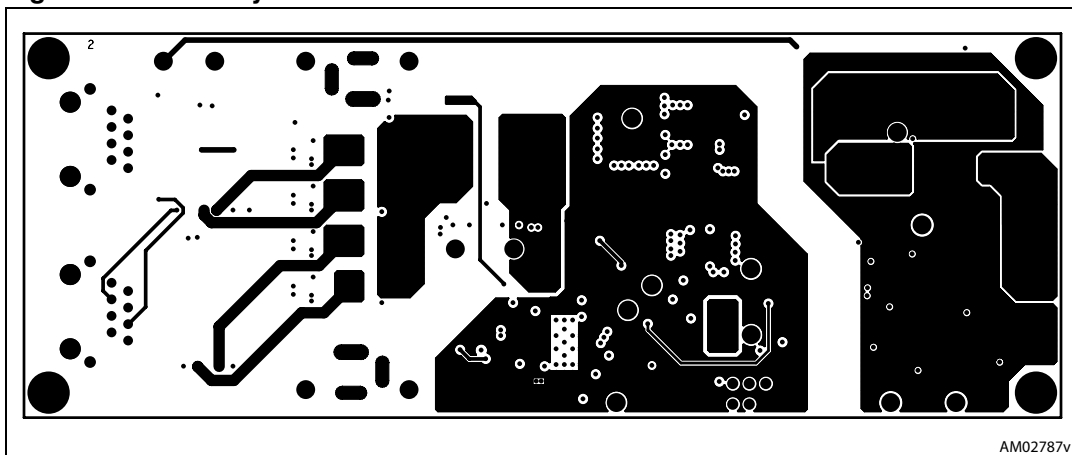
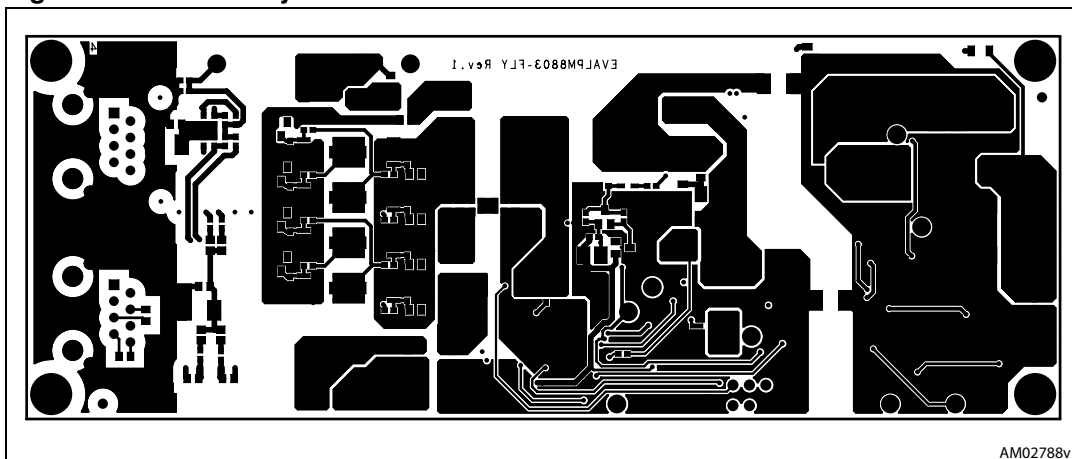


Figure 7. Bottom layer

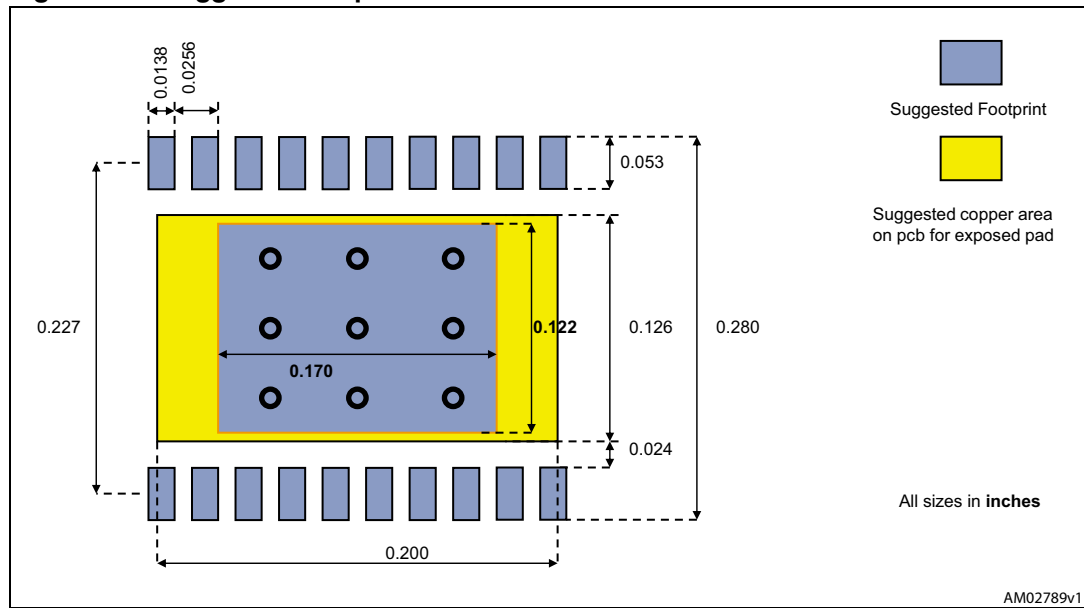


3 PM8803 suggested footprint

Figure 8 shows the suggested footprint for the HTSSOP20 with exposed pad package of PM8803.

Dimensions in Figure 8 are not to scale.

Figure 8. Suggested footprint for PM8803



4 Revision history

Table 2. Document revision history

Date	Revision	Changes
16-May-2011	1	Initial release

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