AN3390
Application note

EEPROM emulation in STM32F2xx microcontrollers

Introduction

EEPROMs (Electrically Erasable Programmable Read-Only Memory) are often used in industrial applications to store updateable data. An EEPROM is a type of permanent (non-volatile) memory storage system used in complex systems (such as computers) and other electronic devices to store and retain small amounts of data in the event of power failure.

For low-cost purposes, external EEPROM can be replaced using one of the following features of STM32F2xx:

- On-chip 4 Kbytes backup SRAM
- On-chip Flash, with specific software algorithm

The STM32F2xx features 4 Kbytes backup SRAM that can be powered from the VBAT supply when the main VDD supply is powered off.

This backup SRAM can be used as internal EEPROM (without any additional software) as long as the VBAT is present (typically in battery powered application) with the advantage of high speed access at CPU frequency.

However, when the backup SRAM is used for other purposes and/or the application does not use the VBAT supply, the on-chip Flash memory (with a specific software algorithm) can be used to emulate EEPROM memory.

This application note describes the software solution for substituting standalone EEPROM by emulating the EEPROM mechanism using the on-chip Flash of STM32F2xx devices.

Emulation is achieved by employing at least two sectors in the Flash. The EEPROM emulation code swaps data between the sectors as they become filled, in a manner that is transparent to the user.

The EEPROM emulation driver supplied with this application note meets the following requirements:

- Lightweight implementations offering a simple API that consists of three functions for initialization, read data and write data, and reduced footprint.
- Simple and easily updateable code model
- Clean-up and internal data management transparent to the user
- Background sector erase
- At least two Flash memory sectors to be used, more if possible for wear leveling

The EEPROM size to be emulated is flexible, within the limits and constraints of the sector size, and allows for a maximum EEPROM size.

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1 Main differences between external and emulated EEPROM

EEPROM is a key component of many embedded applications that require non-volatile storage of data updated with byte or word granularity during run time.

Microcontrollers used in these systems are more often based on embedded Flash memory. To eliminate components, save PCB space and reduce system cost, the STM32F2xx Flash memory may be used instead of external EEPROM for simultaneous code and data storage.

Unlike Flash memory, however, external EEPROM does not require an erase operation to free up space before data can be rewritten. Special software management is required to store data in embedded Flash memory.

The emulation software scheme depends on many factors, including the EEPROM reliability, the architecture of the Flash memory used, and the product requirements.

The main differences between embedded Flash memory and external serial EEPROM are the same for any microcontroller that uses the same Flash memory technology (it is not specific to the STM32F2xx family products). The major differences are summarized in *Table 1*.

Table 1. Differences between external and emulated EEPROM

Feature	External EEPROM (for example, M24C64: I²C serial access EEPROM)	Emulated EEPROM using on-chip Flash memory	Emulated EEPROM using on-chip backup SRAM memory (1)
Write time	– Random byte Write within 5 ms. Word program time = 20 ms – Page (32 bytes) Write within 5 ms. Word program time = 625 µs	Half-word program time: from 28 µs to 251 ms (2)	CPU speed with 0 wait state
Erase time	N/A	Sector (large page) Erase time: from 1s to 3 s (depending on the sector size)	NA
Write method	– Once started, is not CPU-dependent – Only needs proper supply	Once started, is CPU-dependent. If a Write operation is interrupted by CPU reset, the EEPROM Emulation algorithm is stopped, but current Flash write operation is not interrupted by a software reset. Can be accessed as bytes (8 bits), half words (16 bits) or full words (32 bits).	Can be accessed as bytes (8 bits), half words (16 bits) or full words (32 bits). Write operation is interrupted by a software reset.

Table 1. Differences between external and emulated EEPROM (continued)

Feature	External EEPROM (for example, M24C64: I²C serial access EEPROM)	Emulated EEPROM using on-chip Flash memory	Emulated EEPROM using on-chip backup SRAM memory (1)
Read access	– Serial: a hundred µs – Random word: 92 µs – Page: 22.5 µs per byte	Parallel: (at 120 MHz) the access time by half-word is from 0.44 µs to 332 µs (2)	CPU speed with 1 wait state
Write/Erase cycles	1 million Write cycles	10 kilocycles by sector (large page). Using multiple on-chip Flash memory pages is equivalent to increasing the number of write cycles. See *Section 3.4: Cycling capability and page allocation*.	No limit as long as VBAT is present

1. For more information about the backup SRAM usage, refer to “Battery backup domain” in *STM32F2xx reference manual* (RM0033).
2. For further detail, refer to *Chapter 2.5: EEPROM emulation timing*.

1.1 Difference in write access time

Because Flash memories have a shorter write access time, critical parameters can be stored faster in the emulated EEPROM than in an external serial EEPROM, thereby improving data storage.

1.2 Difference in erase time

The difference in erase time is the other major difference between a standalone EEPROM and emulated EEPROM using embedded Flash memory. Unlike Flash memories, EEPROMs do not require an erase operation to free up space before writing to them. This means that some form of software management is required to store data in Flash memory. Moreover, as the erase process of a block in the Flash memory does not take long, power shutdown and other spurious events that might interrupt the erase process (a reset, for example) should be considered when designing the Flash memory management software. To design robust Flash memory management software a thorough understanding of the Flash memory erase process is necessary.

Note: In the case of a CPU reset, ongoing sector erase or mass erase operations on the STM32F2xx embedded Flash are not interrupted.

1.3 Similarity in writing method

One of the similarities between external EEPROM and emulated EEPROM with the STM32F2xx embedded Flash is the writing method.

- Standalone external EEPROM: once started by the CPU, the writing of a word cannot be interrupted by a CPU reset. Only a supply failure will interrupt the write process, so

properly sizing the decoupling capacitors can secure the complete writing process inside a standalone EEPROM.

- Emulated EEPROM using embedded Flash memory: once started by the CPU, the write process can be interrupted by a power failure. In the case of a CPU reset, ongoing word write operation on the STM32F2xx embedded Flash are not interrupted. The EEPROM algorithm is stopped, but the current Flash word write operation is not interrupted by a CPU reset.

2 Implementing EEPROM emulation

2.1 Principle

EEPROM emulation is performed in various ways, taking into consideration the Flash memory limitations and product requirements. The approach detailed below requires at least two Flash memory sectors of identical size allocated to non-volatile data: one that is initially erased, and offers byte-by-byte programmability; the other that is ready to take over when the former sector needs to be garbage-collected. A header field that occupies the first half word (16-bit) of each sector indicates the sector status. Each of these sectors is considered as a page, and called Page0 and Page1 in the rest of this document.

The header field is located at the base address of each page and provides the page status information.

Each page has three possible states:

- **ERASED**: the page is empty.
- **RECEIVE_DATA**: the page is receiving data from the other full page.
- **VALID_PAGE**: the page contains valid data and this state does not change until all valid data is completely transferred to the erased page.

Figure 1 shows how the page status changes.

Figure 1. Header status switching between page0 and page1

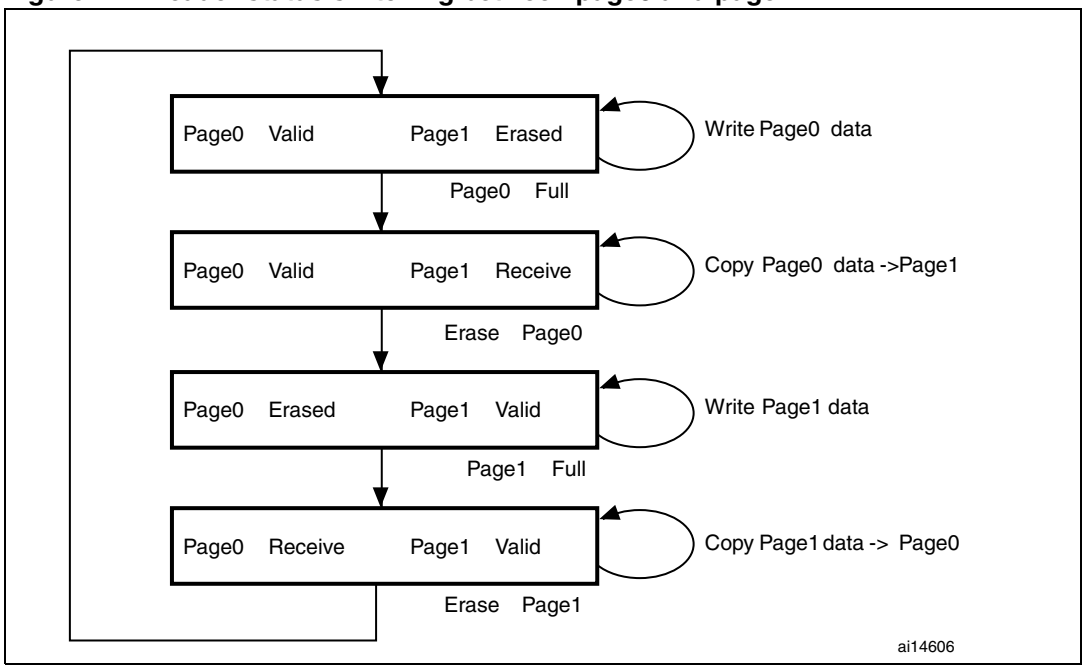


Table 2. Emulated pages possible status and corresponding actions

Page1	Page0		
	ERASED	**RECEIVE_DATA**	**VALID_PAGE**
ERASED	**Invalid state** **Action:** Erase both pages and format page0	**Action:** Erase Page1 and mark Page0 as VALID_PAGE	**Action:** Use page0 as the valid page and erase page1
RECEIVE_DATA	**Action:** Erase Page0 and mark Page1 as VALID_PAGE	**Invalid state** **Action:** Erase both pages and format page0	**Action:** Use page0 as the valid page & transfer the last updated variables from page0 to page1 & mark page1 as valid & erase page0
VALID_PAGE	**Action:** Use page1 as the valid page and erase page0	**Action:** Use page1 as the valid page & transfer the last updated variables from page1 to page0 & mark page0 as valid & erase page1	**Invalid state** **Action:** Erase both pages and format page0

Generally, when using this method, the user does not know the variable update frequency in advance.

The software and implementation described in this document use two Flash memory sectors of 16 Kbytes (sector 2 and sector 3) to emulate EEPROM.

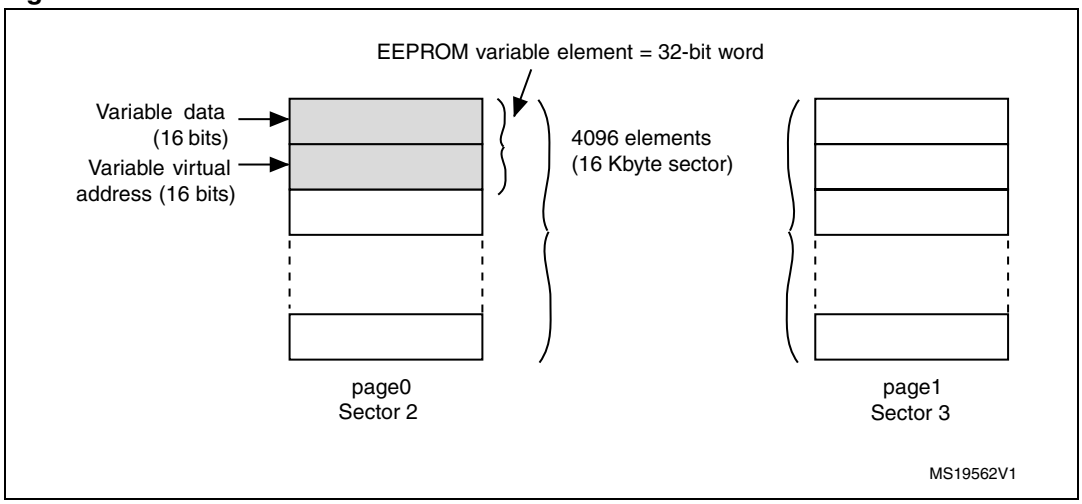
Note: The choice of sectors 2 and 3 is due to the small size of these sectors compared with the other sectors of the STM32F2xx Flash memory (the main memory block in the STM32F2xx Flash memory is divided as described in Table 3: STM32F2xx Flash memory sectors). Large sectors can be used, depending on application and user needs.

Table 3. STM32F2xx Flash memory sectors

Name	Sector Size
Sectors 0 to 3	16 Kbyte
Sector 4	64 Kbyte
Sectors 5 to 11	128 Kbyte

Each variable element is defined by a virtual address and a value to be stored in Flash memory for subsequent retrieval or update (in the implemented software both virtual address and data are 16 bits long). When data is modified, the modified data associated with the earlier virtual address is stored into a new Flash memory location. Data retrieval returns the up to date data value.

Figure 2. EEPROM variable format



2.2 Case of use: application example

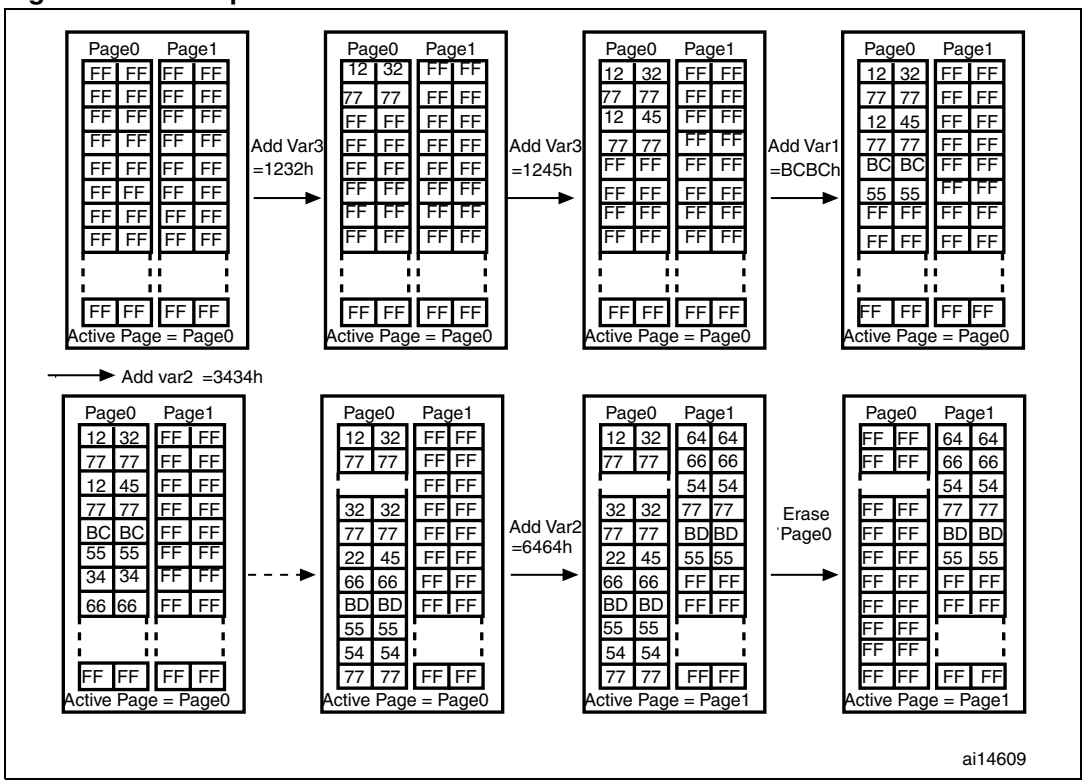
The following example shows the software management of three EEPROM variables (Var1, Var2 and Var3) with the following virtual addresses:

Var1 virtual address 5555h

Var2 virtual address 6666h

Var3 virtual address 7777h

Figure 3. Data update flow



2.3 EEPROM emulation software description

This section describes the driver implemented for EEPROM emulation using the STM32F2xx Flash memory driver provided by STMicroelectronics.

A sample demonstration program is also supplied to demonstrate and test the EEPROM emulation driver using the three variables Var1, Var2 and Var3 defined in the *VirtAddVarTab[]* table declared in the software *main.c* file.

The project contains three source files in addition to the Flash memory library source files:

- ***eeprom.c***: contains the EEPROM emulation firmware functions:

```
EE_Init()
EE_Format()
EE_FindValidPage()
EE_VerifyPageFullWriteVariable()
EE_ReadVariable()
EE_PageTransfer()
EE_WriteVariable()
```

- ***eeprom.h***: contains the functions prototypes and some declarations. You can use this file to adapt the following parameters to your application requirements:
  - Flash sectors to be used (default: sector 2 and Sector 3)
  - The device voltage range (default: range 4, 2.7V to 3.6V).

    In the EEPROM emulation firmware, the FLASH_ProgramHalfWord() function is used to program the memory. This function can only be used when the device

voltage is in the 2.1V to 3.6V range. As consequence, if the device voltage range is 1.8V to 2.1 V in your application, you have to use the FLASH_ProgramByte() function instead, and adapt the firmware accordingly.

  - Number of data variables to be used (default: 3)

- ***main.c***: this application program is an example using the described routines in order to write to and read from the EEPROM.

User API definition

The set of functions contained in the *eeprom.c* file, that are used for EEPROM emulation, are described in the table below:

Table 4. API definition

Function name	Description
`EE_Init()`	Sector header corruption is possible in the event of power loss during data update or sector erase / transfer. In this case, the `EE_Init()` function will attempt to restore the emulated EEPROM to a known good state. This function should be called prior to accessing the emulated EEPROM after each power-down. It accepts no parameters. The process is described in *Table 2: Emulated pages possible status and corresponding actions on page 9*.
`EE_Format()`	This function erases page0 and page1 and writes a VALID_PAGE header to page0.
`EE_FindValidPage()`	This function reads both page headers and returns the valid page number. The passed parameter indicates if the valid page is sought for a write or read operation (READ_FROM_VALID_PAGE or WRITE_IN_VALID_PAGE).
`EE_VerifyPageFullWrite Variable()`	It implements the write process that must either update or create the first instance of a variable. It consists in finding the first empty location on the active page, starting from the end, and filling it with the passed virtual address and data of the variable. In the case the active page is full, the PAGE_FULL value is returned. This routine uses the parameters below: Virtual address: may be any of the three declared variables' virtual addresses (Var1, Var2 or Var3) Data: the value of the variable to be stored This function returns FLASH_COMPLETE on success, PAGE_FULL if there is not enough memory for a variable update, or a Flash memory error code to indicate operation failure (erase or program).
`EE_ReadVariable()`	This function returns the data corresponding to the virtual address passed as a parameter. Only the last update is read. The function enters in a loop in which it reads the variable entries until the last one. If no occurrence of the variable is found, the ReadStatus variable is returned with the value "1", otherwise it is reset to indicate that the variable has been found and the variable value is returned on the Read_data variable.

Table 4. API definition (continued)

Function name	Description
`EE_PageTransfer()`	It transfers the latest value of all variables (data with associated virtual address) from the current page to the new active page. At the beginning, it determines the active page, which is the page the data is to be transferred from. The new page header field is defined and written (new page status is RECEIVE_DATA given that it is in the process of receiving data). When the data transfer is complete, the new page header is VALID_PAGE, the old page is erased and its header becomes ERASED.
`EE_WriteVariable()`	This function is called by the user application to update a variable. It uses the `EE_VerifyPageFullWriteVariable()`, and `EE_PageTransfer()` routines that have already been described.

Note: The following functions can be used to access the emulated EEPROM:

- EE_Init()

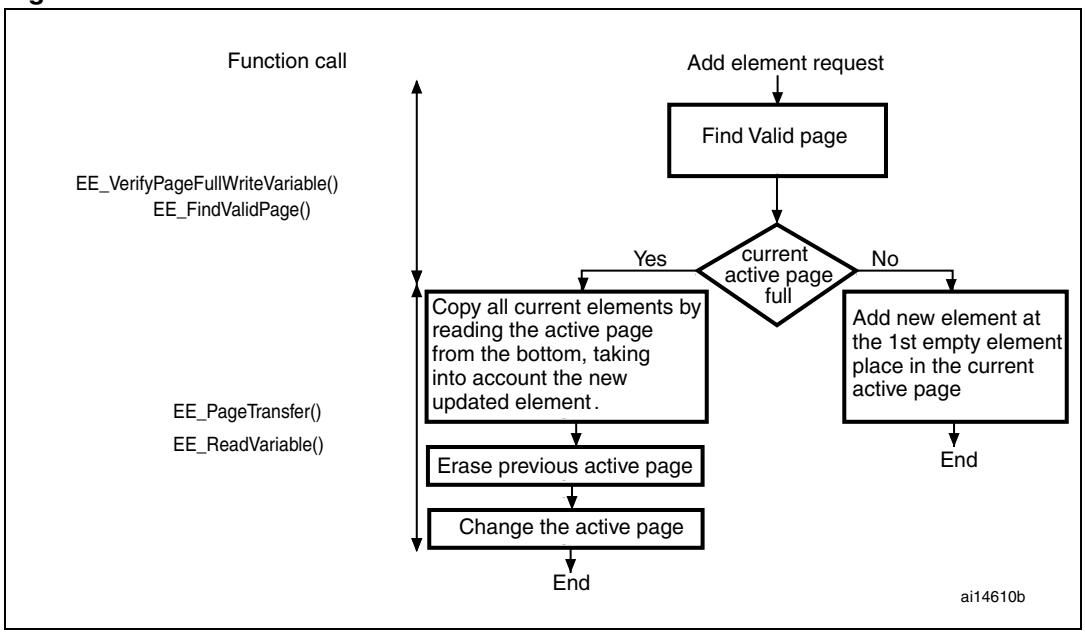
- EE_ReadVariable()

- EE_WriteVariable()

These functions are used in the application code delivered with this application note.

Figure 4 shows the procedure for updating a variable entry in the EEPROM.

Figure 4. WriteVariable flowchart



Key features

- User-configured emulated EEPROM size
- Increased Flash memory endurance: page erased only when it is full
- Non-volatile data variables can be updated infrequently
- Interrupt servicing during program/erase is possible

2.4 EEPROM emulation memory footprint

Table 5 details the footprint of the EEPROM emulation driver in terms of Flash size and RAM size.

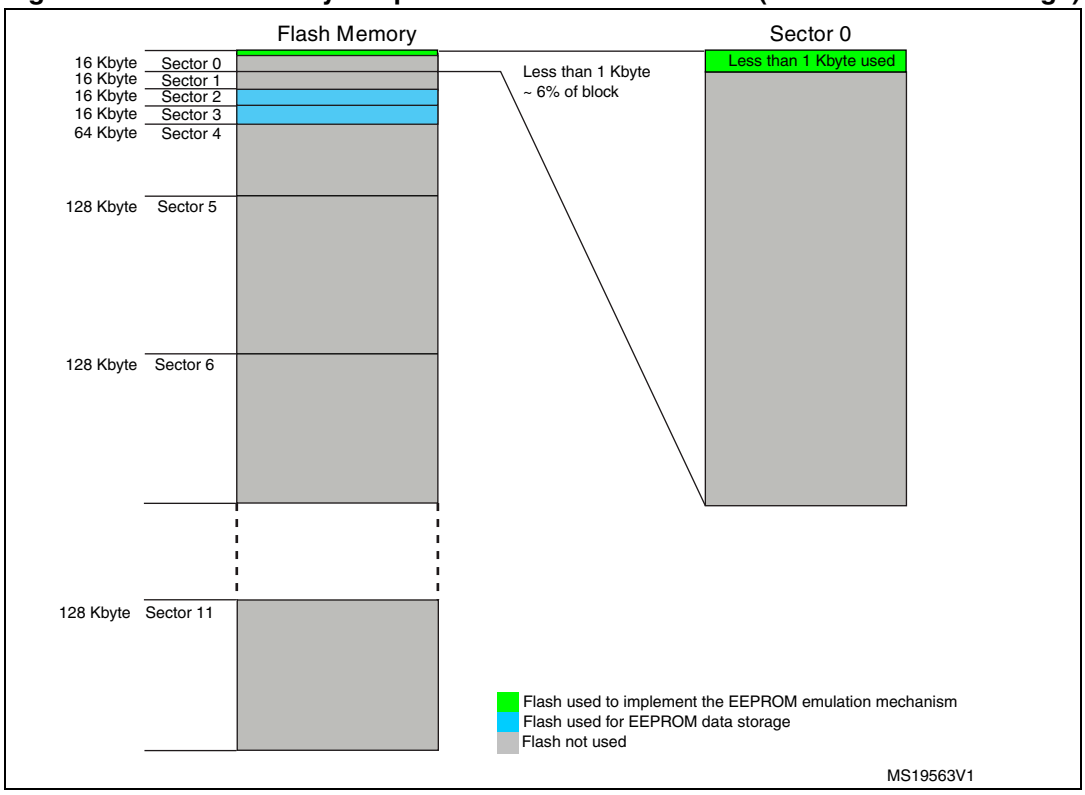
The table and figure below have been determined using the IAR EWARM 6.10 tool with High Size optimization level.

Table 5. Memory footprint for EEPROM emulation mechanism

Mechanism	Minimum(1) required code size (bytes)	
	Flash	SRAM
EEPROM emulation software mechanism	984	6

1. Based on one 32-bit variable (16-bit for address and 16-bit for data). The SRAM memory used increases depending on the number of variables used.

Figure 5. Flash memory footprint for EEPROM emulation (mechanism and storage)



2.5 EEPROM emulation timing

This section describes the timing parameters associated with the EEPROM emulation driver based on two 16 Kbyte EEPROM page sizes.

All timing measurements are performed:

- STM32F207IGH6 Revision Y
- With the voltage range 3 (2.7 V to 3.6 V)
- System clock at 120 MHz, Flash prefetch and cache features enabled
- With execution from Flash
- At room temperature

Table 6 lists the timing values for EEPROM.

Table 6. EEPROM emulation timings with a 120 MHz system clock

Operation	EEPROM emulation timings		
	Minimum (µs)	Typical (ms)	Maximum (µs)
Typical (1) variable(2) Write operation in EEPROM	28	-	330
Variable Write operation with page swap (3) in EEPROM	-	251	-
Variable Read Operation from EEPROM (4)	0.44	-	332
EEPROM Initialization for the 1st time (5)	-	510	-
Typical EEPROM Initialization(6)	-	241	-

1. Write with no page swap. The minimum value refers to a write operation of a variable in the beginning of the Flash sector and the maximum value refers to a write operation in the end of the Flash sector. The difference between the minimum and maximum values is due to the time taken to find a free Flash address to store the new data.
2. Variable size used is 32-bit (16-bit for the virtual address and 16-bit for the data)
3. Page swapping is done when the valid page is full. It consists of transferring the last stored data for each variable to the other free page and erasing the full page.
4. The minimum value refers to a read operation of the 1st variable stored in the Flash sector and the maximum value refers to a read operation of the last variable -1. The difference between the minimum and maximum values is due to the time taken to find last stored variable data.
5. When the EEPROM mechanism is run for the 1st time or for invalid status (refer to *Table 2: Emulated pages possible status and corresponding actions on page 9* for more detail), the two pages are erased and the page used for storage is marked as VALID_PAGE.
6. A typical EEPROM initialization is performed when a valid page exists (the EEPROM has been initialized at least once). During a typical EEPROM initialization, one of the two pages is erased (see *Table 2: Emulated pages possible status and corresponding actions on page 9* for more detail).

3 Embedded application aspects

This section provides advice on how to overcome software limitations in embedded applications and how to fulfill the needs of different applications.

3.1 Data granularity management

Emulated EEPROM can be used in embedded applications where non-volatile storage of data updated with a byte, half-word or word granularity is required. It generally depends on the user requirements and Flash memory architecture (for example, stored data length, write access).

The STM32F2xx on-chip Flash memory allows 8-bit, 16-bit or word programming depending on the voltage range used as described in *Table 7*.

Table 7. Flash program functions

Data granularity	Function name	Functional Voltage range
by Word(32-bit)	FLASH_ProgramWord	From 2.7 V to 3.6 V.
by half word(16-bit)	FLASH_ProgramHalfWord	From 2.1 V to 3.6 V.
by byte(8-bit) (1)	FLASH_ProgramByte	All the device supply voltage ranges.

1. Programming on a byte-by-byte basis: writing by byte offers the possibility of storing more data variables. The performance may however be reduced when using the FLASH_ProgramByte() function. We recommend that you use the FLASH_ProgramHalfWord() function. Both virtual address and data can be written simultaneously as a half word.

3.2 Wear leveling: Flash memory endurance improvement

In the STM32F2xx on-chip Flash memory, each sector can be programmed or erased reliably around 10 000 times.

For write-intensive applications that use more than two pages (3 or 4) for the emulated EEPROM, it is recommended to implement a wear-leveling algorithm to monitor and distribute the number of write cycles among the pages.
When no wear-leveling algorithm is used, the pages are not used at the same rate. Pages with long-lived data do not endure as many write cycles as pages that contain frequently updated data. The wear-leveling algorithm ensures that equal use is made of all the available write cycles for each sector.

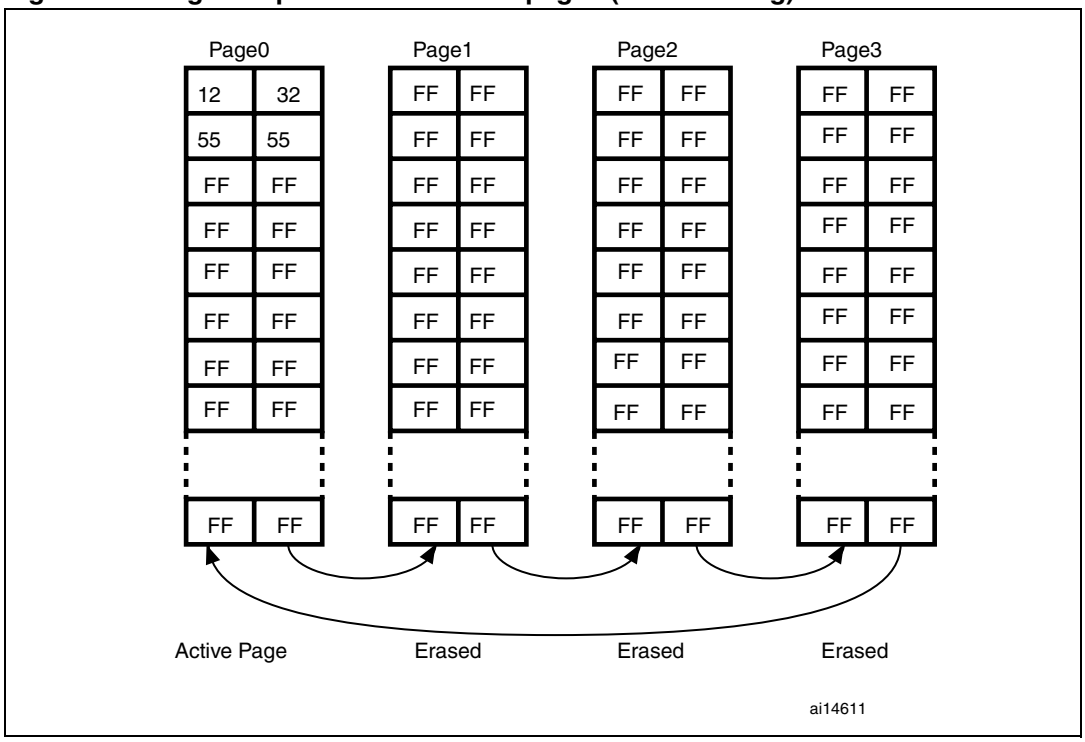
Note: The main memory block in the STM32F2xx Flash memory is divided as described in Table 3: STM32F2xx Flash memory sectors.

3.2.1 Wear-leveling implementation example

In this example, in order to enhance the emulated EEPROM capacity, four sectors will be used (sector5 as Page0, sector6 as Page1, sector7 as Page2 and sector8 as Page3).

The wear-leveling algorithm is implemented as follows: when page *n* is full, the device switches to page *n+1*. Page *n* is garbage-collected and then erased. When it is the turn of Page3 to be full, the device goes back to Page0, Page3 is garbage-collected then erased and so on (refer to *Figure 6*).

Figure 6. Page swap scheme with four pages (wear leveling)



In the software, the wear-leveling algorithm can be implemented using the `EE_FindValidPage()` function (refer to *Table 4*).

3.3 Page header recovery in case of power loss

Data or page header corruption is possible in case of a power loss during a variable update, page erase or transfer.

To detect this corruption and recover from it, the *`EE_Init()`* routine is implemented. It should be called immediately after power-up. The principle of the routine is described in this application note. The routine uses the page status to check for integrity and perform repair if necessary.

After power loss, the *`EE_Init()`* routine is used to check the page header status. There are 9 possible status combinations, three of which are invalid. *Table 2: Emulated pages possible status and corresponding actions on page 9* shows the actions that should be taken based on the page statuses upon power-up.

3.4 Cycling capability and page allocation

3.4.1 Cycling capability

A program/erase cycle consists of one or more write accesses and one page erase operation.

When the EEPROM technology is used, each byte can be programmed and erased a finite number of times, typically in the range of 10 000 to 100 000.

However, in embedded Flash memory, the minimum erase size is the sector and the number of program/erase cycles applied to a sector is the number of possible erase cycles. The STM32F2xx's electrical characteristics guarantee 10 000 program/erase cycles per sector. The maximum lifetime of the emulated EEPROM is thereby limited by the update rate of the most frequently written parameter.

The cycling capability depends on the amount/size of data that the user wants to handle.

In this example, two sectors (of 16 Kbytes) are used and programmed with 16-bit data. Each variable corresponds with a 16-bit virtual address. That is, each variable occupies a word of storage space. A sector can store 16 Kbytes multiplied by the Flash memory endurance of 10 000 cycles, giving a total of 160 000 Kbytes of data storage capacity for the lifetime of one page in the emulated EEPROM memory. Consequently, 320 000 Kbytes can be stored in the emulated EEPROM, provided that two pages are used in the emulation process. If more than two pages are used, this number is multiplied accordingly.

Knowing the data width of a stored variable, it is possible to calculate the total number of variables that can be stored in the emulated EEPROM area during its lifetime.

3.4.2 Flash page allocation

The sector size and the sector number needed for an EEPROM emulation application can be chosen according to the amount of data written during the lifetime of the system.

For example, a 16-Kbyte page with 10 Kbyte erase cycles can be used to write a maximum of 160 megabytes during the lifetime of the system. A 128-Kbyte page can be used to write a maximum of 1280 megabytes during the lifetime of the system.

Free variable space can be calculated as:

FreeVarSpace = (PageSize) / (VariableTotalSize) - [NbVar+1]

Where:

- **Page size**: page size in bytes (for example, 16 Kbytes)
- **NbVar**: number of variables in use (for example, 10 variables)
- **VariableTotalSize**: number of bytes used to store a variable (address and data)
  - VariableTotalSize = 8 for 32-bit variables with (32-bit data + 32-bit virtual address)
  - VariableTotalSize = 4 for 16-bit variables with (16-bit data + 16-bit virtual address)
  - VariableTotalSize = 2 for 8-bit variables with (8-bit data + 8-bit virtual address)

An estimation of the pages needed to guarantee predictable Flash operation during the application lifetime can be calculated as following:

Required page number:

NbPages = NbWrites / (PageEraseCycles * FreeVarSpace)

Where:

- **NbPages** = number of pages needed
- **NbWrites** = total number of variable writes
- **PageEraseCycles** = number of erase cycles of a page

Note: If variables are 16-bit, each variable takes 32-bit (16-bit data, with a 16-bit virtual address), which means that each variable uses 4 bytes of Flash memory each time new data is written. Each 16-Kbyte (or 128-Kbyte) page can take 4096 (or 32768) variable writes before it is full.

Note: This calculation is a slightly conservative estimation.

Case of use example

To design an application that updates **20** different variables, every **2** minutes for **10** years:

- NbVar = **20**
- NbWrites = **10** * 365 * 24 * (60/**2**) * NbVar = ~52 million writes

- If variables are 8-bit data, with an 8-bit virtual address, the number of pages needed to guarantee non-volatile storage of all this data, is:
  - Two pages of 16 Kbytes or
  - Two pages of 128 Kbytes
- If variables are 16-bit data, with a 16-bit virtual address, the number of pages needed to guarantee non-volatile storage of all this data, is:
  - Two pages of 16 Kbytes or
  - Two pages of 128 Kbytes
- If variables are 32-bit data, with 32-bit virtual address, the number of pages needed to guarantee non-volatile storage of all this data, is:
  - Three pages of 16 Kbytes or
  - Two pages of 128 Kbytes

Table 8. Application design

Variable size	Number of writes (NbWrites)	Total amount of data to write (in bytes)	Page size (Kbytes)	Page erase cycles	Number of pages needed	Number of pages used (1)
8-bit	52 560 000	105 120 000	16	10000	0.6	2
			128		0.1	
16-bit	52 560 000	210 240 000	16	10000	1.3	2
			128		0.2	
32-bit	52 560 000	420 480 000	16	10000	2.6	3
			128		0.3	2

1. A minimum of two pages is needed to emulate the EEPROM

3.5 Real-time consideration

The provided implementation of the EEPROM emulation firmware runs from the internal Flash, thus access to the Flash will be stalled during operations requiring Flash erase or programming (EEPROM initialization, variable update or page erase). As a consequence, the application code is not executed and the interrupt can not be served.

This behavior may be acceptable for many applications, however for applications with real-time constraints, you need to run the critical processes from the internal RAM.

In this case:

1. Relocate the vector table in the internal RAM.
2. Execute all critical code and interrupt service routines from the internal RAM. the compiler provides a keyword to declare functions as a RAM function; the function is

copied from the Flash to the RAM at system startup just like any initialized variable. It is important to note that for a RAM function, all used variable(s) and called function(s) should be within the RAM.

4 Revision history

Table 9. Document revision history

Date	Revision	Changes
06-Jun-2011	1	Initial release.
07-Nov-2011	2	Updated *Section 1: Main differences between external and emulated EEPROM* title, and write time, erase time, read access time, and notes in *Table 1*. Updated *Section 1.2: Difference in erase time* and *Section 1.3: Similarity in writing method*. Added *Table 2: Emulated pages possible status and corresponding actions*. Modified `EE_PageTransfer()` description in *Table 4: API definition*. Updated *Table 6: EEPROM emulation timings with a 120 MHz system clock*. Added *Section 3.5: Real-time consideration*.

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