AN3399

L99PM62GXP external voltage regulation with bipolar transistor

Introduction

The following application note describes the L99PM62GXP external schematic and relevant characteristics for operating an external voltage regulation for driving a load up to 200 mA.

The first paragraph contains the detailed schematic description. The second paragraph contains exhaustive static so that dynamic evaluations and demonstrates the regulation stability in case of V_S and/or current load variations.

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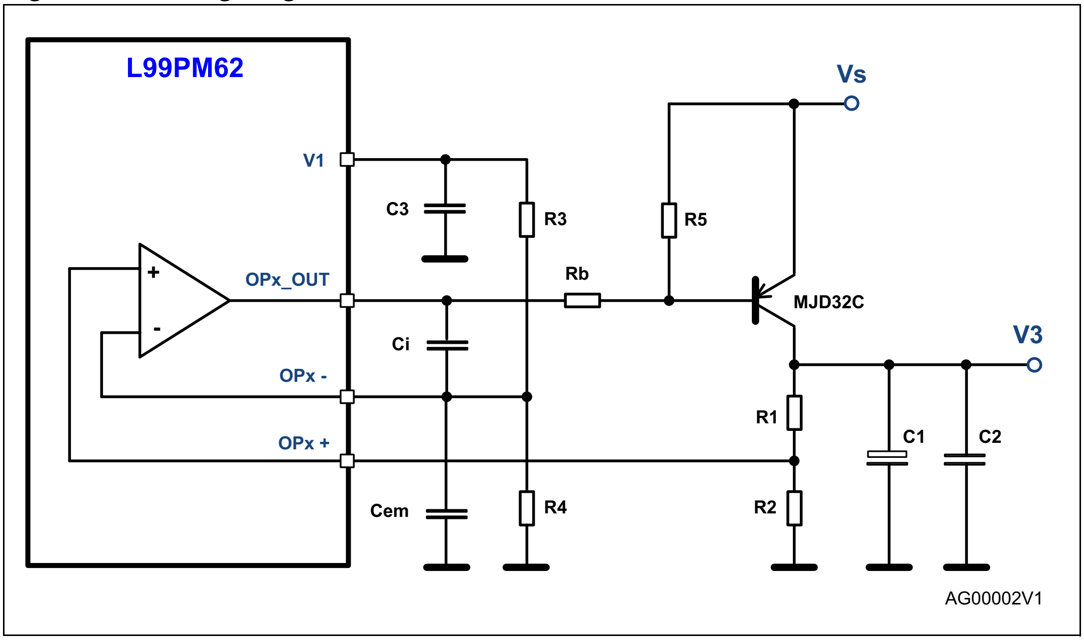
1 Voltage regulation circuit schematics

1.1 Regulation with external PNP without current limitation

Figure 1. Voltage regulation with external PNP



The *Figure 1* is an example of recommended circuit for voltage regulation with external transistor. As a reference voltage source was used 5V1 voltage regulator of L99PM62GXP.

Parameters of circuit at *Figure 1* are:

- Output voltage = 5.0 V
- Output current from 0 to approx. 1 A (no limitation), for V_S +-12 V
- V_S operation range from 5.5 to 18 V; for output current up to 200 mA the theoretical minimum operational range is from 5.2 V. (V_S is the voltage after reverse polarity protection).

The output voltage is possible set by change of R1 and R2 value. In case of R3 = R4 the U3 is possible express from equation:

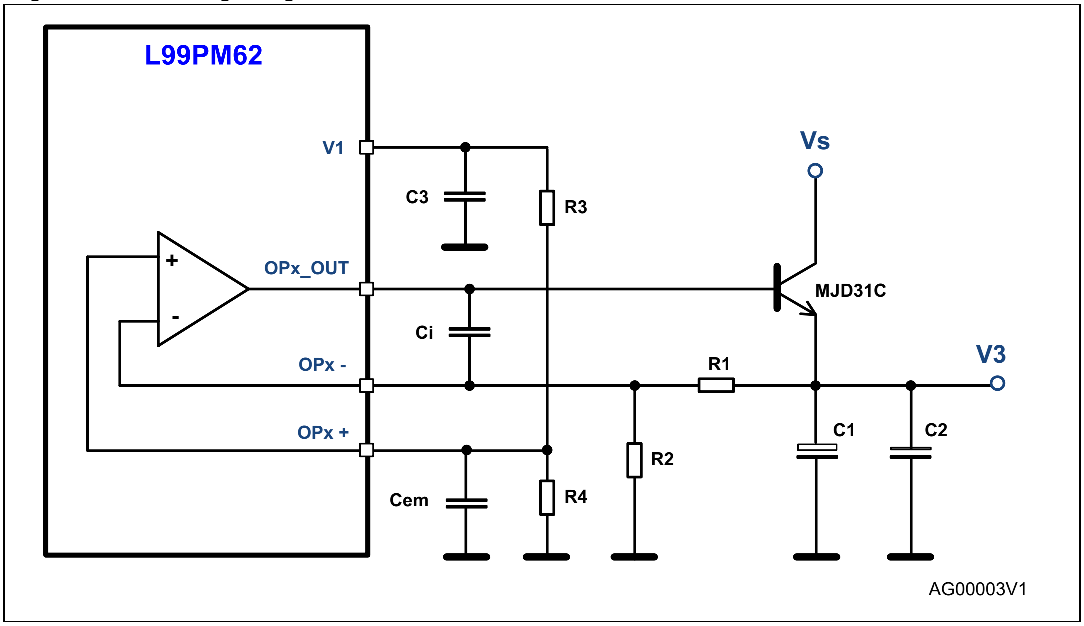
$$U_3 = U_{5V1} \times \frac{R_4}{R_3 + R_4} \times \frac{R_1 + R_2}{R_2}[V]$$

Important requirement is to ensure the voltage on OP_- and OP_+ inputs is bellow 3 V.

1.2 Regulation with external NPN without current limitation

The *Figure 2* is the modified circuit of external voltage regulation circuit with external NPN transistor.

Figure 2. Voltage regulation with external NPN



The advantage of this circuit is fewer amounts of external components. However this is balanced by lower V_S operation range in comparison to PNP regulation circuit.

Parameters of circuit at *Figure 2* are:

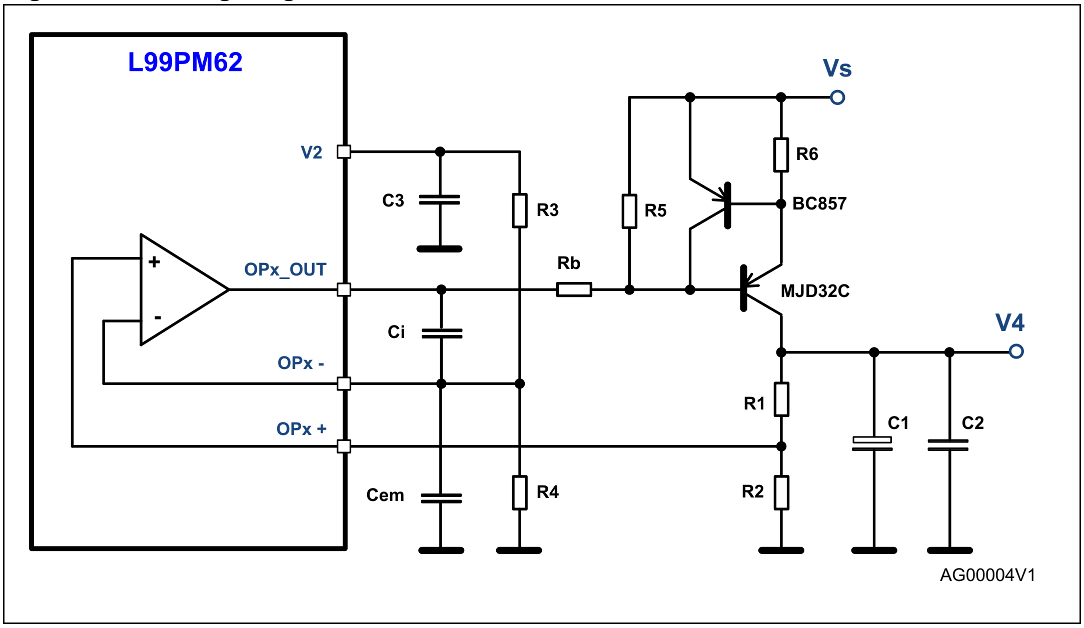
- Output voltage = 5.0 V
- Output current from 0 to 1 A – (no limitation)
- V_S operation range from 6 to 18 V (V_S is the voltage after reverse polarity protection)

As in previous case the output voltage is possible set by change of R1 and R2 value. In case of R3 = R4 the U3 is possible express from equation:

$$U_3 = U_{5V1} \times \frac{R_4}{R_3 + R_4} \times \frac{R_1 + R_2}{R_2} [V]$$

1.3 Voltage regulation and current limitation with external PNP

Figure 3. Voltage regulation and current limitation with external PNP



This circuit is a light modification of circuit from *Figure 1*, extended for current limitation. Transistor T2 (BC857) together with resistor R6 limits output current, which is possible adjust be change or R6 value. The voltage drop at R6 for maximum current should be about 0,65 V.

Parameters of circuit form *Figure 3* are following:

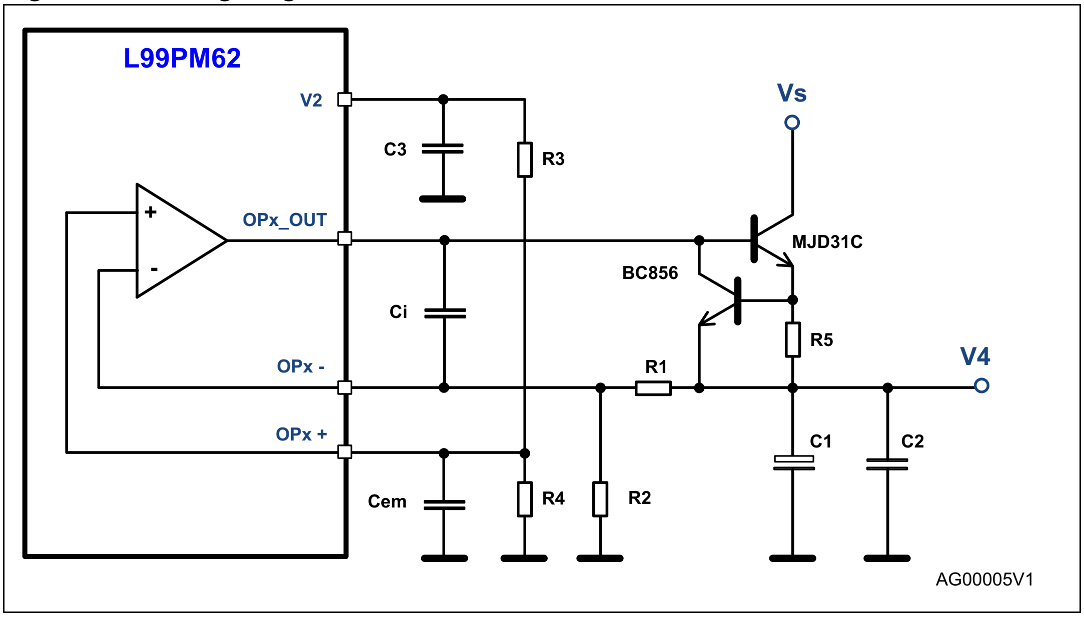
- Output voltage = 5 V
- Output current limited at 200 mA
- V_S operation range 5.8 V to 18 V (28 V absolute maximum ratings)

The output voltage is possible adjust like in original schematics by change or R1 and R2 resistors without impact to current limitation. For sure the V_S operational range (low limit) corresponds to selected output voltage.

1.4 Voltage regulation and current limitation with external NPN

The *Figure 4* is the slightly modified circuit from *Figure 1* for voltage regulation with current limitation using external NPN.

Figure 4. Voltage regulation and current limitation with external NPN



This circuit is a modification of circuit from *Figure 2* extended with the current limitation feature provided by resistor R5 and transistor T2 (BC856). The output voltage is possible adjust like in original schematics by change or R1 and R2 resistors without impact on the current limitation. For sure the V_S operational range (low limit) corresponds to selected output voltage.

Parameters of circuit from *Figure 4* are following:

- Output voltage = 5 V
- Output current limited at 200 mA
- V_S operation range 6.5 V to 18 V (28 V absolute maximum ratings)

2 Evaluations of circuit with PNP and current limitation

2.1 Static characteristics

2.1.1 Standby current

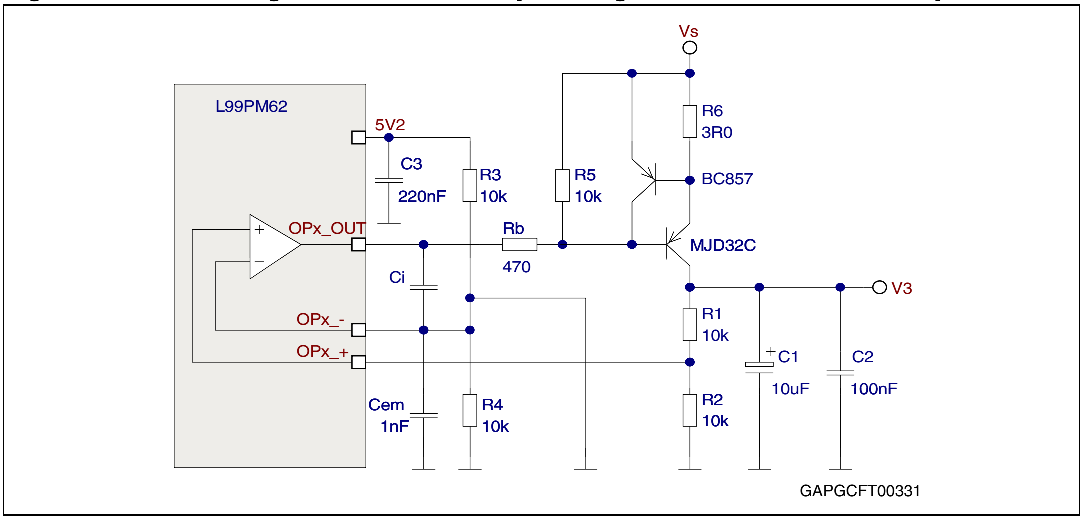
The V_S current in OFF state was evaluated for the most recommended circuit of voltage regulation and current limitation with external PNP transistor (see *Figure 1*).

The 5V2 voltage regulator was switched OFF by SPI in Active Mode Configuration. There was observed a small current from V_3 output caused by residual voltage of 5V2 voltage regulator.

- $V_S = 12$ V
- $I_{Vs} = 0.279$ mA
- $I_{op\_out} = 0.052$ mA
- $I_3 = 0.22$ mA
- R_1, R_2, R_3, R_4, $R_5 = 10$ K

This current will be significantly decreased by switching the device in V1stby Mode which turns OFF the operational amplifier (see *Figure 5*).

Figure 5. Removing residual current by turning L99PM62GXP in standby mode



Conclusion

A residual current can be observed in the load in case the reference voltage 5V2 is turned OFF and L99PM62GXP is maintained on active more.

By turning L99PM62GXP in any standby mode (V1stby or Vbatstby), this residual current will be removed.

2.1.2 Line regulation 6-18 V

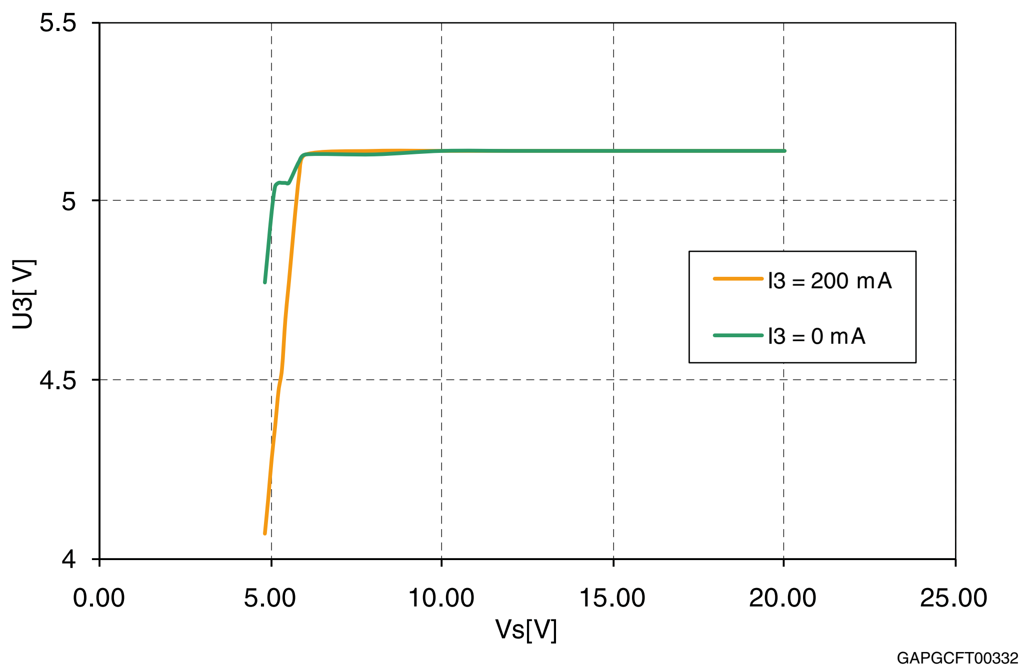
Influence of V_S variation on the V_3 voltage regulation

- V_S range from 4.8 to 18 V
- I_3 current from 0 to 200 mA
- R_1, R_2, R_3, R_4, R_5 = 10 K
- V_2 (measured) = 5.15 V
- Temperature = 25 °C ambient

Table 1. V_3 to V_S dependence

V_S[V]	V_3[V] (I_3 = 0 mA)	V_3[V] (I_3 = 200 mA)
4,80	4,77	4,07
4,90	4,87	4,17
5,00	4,97	4,28
5,10	5,04	4,37
5,20	5,05	4,47
5,30	5,05	4,53
5,40	5,05	4,67
5,50	5,05	4,77
5,80	5,11	5,07
6,00	5,13	5,13
8,00	5,13	5,14
10,00	5,14	5,14
12,00	5,14	5,14
14,00	5,14	5,14
16,00	5,14	5,14
18,00	5,14	5,14
20,00	5,14	5,14

Figure 6. V_3 to V_S dependence



2.1.3 Load regulation up to 250 mA

Influence of I_3 output current on V_3 voltage regulation

- V_S = 6, 12, 18V
- R_1, R_2, R_3, R_4, R_5 = 10 K
- I_3 range = from 0 to 250 mA (with current limitation on 220 mA)
- Temperature = 25 °C ambient

Table 2. V_3 to I_3 dependence for V_S = 6, 12, 18 V

I_3[mA]	V_3[V] (V_S = 6 V)	V_3[V] (V_S = 12 V)	V_3[V] (V_S = 18V)
0	5,13	5,14	5,14
10	5,13	5,14	5,14
20	5,13	5,14	5,14
50	5,13	5,14	5,14
100	5,13	5,14	5,14
200	5,13	5,13	5,14
210	5,13	5,13	5,14
215	5,13	5,13	5,14
217	4,95	5,13	5,14
218	0,07	5,13	5,14
222		0,07	0,07

Figure 7. V_3 to I_3 dependence

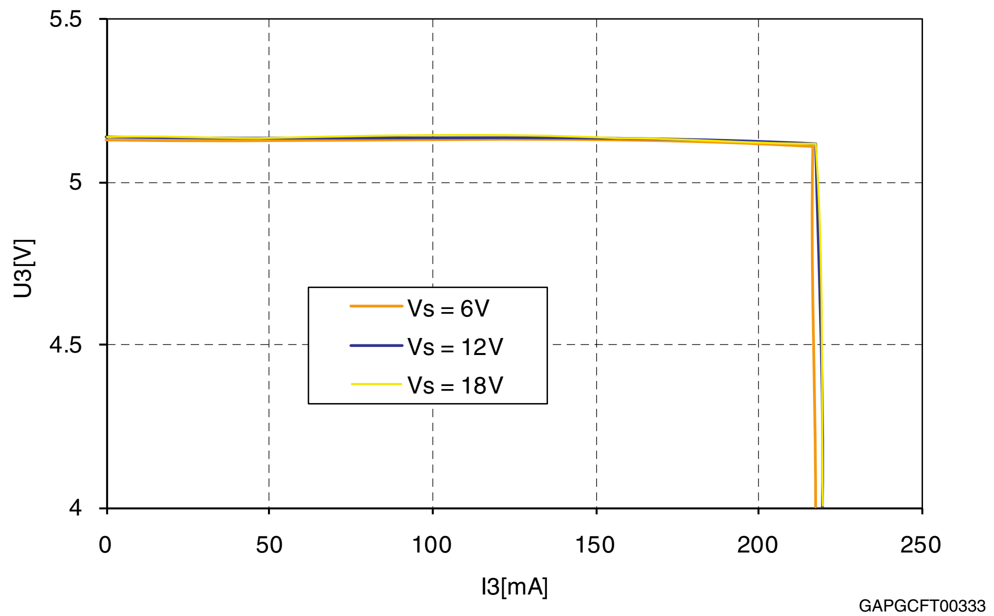
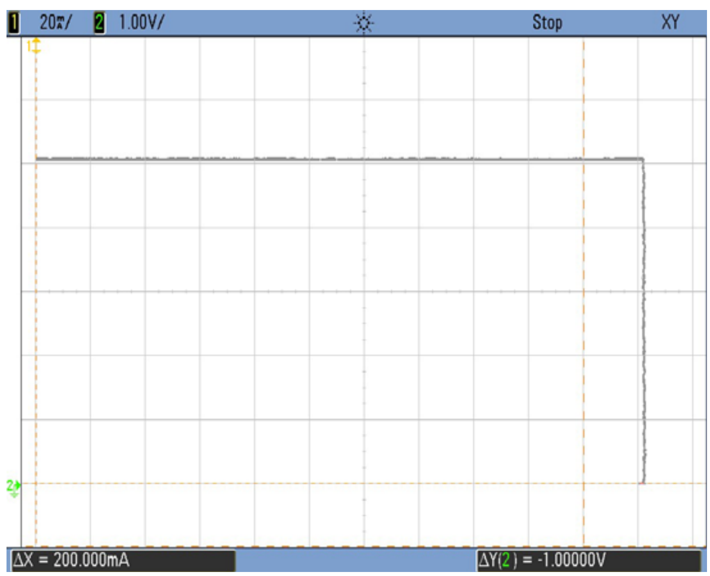


Figure 8. Screenshot of load regulation (from 0 to 220 mA - current limitation)



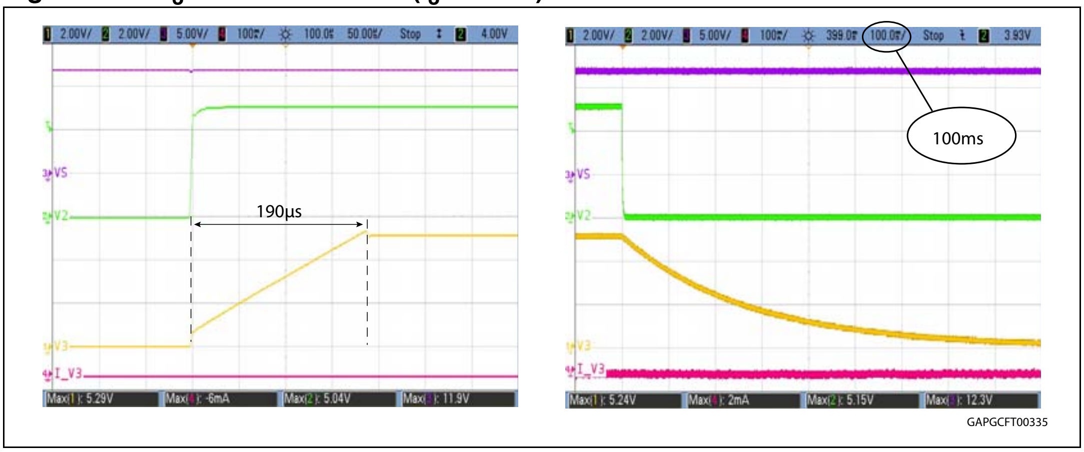
2.2 Dynamical characteristics

2.2.1 V_3 switching ON / OFF

The V_3 voltage regulator switching ON / OFF by turning ON / OFF reference - the 5V2 voltage regulator. All measurements were done for circuit from *Figure 4: Voltage regulation* *and current limitation with external NPN*.

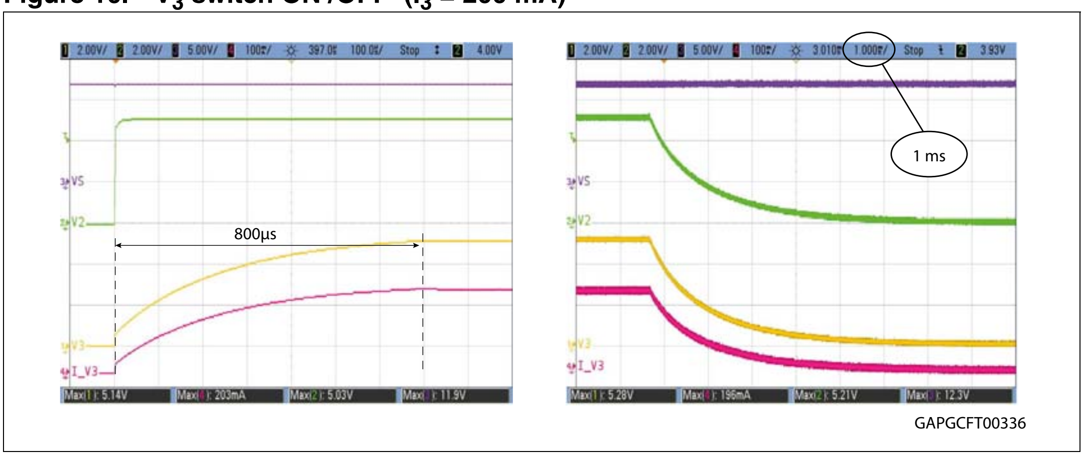
- R_1, R_2, R_3, R_4, R_5 = 10 K
- V_S = 12 V
- I_3 from 0 to 200 mA and short circuit
- Temperature = 25 °C ambient
- Switching = V_3 to open load:

Figure 9. V_3 switch ON / OFF (I_3 = 0 mA)



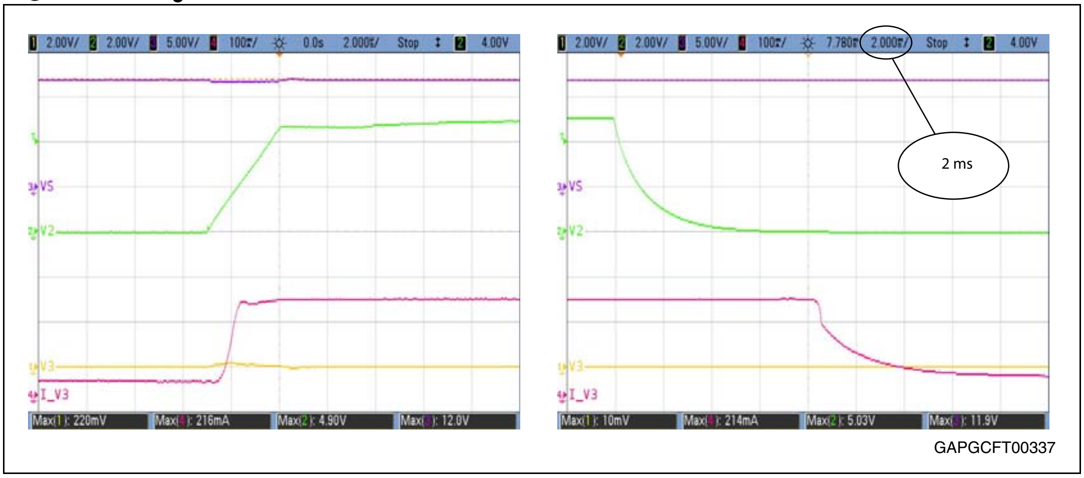
Switching V_3 with resistive load 25 Ω, (200mA @ 5 V)

Figure 10. V_3 switch ON /OFF (I_3 = 200 mA)



Switching V_3 to short circuit. The current protection circuit limits current to 220 mA.

Figure 11. V_3 switch ON /OFF to shortcut

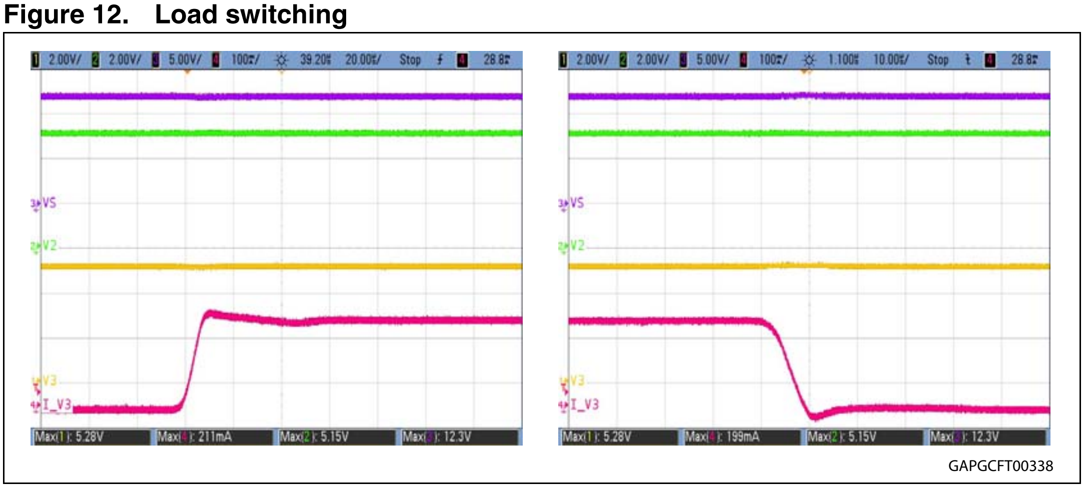


2.2.2 Load switch ON/OFF

Measurements were done for circuit from *Figure 4*. As load an electronically controlled load was used with following preset parameters:

- R_1, R_2, R_3, R_4, R_5 = 10 K
- Device type = Chroma 63103
- Mode = constant current low
- Current = 200 mA
- Slope = 250 mA/µs (falling and rising)

Figure 12. Load switching



2.2.3 Influence of C_i and C_1 on the V_3 switch and load variation response

For the circuit from *Figure 4* the influence of capacitors C_i and C_1 to the regulator switching ON/OFF response for V_3 output open load and 25 Ω load (200 mA @ 5 V) were tested.

The influence to the load regulation by switching ON / OFF load of 200 mA (electronic controlled load was used for these tests) were also tested.

The capacitors influence was tested on following combinations C_i and C_1:

Table 3. Capacitors combinations

Combination	C_i [nF]	C_1 [µF]
1	0	0
2	1n	0
3	10n	0
4 - default	0	10M
5	1n	10M
6	10n	10M

Figure 13. Combination n°1 - I_3 = 0; I_3 = 200 mA

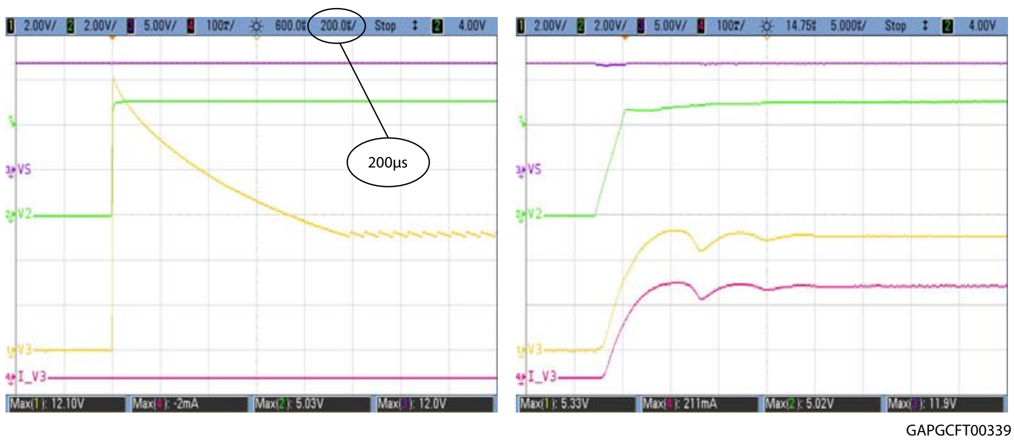


Figure 14. Combination n°1 - C_i = 0; C_1 = 0; load switch ON

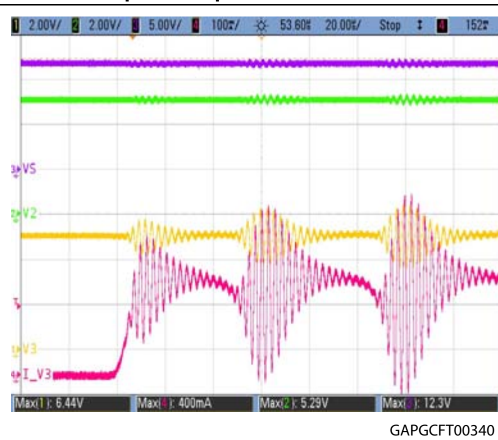


Figure 15. Combination n°2 - I_3 = 0; C_i = 1 nF; C_1 = 0

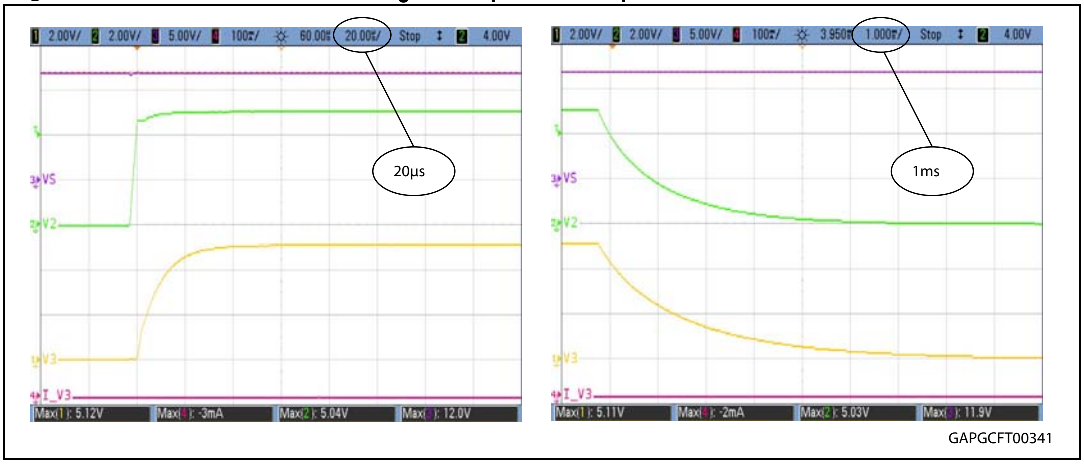


Figure 16. Combination n°2 - I_3 = 200 mA; C_i = 1 nF; C_1 = 0

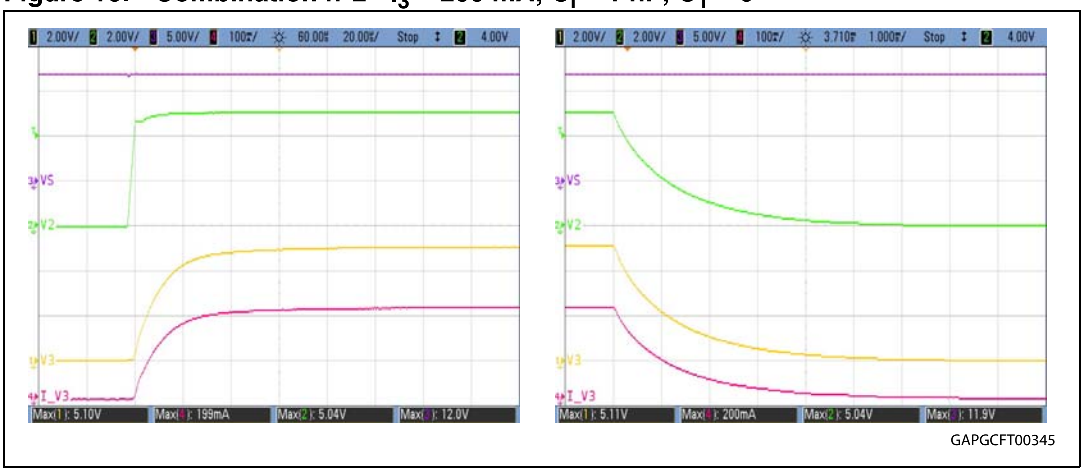


Figure 17. Combination n°2 - C_i = 1 nF; C_1 = 0; load switch ON/OFF

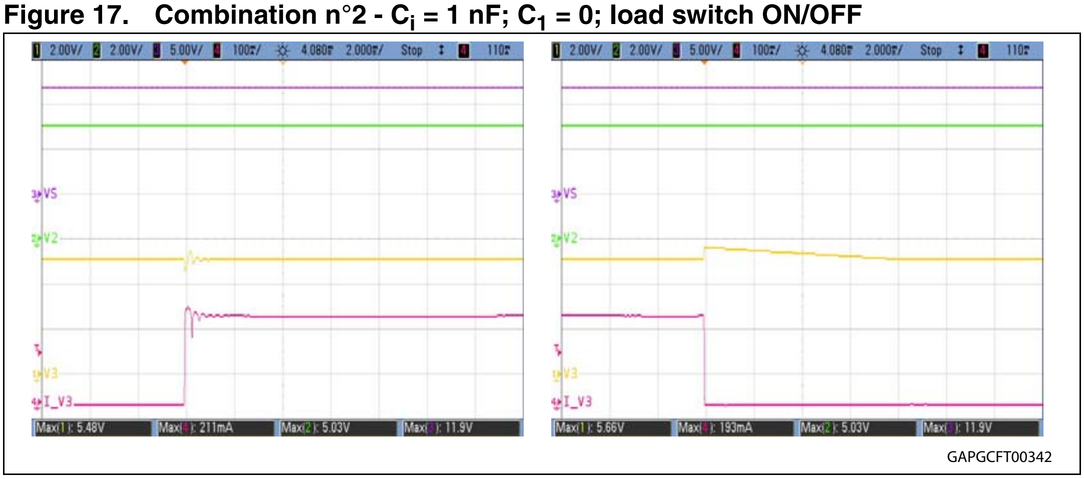


Figure 18. Combination n°3 - I_3 = 0; C_i = 10 nF; C_1 = 0

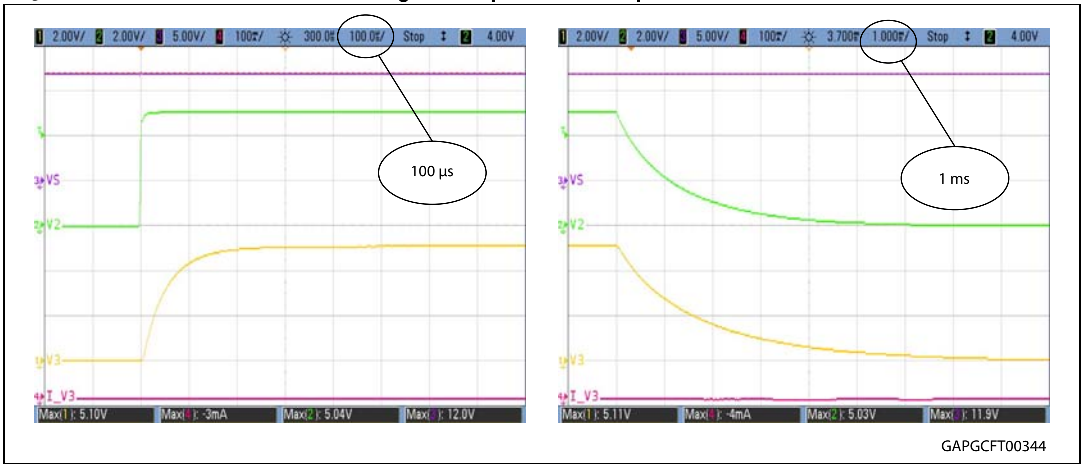


Figure 19. Combination n°3 - I_3 = 200 mA; C_i = 10 nF; C_1 = 0

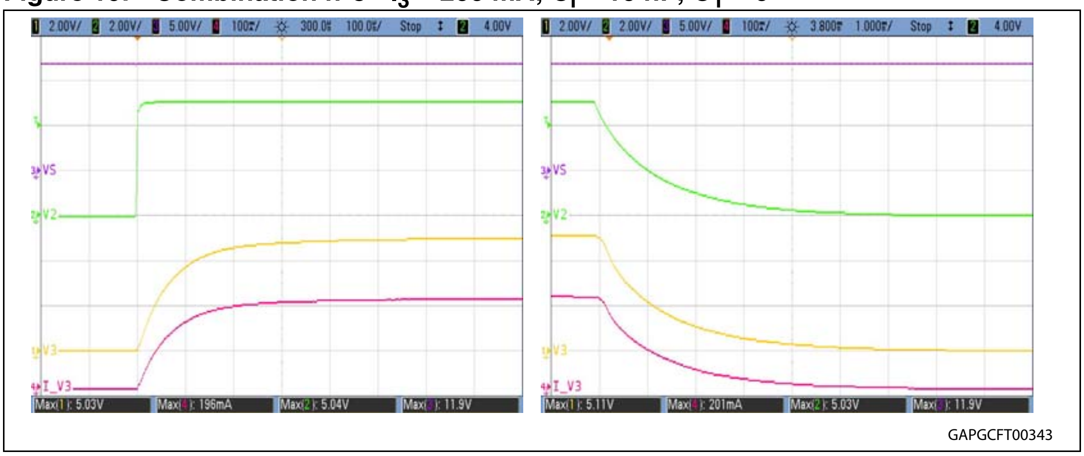


Figure 20. Combination n°3 - C_i = 10 nF; C_1 = 0; load switch ON/OFF

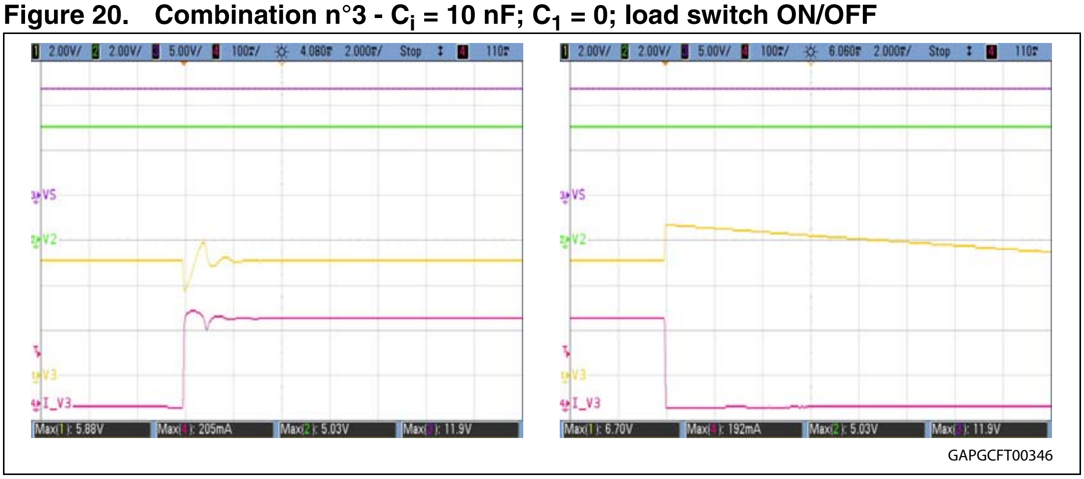


Figure 21. Combination n°5 - I_3 = 0; C_i = 1 nF; C_1 = 10 µF

Figure 22. Combination n°5 - I_3 = 200 mA; C_i = 1 nF; C_1 = 10 µF

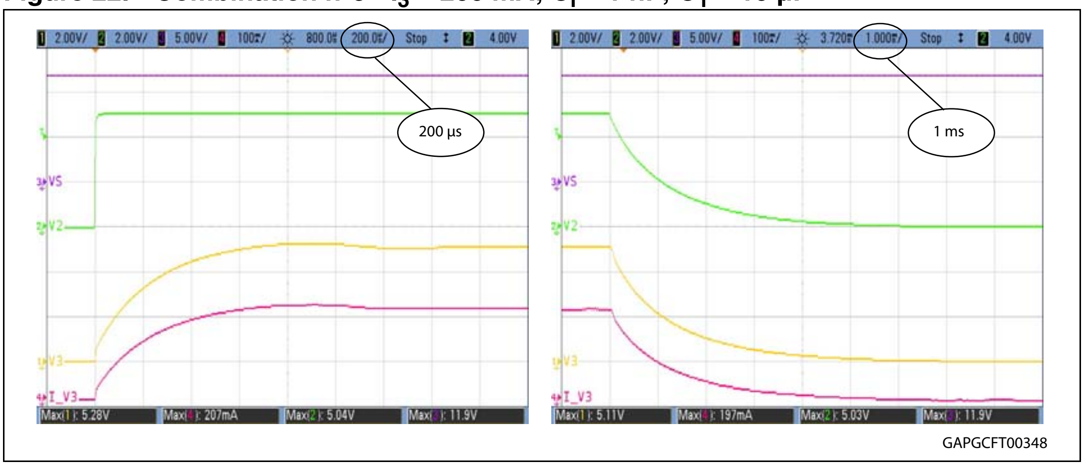


Figure 23. Combination n°5 - C_i = 1 nF; C_1 = 10 µF; load switch ON/OFF

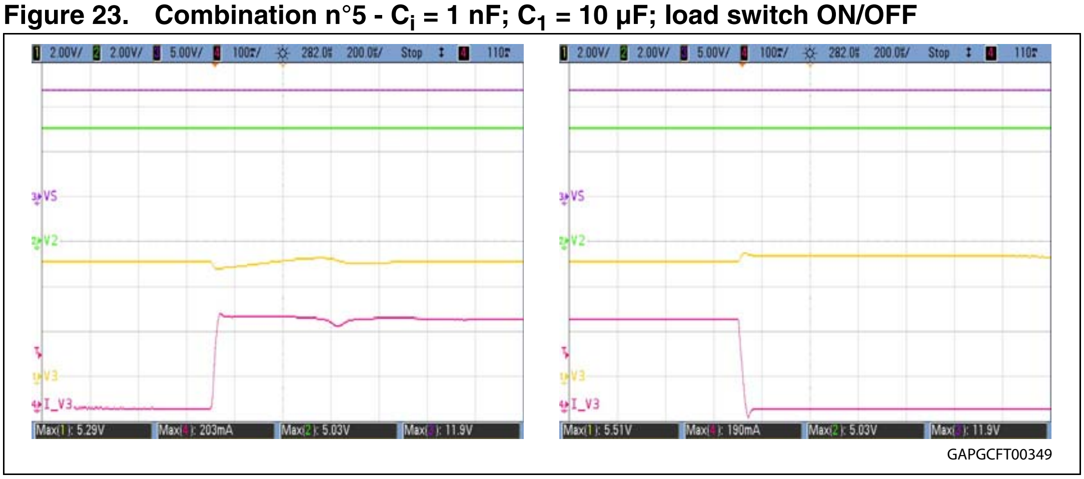


Figure 24. Combination n°6 - $I_3 = 0$; $C_i = 10$ nF; $C_1 = 10$ µF

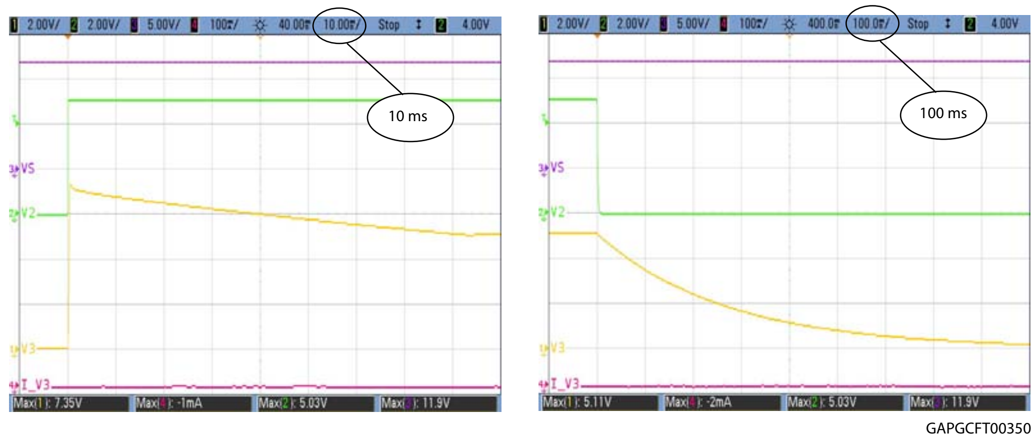


Figure 25. Combination n°6 - $I_3 = 200$ mA; $C_i = 10$ nF; $C_1 = 10$ µF

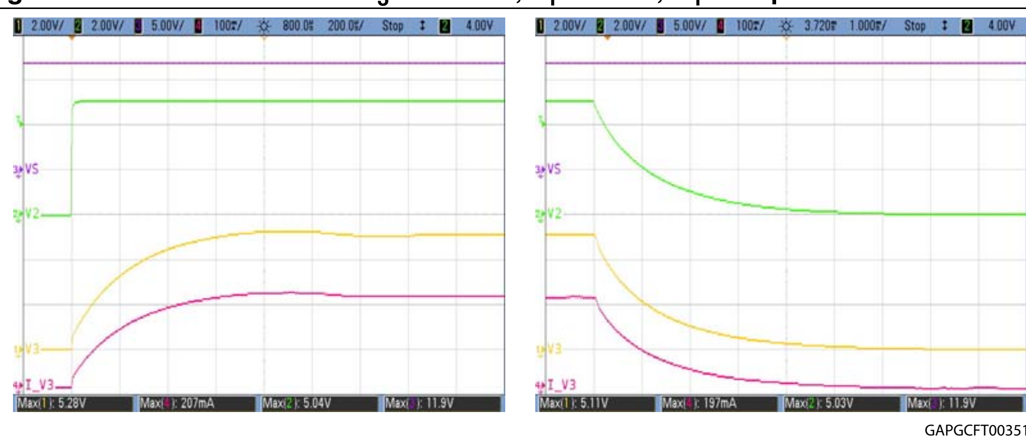
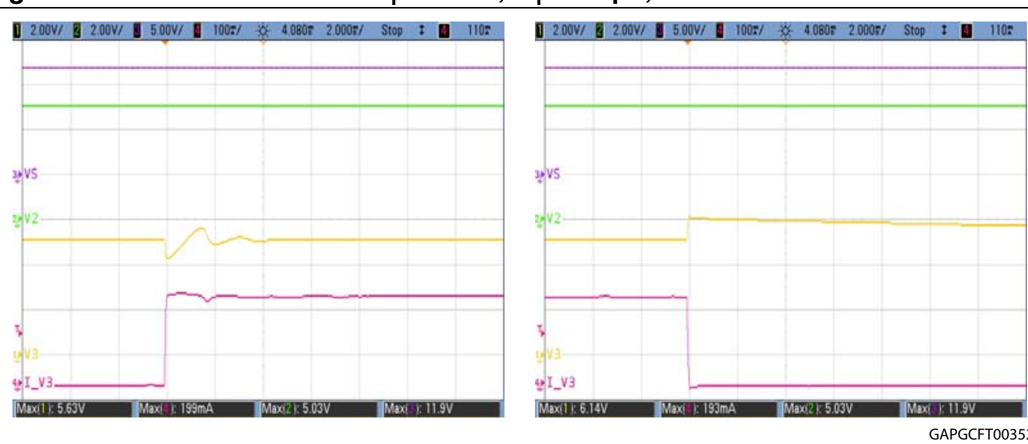


Figure 26. Combination n°6 - $C_i = 10$ nF; $C_1 = 10$ µF; load switch ON/OFF



2.2.4 V_S cranking measurement

Screenshots of behavior in case of V_S cranking pulse for various pulse widths are at the next figures. In case V_S reaches level for POR the V_2 is switched off and as a consequence V_3 is switched off as well.

Figure 27. V_S cranking (1 ms pulse)

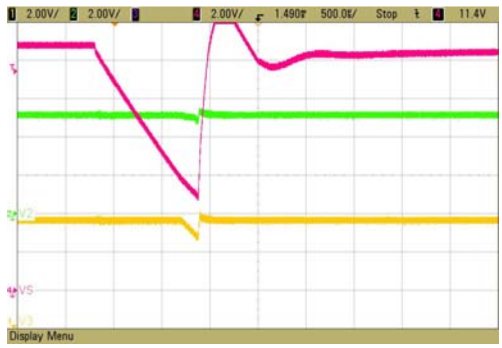


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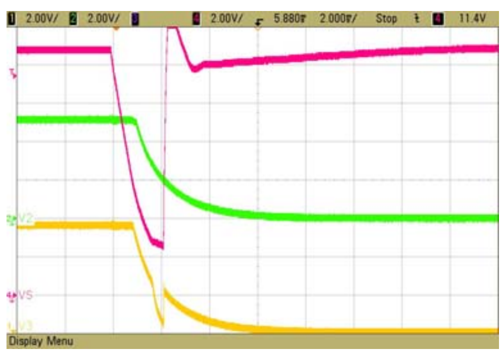
Figure 27 is a screenshot of V_S cranking pulse 1 ms width. The V_S under-voltage flag was set in status register, but V_2 remains ON.

Figure 28. V_S cranking (pulse 2 ms)



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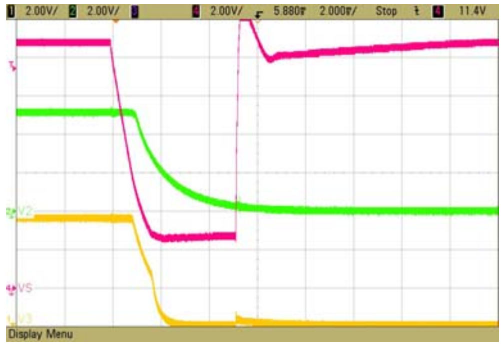
On *Figure 28* V_S reaches the level of power on reset. V_2 was switched OFF and cold start diagnosis bit was signalized in status registers.

Figure 29. V_S cranking (pulse 5 ms)



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Appendix A Reference document

1. Power management IC with LIN and high speed CAN (L99PM62GXP, Doc ID 17639)

Revision history

Table 4. Document revision history

Date	Revision	Changes
19-May-2011	1	Initial release.
19-Sep-2013	2	Updated Disclaimer.