AN3981
Application note

LED array drivers

Introduction

The use of LEDs in applications like displays, information and advertising panels, signs, traffic signals, automotive lighting and architectural lighting is becoming more and more common.

LED array drivers, with accurate constant current regulation and embedded serial interfaces, offers a solution that is suitable for most of the above mentioned applications.

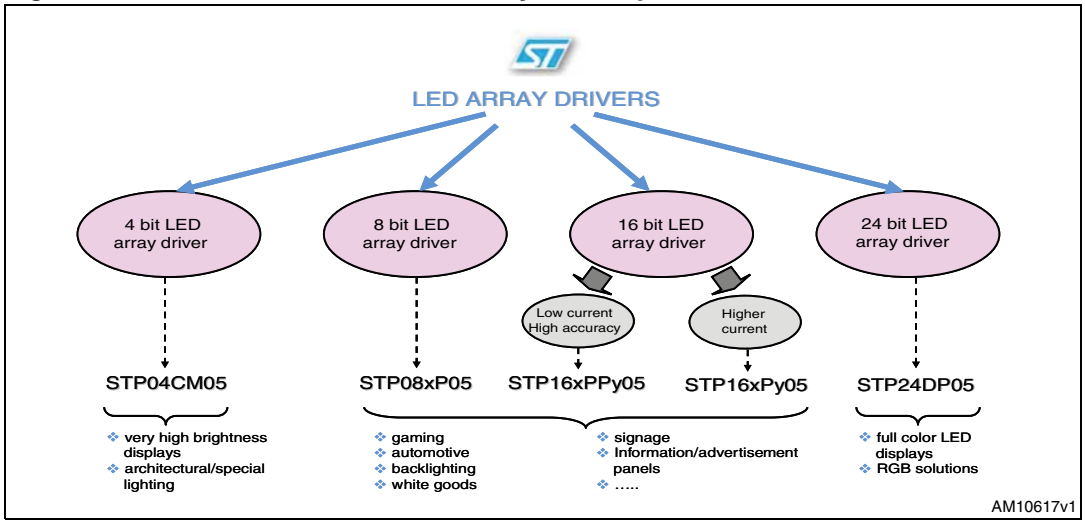
This document provides an overview of the STMicroelectronics portfolio of LED array drivers.

According to the application, some specific features may be relevant:

- Brightness adjustment through PWM dimming
- Very high current accuracy
- Diagnostic capability to detect faulty LEDs
- Low power consumption

Moreover, the choice of the most appropriate product is driven also by the array length (number of LED current generators), the LED current, type of LED (single color or RGB), etc.

Figure 1. STMicroelectronics LED array drivers portfolio



The wide variety of STMicroelectronics LED array drivers allows the selection of a dedicated solution for a certain application. STMicroelectronics portfolio is summarized in *Figure 1*. The following sections describe all the product family main features.

Furthermore, the document focuses on the guidelines that ease the use of these products in the final application and also provides some particular application ideas.

Contents

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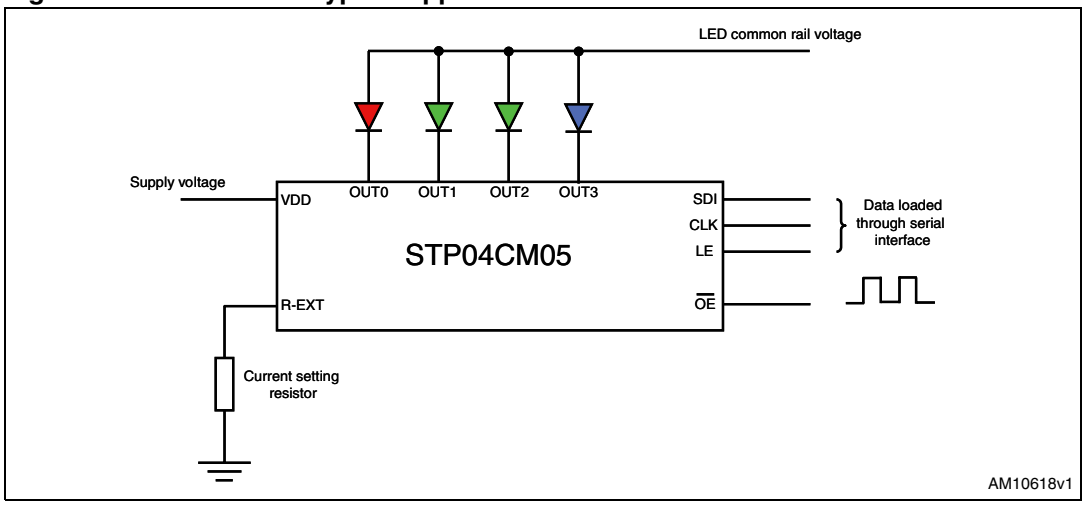
1 STP04CM05 - 4-bit LED array driver

1.1 Main features

- Four constant current output channels
- Adjustable output current from 80 mA to 400 mA through an external resistor
- 20 V current generators rated voltage
- Supply voltage from 3.3 V to 5.5 V.

Figure 2. STP04CM05 typical application circuit



1.2 Applications

The possibility to set a current up to 400 mA per channel makes this product suitable for those applications where high power LEDs are the preferred solution.

Very high brightness display and architectural and special lighting (mood lighting) are common examples of the use of the STP04CM05.

1.3 Block diagram

Figure 3 represents the block diagram of the STP04CM05.

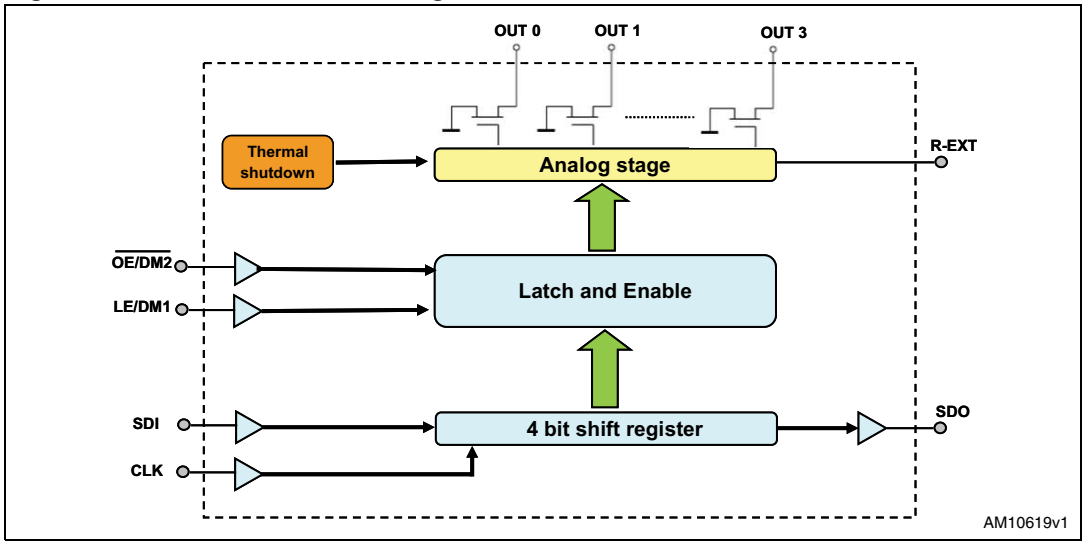
The 4-bit shift register contains the digital data loaded through the SDI pin. The “Latch and Enable” block contains the digital word loaded from the 4-bit shift register once the LE pulse has been detected.

The “Analog stage” represents the circuitry to drive each current generator consistently with the digital word contained in the “Latch and Enable” block, setting the correct current in accordance with the resistor connected to the REXT pin. This block is enabled by the $\overline{OE}$ pin.

The Thermal shutdown block monitors the junction temperature and switches the current generators off if this temperature goes over the thermal shutdown threshold (typically 170 °C), independent to the actual status of the generators. The generators go back to the

previous status if the junction temperature falls, typically 15-20 °C, below the thermal shutdown threshold.

Figure 3. STP04CM05 block diagram



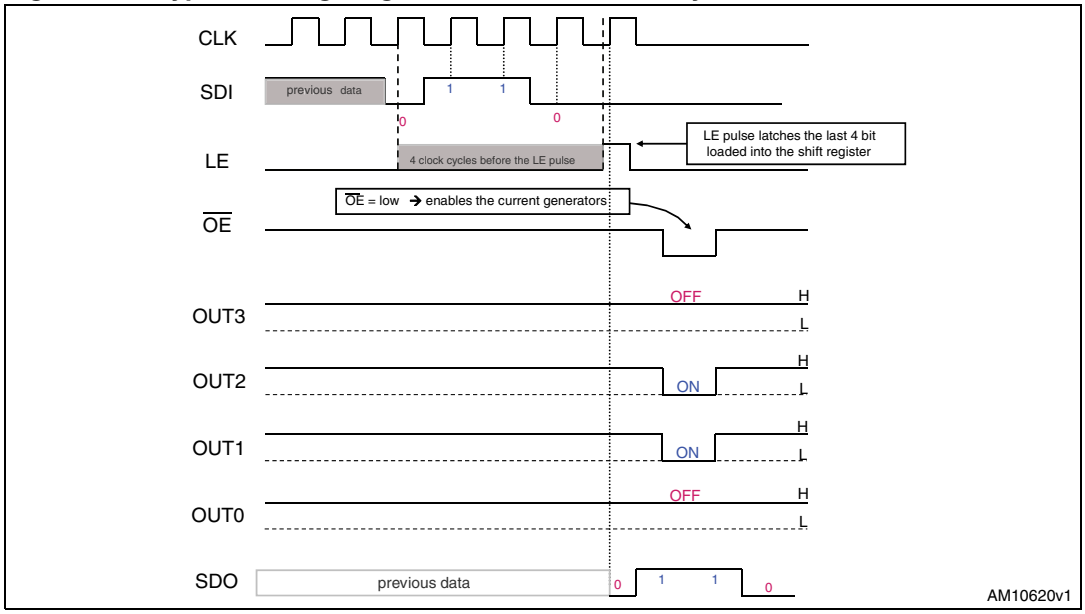
1.4 SPI data sending

Figure 4 shows a typical timing diagram of a 4-bit LED driver.

The LE pulse latches the last 4 bits loaded into the shift register through the SDI pin and sampled by the last 4 clock rising edges.

As long as the $\overline{OE}$ pin is high, all current generators are not active. Once $\overline{OE}$ is set low, the current generators are enabled and their status is determined by the data latched by the last LE pulse.

Figure 4. Typical timing diagram for a 4-bit LED array driver



1.5 Current setting

The output current of all channels can be programmed through one external resistor in the range 80-400 mA.

The choice of the resistor value can be made using the curve below (*Figure 5*) or using the following formula:

Equation 1

$$R_{EXT} = \left(\frac{V_{REF}}{I_{OUT}}\right) \cdot 64$$

where V_{REF} = 1.25 V.

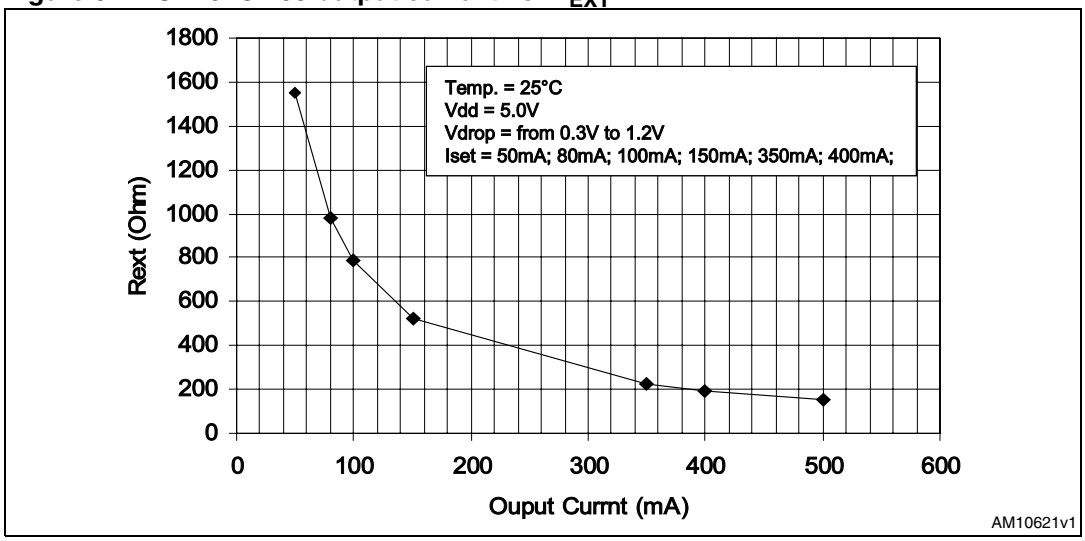
For example, if a current of 100 mA per channel must be programmed, according to *Equation 1*, the external resistor value is:

Equation 2

$$R_{EXT} \cong \left(\frac{1.25}{0.1}\right) \cdot 64 \quad = 800\Omega$$

The STP04CM05 is characterized by a high current accuracy between channels (typically ±1%, maximum ±1.5%). The current accuracy between chips is maximum ±6%.

Figure 5. STP04CM05 output current vs. R_{EXT}



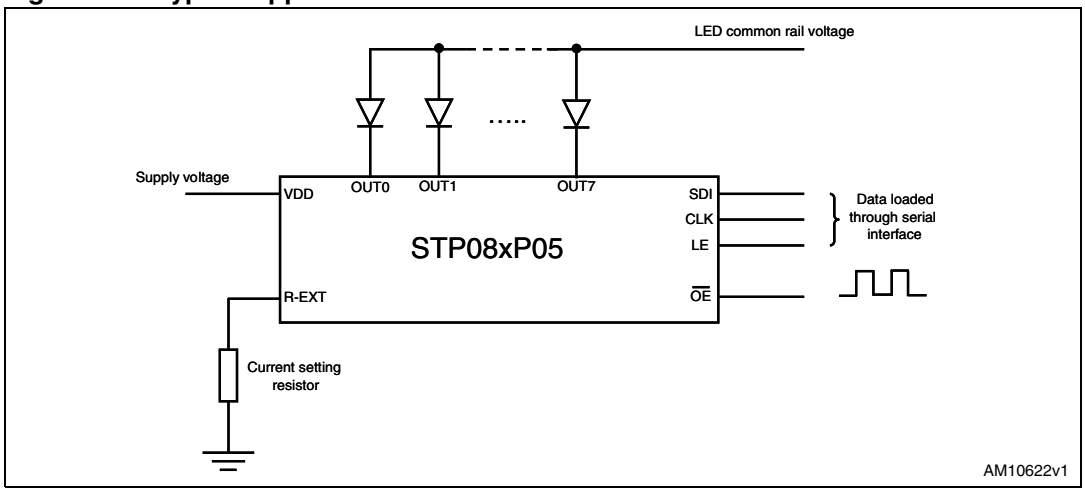
2 8-bit LED array drivers

2.1 Main features

The 8-bit LED array driver family is composed of two products: the STP08CP05 and STP08DP05.

- Eight constant current output channels
- Adjustable output current from 5 to 100 mA through an external resistor
- Short and open output error detection (only for the STP08DP05)
- 20 V current generators rated voltage
- Supply voltage from 3.3 V to 5.5 V.

Figure 6. Typical application circuit for STP08xP05 devices



2.2 Applications

This family is suitable for several applications in different market segments, such as gaming machines, white goods, LED signage, and automotive LED lighting.

2.3 Block diagram

Figure 7 represents the block diagram valid for the 8-bit LED array driver family.

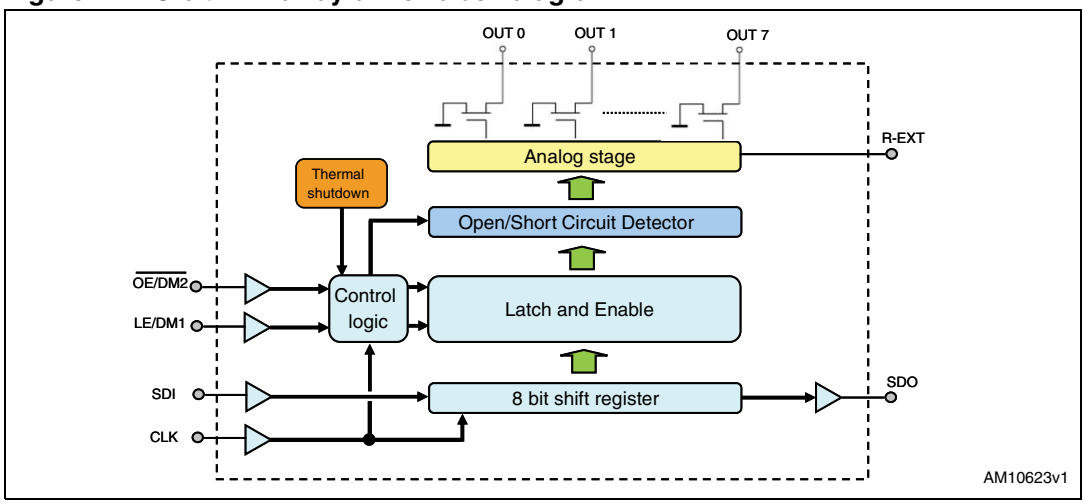
The 8-bit shift register contains the digital data loaded through the SDI pin. The “Latch and Enable” block contains the digital word loaded from the 8-bit shift register once the LE pulse has been detected.

The “Analog stage” represents the circuitry to drive each current generator consistently with the digital word contained in the “Latch and Enable” block, setting the correct current in accordance with the resistor connected to the REXT pin. This block is enabled by the $\overline{OE}$ pin.

The “Control logic” block decodes the signal sequence provided to the LE and $\overline{OE}$ pin for entering and ending the error detection, performed by the block “Open/Short-Circuit Detector”.

The Thermal shutdown block monitors the junction temperature and switches the current generators off if this temperature goes over the thermal shutdown threshold (typically 170 °C), independent to the actual status of the generators. The generators go back to the previous status if the junction temperature falls, typically 15-20 °C, below the thermal shutdown threshold.

Figure 7. 8-bit LED array driver block diagram



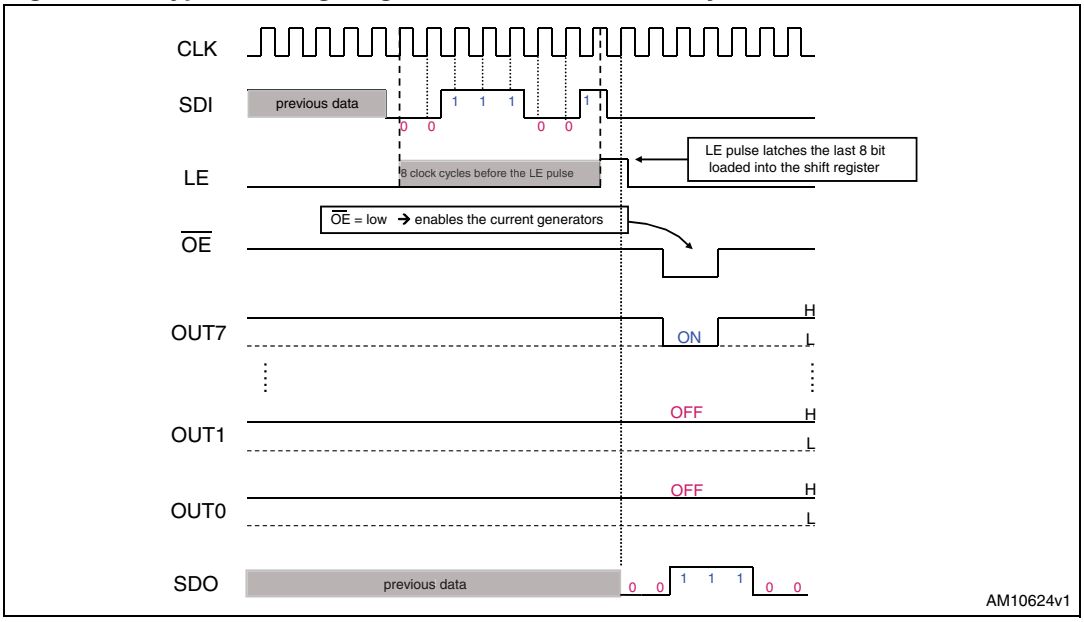
2.4 SPI data sending

Figure 8 shows a typical timing diagram of an 8-bit LED driver.

The LE pulse latches the last 8 bits loaded into the shift register through the SDI pin and sampled by the last 8 clock rising edges.

As long as the $\overline{OE}$ pin is high, all current generators are not active. Once $\overline{OE}$ is set low, the current generators are enabled and their status is determined by the data latched by the last LE pulse.

Figure 8. Typical timing diagram for an 8-bit LED array driver



2.5 Current setting

The output current of all channels can be programmed through one external resistor in the range 5-100 mA. The choice of the resistor value can be made using the curve below (*Figure 9*) or using the following formula:

Equation 3

$$R_{EXT} = \left(\frac{V_{REF}}{I_{OUT}}\right) \cdot 16$$

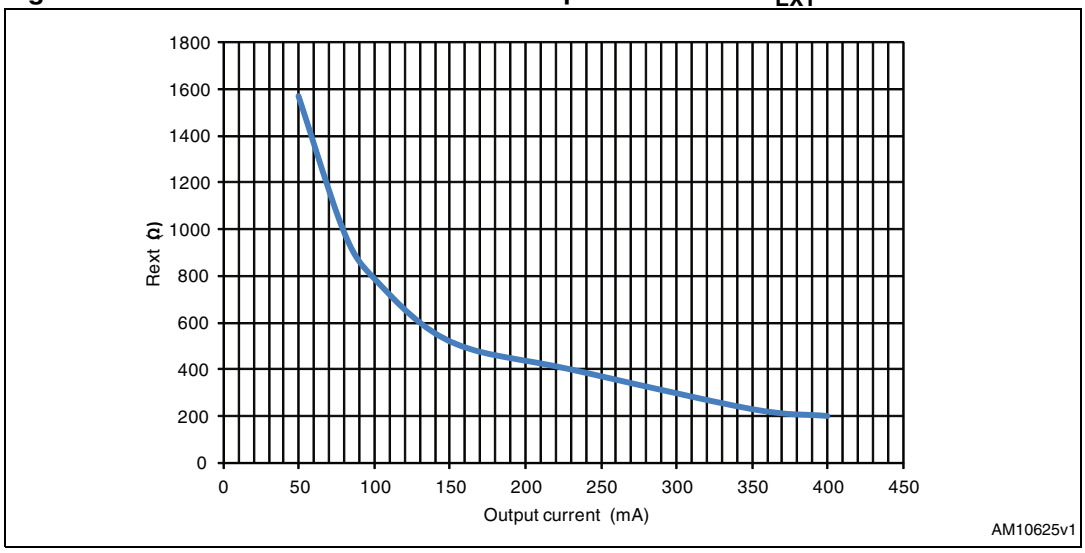
where V_{REF} = 1.25 V.

For example, if a current of 20 mA per channel must be programmed, according to *Equation 1*, the external resistor value is:

Equation 4

$$R_{EXT} \cong \left(\frac{1.25}{0.02}\right) \cdot 16 = 1k\Omega$$

Figure 9. STP08CP05 and STP08DP05 output current vs. R_{EXT}



The current accuracy of both the STP08CP05 and STP08DP05 is typically ±1.5% between channels and a maximum of ±3% chip-to-chip.

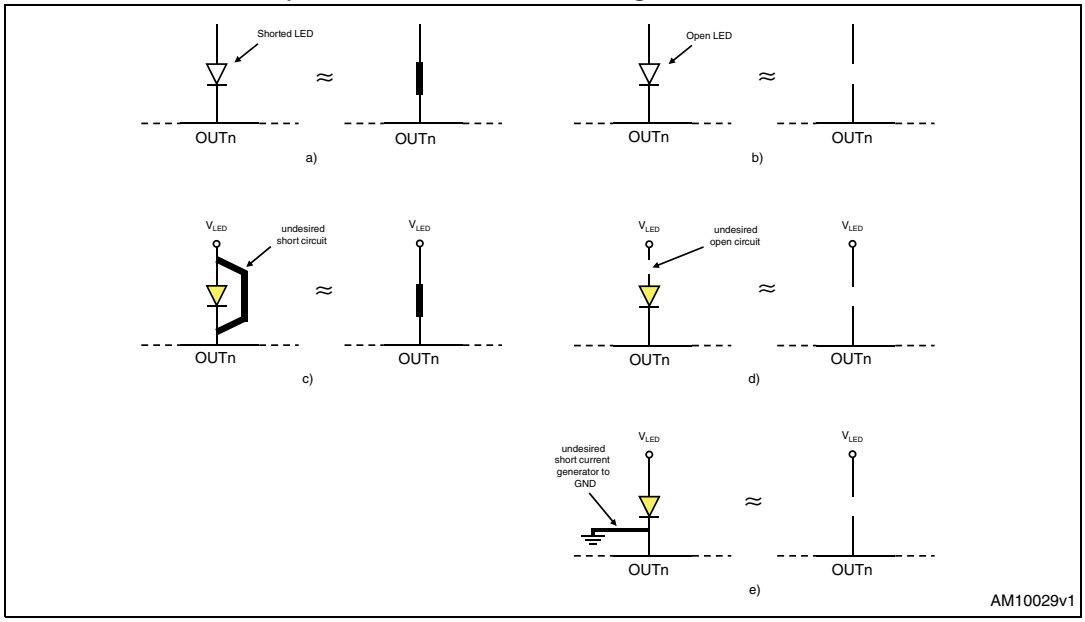
2.6 Error detection

The meaning of “error detection” is the detection of the faulty conditions that may occur on each channel due to:

- the LED, which can be damaged and behaves abnormally as a short or open circuit
- any undesired event that can prevent the LED from working correctly (interruption of the PCB - printed circuit board - trace connecting the LED to V_{LED} or to the current generator, short-circuit from current generator to ground or V_{LED}).

All these possible events are summarized in *Figure 10*.

Figure 10. Fault conditions detected by error detection mode: a) shorted LED; b) open LED; c) short-circuit from current generator to V_{LED}; d) open channel; e) short-circuit from current generator to GND



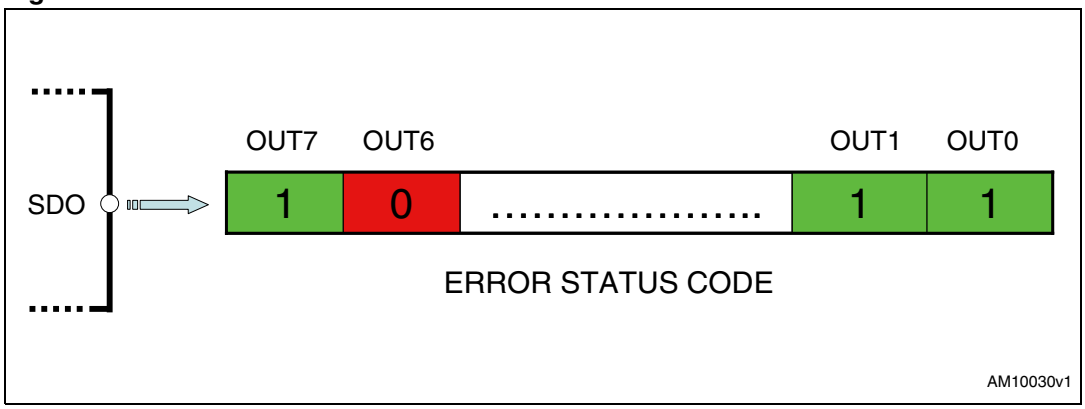
The diagnostic circuitry embedded in the STP08DP05 can detect these faulty conditions (in accordance with the detection thresholds of *Table 1*) and provide the results of the detection as an “Error status code” coming out of the SDO pin (see *Figure 11*), with “0” logic level indicating a faulty channel, whereas a “1” logic level indicates a “good” channel.

Table 1. Detection conditions

Detection conditions	Detection result
I_{ODEC}(1) = 0.5·I_O(2)	Open channel or output short to GND detected
I_{ODEC} = 0.5·I_O	No error detected
V_O = 2.5 V	LED short-circuit or LED shorted to supply voltage
V_O = 2.2 V	No error detected

1. I_{ODEC} is the detected output current in detection mode.
2. I_O is the programmed output current.

Figure 11. Error status code



The error detection process can be divided into three phases:

1. Entering detection mode. From “normal mode” the device can enter “error mode” through a logic key (*Figure 12*), which is a logic sequence of the $\overline{OE/DM2}$ and LE/DM1 signals over five CLK cycles. After these five CLK cycles, the device is in “error detection mode” and ready for sampling data on the SDI pin
2. Error detection. Once the device has entered “error detection mode”, an 8-bit string should be loaded into the shift register through the SDI pin in order to set the outputs in accordance with the diagnostic demands (only the outputs that are on are checked by the error detection process). Therefore, if the user wants to check all the outputs, a string with all “1” must be sent. After that the outputs are ready for the detection process, which starts when $\overline{OE/DM2}$ is set low. The device drives LEDs in order to analyze if an open or short condition has occurred. The $\overline{OE/DM2}$ must remain low for at least 1 µs to complete the detection process. As shown in *Figure 14*, during the detection process, at least three clock pulses are necessary: two pulses as soon as the $\overline{OE/DM2}$ is set low, and one clock pulse before ending the detection process. Once the $\overline{OE/DM2}$ is set high, the error status code is available at the SDO pin. To download the complete error string, at least 8 clock pulses are necessary
3. Resuming normal mode. The device quits detection mode and returns to normal mode through an exit logic key (*Figure 13*), a logic sequence over five clock pulses.

Figure 12. Digital key for entering error detection mode in 8-bit LED drivers

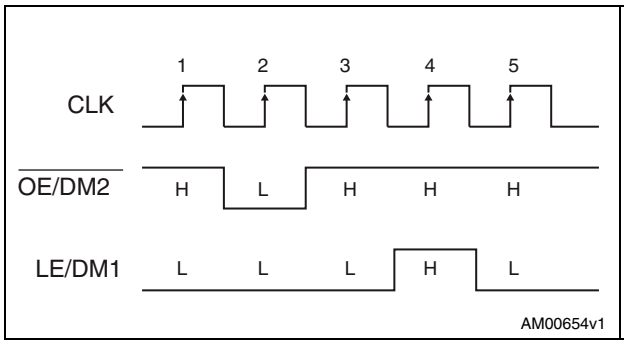
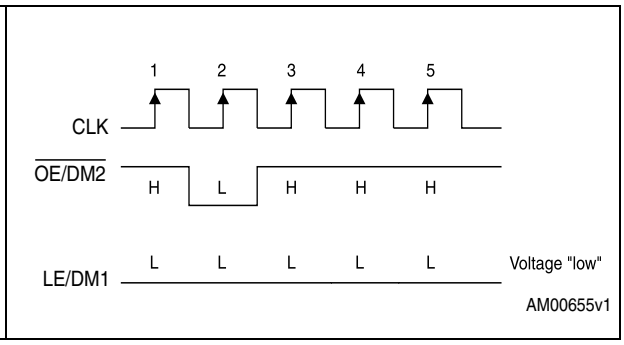


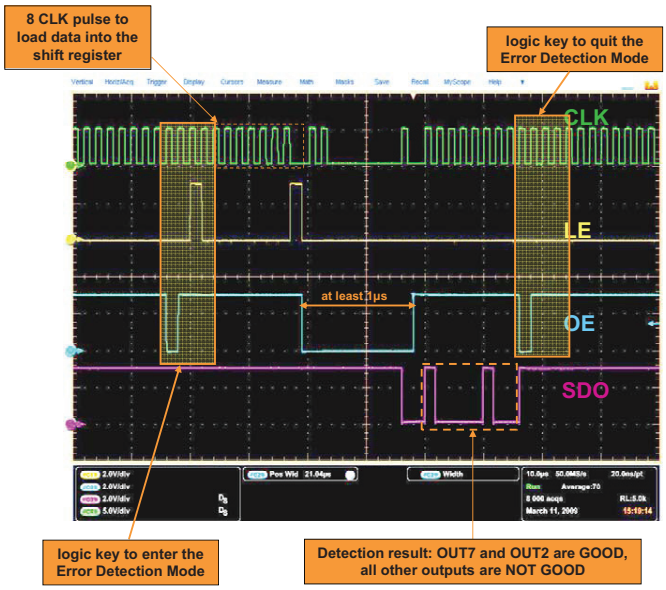
Figure 13. Digital key for exiting error detection mode in 8-bit LED drivers



For proper device operation, the entering sequence must be followed by a resuming sequence as it is not possible to insert consecutive equal sequences.

Figure 14 shows an example of error detection where OUT7 and OUT2 are good, whereas all other outputs are considered faulty.

Figure 14. Example of error detection with OUT7 and OUT2 good and all other outputs faulty



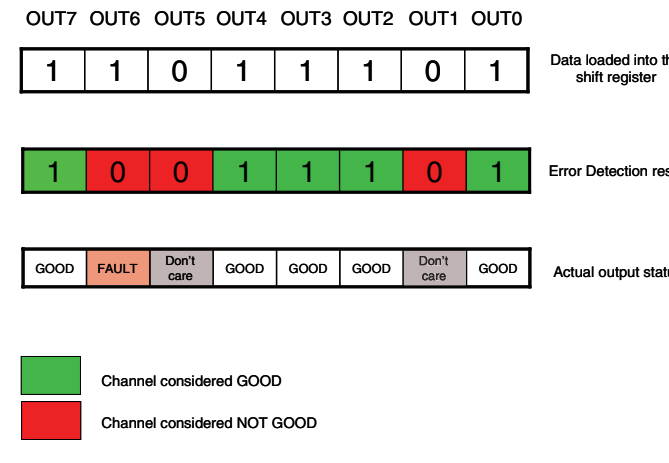
2.6.1 Correctness of the error detection results

It is important to underline that the result of the diagnostic process must be compared with the data loaded into the shift register.

In fact, if a channel is not switched on, the result of the detection is “0” anyway.

It is recommended to follow the approach shown in *Figure 15*.

Figure 15. Error detection results interpretation

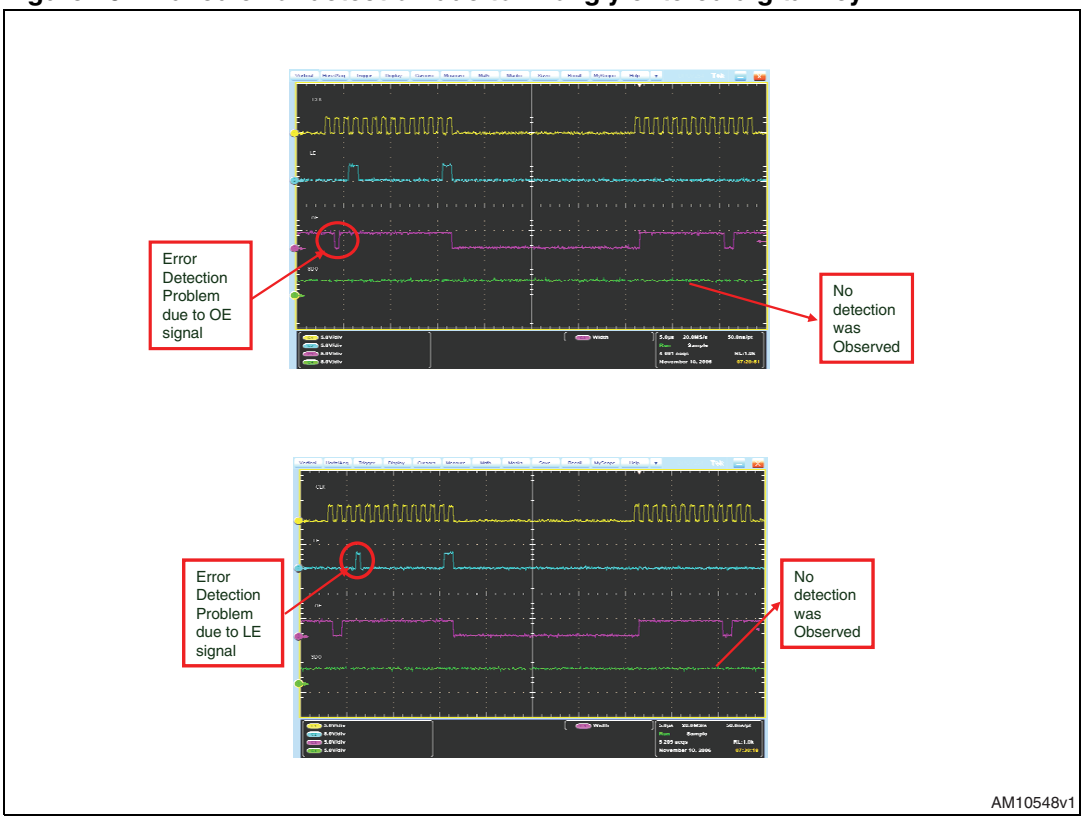


The correct interpretation of the detection results can be affected by any setup/hold time problem. For this reason it is recommended to synchronize all signals with the falling edge of the CLK signal.

If this is not possible, it is advisable to start the $\overline{OE}$ signal (for example) typically 20 ns after the rising edge of the CLK signal.

Figure 16 shows a typical problem in error detection mode due to the wrong digital key: the device does not recognize it (due to an incorrect $\overline{OE}$ timing or LE timing), no error detection is performed, so data coming out of the SDO pin does not represent the error status code, as expected.

Figure 16. Failed error detection due to wrongly entered digital key



Another incorrect result of the error detection can occur if the choice of the LED supply voltage is not appropriate. The rules to suitably define the LED supply voltage are discussed in *Section 5.1*.

3 16-bit LED array drivers

3.1 Main features

The 16-bit LED array driver family contains several products with the following common features:

- Sixteen constant current output channels
- Adjustable output current through an external resistor (current ranges indicated in *Table 2* below)
- Error detection (only some devices, see *Table 2*)
- Auto shutdown and auto wake-up functions (only some devices, see *Table 2*)
- 20 V current generators rated voltage
- Supply voltage from 3.3 V to 5.5 V.

Figure 17. Typical application circuit for STP16xPyy05 devices

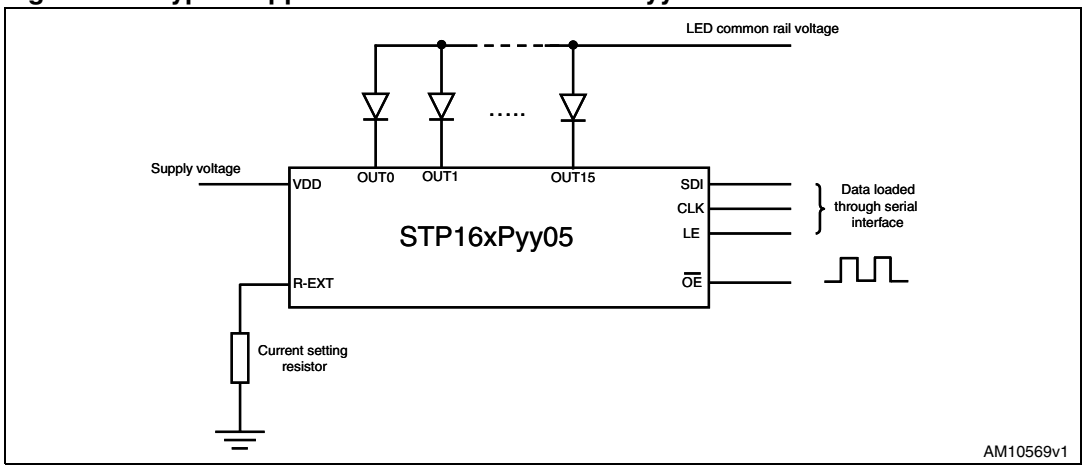


Table 2 provides a general overview of the products belonging to this family.

Table 2. 16 bit LED array driver overview

P/N	I_{LED} [mA]	Error detection	Auto shutdown	Balanced T_{ON}/T_{OFF}
STP16CP05	5÷100			
STP16CPC05	5÷100			•
STP16CPP05	3÷40			
STP16CPS05	5÷100		•	
STP16CPPS05	3÷40		•	
STP16DP05	5÷100	•		
STP16DPP05	3÷40	•		
STP16DPS05	5÷100	•	•	
STP16DPPS05	3÷40	•	•	
STP16CPC26	3÷90			•(1)

1. almost balanced, see dedicated section

3.2 Applications

Considering the large number of features this family can offer, the applications where these products can be used are numerous: large displays for advertisements or information, white goods, LED signage, traffic signals, gaming machines, display backlighting, solar cells and battery supplied LED panels, etc.

3.3 Block diagram

Figure 18. 16-bit LED array driver block diagram

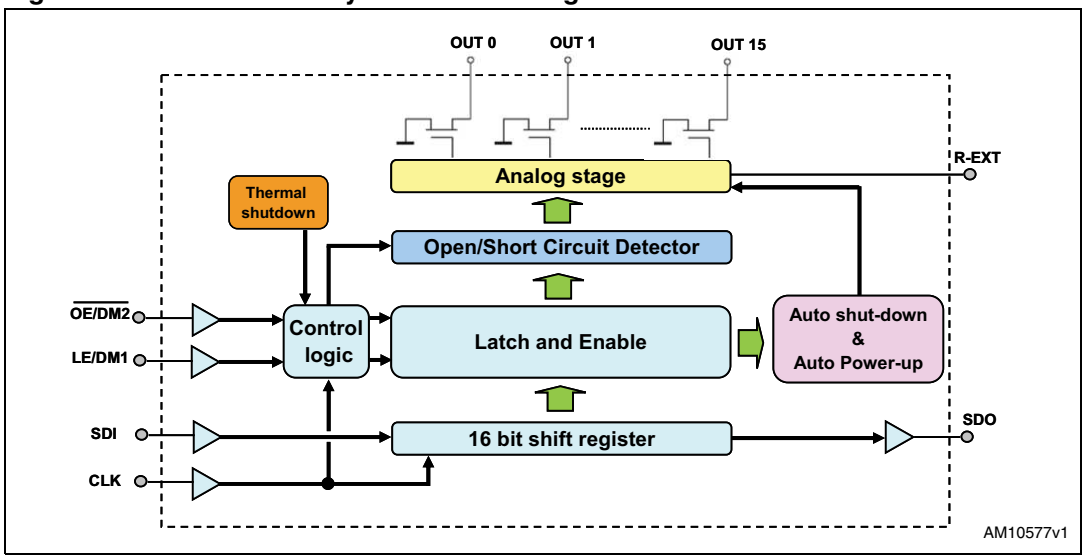


Figure 18 represents the block diagram valid for the 16-bit LED array driver family.

The16-bit shift register contains the digital data loaded through the SDI pin. The “Latch and Enable” block contains the digital word loaded from the 16-bit shift register once the LE pulse has been detected.

The “Analog stage” represents the circuitry to drive each current generator consistently with the digital word contained in the “Latch and Enable” block, setting the correct current in accordance with the resistor connected to the REXT pin. This block is enabled by the $\overline{OE}$ pin.

The “Control Logic” block decodes the signal sequence provided to the LE and $\overline{OE}$ pin for entering and ending the error detection, performed by the block “Open/Short-Circuit Detector”.

The “Auto Shutdown & Auto Power-up” (see *Section 3.7*) block monitors the current generators in order to put the device in auto shutdown (when all outputs are off) or to trigger the auto power-up (at least one output switched on again).

The Thermal shutdown block monitors the junction temperature and switches the current generators off if this temperature goes over the thermal shutdown threshold (typically 170 °C), independent to the actual status of the generators. The generators return to the previous status if the junction temperature falls, typically 15-20 °C, below the thermal shutdown threshold.

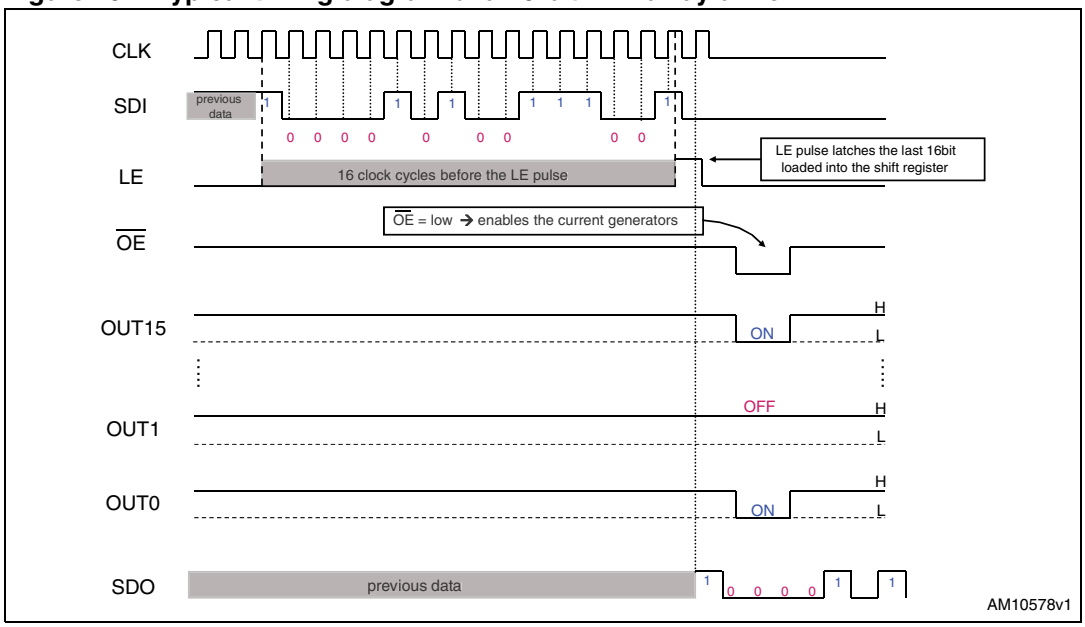
3.4 SPI data sending

Figure 19 shows a typical timing diagram of a16-bit LED driver.

The LE pulse latches the last 16 bits loaded into the shift register through the SDI pin and sampled by the last 16 clock rising edges.

As long as the $\overline{OE}$ pin is high, all current generators are not active. Once $\overline{OE}$ is set low, the current generators are enabled and their status is determined by the data latched by the last LE pulse.

Figure 19. Typical timing diagram of a 16-bit LED array driver



3.5 Current setting

The output current of all channels can be programmed through one external resistor. According to *Table 2*, some devices can regulate a current in the range 3-40 mA, whereas other devices can regulate a current from 5 mA to 100 mA. The choice of the resistor value can be made using the curve below (*Figure 20*) or using the following formula:

Equation 5

$$R_{EXT} = \left(\frac{V_{REF}}{I_{OUT}}\right) \cdot 16$$

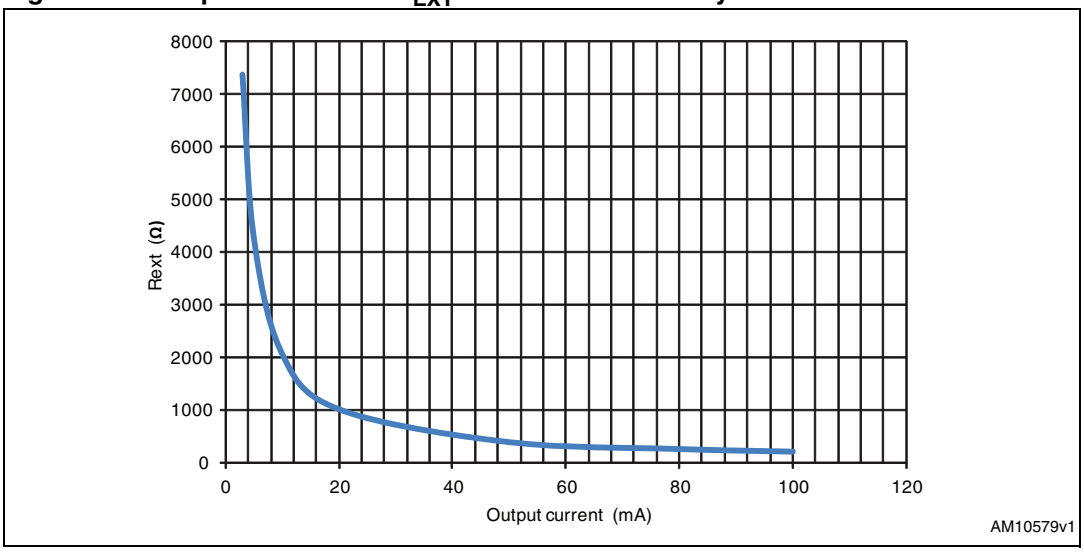
where V_{REF} = 1.25 V.

For example, if a current of 20 mA per channel must be programmed, according to *Equation 1*, the external resistor value is:

Equation 6

$$R_{EXT} \cong \left(\frac{1.25}{0.02}\right) \cdot 16 = 1\text{k}\Omega$$

Figure 20. Output current vs. R_{EXT} for a 16-bit LED array driver



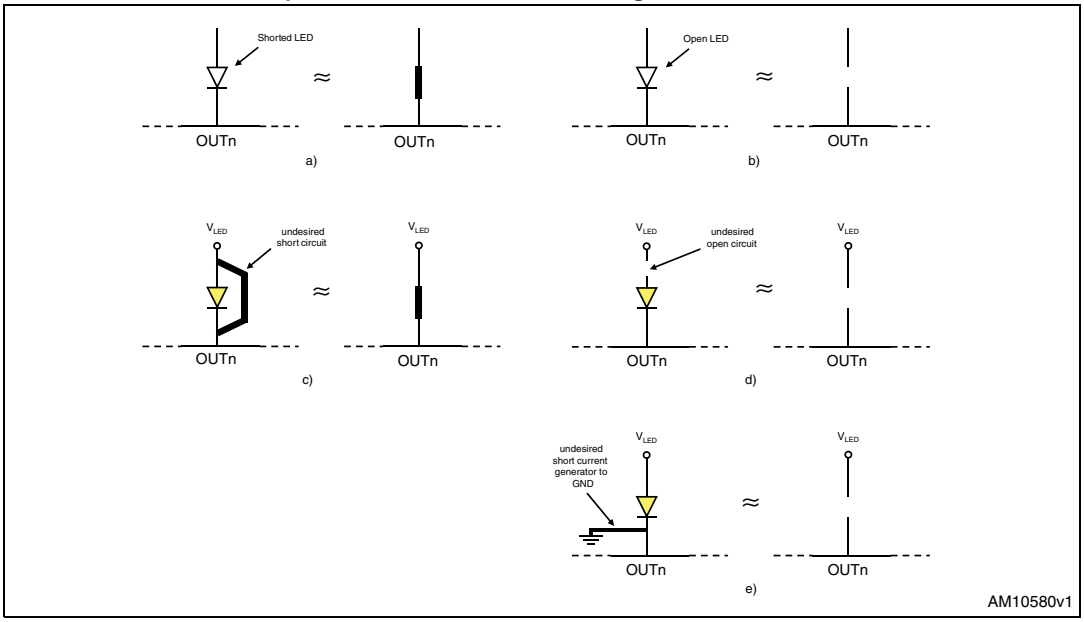
3.6 Error detection

The meaning of “error detection” is the detection of the faulty conditions that may occur on each channel due to:

- the LED, which can be damaged and behaves abnormally as a short or open circuit
- any undesired event that can prevent the LED from working correctly (interruption of the PCB - printed circuit board - trace connecting the LED to V_{LED} or to the current generator, short-circuit from current generator to ground or V_{LED}).

All these possible events are summarized in *Figure 21*.

Figure 21. Fault conditions detected by error detection mode: a) shorted LED; b) open LED; c) short-circuit from current generator to V_{LED}; d) open channel; e) short-circuit from current generator to GND



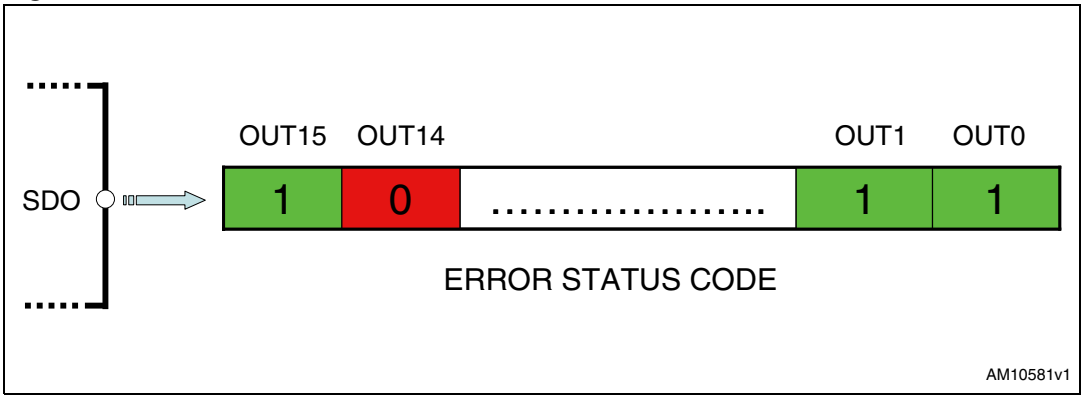
The diagnostic circuitry embedded in the STP16DPxy05 can detect these faulty conditions (in accordance with the detection thresholds of *Table 3*) and provide the results of the detection as an “Error status code” coming out of the SDO pin (see *Figure 22*), with “0” logic level indicating a faulty channel, whereas “1” logic level indicates a “good” channel.

Table 3. Detection conditions

Detection conditions	Detection result
I_{ODEC}(1) = 0.5·I_O(2)	Open channel or output short to GND detected
I_{ODEC} = 0.5·I_O	No error detected
V_O = 2.4 V	Short on LED or short to LED supply voltage
V_O = 2.2 V	No error detected

1. I_{ODEC} is the detected output current in detection mode.
2. I_O is the programmed output current.

Figure 22. Error status code



The error detection process can be divided into three phases:

1. Entering detection mode. From “normal mode” the device can enter “error mode” through a logic key (*Figure 23*), which is a logic sequence of the $\overline{OE/DM2}$ and LE/DM1 signals over five CLK cycles. After these five CLK cycles, the device is in “error detection mode” and ready for sampling data on the SDI pin
2. Error detection. Once the device has entered “error detection mode”, an 8-bit string should be loaded into the shift register through the SDI pin in order to set the outputs in accordance with the diagnostic demands (only the outputs that are on are checked by the error detection process). Therefore, if the user wants to check all the outputs, a string with all “1” must be sent. After that the outputs are ready for the detection process, which starts when $\overline{OE/DM2}$ is set low. The device drives LEDs in order to analyze if an open or short condition has occurred. The $\overline{OE/DM2}$ must remain low for at least 1 µs to complete the detection process. As shown in *Figure 25*, during the detection process, at least three clock pulses are necessary: two pulses as soon as the $\overline{OE/DM2}$ $\overline{OE-R}$ is set low, one clock pulse before ending the detection process. Once the $\overline{OE/DM2}$ is set high, the error status code is available at the SDO pin. To download the complete error string, at least 8 clock pulses are necessary
3. Resuming normal mode. The device quits detection mode and returns to normal mode through an exit logic key (*Figure 24*), a logic sequence over five clock pulses.

Figure 23. Digital key for entering error detection mode in 16-bit LED drivers

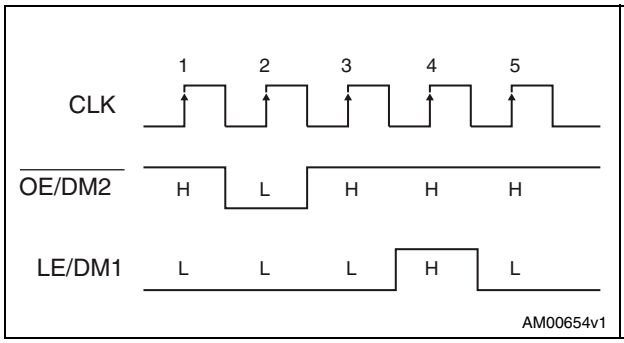
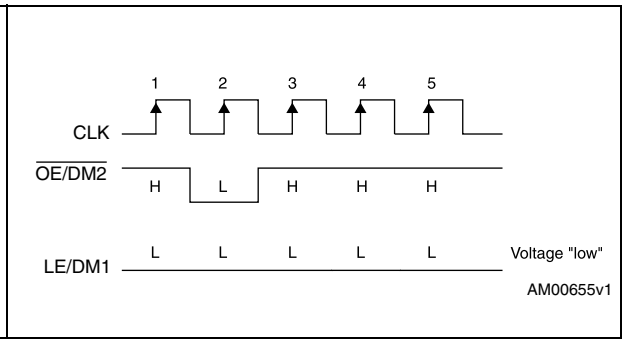


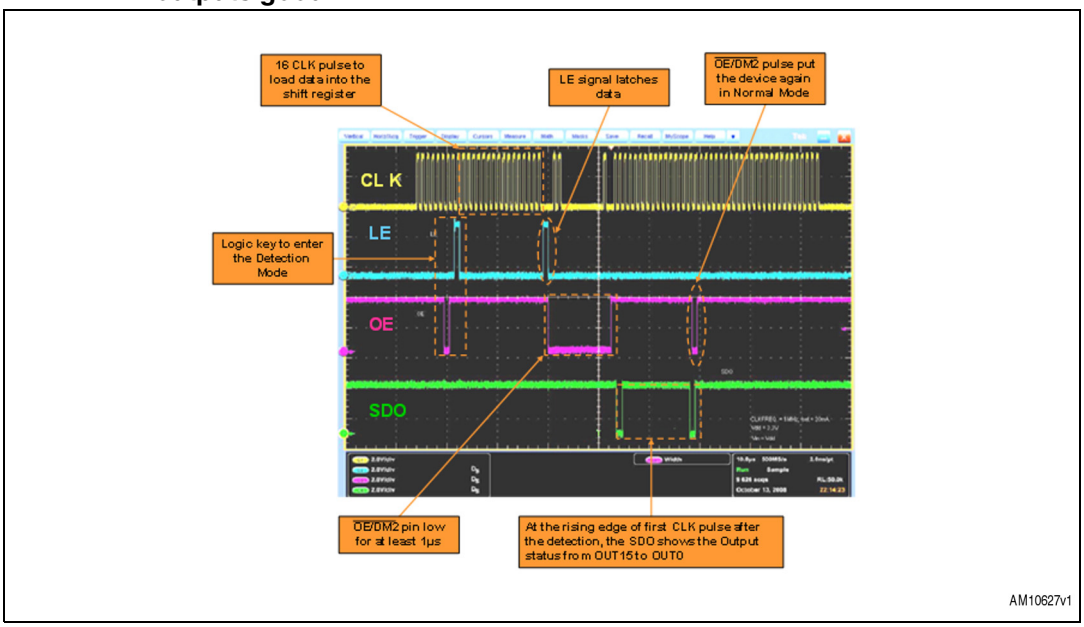
Figure 24. Digital key for exiting error detection mode in 16-bit LED drivers



For proper device operation, the entering sequence must be followed by a resuming sequence as it is not possible to insert consecutive equal sequences.

Figure 25 shows an example of error detection where OUT15 and OUT0 are faulty, whereas all other outputs are considered good.

Figure 25. Example of error detection with OUT15 and OUT0 faulty and all other outputs good



3.6.1 Correctness of the error detection results

It is important to underline that the result of the diagnostic process must be compared with the data loaded into the shift register.

In fact, if a channel is not switched on, the result of the detection is “0” anyway.

It is recommended to follow the approach shown in *Figure 26*.

Figure 26. Error detection results interpretation

The correct interpretation of the detection results can be affected by any setup/hold time problem. Same considerations about $\overline{OE}$ and LE timing done in *Section 4.6.3* apply also to 16-bit LED array drivers.

Incorrect error detection results can be due also to an inappropriate choice of the LED supply voltage. The rules to suitably define the LED supply voltage are discussed in *Section 5.1*.

3.7 Power saving

The auto power-saving feature dramatically reduces the quiescent current of the device in case all outputs are off.

If a string with all “0” is latched, the device automatically enters “Auto shutdown” mode, characterized by a very low current consumption.

If at least a bit “1” is latched, the device automatically powers up again.

3.7.1 Power saving example

Considering an LED panel with a size 5 m x 10 m, an estimated number of ten thousand LED drivers can be assumed.

If LED drivers do not have the power saving feature, the total current consumption is the sum of the supply current of each LED driver, independently of the status of the outputs.

Therefore, considering a typical supply current of 10 mA (in case of maximum output current), the total current consumption is:

Equation 7

$$I_{DD,total} = I_{DD,typ} \cdot n = 10mA \cdot 10000 = 100A$$

where n is the number of LED drivers.

Considering that in the panel (e.g. a panel used in road signage) only a small part of LEDs are active at the same time, it is possible to assume that 30% of the LED drivers must be active at the same time (active means that at least one output is on).

If the power saving features are used, the total current consumption in this case is (assuming a typical supply current in shutdown of around 100 µA):

Equation 8

$$I_{DD,total,power-saving} = I_{DD,typ} \cdot n_{active} + I_{DD,shut-down} \cdot n_{off}$$

Equation 9

$$I_{DD,total,power-saving} = 10mA \cdot 3000 + 100\mu A \cdot 7000 = 30.7A$$

where n_{active} is the number of LED drivers active at the same time, while n_{off} is the number of LED drivers in auto shutdown.The example shows that the power saved is around 70%.

3.8 Current generators performance

In many applications it is required to slow current rising and the falling edge of the current generators to improve the system performance in terms of noise.

The STP16CPC05 provides a suitable solution for this kind of requirement. Its current generators T_{ON} and T_{OFF} are respectively in the order of 100 ns and 80 ns, showing also a balance between the two periods. Similar behavior is shown also by the STP16CPC26. Further details can be found in the relative datasheets.

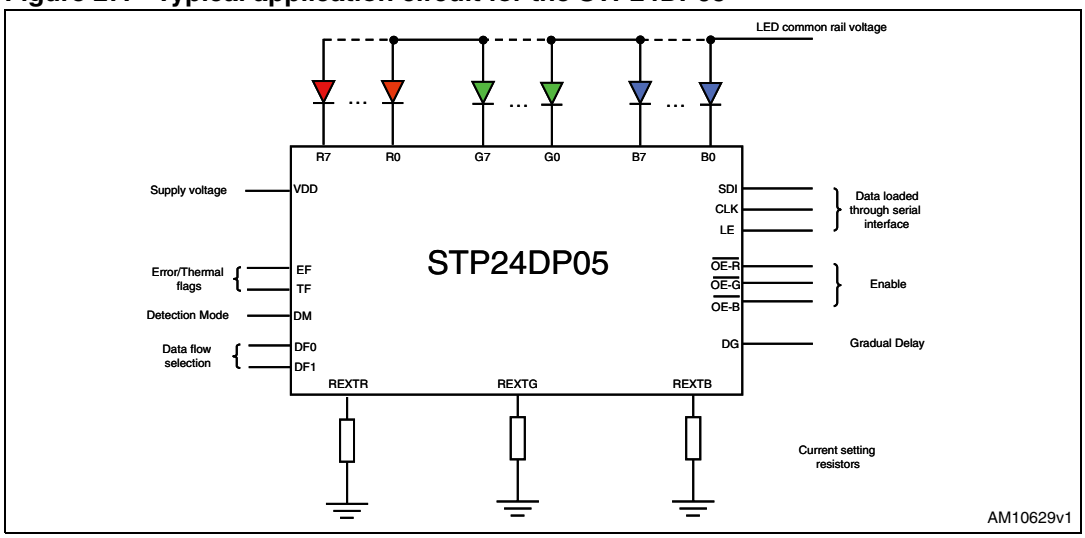
4 STP24DP05

4.1 Main features

The STP24DP05 LED array driver is characterized by the following features:

- Three groups of eight constant current output channels
- Adjustable output current from 5 mA to 80 mA through an external resistor for each group
- Error detection
- Gradual delay
- 20 V current generators rated voltage
- Supply voltage from 3 V to 5.5 V.

Figure 27. Typical application circuit for the STP24DP05



4.2 Applications

The STP24DP05 is tailored mainly to RGB solutions, like full color high resolution LED displays, colored traffic signs, etc.

4.3 Block diagram

Figure 28 shows the simplified internal block diagram of the STP24DP05.

The 24 outputs are organized into three groups of eight outputs each. Assuming an RGB solution, each group is supposed to be dedicated respectively to red, green and blue LEDs.

The current of each group can be adjusted through the resistor connected to the relative REXT pin (REXTR for red, REXTG for green, REXTB for blue).

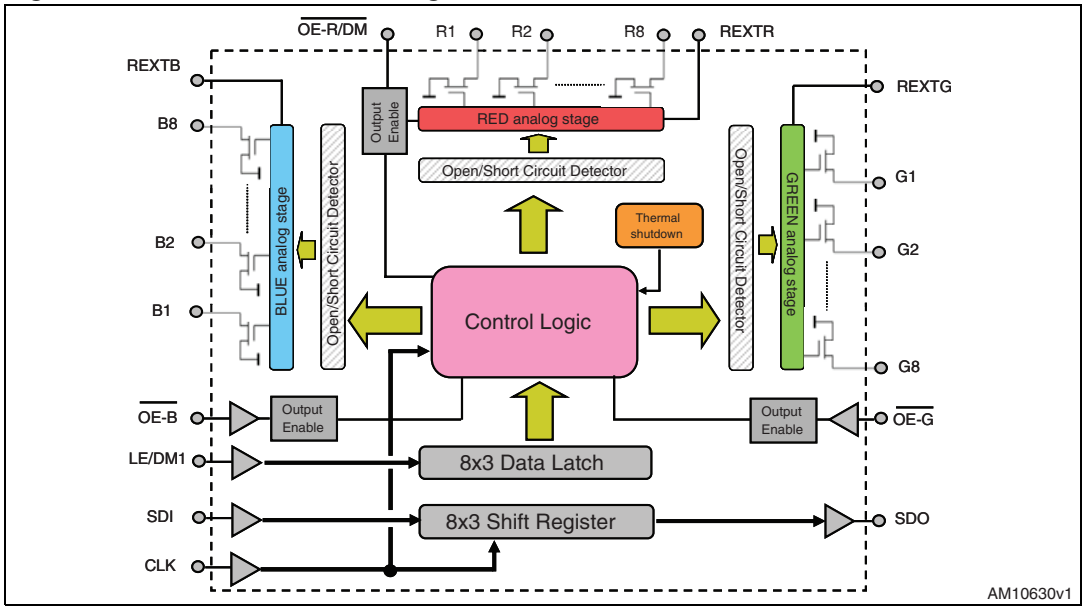
Data are loaded through the SDI pin into the “8x3-bit Shift Register”. Data are latched into the “8x3 Data Latch” block after the LE pulse.

Each color group has its own “Output Enable” block, used to activate or not the eight outputs of the group or to perform a brightness PWM dimming.

Each group has a dedicated analog stage that drives the eight current generators and an “Open/Short-circuit detection” for the diagnostics.

The “Thermal shutdown” block monitors the junction temperature and switches the current generators off if this temperature goes over the thermal shutdown threshold (typically 170 °C), independent to the actual status of the generators. The generators return to the previous status if the junction temperature falls, typically 15-20 °C, below the thermal shutdown threshold.

Figure 28. STP24DP05 block diagram



4.4 SPI data sending

Figure 29 shows a typical timing diagram of the STP24DP05.

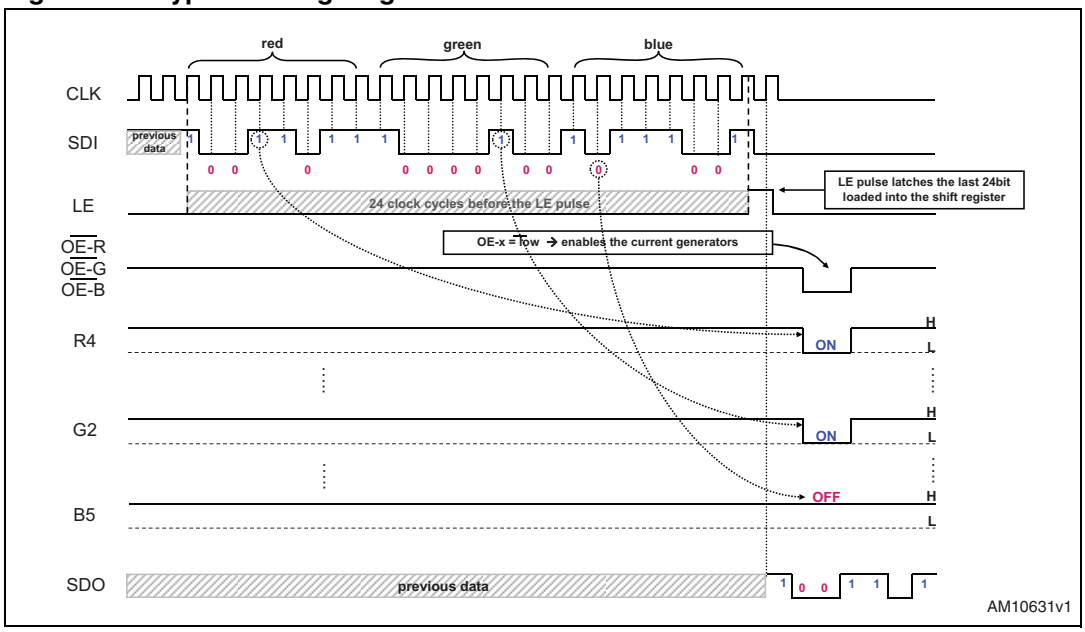
The LE pulse latches the last 24 bits loaded into the shift register through the SDI pin and sampled by the last 24 clock rising edges.

Data are loaded in accordance with the status of the data flow pin (DF0 and DF1, see dedicated section). In *Figure 29* it is assumed that DF0 = 1 and DF1 = 0.

The $\overline{OE}$ pin dedicated to each color group ($\overline{OE}$ -R, $\overline{OE}$ -G and $\overline{OE}$ -B), allows to enable/disable each group independent to the other ones.

As long as the $\overline{OE}$ -x (where x can be R, G or B) pin is high, all current generators belonging to group x are not active. Once $\overline{OE}$ -x is set low, the current generators of group x are enabled.

Figure 29. Typical timing diagram of the STP24DP05



4.5 Current setting

The output current of each group can be separately programmed through an external resistor in the range from 5 mA to 80 mA. The choice of the resistor value can be made using the curve below (*Figure 30*) or using the following formula:

Equation 10

$$R_{EXT} = \left(\frac{V_{REF}}{I_{OUT}}\right) \cdot 16$$

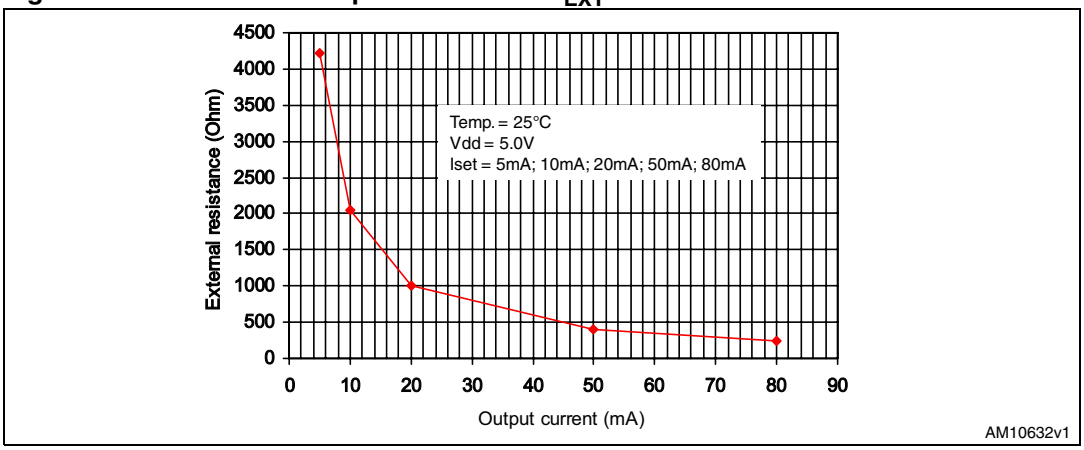
where V_{REF} = 1.25 V.

For example, if a current of 20 mA per channel must be programmed, according to *Equation 1*, the external resistor value is:

Equation 11

$$R_{EXT} \cong \left(\frac{1.25}{0.02}\right) \cdot 16 \quad = \quad 1k\Omega$$

Figure 30. STP24DP05 output current vs. R_{EXT}



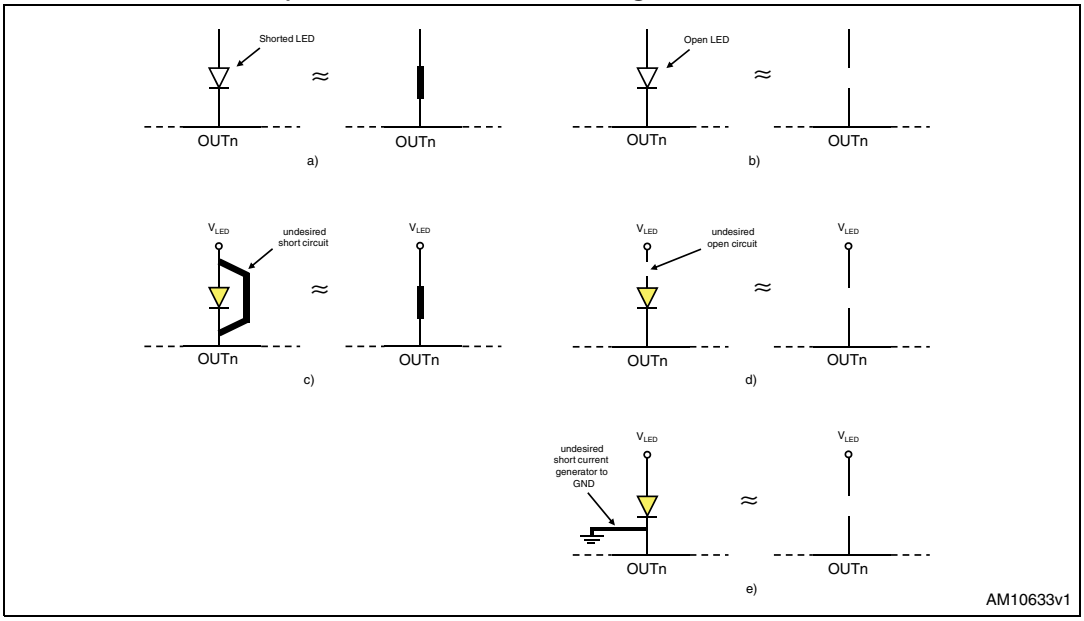
4.6 Error detection

The meaning of “error detection” is the detection of the faulty conditions that could occur on each channel due to:

- the LED, which can be damaged and behaves abnormally as a short or open circuit
- any undesired event that can prevent the LED from working correctly (interruption of the PCB - printed circuit board - trace connecting the LED to V_{LED} or to the current generator, short-circuit from current generator to ground or V_{LED}).

All these possible events are summarized in *Figure 41*.

Figure 31. Fault conditions detected by error detection mode: a) shorted LED; b) open LED; c) short-circuit from current generator to V_{LED}; d) open channel; e) short-circuit from current generator to GND



The diagnostic circuitry embedded in the STP24DP05 can detect these faulty conditions (in accordance with the detection thresholds of *Table 4*) and provide the result of the detection

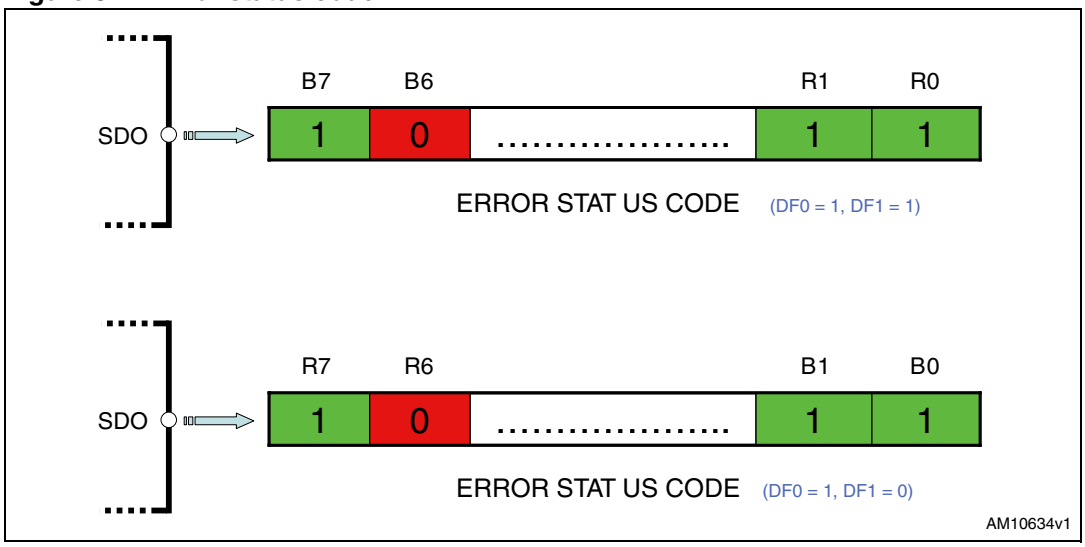
as an “Error status code” coming out of the SDO pin (see *Figure 32*), with “0” logic level indicating a faulty channel, whereas a “1” logic level indicates a “good” channel.

Table 4. Detection conditions

Detection conditions	Detection result
I_{ODEC} (1) = 0.4·I_O(2)	Open channel or output short to GND detected
I_{ODEC} = 0.4·I_O	No error detected
V_O = 2.6 V	Short on LED or short to LED supply voltage
V_O = 2.4 V	No error detected

1. I_{ODEC} is the detected output current in detection mode.
2. I_O is the programmed output current.

Figure 32. Error status code



The device can enter error detection mode in two ways:

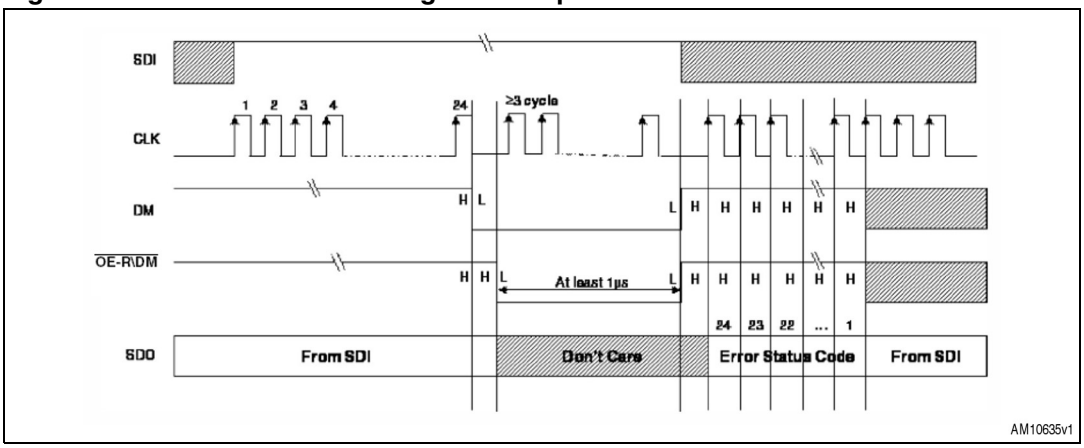
1. setting low the DM pin
2. providing a logic sequence on the $\overline{OE-R}$ and LE pins.

4.6.1 Error detection through the DM pin

As shown in *Figure 33*, the device enters error detection mode when the DM pin is set low. The error detection is performed correctly when the $\overline{OE-R}$ pin is set low for at least 1 µs.

When the DM and $\overline{OE-R}$ pins are set high again, the error status code is available at the SDO pin. 24 CLK cycles are necessary to make the device shift out of the complete error status code.

Figure 33. Error detection through the DM pin



4.6.2 Error detection through $\overline{OE-R}$ and LE

The error detection process activated by the logic sequence of $\overline{OE-R}$ and the LE pin can be divided into three phases:

1. Entering detection mode. From “normal mode” the device can enter “error mode” through a logic key (*Figure 34*), which is a logic sequence of the $\overline{OE-R}$ and LE signals over five CLK cycles. After these five CLK cycles the device is in “error detection mode” and ready for sampling data on the SDI pin
2. Error detection. Once the device has entered “error detection mode”, a 24-bit string should be loaded into the shift register through the SDI pin in order to set the outputs in accordance with the diagnostic demands (only the outputs that are on are checked by the error detection process). Therefore, if the user wants to check all the outputs, a string with all “1” must be sent. After that the outputs are ready for the detection process, which starts when $\overline{OE-R}$ is set low. The device drives LEDs in order to analyze if an open or short condition has occurred. The $\overline{OE-R}$ must remain low for at least 1 µs to complete the detection process. As shown in *Figure 36*, during the detection process, at least three clock pulses are necessary: two pulses as soon as the $\overline{OE-R}$ is set low, one clock pulse before ending the detection process. Once the $\overline{OE-R}$ is set high, the error status code is available at the SDO pin. To download the complete error string, at least 24 clock pulses are necessary
3. Resuming normal mode. The device quits detection mode and returns to normal mode through an exit logic key (*Figure 35*), a logic sequence over five clock pulses.

Figure 34. Digital key for entering error detection mode in 32-bit LED drivers

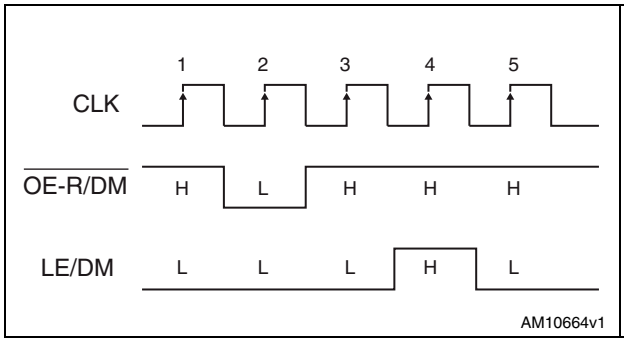
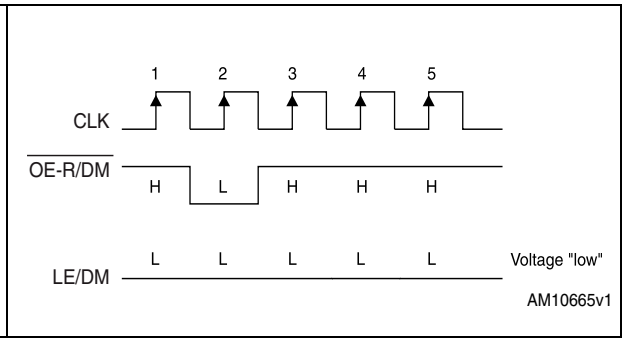


Figure 35. Digital key for exiting error detection mode in 32-bit LED drivers



For proper device operation, the entering sequence must be followed by a resuming sequence as it is not possible to insert consecutive equal sequences.

Figure 36. Example of error detection with the STP24DP05

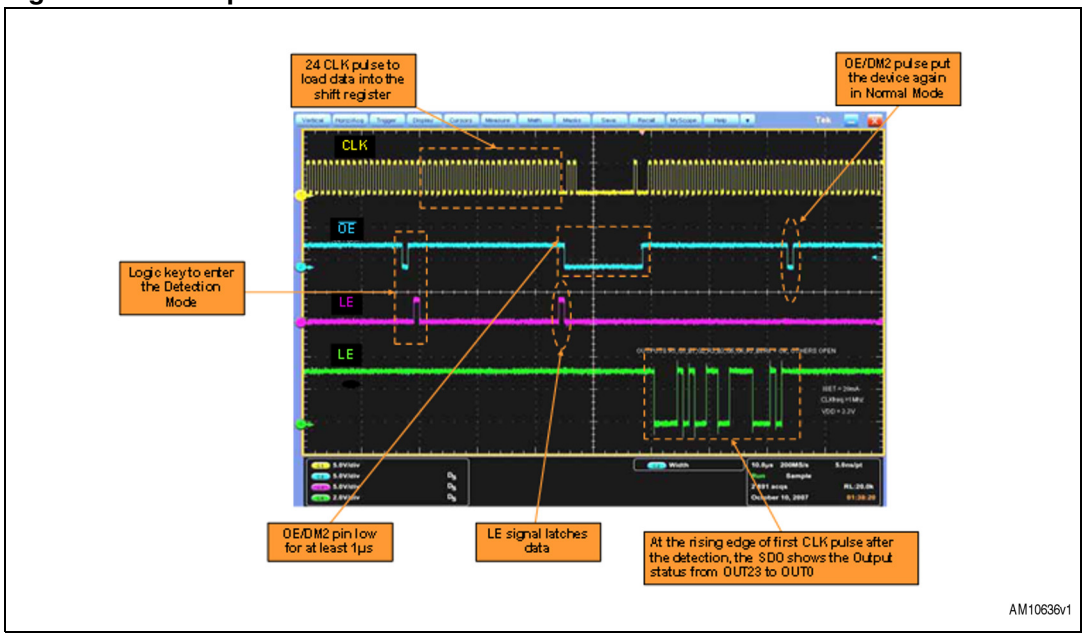


Figure 36 shows an example of error detection where OUT15 and OUT0 are faulty, whereas all other outputs are considered good.

4.6.3 Correctness of the error detection results

It is important to underline that the result of the diagnostic process must be compared with the data loaded into the shift register.

In fact, if a channel is not switched on, the result of the detection is “0” anyway.

It is recommended to follow the approach shown in *Figure 26*.

Figure 37. Error detection results interpretation

The correct interpretation of the detection results can be affected by any setup/hold time problem.

The same considerations regarding $\overline{OE}$ and LE timing, done in *Section 2.6.1*, apply also to 24-bit LED array drivers.

Incorrect results of the error detection can be due also to an inappropriate choice of the LED supply voltage. The rules to suitably define the LED supply voltage are discussed in *Section 5.1*.

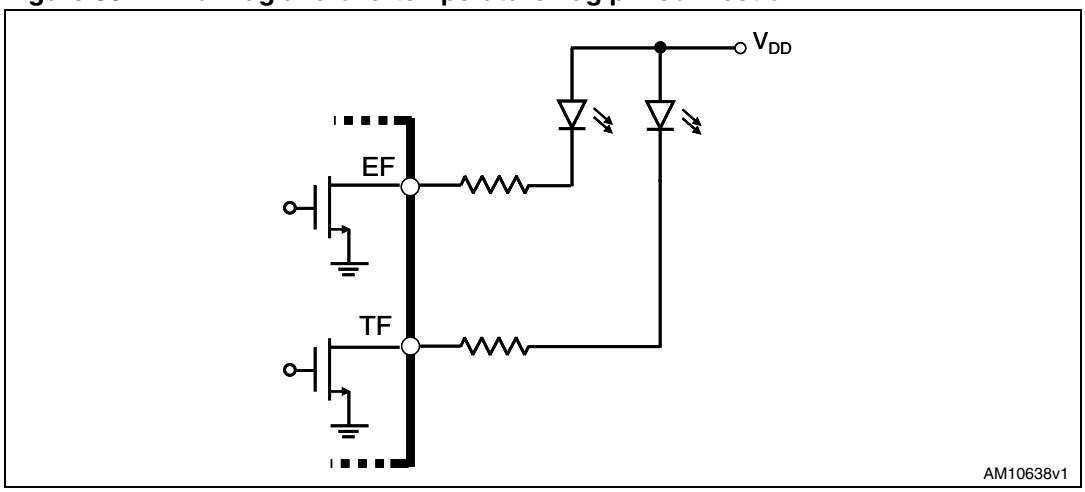
4.7 Flag pins

The EF and TF pins are two open drain outputs dedicated to reporting the STP24DP05, respectively an output faulty condition (detected with the error detection process) or an overtemperature event.

Typically these outputs are externally pulled up, as shown in *Figure 38*.

In case an error or an overtemperature is detected, the internal switch connected to the respective output flag (EF or TF) is turned on.

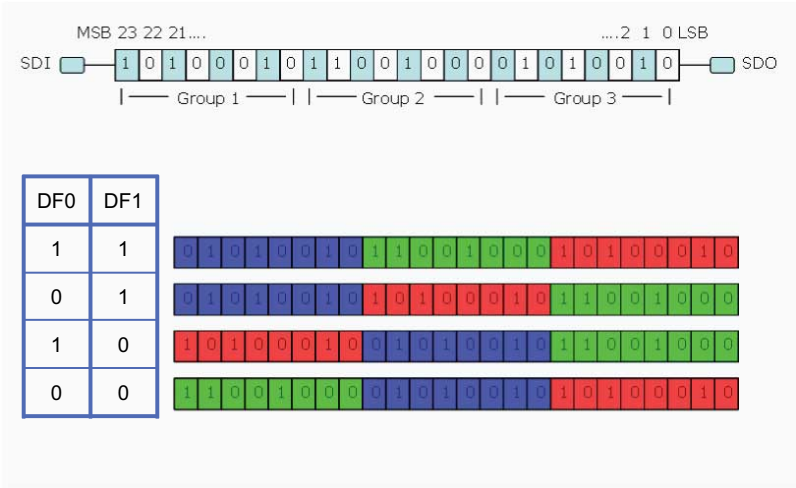
Figure 38. Error flag and overtemperature flag pin connection



4.8 Data flow management

The data are transferred from the shift register to each color group with a sequence defined by the status of pins DF0 and DF1 and clarified in *Figure 39*.

Figure 39. Data flow management



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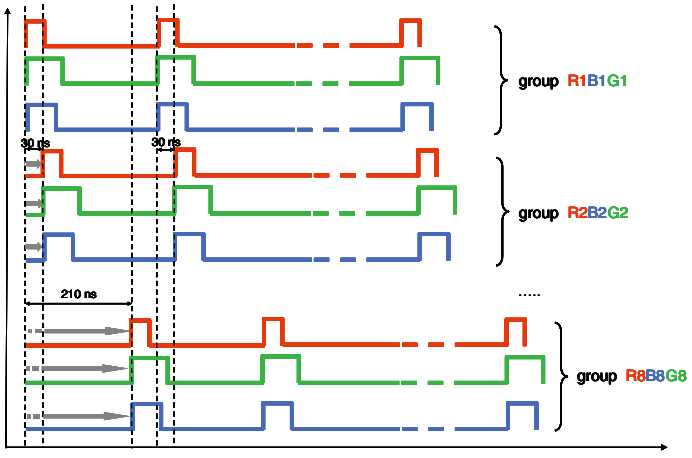
4.9 Gradual output delay

This feature is used to prevent high inrush current due to the simultaneous turning on of all LEDs at the start of a video frame and so reducing the input capacitor value.

The gradual output delay can be activated by setting low the DG pin. A default delay of 30 ns for each group (RGB) is implemented, as clarified by *Figure 40*.

Figure 40. Gradual output delay



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5 Common application information

5.1 LED supply voltage

The choice of the LED supply voltage (VLED) must be made considering several parameters:

- The voltage drop across current generators (V_O), which must be enough to guarantee the desired current (see dedicated section in the relative datasheet)
- The maximum LED forward voltage ($V_{F,max}$)
- The maximum power that can be dissipated by the package under the application ambient conditions
- The accuracy of the supply voltage itself (VLED can vary in range and the minimum value should be considered).

Therefore the minimum LED supply voltage can be calculated as:

Equation 12

$$V_{LED,min} = V_{O,typ} + V_{F,max}$$

The LED supply voltage should be higher than $V_{LED,min}$ (to consider any fluctuation of the involved parameters) but not too high in order to keep low the power dissipation:

Equation 13

$$P_D = V_{DD} \cdot I_{DD} + \sum_{i=1}^{16} V_{O,i} \cdot I_{CHi} .$$

where V_{DD} is the device voltage supply, I_{DD} the device supply current, $V_{O,I}$ and I_{CHi} are, respectively, the voltage drop across the current generator i and the channel current i.

In particular, the power dissipation should be kept below the maximum power dissipation, defined as:

Equation 14

$$P_{D,max} = \frac{(T_j - T_a)}{\theta_{ja}}$$

where T_j and T_a are respectively the junction and the ambient temperature, whereas θ_{ja} is the junction-to-ambient thermal resistance.

To summarize, the choice of the proper power supply must be a trade-off between the correct value assuring the desired LED current and low power dissipation.

In RGB applications, there can be a significant variability of the LED forward voltage (e.g. red LEDs have a lower forward voltage compared to green and blue ones).

In this case the supply voltage must be chosen high enough to correctly switch on the LEDs with the highest forward voltage (green or blue). However, this supply voltage is higher than the voltage required by red LEDs. Therefore, the excess of voltage in the lines with red LEDs drops on the current generators, bringing an increase of the power dissipation and loss of efficiency.

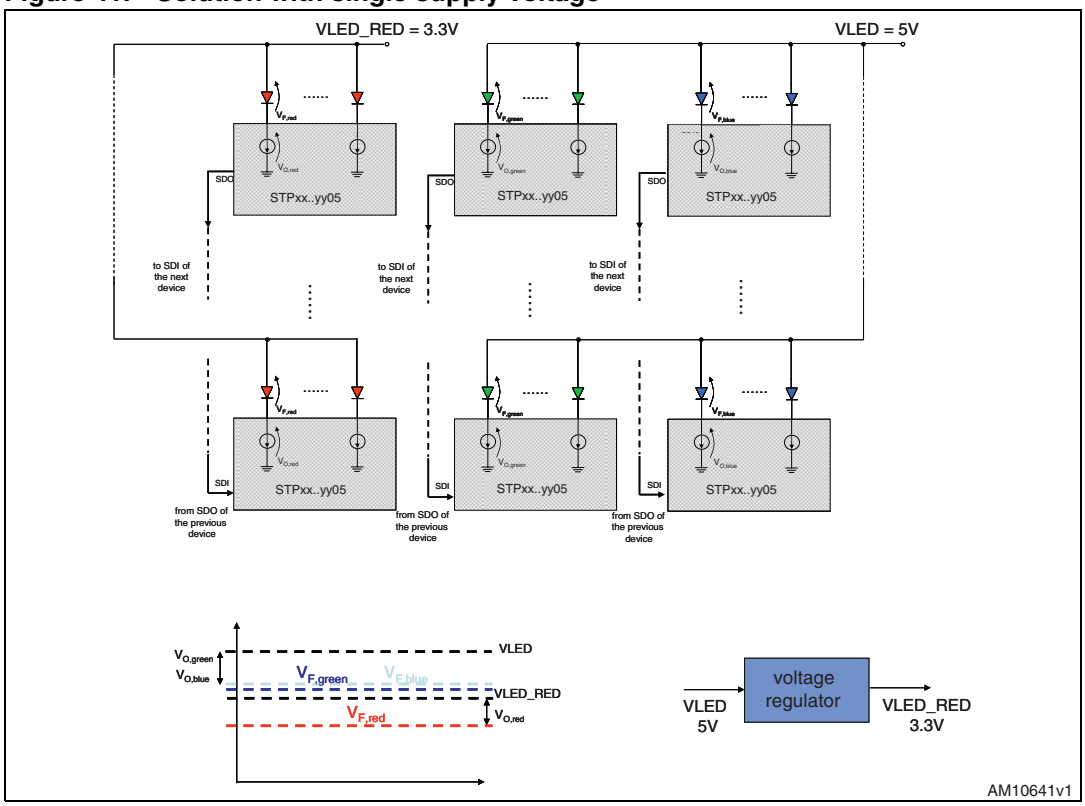
Moreover the extra voltage across the red LEDs driving generators may cause an erroneous shorted LED condition detection.

To avoid these drawbacks, two different approaches are possible:

1. *Figure 41* shows an application with only one voltage rail (VLED). A resistor in series to each red LED is added. In this way, the voltage excess drops across the resistor instead of dropping across the current generators. This solution implies a significant reduction of the power dissipated by the chip. However the total power dissipation does not change and a large part of the power is still wasted on the series resistor.

This not only affects the efficiency, but also raises the cost of the system due to the need to dissipate the generated heat.

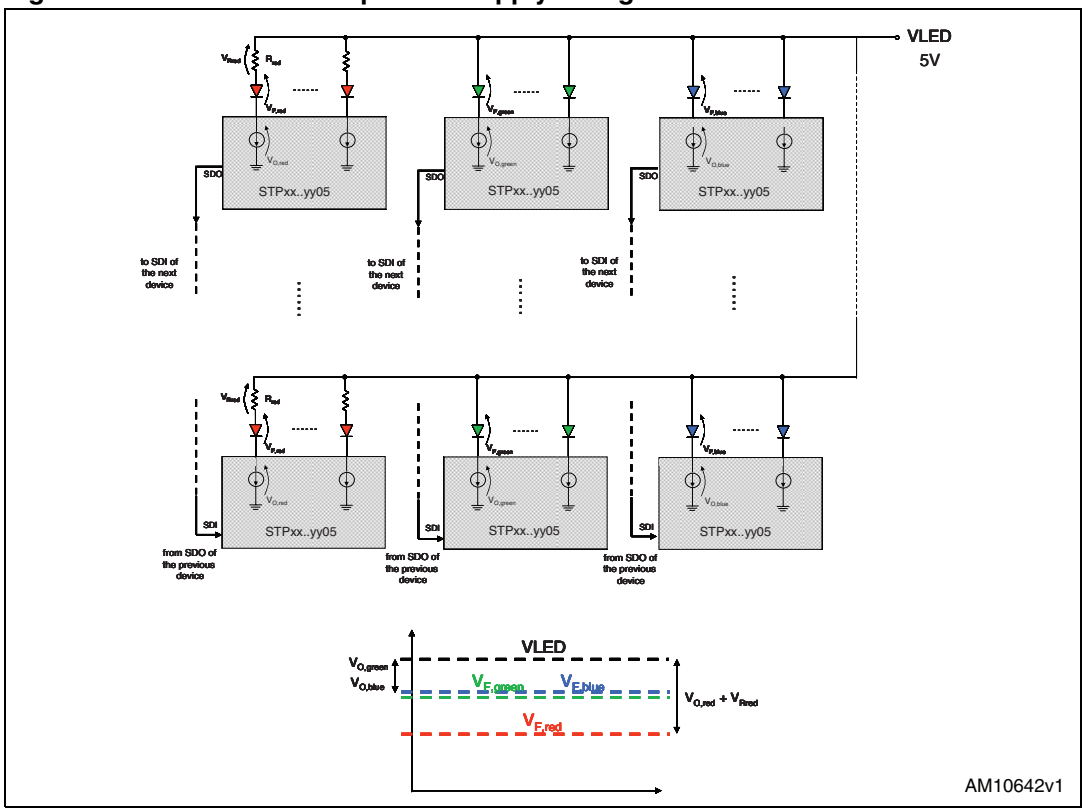
Figure 41. Solution with single supply voltage



2. *Figure 42* shows a solution with two separate voltage rails: one for blue and green LEDs (VLED) and one for red LEDs (VLED_RED), which can be derived from the former (e.g. simply using a switching regulator).

This solution is by far the most advantageous in terms of power dissipation. Voltage rails are tailored to the type of LEDs they drive and the wasted power is significantly reduced as well as the heat produced.

Figure 42. Solution with separated supply voltage for red LEDs



5.1.1 Package selection

The package selection involves several considerations. One of these concerns the choice of the most suitable package considering the power to dissipate and the ambient conditions.

The power to dissipate must be estimated using the relation described in the previous section (*Equation 13*). It mainly depends on the application conditions (i.e. channel current and voltage drop across current generators).

The ambient conditions should be carefully considered and they can be quite different according to the application (e.g. ICs placed close to a large LED video display could work in a very hot ambient due to the LEDs heating).

The devices described in this document can be housed in different packages, summarized in *Table 5*.

Table 5. Thermal resistance junction to case for different packages

#channels	Package	θ_{ja} (°C/W)
4	DIP-14	70
4	SO-14	105
4	HTSSOP-16 (exposed pad)	37.5
8	DIP-16	90
8	SO-16	125

Table 5. Thermal resistance junction to case for different packages (continued)

#channels	Package	θ_{ja} (°C/W)
8	TSSOP-16	140
8	HTSSOP-16 (exposed pad)	37.5
16	SO-24	42.7
16	TSSOP-24	55
16	QSOP-24	55
16	HTSSOP-24 (exposed pad)	37.5
24	TQFP-48	33

The value of the thermal resistance junction-to-ambient (θ_{ja}) indicated in *Table 5* refers to a standard PCB, in accordance with JEDEC guidelines.

It is worth remembering that the θ_{ja} is strongly influenced by the PCB and the actual values can be different to those listed in the table.

However, assuming correct the θ_{ja} in *Table 5*, the maximum power dissipation allowed, according to the ambient temperature, is shown in *Figure 43*, *Figure 44*, *Figure 45* and *Figure 46*.

Figure 43. Maximum power dissipation vs. ambient temperature for different packages for 4-bit LED drivers

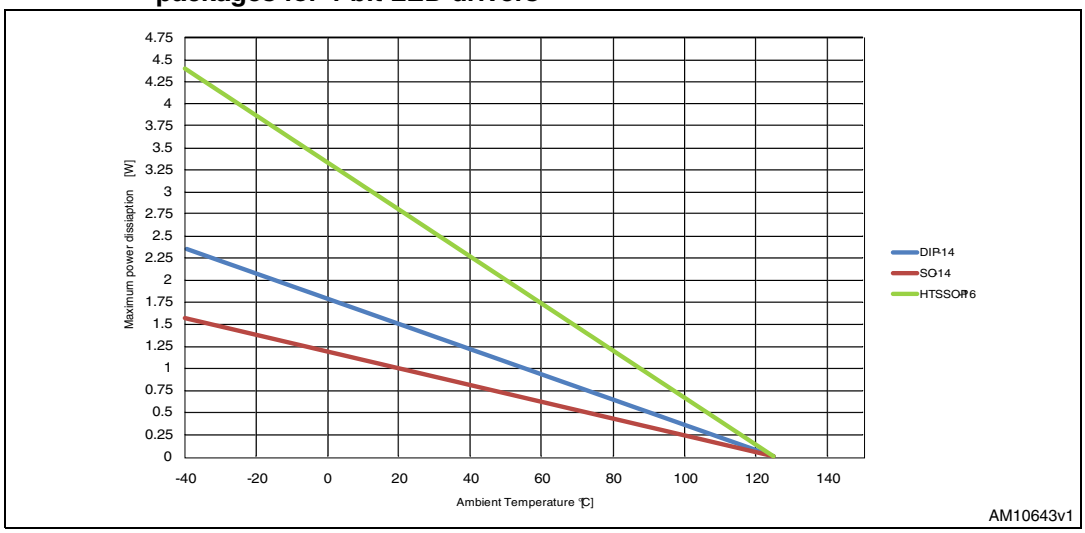


Figure 44. Maximum power dissipation vs. ambient temperature for different packages for 8-bit LED drivers

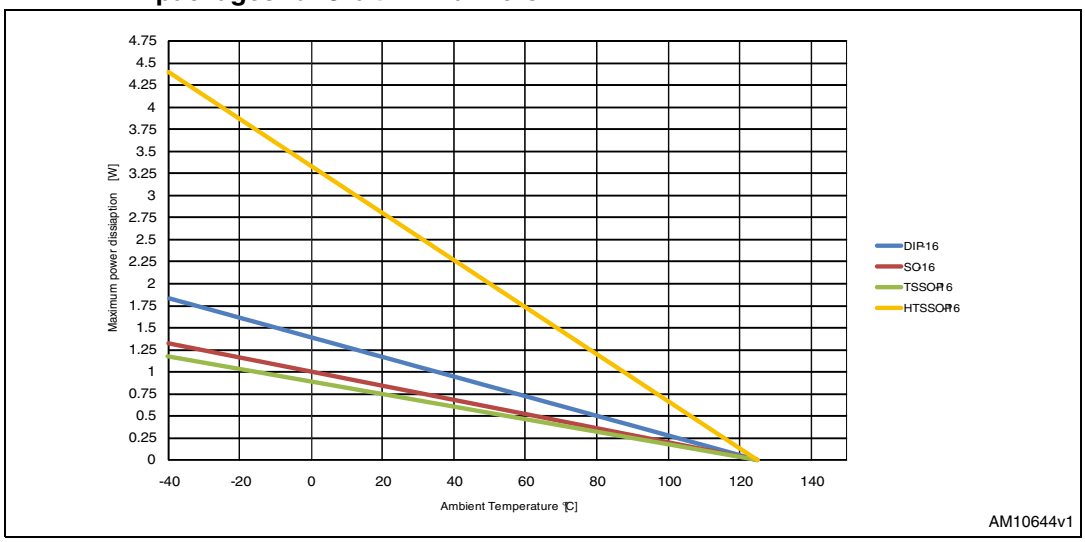


Figure 45. Maximum power dissipation vs. ambient temperature for different packages for 16-bit LED drivers

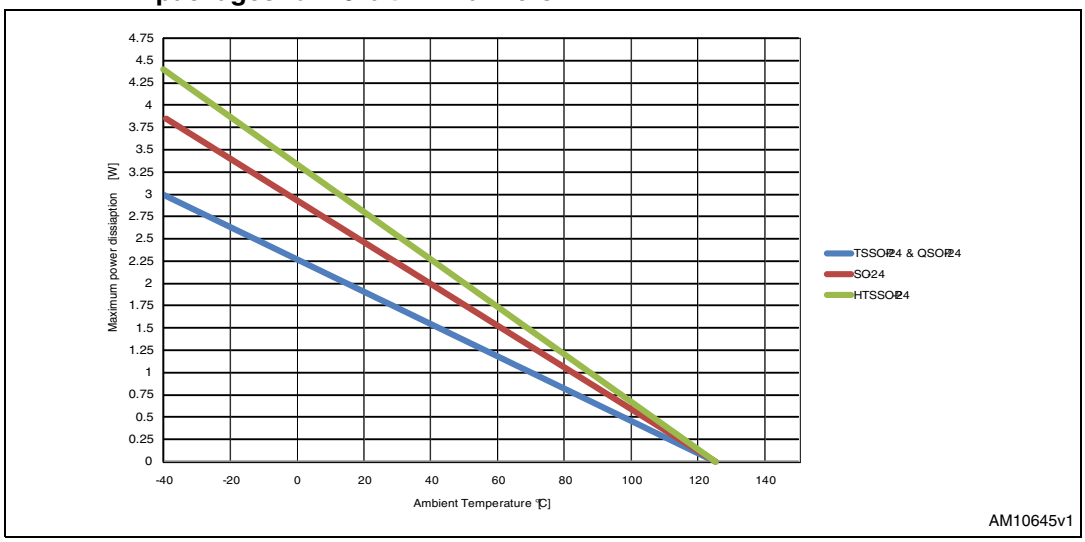
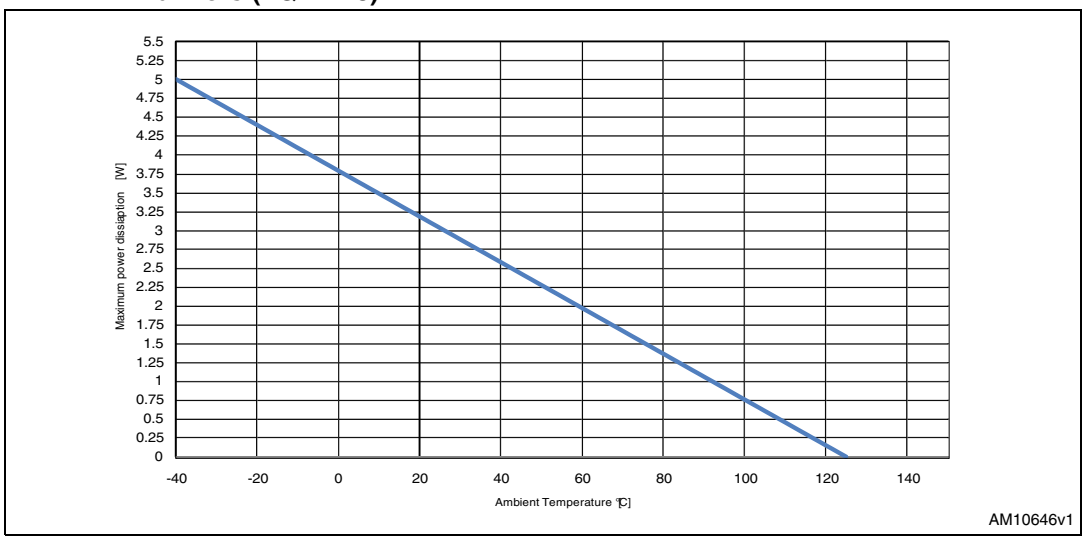


Figure 46. Maximum power dissipation vs. ambient temperature for 24-bit LED drivers (TQFP-48)



Example 1: Applications with a 16-bit LED driver (e.g. traffic signs), one amber LED (60 mA, 2 V-2.2 V forward voltage, depending on current and temperature) per channel.

Assuming an LED voltage rail of 3.3 V, the voltage drop across current generators can be considered around 1.2 V.

The power dissipation, including only the main contribution of the current generators, can be calculated as:

Equation 15

$$P_{DISS} = \sum_{i=1}^{16} V_{O,i} \cdot I_{CH,i} = 16 \cdot 1.2V \cdot 60mA = 1.152W$$

Once the power dissipation has been estimated, the ambient conditions must be taken into account. A large LED panel can produce significant heat and can contribute to a considerable increase of the temperature inside the system.

Figure 47 shows, once the maximum power dissipation is fixed, which ambient temperature range can be covered according to the package.

The TSSOP-24 and the QSOP-24 are surely the least suitable for this application. So the choice is oriented towards the HTSSOP-24 (the best, thanks to the exposed pad) or to the SO-24 (if a lower maximum ambient temperature can be accepted).

Figure 47. Maximum power curves for different packages

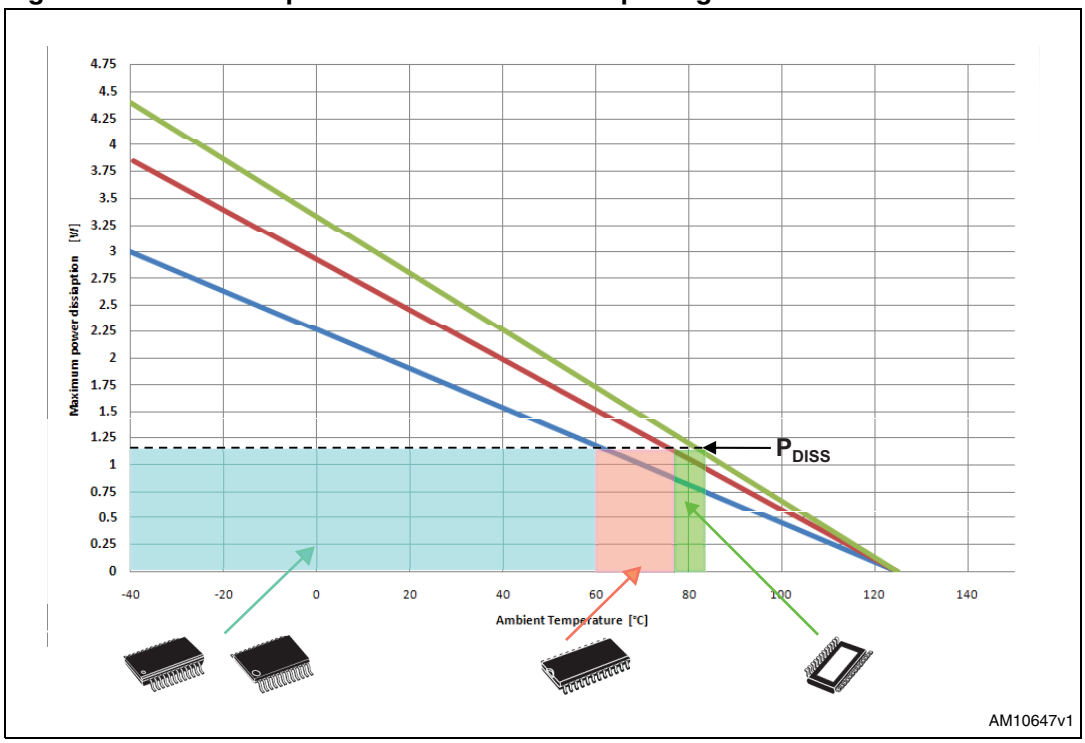


Figure 48 and *49* show the significant difference in terms of power dissipation and, consequently, also of heat generation.

The images have been captured by an infrared (IR) camera.

Two different packages are compared: TSSOP-24 (left) and HTSSOP-24 (right). Although the temperature detected by the IR camera refers to the package surface temperature, it provides, however, an idea regarding the trend of the junction temperature and provides a comparison of the two packages in terms of thermal behavior.

Both images show the STP16CPC26 under the same conditions: all channels on, 60 mA per channel, 1.2 V voltage drop across current generators and 5 V IC voltage supply. The PCB used in both cases is the same.

As described above, in this case the power dissipation is 1.152 W.

The advantage of the exposed pad in HTSSOP-24 compared to TSSOP-24 is evident.

Figure 48. Thermal performance of the TSSOP- 24

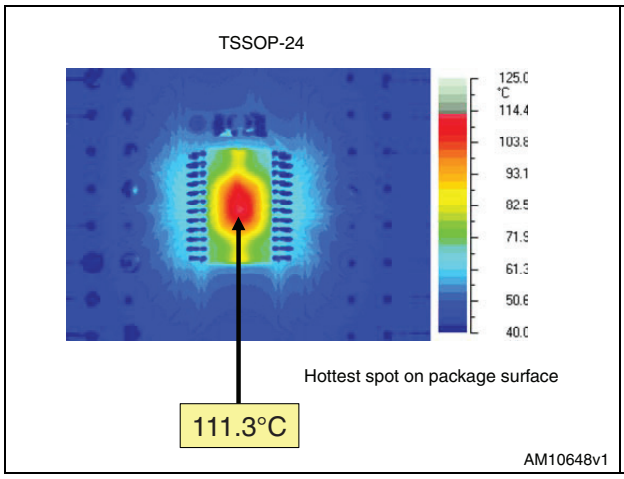
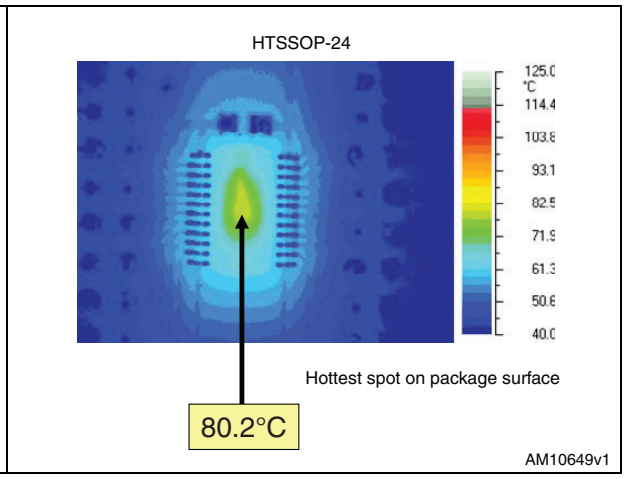


Figure 49. Thermal performance of the HTSSOP - 24

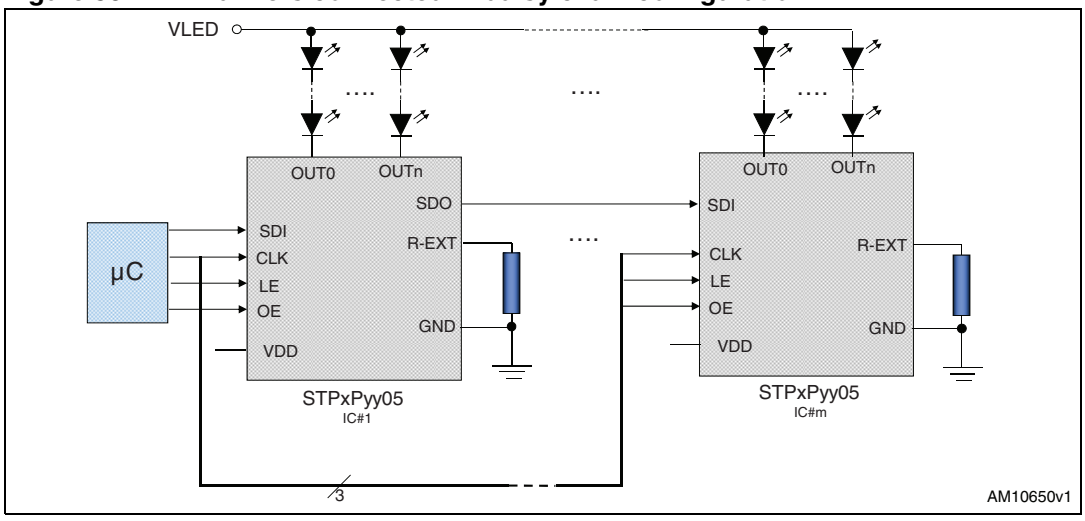


5.2 Daisy chain connection

In real applications, typically, the number of LEDs to drive leads to the use of more drivers.

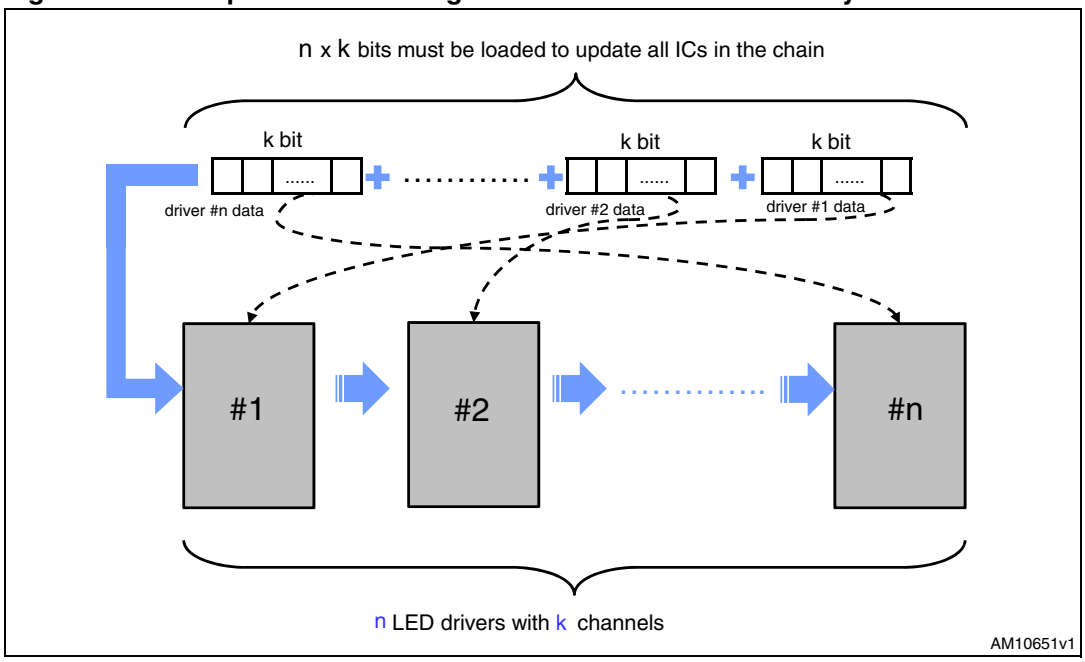
A common configuration (daisy chain) of the drivers is shown in *Figure 50*. This way to connect the drivers implies that all ICs in the chain share some serial interface signals, like CLK, LE and $\overline{OE}$.

Figure 50. LED drivers connected in daisy chain configuration



All data go through each device of the chain. Every time the information (displayed by LEDs) must be updated, the data packet to load contains a number of bits equal to the number of bits necessary for each device (4, 8, 16 or 24) multiplied by the number of devices contained in the chain, as shown in *Figure 51*.

Figure 51. Example of data loading for devices connected in daisy chain



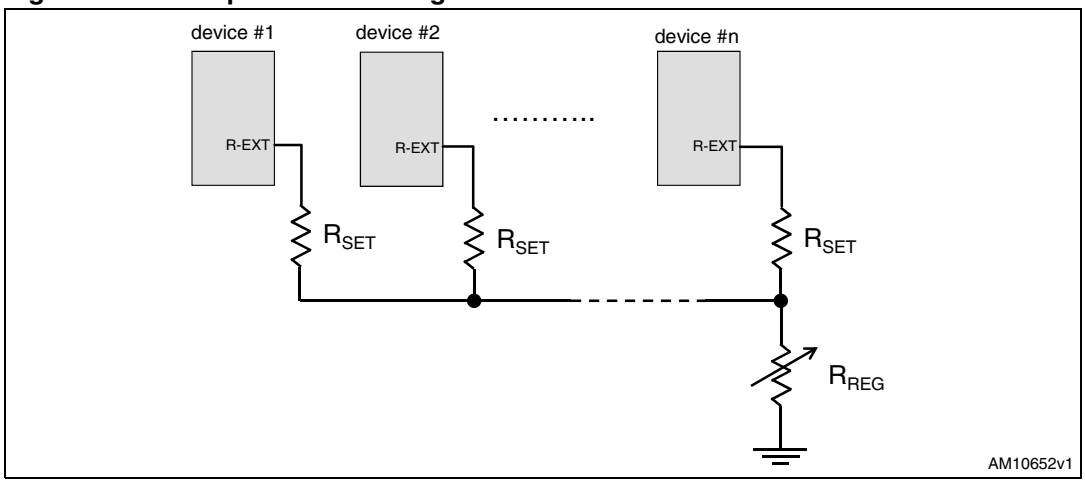
When devices are connected in the daisy chain configuration it is worth making some observations:

- by increasing the number of devices connected in daisy chain, the length of data to load also increases. Therefore it is important to choose a proper data clock frequency considering how often data must be updated
- the correctness of the data transfer from one device to the next and the integrity of the information can be achieved by monitoring the timing of the signals provided to the serial interfaces. In particular, attention should be paid to the delay of data shifted out of each device with respect to the data clock signal and to the compliance with setup and hold times. This is important especially in case of high data clock frequencies.

5.3 Regulating the current in a group

When the current regulation of a group of devices (e.g. connected in daisy chain) is required, the solution shown in *Figure 52* can be used (this is just one proposal and is not the only solution).

Figure 52. Example of current regulation for more devices at the same time



Each device has the setting resistor (R_{SET}) connected to the REXT pin. This resistor has the same value for all devices. The current is adjusted by changing the value of R_{REG} (in this case it is a trimmer).

The maximum current programmed in all devices is achieved with a minimum value of R_{REG}, whereas the minimum current is achieved with the highest value of R_{REG}.

The value of the programmed current in each channel can be calculated using the following relation:

Equation 16

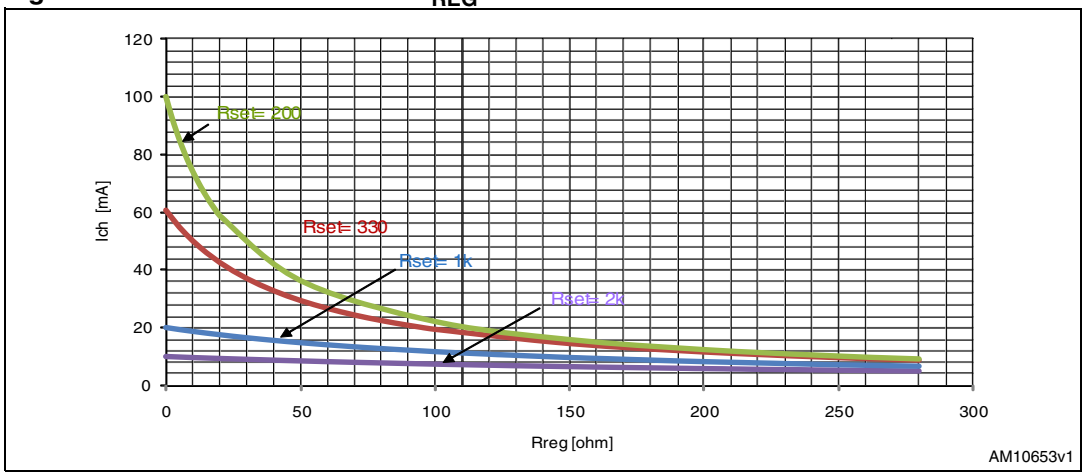
$$I_{CH} = \left[V_{REF} - \frac{n \cdot V_{REF} \cdot R_{REG}}{n \cdot R_{REG} + R_{SET}} \right] \cdot \frac{k}{R_{SET}}$$

where:

- V_{REF} = 1.25 V
- k depends on the device (k=64 for STP04CM05, k=16 for all other devices)
- n is the number of devices.

The curve in *Figure 53* shows the relation between the channel current and R_{REG} for different values of R_{SET} (the curve refers to all devices except the STP04CM05).

Figure 53. Channel current vs. R_{REG}



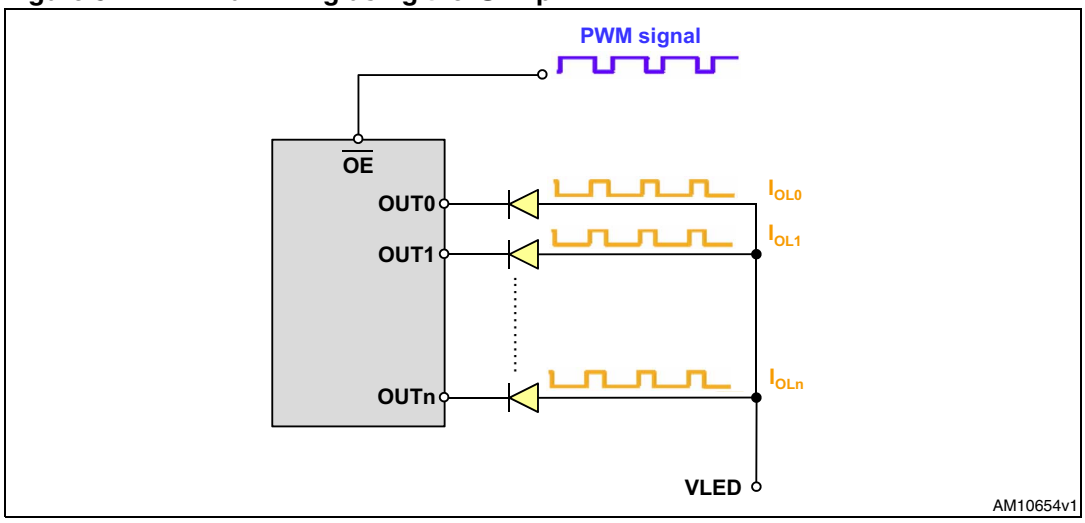
5.4 PWM dimming

In several applications there is the need to adjust the brightness of the LEDs (e.g. for an appropriate color mixing in RGB applications, simply to dim the emitted light, etc.).

Typically, in LED applications brightness adjustment is achieved using a PWM dimming, which controls the mean value of the current flowing through the LEDs, preserving the color of the emitted light at the same time.

In all the devices described in this document, the possibility to adjust the brightness is provided by the $\overline{OE}$ pin (see *Figure 54*). In fact, a PWM signal applied to this pin (with a frequency high enough to not be perceived by the human eye) allows to switch all channels on and off at the same time, therefore achieving a control of the mean value of the current flowing in each channel and, in turn, the brightness of the LEDs.

Figure 54. PWM dimming using the $\overline{OE}$ pin



Although this solution is very simple, in some cases it is not useful:

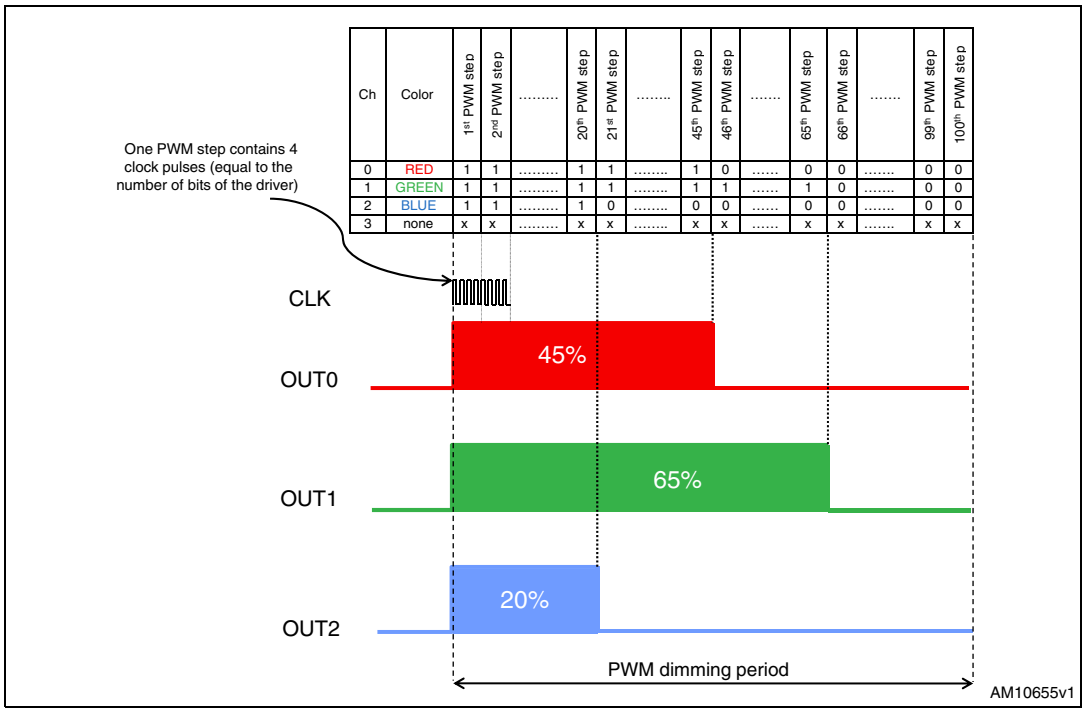
- In color mixing, different duty cycles for each color are necessary in order to reproduce all colors. Only the STP24GPL05 allows regulation of the brightness independently for each color (there is one OE pin per color). For any other device the color mixing can be achieved only if each color is controlled by one device. For instance, if an STP04CM05 is used to drive three LEDs (one red, one green, and one blue, with a channel left open), there is no possibility to correctly mix the color as different color LEDs can not be dimmed separately from each other.
- Generally, every time, for any reason, it is required to change the brightness of each channel separately.

The brightness control of each channel can be achieved using a different approach, which can be more clearly understood with an example. For simplicity it is worth considering a four channel LED driver (STP04CM05).

Assuming that it is required to regulate the brightness from 0% to 100% in 1% steps, 100 different data packets (each one composed of 4 bits) must be sent to complete one dimming cycle. Each packet represents a PWM step.

Figure 55 shows an application example where a duty cycle of 20% for blue, 45% for red and 65% for green is required.

Figure 55. Example showing how to perform a PWM dimming separately for each channel



For 20 PWM steps (resulting in 80 clock pulses), all outputs are on. Then the blue is switched off and for a further 25 PWM steps only green and red are kept on.

From the 46th step on, the green is the only one to remain on for 20 PWM steps. After that all outputs are switched off for the remaining 35 PWM steps, which complete the PWM dimming period.

This way to perform the PWM dimming requires the proper choice of data clock frequency in order to achieve a correct PWM frequency.

A correct PWM frequency means a frequency higher than the frequency perceived by the human eye:

Equation 17

$$f_{DIMM} \geq f_{LIM}$$

where f_{DIMM} is the PWM dimming frequency (inverse of the PWM dimming period) and f_{DIM} is the minimum frequency to prevent the human eye from perceiving the switching of the light.

The PWM dimming frequency depends on the desired number of PWM steps (n_steps), the number of channels of the considered LED driver (n_ch) and the data clock frequency (f_{CLK}):

Equation 18

$$f_{DIMM} = \frac{f_{CLK}}{n\_steps \cdot n\_ch}$$

Therefore the choice of the data clock frequency should comply with the following condition:

Equation 19

$$f_{CLK} \geq n\_steps \cdot n\_ch \cdot f_{LIM}$$

Assuming a dimming frequency higher than 100 Hz, to use a 16-bit LED driver and to require a brightness regulation from 0% to 100% in 0.1% steps, the minimum data clock frequency should be 1.6 MHz.

5.5 Short detection between adjacent pins

When the device is soldered on the application board, undesired short-circuits between adjacent pins can occur.

A strategy to detect these anomalous conditions (although it works only for OUT pins) is provided for those devices that can perform faulty LED detection (STP08DP05, STP16DP05, STP16DPS05, STP16DPPS05 and STP24DP05).

This method is successful if the forward voltage of the LEDs connected to the outputs does not vary in a wide range.

The detection of the possible short-circuit (in this example a short-circuit between the OUT10 and OUT11 pins is assumed) is performed in the following steps:

1. All even outputs are set ON and an error detection is performed. Since OUT10 and OUT11 are shorted, the current of the generator of the output 10 (the only one turned on) is shared between LEDs connected to OUT10 and OUT11 (see *Figure 56* a), resulting in a lower voltage drop across those LEDs (and also lower brightness) and higher voltage drop across both current generators (pins OUT10 and OUT11).

The result of the faulty LED detection is shown below the schematic of *Figure 56* a.

2. The common LED rail voltage (VLED) is progressively increased while performing a continuous LED error detection, until a new output is detected as faulty (OUT10). In fact, it is considered as if it were connected to a shorted LED, since the forward voltage of the LED is lower (half current compared to other channels) and, consequently, the voltage across the current generator exceeds the short detection threshold. Considering the error status code, the conclusion is that a short-circuit can be present between OUT9 and OUT10 or OUT10 and OUT11.
3. To detect where the short is placed, the previous actions are repeated also for odd outputs (see *Figure 56* b). A new error status code is obtained.
4. Comparing the two status codes, it is possible to exactly understand where the short-circuit is placed (see *Figure 56* c).

Figure 57 shows a possible implementation of the above described strategy.

Figure 56. Description of shorted adjacent pin detection strategy

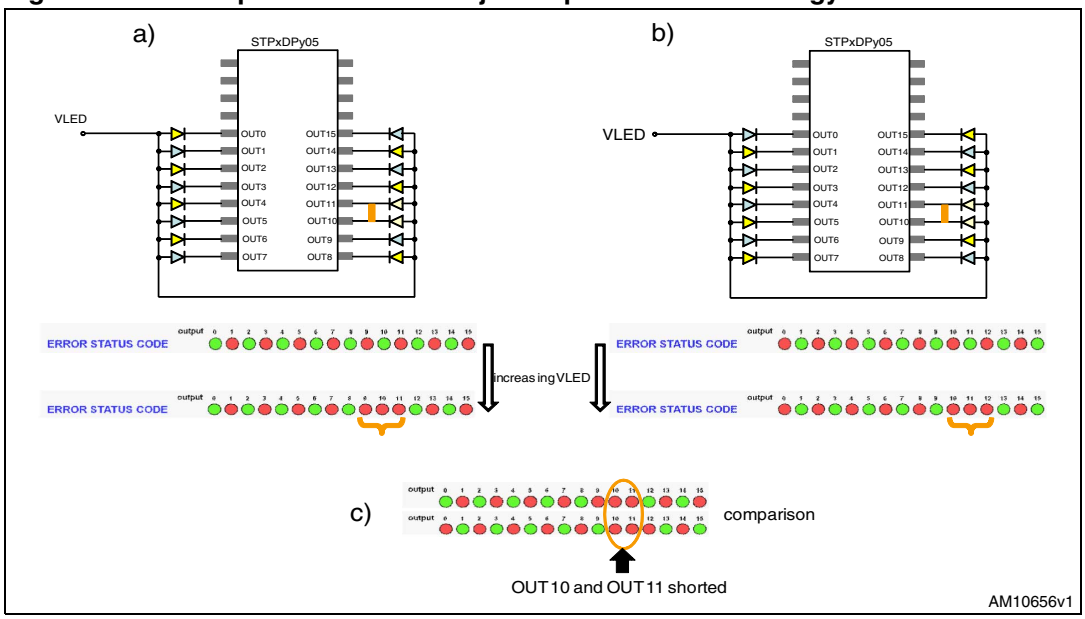
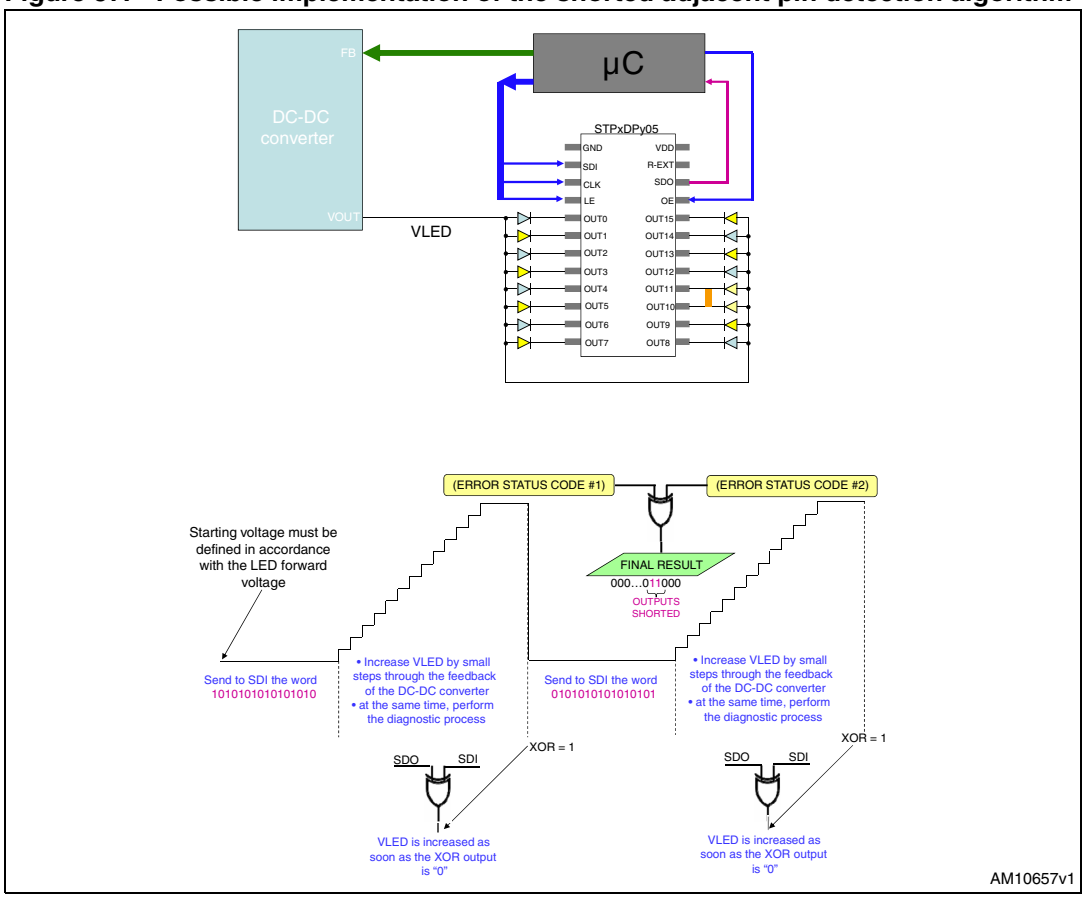


Figure 57. Possible implementation of the shorted adjacent pin detection algorithm



5.6 Higher current requests (outputs in parallel)

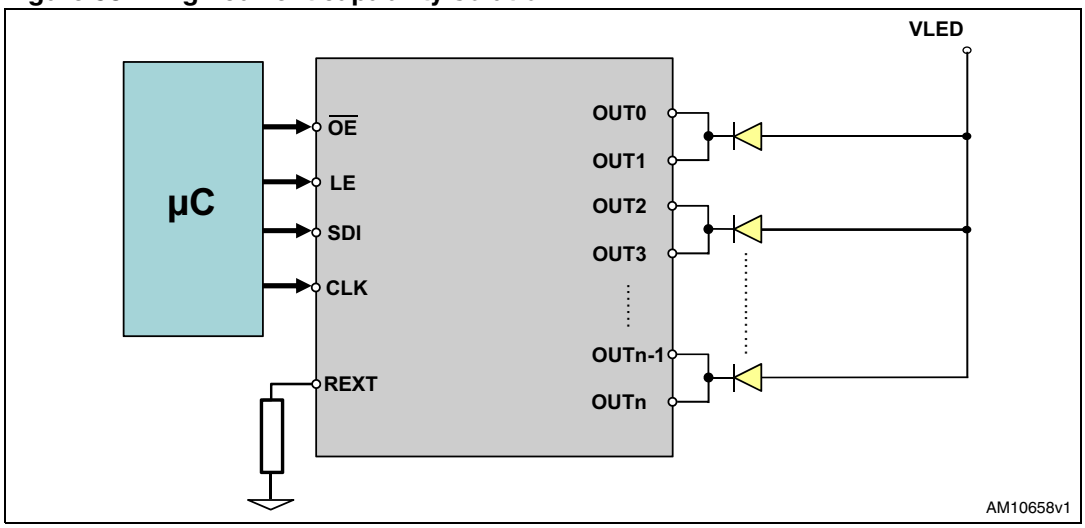
When the application needs to drive high power LEDs, the current demand may be higher than the current provided by a single channel.

In this case a higher current capability can be achieved by connecting together two or more channels (in accordance with the current value which must be regulated).

Figure 58 shows an example of an STP16CP05 used in an application that requires a 150 mA current driving capability.

As the maximum deliverable current per channel is (for this product) 100 mA, only by connecting two channels (75 mA per channel) is it possible to reach the requested value of current.

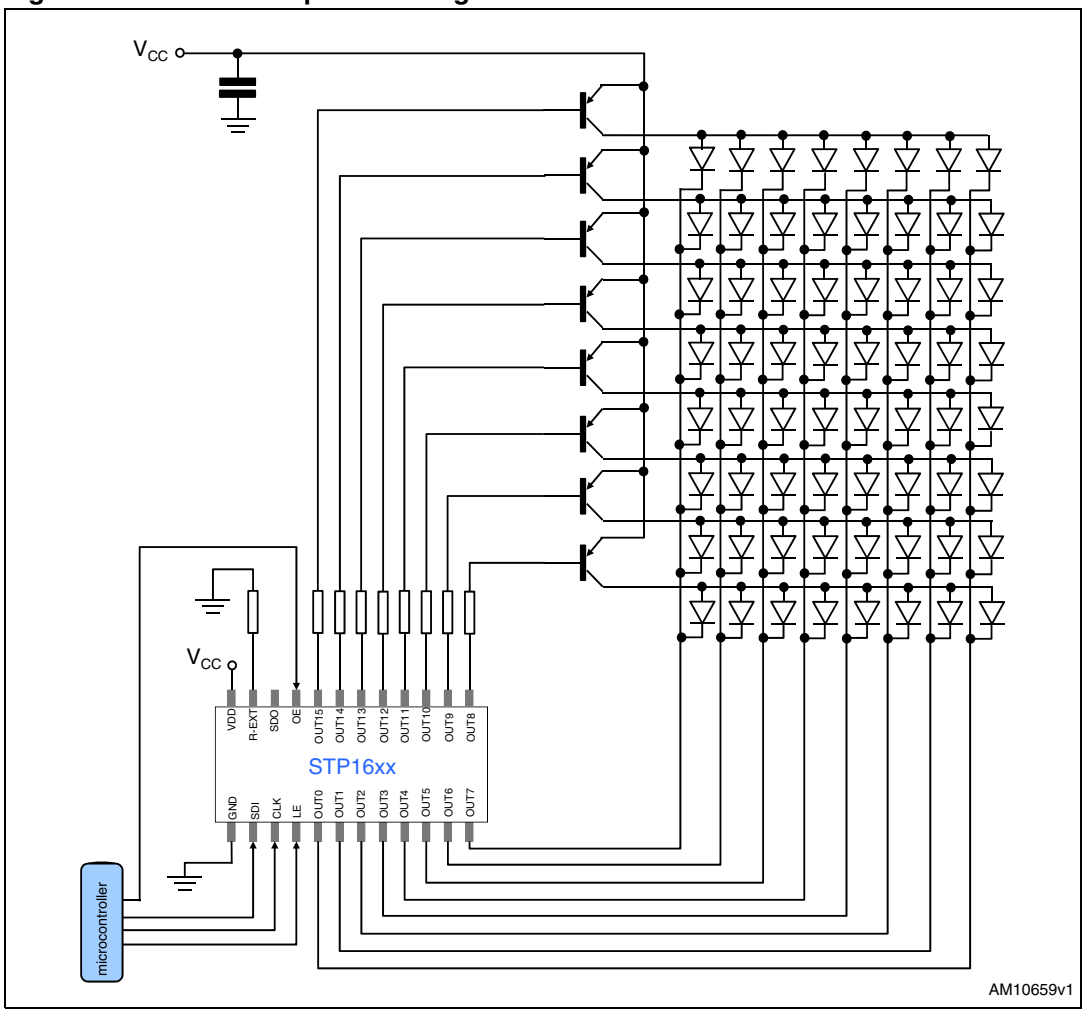
Figure 58. High current capability solution



5.7 LED matrix driving solution

The implementation of common anode (or common cathode) configurations in LED matrix panels allows a reduction in the number of LED drivers. In fact, a matrix of 64 LEDs for example would require 64 channels (e.g. four 16-channel LED drivers) and an LED common voltage rail for all anodes. If a multiplexed solution (common anode) is used, just one LED driver (e.g. STP16xx) is enough, as shown in *Figure 59*.

Figure 59. LED matrix panel driving solution



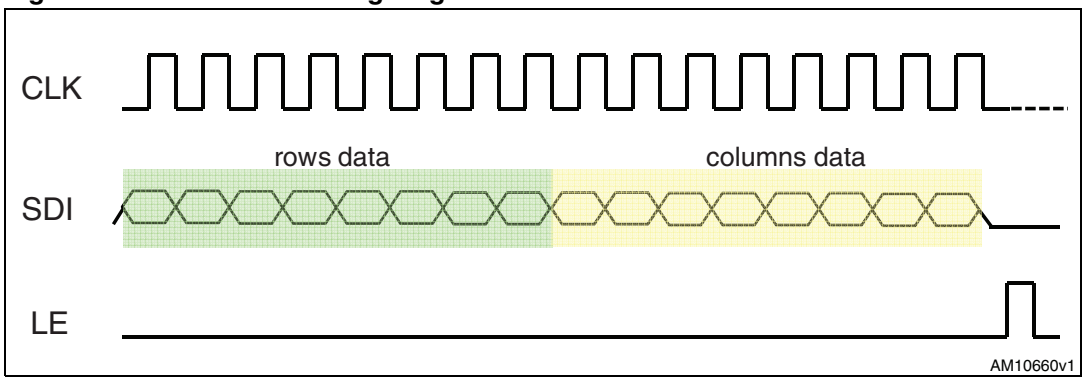
Eight channels out of sixteen are connected to the common cathodes (8 cathodes per channel) and, if turned on, sink current from 1 to 8 LEDs (according to the number of LEDs activated in each column).

The remaining channels are dedicated to driving the base of 8 transistors (used as switches), each one used to connect or not eight anodes (of the same row) to the LED voltage rail (if any, or to VCC if the voltage supply is the same as that which sources the IC).

The timing diagram in *Figure 60* shows how to send data properly in order to correctly display the desired information.

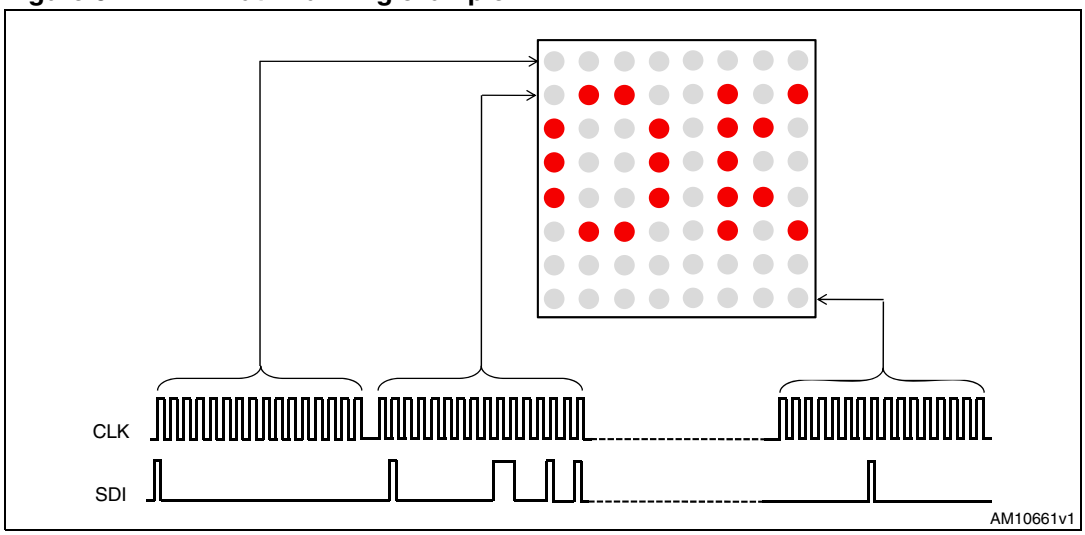
Each 16-bit group is used to select the row (bit 15 to bit 8) and the column (bit 7 to bit 0) of the matrix. The complete image, considering a matrix of 8x8, is built in 8 cycles. Each cycle is used to select a row (activating more columns) or a column (activating more rows).

Figure 60. LED matrix timing diagram



The example in *Figure 60* shows which data are provided to the LED matrix panel to display the desired message (“OK”). In this case each cycle address one row.

Figure 61. LED matrix driving example



6 PCB layout guidelines

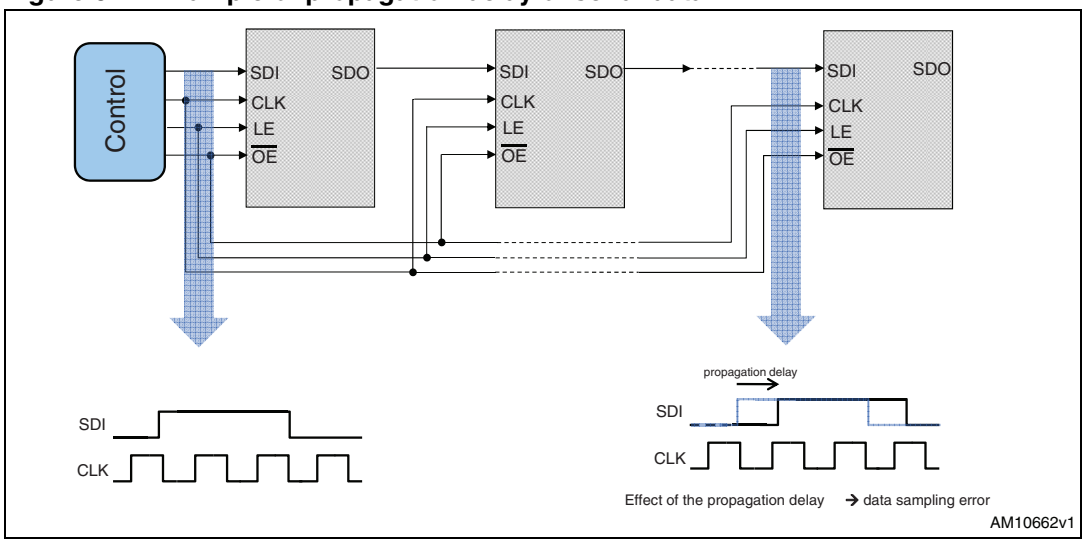
The aim of this section is to provide some recommendations that may be useful in designing the application PCB.

General suggestions for PCB design are always valid.

Beyond general recommendations, there are some other equally important considerations, tailored to this device family.

In daisy chain configurations, for example, the serial data is delayed every time it passes through a new device, while other signals are provided directly to each device by the control system (see *Figure 62*).

Figure 62. Example of propagation delay of serial data



In order to correctly sample the data, the clock rising edge must occur when the desired serial data is present, and at the SDI input of the next device, and already stable (the data setup time must be respected). If the propagation delay of the devices in the chain is high, it is likely that the clock rising edge samples erroneously a different data (the next one and one bit of the data word is lost) or samples incorrectly the data.

To prevent this kind of error, it is worth monitoring the propagation delay of the data and of the clock (but also other signals, e.g. the LE, are important) and, if necessary, the clock should be conveniently conditioned.

It is also important to consider how the voltages (the device voltage supplies VDD and the LED voltage rail VLED) are connected (same source or separate).

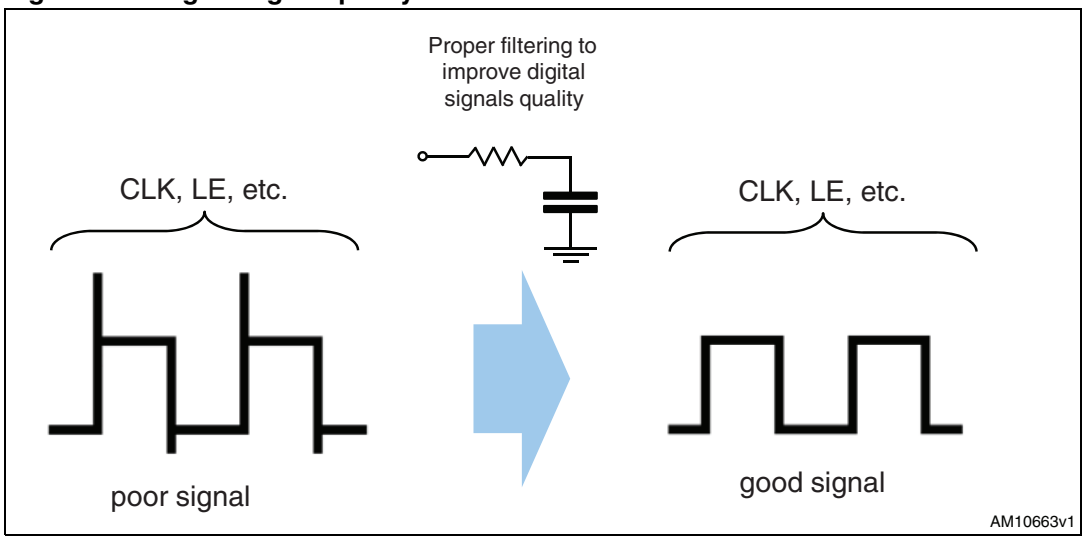
Particular attention should be paid to the correct filtering of the voltages. Too noisy VDD, for instance, could damage the IC.

For this reason a proper filtering of the voltages is necessary and it is recommended to put a capacitor very close to the supply voltage pins of the device.

Also the integrity of the digital signals (CLK, LE, etc.) should be checked, preventing devices from receiving over driving signals (see *Figure 63*).

Suitable solutions should be implemented in case of poor signals (*Figure 63*).

Figure 63. Digital signal quality



Other recommendations involve the position of the devices on the application board compared to the LED arrangements. Some precautions should be considered (avoiding too long wires or traces, tortuous paths, careful clock distribution, etc.), although there are often also restrictions due to the application itself (e.g. shape of the board, particular LED arrangement, etc.).

Finally, for correct power dissipation and to prevent overheating of the device, it is very important to properly solder the exposed pad of the package (if present in the selected package) to the dedicated copper pad, following the indications (in terms of size) provided for that kind of package.

7 Revision history

Table 6. Document revision history

Date	Revision	Changes
13-Jan-2012	1	Initial release.