AN4057
Application note

SPC560Pxx, SPC56APxx, RPC56APxx power up HW guideline

Introduction

This application note is addressed to system hardware designers using STMicroelectronics® SPC560Pxx/SPC56APxx/RPC56APxx microcontrollers. It gives design references to ensure a reliable microcontroller power up sequence also in the condition of an offset voltage on the high voltage regulator supply pin $V_{DD\_HV\_REG}$ at power up.

The use of the SPC560Pxx/SPC56APxx/RPC56APxx internal voltage regulator requires a specific design ST approved ballasts with the recommended supporting network described in the latest revision of the device data sheet (for further details see *Section Appendix A: Additional information*). It is important to respect the power on sequence conditions, ensuring a monotonic supply ramp starting at ground level and respecting the min and max slew rate on $V_{DD\_HV\_REG}$.

This application note covers:

- Recommended power on sequence conditions;
- Possible deviations injecting an offset voltage on $V_{DD\_HV\_REG}$ and its impact on microcontroller power up;
- Optional proposals to eliminate the effect of offset voltage on $V_{DD\_HV\_REG}$ pin.

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1 Overview

These SPC560Pxx/SPC56APxx/RPC56APxx microcontrollers are members of a new microcontroller family built on the Power Architecture®. The device is supplied externally with a single voltage supply, which can be either 5 V or 3.3 V depending on application requirements. Internally the chip operates with 2 supply voltages, namely the main supply (5 V or 3.3 V) and the core logic supply (1.2 V).

This document provides the guidelines for the recommended configuration of the high and low voltage supply for the internal regulator in order to ensure the correct power up sequence of the microcontroller.

The note describes the application fault conditions that may offset $V_{DD\_HV\_REG}$ significantly and mitigating circuitries to ensure reliable power up in case of these fault conditions. The standard supply circuitry and sequence used in the recommended conditions of initial power up on $V_{DD\_HV\_REG}$ pin starting from ground level are described in the SPC560Pxx/SPC56APxx/RPC56APxx data sheet (for further details see *Section Appendix A: Additional information*).

Possible causes of fault conditions injecting an offset voltage on $V_{DD\_HV\_REG}$ pin are described in the following list:

- Supply microcontrollers I/O V_{IN} while the microcontroller is switched off with shorted supply for $V_{DD\_HV\_REG}$ and $V_{DD\_HV\_IO}$ pins
- Offset voltage injected on $V_{DD\_HV\_REG}$ by external signal(s) shorted to battery.

1.1 Power up sequencing

Preventing an overstress event or a malfunction within and outside the device, the SPC560Pxx/SPC56APxx/RPC56APxx implements a specific power up sequence, as described in the data sheet, to ensure each module is started only when all conditions for switching it ON are available.

In case of a fault condition on the application board, that sequence may not be respected, causing the device not to exit the power up.

Two possible fault conditions are described in the following sections. However, if the fault cause is removed, the device (while within the absolute maximum ratings) works again, without getting damaged, powering up properly.

2 Offset voltage on $V_{DD\_HV\_REG}$ and voltage regulator circuitry

2.1 Offset voltage on $V_{DD\_HV\_REG}$: problem description

$V_{DD\_HV\_REG}$ offset on the devices SPC560Pxx/SPC56APxx/RPC56APxx, before the module is powered up, may in some cases prevent the power up device correctly.

A $V_{DD\_HV\_REG}$ offset before a correct power up supply sequence can set the POR device logic to an undefined state, preventing the internal logic to switch correctly and initialize the internal V_{DD_LV} circuitry. The internal regulator remains in power down. The consequence is that the microcontroller is not able to exit reset.

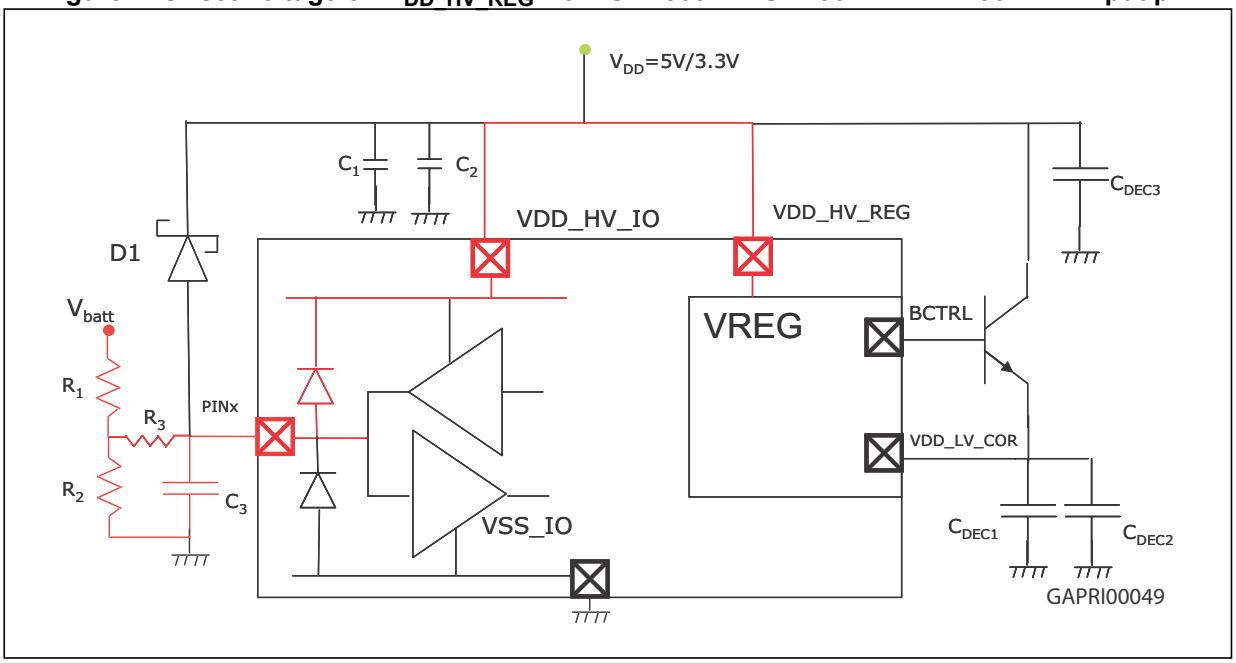
2.1.1 Possible application paths to induce a $V_{DD\_HV\_REG}$ offset voltage

Figure 1 describes a GPIO configuration with the pin connected to an externally supplied signal (V_{batt}).

If V_{batt} is powered while MCU V_{DD} is not yet provided, GPIO protection circuitry (diode) induces a voltage on $V_{DD\_HV\_IO}$.

In case $V_{DD\_HV\_IO}$ is directly connected to $V_{DD\_HV\_REG}$, the induced voltage is propagated to the internal regulator. The same consideration is done when using an external diode, D1 in *Figure 1*, connecting GPIO V_{IN} to V_{DD}.

Figure 1. Offset voltage on $V_{DD\_HV\_REG}$ from SPC560Pxx/SPC56APxx/RPC56APxx input pin

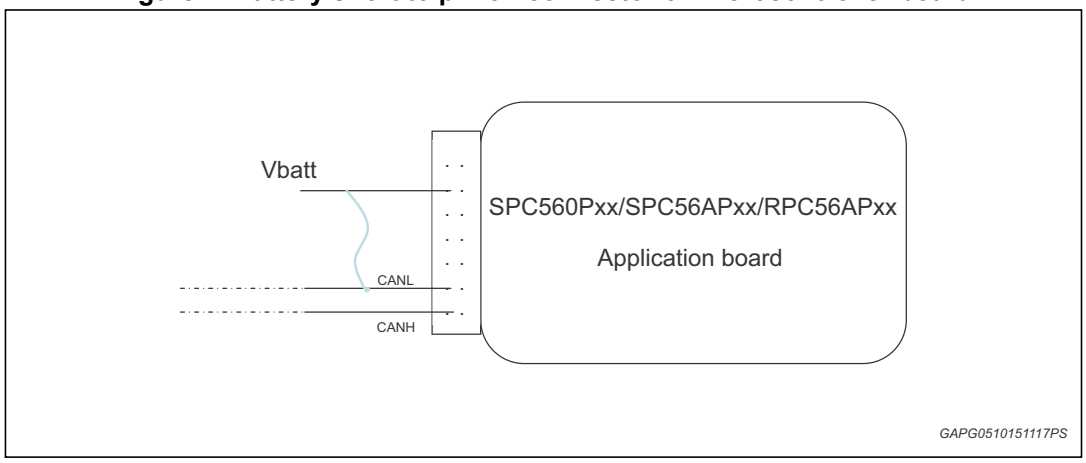


2.1.2 Battery short to pin on connector of microcontroller board

Another possible cause of an initial offset on $V_{DD\_HV\_REG}$ is battery short to any pin of the board connector.

The short to battery can be propagated through various components (ASSP, ASICs, Com Drivers) to the $V_{DD\_HV\_REG}$ as these components typically share the same supply.

Figure 2. Battery short to pin on connector of microcontroller board



2.2 HW guidelines for high/low voltage supply of the internal regulator with offset voltage on $V_{DD\_HV\_REG}$

In general an offset voltage must be avoided to pre-charge $V_{DD\_HV\_REG}$ through parasitic paths. The MCU supply must power on from GND to power supply with a monotonic ramp rate, minimum and maximum value as described in the data sheet (T_{vdd}). In case of a fault condition, injecting an offset to $V_{DD\_HV\_REG}$ while the MCU is not supplied, the following modifications on the module can prevent the device from remaining in reset. The supply voltage conditions are still respected.

Possible HW solutions on the supplying circuitry of the microcontroller to allow a correct power up sequence, in case of an offset build up on $V_{DD\_HV\_REG}$ pin are:

- Resistive network between $V_{DD\_HV\_REG}$, $V_{DD\_LV\_REG}$ and GND;
- Active discharge on V_{DD} or $V_{DD\_HV\_REG}$ at power up;
- Other application means to prevent the presence of an offset on $V_{DD\_HV\_REG}$ during power up.

2.2.1 Resistors partition network

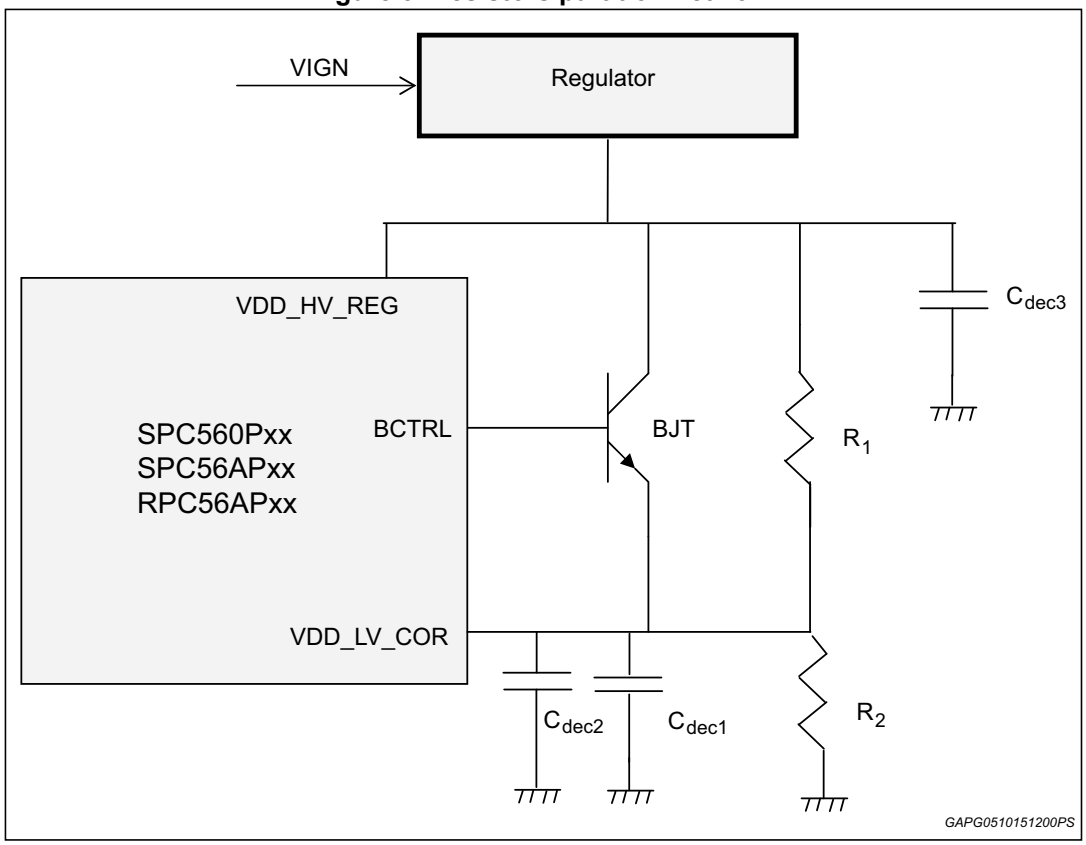
This solution with two partitioning resistors, shown in *Figure 3*, enables $V_{DD\_LV\_REG}$ to be pre-conditioned and the internal $V_{DD\_LV\_REG}$ to be forced into a defined state as soon as the ballast regulator turns-on.

Table 1. Resistor partition network values

	Symbol	Parameter	Value	Unit
$V_{DD\_HV\_REG}$@ 5 V	R1	Resistor between $V_{DD\_HV\_REG}$/ballast emitter and ballast collector	910	Ω
	R2	Resistor between ballast emitter and ground	300	Ω
$V_{DD\_HV\_REG}$@ 3.3 V	R1	Resistor between $V_{DD\_HV\_REG}$/ballast emitter and ballast collector	510	Ω
	R2	Resistor between ballast emitter and ground	300	Ω

Static consumption has to be considered into the board voltage regulator design.

Figure 3. Resistors partition network



2.2.2 $V_{DD\_HV\_REG}$ pin active path to ground

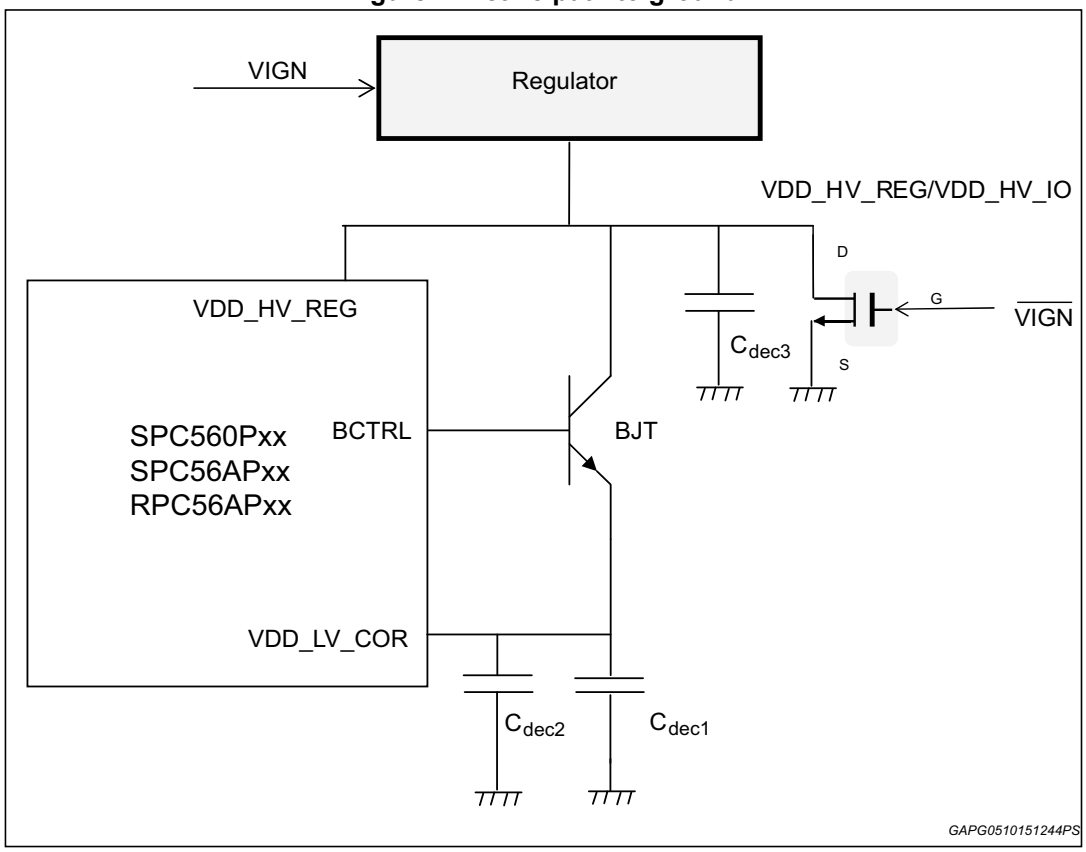
Another solution is to add a controlled active path to ground on $V_{DD\_HV\_REG}$/$V_{DD\_HV\_IO}$ that forces these pins to ground when the microcontroller is switched off or discharges the $V_{DD\_HV\_REG}$ at start up.

Figure 4 describes a generic configuration that uses the enable signal of an external regulator, VIGN, to drive the gate of NFET to force $V_{DD\_HV\_REG}$/$V_{DD\_HV\_IO}$ pin to ground.

When the external regulator is off there is a discharge path of the current from the $V_{DD\_HV\_REG}$/$V_{DD\_HV\_IO}$.

It has to be granted that the V_{DD} rises with the required monotonic slew rate before any fault condition can build up an offset on $V_{DD\_HV\_REG}$, prior to the release of the active discharge circuit.

Figure 4. Active path to ground



3 SPC560Pxx/SPC56APxx/RPC56APxx devices affected

Table 2 lists the STMicroelectronics SPC560Pxx/SPC56APxx/RPC56APxx devices and revisions that are affected by the previously described phenomenon.

Table 2. SPC560Pxx/SPC56APxx/RPC56APxx devices affected from $V_{DD\_HV\_REG}$ offset issue

Part number	Package device marking mask identifier and silicon version	MIDR1 register
SPC560P34xx/P40xx	AB - cut 1.1 (and older)	MAJOR_MASK[3:0]: 4'b0000 MINOR_MASK[3:0]: 4'b0001
SPC560P50xx/P44xx	BD - cut 3.4 (and older)	MAJOR_MASK[3:0]: 4’b0001 MINOR_MASK[3:0]: 4’b0101
SPC560P60xx/P54xx SPC56AP60xx/AP54xx RPC56AP60xx	AA - cut 1.0	MAJOR_MASK[3:0]: 4’b0000 MINOR_MASK[3:0]: 4’b0000

Appendix A Additional information

A.1 Reference document

- 32-bit Power Architecture® based MCU with 1088 KB Flash memory and 80 KB RAM for automotive chassis and safety applications (SPC560P54x, SPC560P60L3, SPC56AP54L3, SPC56AP60x, Doc ID 18340)
- 32-bit Power Architecture® based MCU with 320 KB Flash memory and 20 KB RAM for automotive chassis and safety applications (SPC560P34L1, SPC560P34L3, SPC560P40L1, SPC560P40L3, Doc ID 16100)
- 32-bit Power Architecture® based MCU with 576 KB Flash memory and 40 KB SRAM for automotive chassis and safety applications (SPC560P44L3, SPC560P44L5, SPC560P50L3, SPC560P50L5, Doc ID 14723)

Revision history

Table 3. Document revision history

Date	Revision	Changes
01-Mar-2012	1	Initial release.
13-Sep-2013	2	Updated disclaimer.
29-Oct-2015	3	Robust root part numbers added.