AN4076
Application note

Two or three shunt resistor based current sensing circuit design in 3-phase inverters

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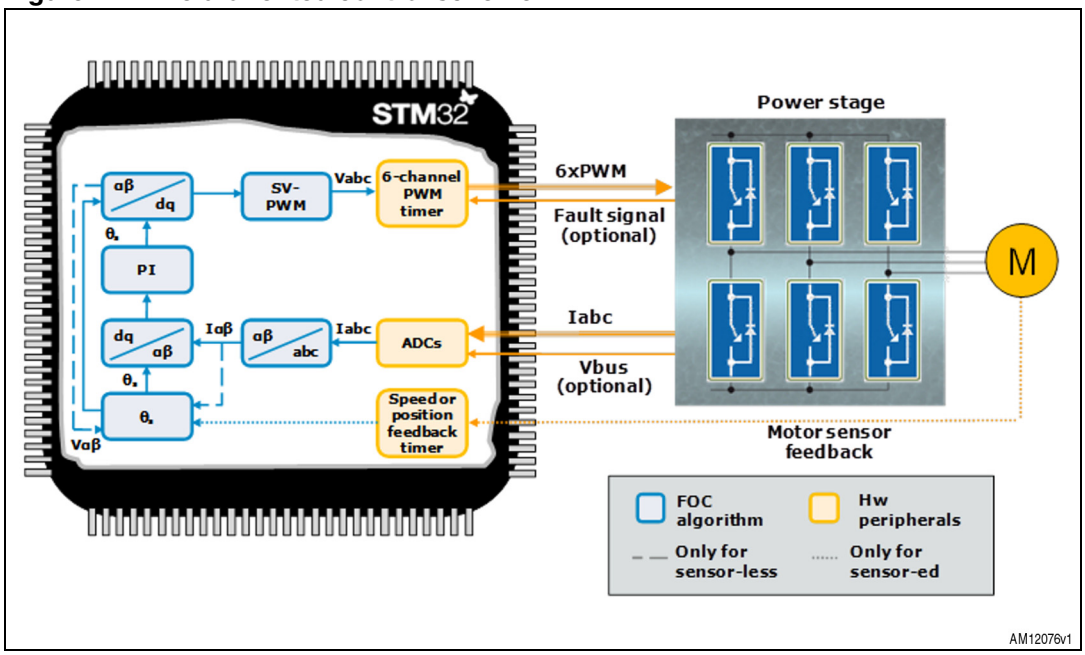
Introduction

The ever increasing market demand for energy efficient systems - from motor vehicles to home appliances, robotics to medical equipment, etc. - is pushing toward the adoption of more and more efficient electric motors (e.g. 3-phase synchronous motors) and drives. The field oriented control (FOC) scheme meets this demand while allowing, at the same time, the achievement of a better regulation of electric motor torque and speed together with a higher efficiency compared with many other solutions available on the market today.

This leads firstly to energy savings but at the same time to better performing systems: more silent dishwashers and washing machines, better temperature regulation in air conditioned environments or in refrigerators, higher autonomy in electric vehicles and much more. As shown in *Figure 1*, the FOC scheme requires a knowledge of the controlled 3-phase motor current; very often (for sensorless implementations) this is the only direct feedback between the control unit and the electric motor. A precise and accurate motor current measurement is therefore essential for the purpose of achieving satisfactory drive performance and, on the contrary, an untailored sensing circuit may prevent the systems from even running.

Figure 1. Field oriented control scheme



Several hardware topologies can be used to measure motor currents; the aim of this document is to provide designers with some useful tips for the design of the motor current sensing circuit in a case where two (or three) shunt resistors, placed on the bottom of two (or three) inverter legs, are used.

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1 Current sensing circuit design guidelines

Figure 2 shows, in more detail, the block diagram of the power stage where two (or three) shunt resistors are placed on the bottom of two (or three) inverter legs.

Figure 2. Power stage block diagram (three-shunt-resistor case)

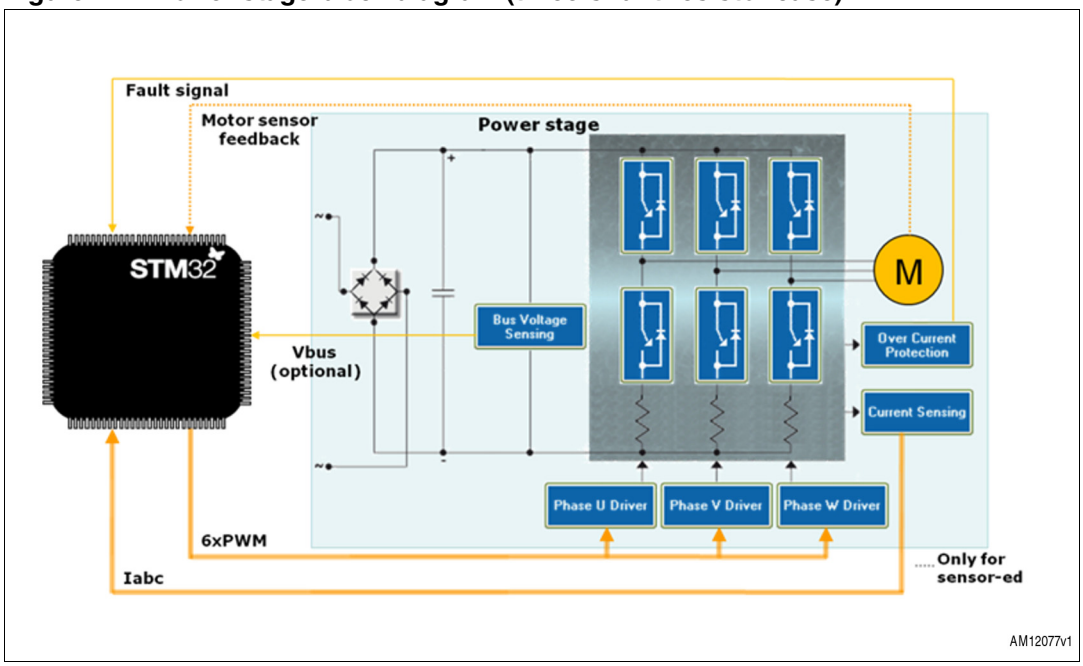
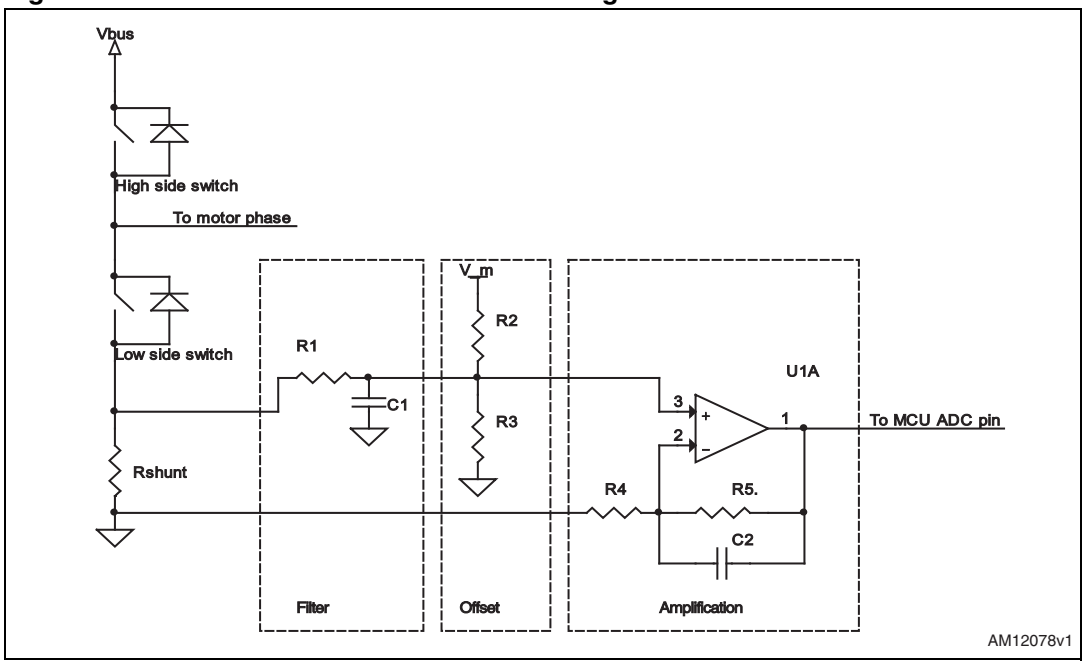


Figure 3 is the electrical circuit actually used for the proper conditioning of the signals on each of the two (or three) shunt resistors (generically referred to as 'Current sensing' in *Figure 2*). The voltage across the shunt resistor is filtered, shifted and finally amplified. Each of these tasks requires attention and are discussed separately.

Figure 3. Motor current feedback conditioning circuit



1.1 Shunt resistors dimensioning

The starting point for the design of the current sensing network is the dimensioning of the shunt resistor (R_{shunt}). The bigger the resistor value, the higher the voltage drop for a given current, and therefore the available useful signal. On the other hand, power dissipation on the shunt resistor increases together with its resistance value, so the value of resistance mainly depends on what is the maximum power dissipation (P_{MAX}) acceptable for the component.

It is therefore important to know how to calculate the power dissipation on the shunt resistor as a function of the expected maximum motor current (that is the motor rated phase current).

In fact, it must be noted that the motor phase current really flows through the shunt resistor only if the low-side transistor of the same leg is turned on. Fortunately, if we consider a full motor phase current electrical period, the average duty cycle applied to the low-side switch is always 50% in ideal conditions (constant bus voltage, constant torque and speed, sinusoidal motor B-emf, …), independently from the modulation index which is used for the space vector modulation (SV-PWM) and which fixes the portion of bus voltage really applied to the motor phases.

Additionally, as shown in *Figure 4*, the SV-PWM duty cycle applied at angle $\theta+\Pi$ is complementary to the duty cycle applied at θ. For this reason the integral $\int_0^T i_R^2(t)dt$ may be graphically computed (see red lines of *Figure 4*) as $\frac{1}{2}\int_0^T i_S^2(t)dt$ ($i_S(t)$ being the motor phase current and $i_R(t)$ the resistor current).

Power dissipated on shunt resistor:

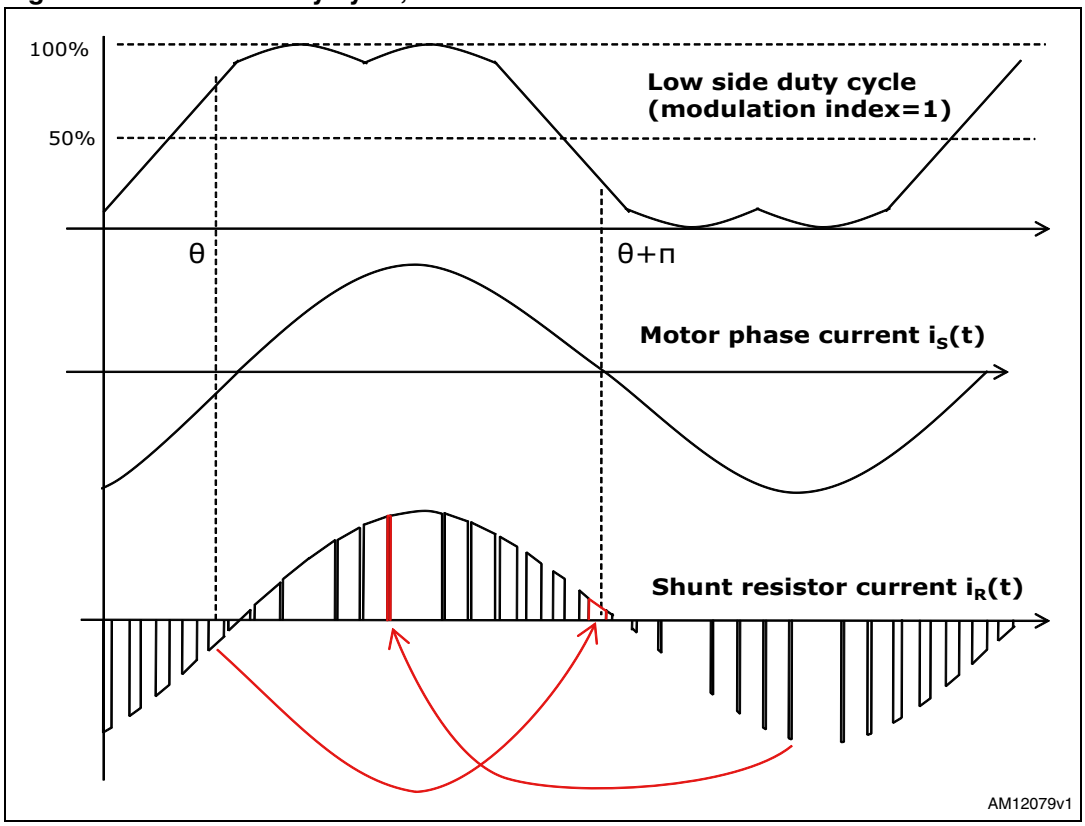
$$P = \frac{1}{T}\int_0^T v(t)i(t)dt = \frac{R_{shunt}}{T}\int_0^T i_R^2(t)dt$$

can therefore be expressed as:

$$\frac{R_{shunt}}{2T}\int_0^T i_S^2(t)dt = \frac{R_{shunt}\cdot I_{sRMS}^2}{2}$$

where I^2_{sRMS} is the motor phase current RMS value. Note that this does not depend on modulation index or voltage-current phase shift.

Figure 4. SV-PWM duty cycle, motor current and shunt resistor current



Finally, it is then possible to compute the shunt resistor value as $R_{shunt} = \frac{2P_{MAX}}{I^2_{SRMS}}$.

1.2 Signal filtering section

When the lower transistor of a leg turns on, there is a very high di/dt in the shunt resistor (especially considering the recovery current of the diode in anti-parallel to the upper switch). Due to the always present parasitic elements (e.g. series inductance of the traces or the shunt resistor itself), this di/dt causes the establishing of oscillations on the voltage on the shunt resistor delaying its settling-down to the real motor phase current (see also *Figure 5* and *6*).

Although oscillations may be reduced by minimizing the parasitic inductance of the traces (proportional to their length and inversely proportional to their width), some filtering is always necessary to clean up the feedback signal and possibly make it go to its steady-state faster, enlarging in this way the range of time during which the current feedback signals may be read by the downstream microcontroller unit.

On the other hand, the filtering can't be too strong because, as already mentioned, the current flows in the shunt resistor only during the on-time of the low-side switch. Considering that the duty cycle applied to this transistor can be very low and that the FOC algorithm requires the current to be read each PWM cycle, having a strong filtering would in fact result in a sensible limitation of the minimum duty cycle applicable (i.e. of the bus voltage exploitation) for keeping the current reading possible.

A tailoring of the filtering stage would be then required for each new design (as it depends on the speed of the switch turn-on, the diode recovery charge, the parasitic inductances, etc.). As a general guideline, an RC filter with a time constant between 100 ns and 200 ns usually accomplishes this task pretty well. If necessary, a further RC filter with similar time constant may be added in the amplifying section by putting a capacitor (C2 in *Figure 3*) in parallel to the feedback resistor.

1.3 Amplification section

After each of the signals on the shunt resistors have been filtered, amplification is required for each of them in order to adapt the signals to the range of voltage that can be read by the analog-to-digital converter (ADC) peripheral embedded in the microcontroller unit (MCU). The non-inverting configuration shown in *Figure 3* is usually used in STEVAL boards.

As can be seen, as the signal on the shunt resistor can be both positive and negative, while the MCU can only read positive voltage, an offset is added (R2, R3) so that the output of the op amp equals about half of the MCU supply voltage when no current flows in the shunt resistor. This offset stage, on the other hand, introduces attenuation (1/G1) of the useful signal which, together with the gain of the non-inverting configuration (G2, fixed by R4 and R5), contributes to the overall gain (G).

As mentioned, the goal here is to establish the overall amplification network gain (G) so that the voltage on the shunt resistor corresponding to the maximum motor allowed current ($I_{s\ max}$, peak vale of motor rated current) fits the range of voltages readable by the ADC. In particular, gain G and polarization voltage on the output should be chosen so that the range $[-G \cdot R_{shunt} \cdot I_{Smax}; G \cdot R_{shunt} \cdot I_{Smax}]$ covers between 85% and 90% of the

range [0; ADC V_{supply}] leaving the remaining 10-15% as an unavoidable margin in case of not perfect current regulation.

It's clear that in order to maximize the op amp output swing, and therefore the current reading accuracy, it is better to use output rail-to-rail amplifiers able to reach very low voltages (tens of mV) and voltages very close to supply voltage (in case this is the same as ADC supply voltage) before saturating.

It must be noted that, once G is fixed, it is better to compose it by lowering the initial attenuation 1/G1 as much as possible and, therefore, also gain G2. This is important not only to maximize the signal by noise ratio but also to reduce the effect of the op amp intrinsic offset on the output (proportional to G2).

The attached spreadsheet ('Current sensing amplification stage design tool.xlsx ') is intended to be used as a tool for helping designers find the proper values of the resistor

fixing gains G1, G2, G, by keeping the output polarization voltage and the maximum readable current under control.

Finally, it is worth adding some considerations about the necessary dynamic behavior of the op amp. As mentioned, the current flows into the shunt resistor only during the on-time of the corresponding low-side transistor while it equals zero during the off-time. Therefore, when the motor current is close to its peak value, the shunt resistor drop voltage quickly jumps from zero to $R_{shunt} \cdot I_{Smax}$. In order to avoid any delay in the amplification stage (that, as already mentioned, would result in a limitation of the bus voltage exploitation), the output of the op amp must be able to quickly react to this input signal.

The dynamic parameter measuring the speed of the op amp response to high input signals is called slew rate; when using the STM32Fxxx MCU supplied at 3.3 V, a minimum slew rate of about 2 V/µs is required so as to ensure that the op amp output voltage is able to swing from the polarization value to its maximum value in less than 1 µs.

The TSV91x, L639x and SLLIMM embedded op amps are therefore perfectly suitable for the amplification of R_{shunt} voltage thanks to their rail-to-rail, supply voltage range and slew rate characteristics.

2 Layout recommendations

In order to maximize the signal by noise ratio it is very important to accurately design the layout of the printed circuit board (PCB) following some basic principles:

- With reference to *Figure 3*, and for each of the shunt resistors, directly connect R1 and R4 terminals to shunt resistor terminals. Furthermore, these two should go close to each other from resistor to op amp to minimize the introduction of differential electrical noise.
- Keep traces between resistors and op amps far away from high voltage traces (even if on different PCB layers). This would help avoid capacitive couplings.
- Try to place operational amplifiers and related components as close as possible to shunt resistors.
- Follow the suggestions reported in AN2834 about “How to get the best ADC accuracy in STM32F10xxx devices”.

3 Current feedback signal typical waveforms

Figure 5 shows some typical waveforms in the motor current electrical period timeframe:

- Channel 2 is the command for the low-side switch (turn-on signal low level)
- Channel 3 is the motor current feedback conditioned signal (at the op amp output)
- Channel 1 is the voltage on the shunt resistor
- Motor phase current is not reported but can be considered equal to the envelop of the channel 3 waveform.

Figure 6 shows a particular of *Figure 5* in a portion of the PWM period. It's possible to see that voltage oscillations on the shunt resistor are bigger compared to the conditioned signal and that the conditioned signal goes to its steady-state 1 µs later than the low-side turn-on command (T_{rise} time equal to 1 µs).

As a general rule, having a T_{rise} in the range of 1µs is a good achievement for motor powers in the range of 100 W; a 2 µs range is, on the other hand, achievable if power is more in the range of 1HP or higher.

Figure 5. Typical waveform in the motor current electrical period timeframe

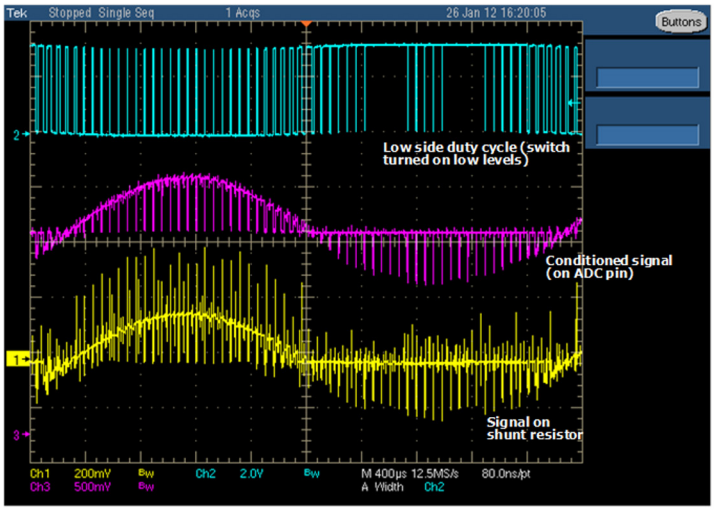
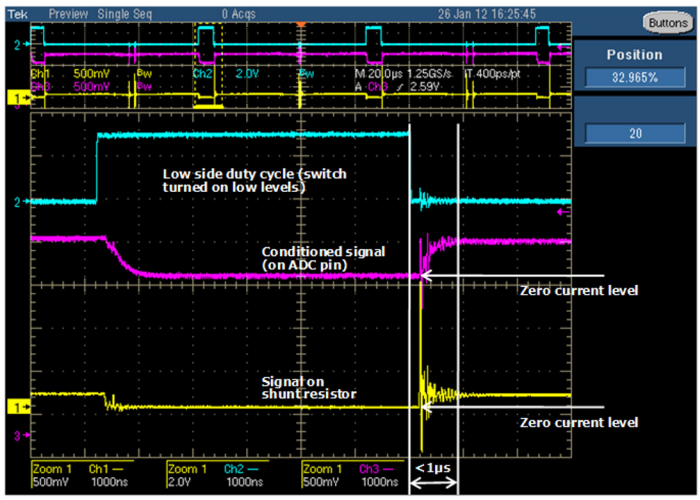


Figure 6. Typical waveforms in the PWM period timeframe



4 References

1. Current sensing amplification stage design tool.xlsx
2. TSV91x datasheet
3. STGIPN3H60 datasheet
4. SLLIMM™ (small low-loss intelligent molded modules) device datasheet
5. STM32Fxxx device datasheets, ARM-based 32-bit MCU
6. L6390 datasheet
7. AN2834 application note.

5 Revision history

Table 1. Document revision history

Date	Revision	Changes
19-Oct-2012	1	Initial release