AN4077
Application note

100 W transition-mode PFC pre-regulator with the new L6564H

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Introduction

This application note describes a demonstration board based on the new transition-mode PFC controller L6564H and presents the results of its bench evaluation. The board implements a 100 W, wide-range mains input, PFC pre-conditioner suitable for ballast, adapters, flat screen displays, and all SMPS having to meet the IEC61000-3-2 or the JEITA-MITI standards.

The L6564H is a current-mode PFC controller operating in transition mode (TM) which embeds the same features existing in the L6564 with the addition of a high-voltage startup source. These functions make the IC especially suitable for applications that must be compliant with energy saving regulations and where the PFC pre-regulator works as the master stage.

Figure 1. EVL6564H-100W: L6564H 100 W TM PFC demonstration board

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1 Main characteristics and circuit description

SMPS main features are listed below:

Table 1. Main characteristics and circuit description

Parameter	Value
Line voltage range	90 to 265V_{ac}
Minimum line frequency (fL)	47Hz
Regulated output voltage	400 V
Rated output power	100 W
Maximum 2fL output voltage ripple	20V pk-pk
Hold-up time	10 ms (V_{DROP} after hold-up time: 300V)
Minimum switching frequency	40kHz
Minimum estimated efficiency	92% (@V_{in}=90 V_{ac}, P_{out}=100 W)
Maximum ambient temperature	50°C
PCB type and size	Single-side, 35 µm, CEM-1, 90x83 mm

This demonstration board implements a power factor correction (PFC) pre-regulator, 100 W continuous power on a regulated 400 V rail from a wide-range mains voltage and provides for the reduction of the mains harmonics, allowing the European EN61000-3-2 or the Japanese JEITA-MITI standard to be met. The regulated output voltage is typically the input for the cascaded isolated DC-DC converter that provides the output rails required by the load.

The board is designed to allow full load operation in still air.

The power stage of the PFC is a conventional boost converter, connected to the output of the rectifier bridge D1. It is completed by the coil L2, the diode D3 and the capacitor C6. The boost switch is represented by the Power MOSFET Q1. The NTC R1 limits the inrush current at switch-on. It has been connected on the DC rail, in series to the output electrolytic capacitor, in order to improve efficiency during low line operation because the RMS current flowing into the output stage is lower than the current flowing into the input stage at the same input voltage, therefore efficiency is increased. The board is equipped with an input EMI filter necessary to filter the commutation noise coming from the boost stage.

At startup, the L6564H is powered by the V_{CC} capacitor C11 that is charged via the high voltage startup source, the L2 secondary winding and the charge pump circuit (C7, R4, D4 and D5) then generate the V_{CC} voltage powering the L6564H during normal operations. The L2 secondary winding is also connected to the L6564H pin #11 (ZCD) through the resistor R5. Its purpose is to supply the information that L2 has demagnetized, needed by the internal logic for triggering a new switching cycle.

The divider R9, R12, R17 and R19 provides, to the L6564H multiplier, the information of the instantaneous mains voltage that is used to modulate the peak current of the boost.

The resistors R2, R8, R10 with R13 and R14 are dedicated to sensing the output voltage and feed the L6564H the feedback information necessary to maintain the output voltage

regulated. The components C9, R18 and C8 are the error amplifier compensation network necessary to keep the required loop stability.

The peak current is sensed by resistors R25 and R26 in series to the MOSFET and the signal is fed into pin #4 (CS) of the L6564H via the filter by R24 and C15.

The capacitor C13 and the parallel resistor R27 complete an internal peak-holding circuit that derives the information on the RMS mains voltage. The voltage signal at this pin, a DC level equal to the peak voltage on pin #3 (MULT), is fed to a second input to the multiplier for the 1/V2 function necessary to compensate the control loop gain dependence on the mains voltage. Additionally, pin #5 (VFF) is internally connected to a comparator providing the brownout (AC mains undervoltage) protection. A voltage below 0.8 V shuts down (not latched) the IC and brings its consumption to a considerably lower level. The L6564H restarts as the voltage at the pin rises above 0.88 V.

The divider R3, R6, R11 and R15 provides, to the L6564H pin #6 (PFC_OK), the information regarding the output voltage level. It is required by the L6564H output voltage monitoring and disable functions used for PFC protection purposes.

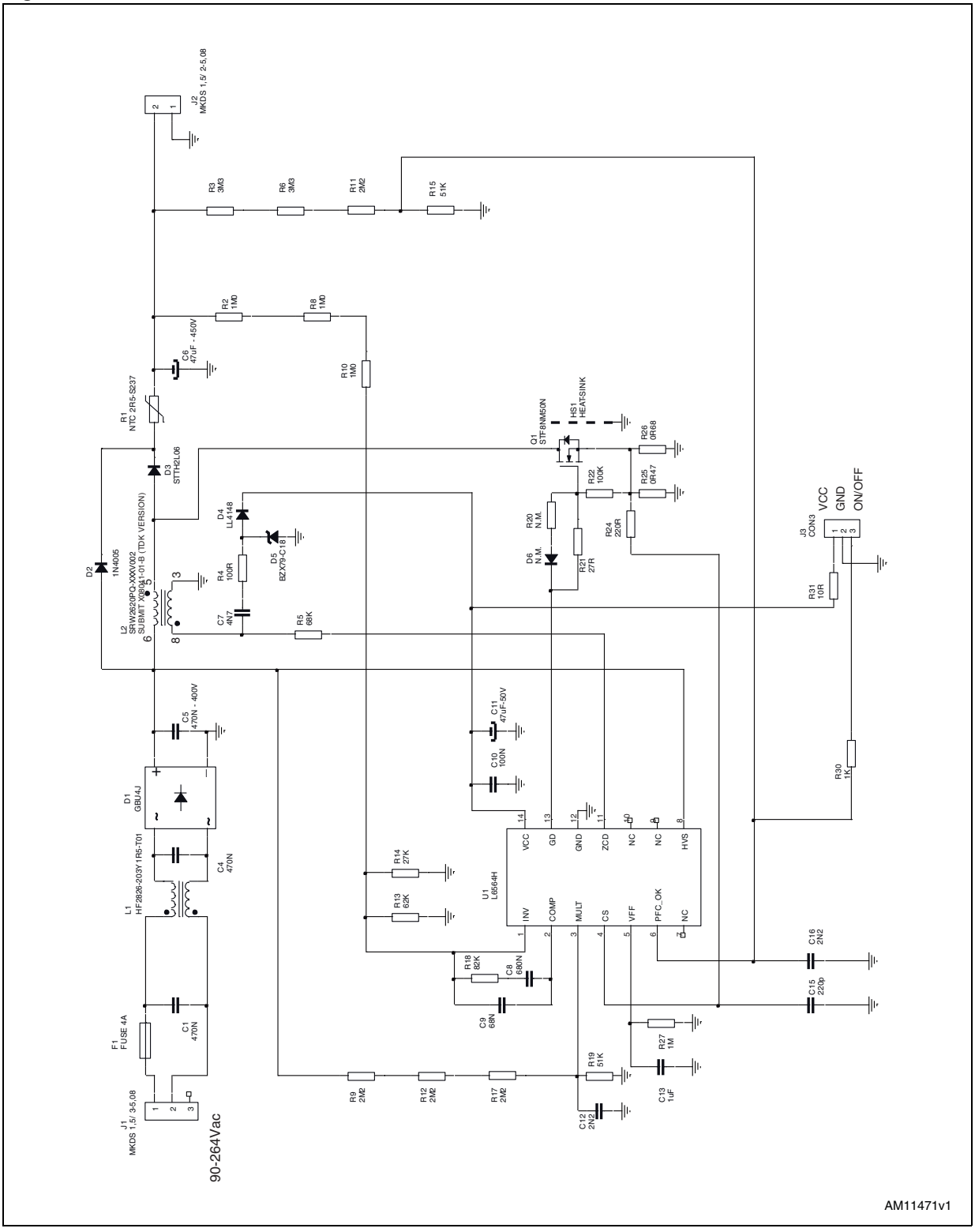
If the voltage on the pin exceeds 2.5 V, the IC stops switching and restarts as the voltage on the pin falls below 2.4 V. However, if at the same time the voltage of the INV pin falls below 1.66 V, a feedback failure is assumed. In this case the device is latched off. Normal operation can be resumed only by cycling V_{CC}, bringing its value lower than 6 V before moving up to turn-on threshold.

Additionally, if the voltage on pin #6 (PFC_OK) is tied below 0.23 V, the L6564H is shut down. To restart the L6564H operation the voltage on pin #6 (PFC_OK) must increase above 0.27 V. This function can be used as a remote on/off control input.

To allow the interfacing of the board with a D2D converter the connector J3 allows the L6564H to be powered with an external V_{CC} and also the IC operation to be controlled via pin #6 (PFC_OK).

2 Electrical diagram

Figure 2. EVL6564H-100W TM PFC demonstration board electrical schematic



3 Bill of material

Table 2. EVL6564H-100W TM PFC demonstration board bill of material

Des.	Part type/part value	Case/package	Description	Supplier
C1	470N	DWG	X2 p.15mm B32922C3474K	EPCOS
C4	470N	DWG	X2 p.15mm B32922C3474K	EPCOS
C5	470N-400V	DWG	400 V-Film cap-B32653A4474	EPCOS
C6	47 µF-450 V	Dia. 18X31.5mm	450 V-Aluminium Elcap-ED series-105°C	Nippon-chemicon
C7	4N7	1206	100 V CERCAP-general purpose	AVX
C8	680N	1206	25 V CERCAP-general purpose	AVX
C9	68N	0805	50 V CERCAP-general purpose	AVX
C10	100N	1206	50 V CERCAP-general purpose	AVX
C11	47 µF-50V	Dia. 5X10mm	50 V-Aluminium Elcap-YXF series-105°C	Rubycon
C12	2N2	1206	50 V CERCAP-general purpose	AVX
C13	1 µF	0805	25 V CERCAP-general purpose	AVX
C15	220p	0805	50 V CERCAP-general purpose	AVX
C16	2N2	1206	50 V CERCAP-general purpose	AVX
D1	GBU4J	STYLE GBU-DWG	Single-phase bridge rectifier	Vishay
D2	1N4005	DO-41	Rectifier-general purpose	Vishay
D3	STTH2L06	DO-41	Ultrafast high-voltage rectifier	ST
D4	LL4148	Minimelf	High-speed signal diode	Vishay
D5	BZX79-C18	DO-35	ZENER diode	Vishay
D6	N.M.	Minimelf		
F1	Fuse 4 A	DWG	Fuse T4A-time delay	Wichmann
HS1	Heatsink	DWG	Heatsink for D1& Q1	
JPX1	MKDS 1,5/ 3-5,08	DWG	PCB Term. block, screw conn., pitch 5mm-3 W	Phoenix contact
JPX2	MKDS 1,5/ 2-5,08	DWG	PCB Term. block, screw conn., pitch 5mm-2 W	Phoenix contact
JPX3	CON3	DWG	PCB term. block, pitch 2.5mm-3 W	Molex
L1	HF2826-203Y1R5-T01	DWG	Input EMI filter-20mH-1.5 A	TDK
L2	SRW2620PQ-XXXV002	DWG	PFC inductor	TDK
Q1	STF8NM50N	TO-220FP	N-channel Power MOSFET	ST
R1	NTC 2R5-S237	DWG	NTC resistor P/N B57237S0259M000	EPCOS

Table 2. EVL6564H-100W TM PFC demonstration board bill of material (continued)

Des.	Part type/part value	Case/package	Description	Supplier
R2	1M0	1206	SMD standard film res.-1/4 W-1%-100 ppm/°C	Vishay
R3	3M3	1206	SMD standard film res.-1/4 W-1%-100 ppm/°C	Vishay
R4	100R	1206	SMD standard film res.-1/4 W-1%-100 ppm/°C	Vishay
R5	68 K	1206	SMD standard film res.-1/4 W-1%-100 ppm/°C	Vishay
R6	3M3	1206	SMD standard film res.-1/4 W-1%-100 ppm/°C	Vishay
R8	1M0	1206	SMD standard film res.-1/4 W-1%-100 ppm/°C	Vishay
R9	2M2	1206	SMD standard film res.-1/4 W-1%-100 ppm/°C	Vishay
R10	1M0	1206	SMD standard film res.-1/4 W-1%-100 ppm/°C	Vishay
R11	2M2	1206	SMD standard film res.-1/4 W-1%-100 ppm/°C	Vishay
R12	2M2	1206	SMD standard film res.-1/4 W-1%-100 ppm/°C	Vishay
R13	62 K	0805	SMD standard film res.-1/4 W-1%-100 ppm/°C	Vishay
R14	27 K	0805	SMD standard film res.-1/8 W-1%-100 ppm/°C	Vishay
R15	51 K	1206	SMD standard film res.-1/4 W-1%-100 ppm/°C	Vishay
R17	2M2	1206	SMD standard film res.-1/4 W-1%-100 ppm/°C	Vishay
R18	82 K	0805	SMD standard film res.-1/8 W-5%-250 ppm/°C	Vishay
R19	51 K	1206	SMD standard film res.-1/4 W-5%-250 ppm/°C	Vishay
R20	N.M.	0805		
R21	27R	1206	SMD standard film res.-1/4 W-1%-100 ppm/°C	Vishay
R22	100 K	0805	SMD standard film res.-1/8 W-5%-250 ppm/°C	Vishay
R24	220R	PTH	SFR25 AXIAL stand. film res.-0.4 W-5%-250 ppm/°C	Vishay
R25	0R47	PTH	SFR25 AXIAL stand. film res.-0.4 W-5%-250 ppm/°C	Vishay
R26	0R68	PTH	SFR25 AXIAL stand. film res.-0.4 W-5%-250 ppm/°C	Vishay
R27	1 M	0805	SMD standard film res.-1/4 W-1%-100 ppm/°C	Vishay
R30	1 K	1206	SMD standard film res.-1/4 W-5%-250 ppm/°C	Vishay
R31	10R	1206	SMD standard film res.-1/4 W-5%- 250 ppm/°C	Vishay
U1	L6564H	SO - 16	IC controller	ST

4 Test results and significant waveforms

4.1 Harmonic content measurement

One of the main purposes of a PFC pre-conditioner is the correction of input current distortion, decreasing the harmonic contents below the limits of the relevant regulations. Therefore, this demonstration board has been tested according to the European standard EN61000-3-2 Class-D and Japanese standard JEITA-MITI Class-D, at full load at both the nominal input voltage mains. The circuit is able to reduce the harmonics well below the limits of both regulations from full load down to light load (measurements are reported in *Figure 3* and *Figure 4*). Please note that all measurements and waveforms have been done using a Pi-filter for filtering the noise coming from the circuit, using a 20 mH common mode choke and two 470NF-X2 filter capacitors.

Figure 3. L6564H 100 W TM PFC demonstration board: compliance to EN61000-3-2 standard

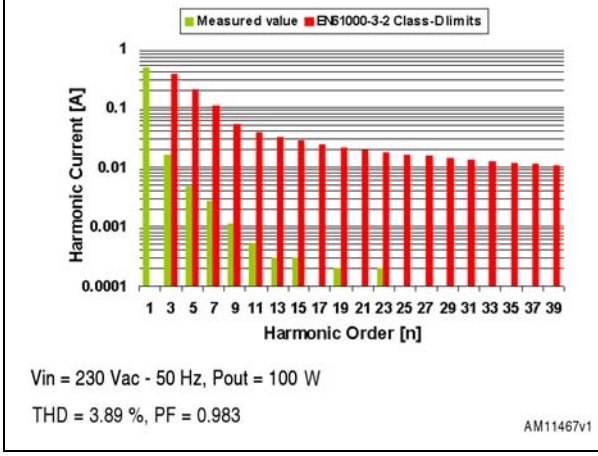
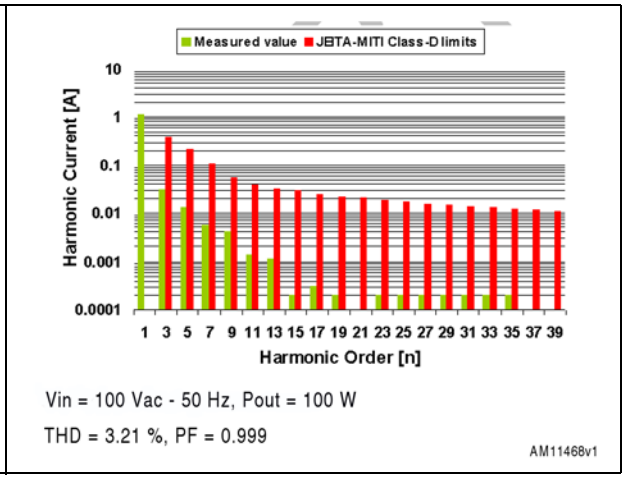


Figure 4. L6564H 100 W TM PFC demonstration board: compliance to JEITA-MITI standard



For user reference, waveforms of the input current and voltage at the nominal input voltage mains and different load conditions are reported in *Figure 5* and *Figure 6*.

Figure 5. L6564H 100 W TM PFC demonstration board: input current waveform at 230 V-50 Hz-100 W load

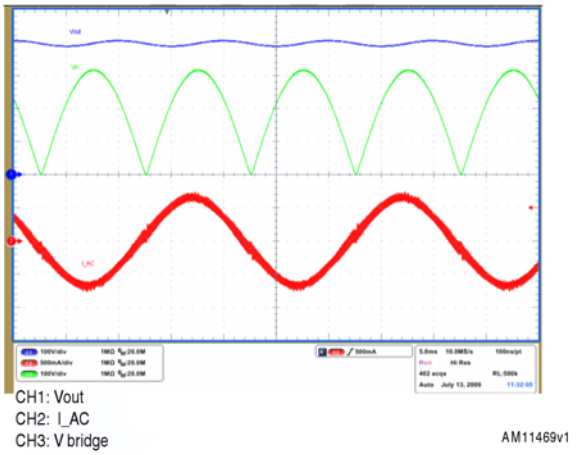
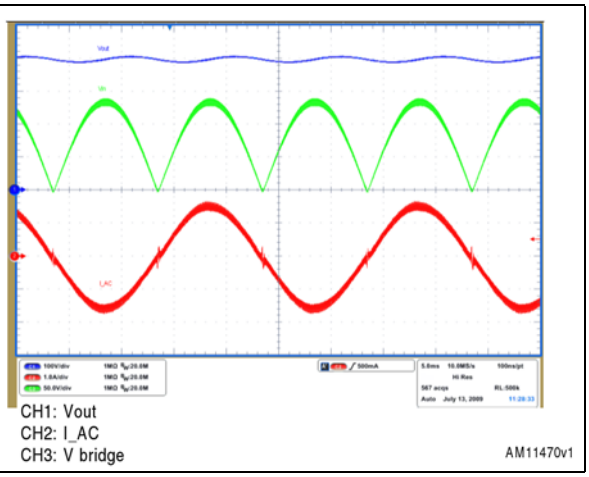


Figure 6. L6564H 100 W TM PFC demonstration board: input current waveform at 100 V-50 Hz-100 W load



The power factor (PF) and the total harmonic distortion (THD) have been measured too and the results are reported in *Figure 7* and *Figure 8*. As can be seen, the PF remains close to unity throughout the input voltage mains and the total harmonic distortion is very low.

Figure 7. L6564H 100 W TM PFC demonstration board: power factor vs output power

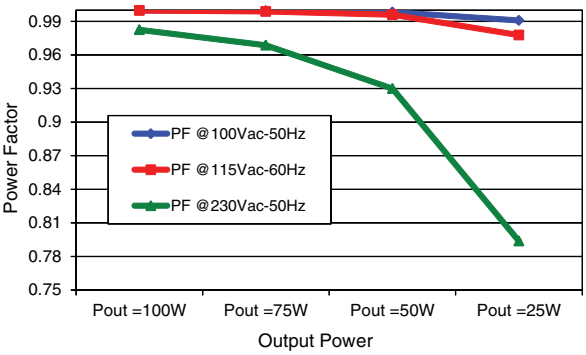
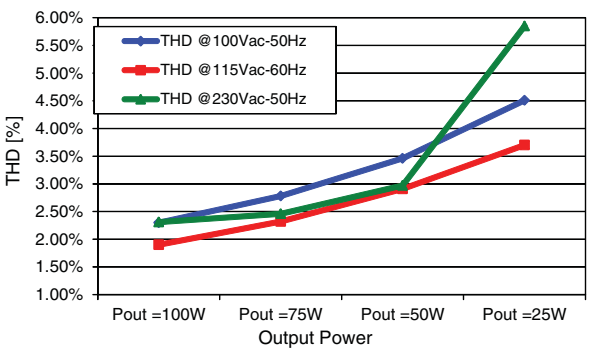


Figure 8. L6564H 100 W TM PFC demonstration board: THD vs output power



The measured efficiency is shown in *Figure 9*, measured according to the ES-2 requirements: it is very good at all load and line conditions. At full load it is always higher than 94%, making this design suitable for high efficiency power supply. The average efficiency calculated according to the ES-2 requirements at different nominal mains voltage are reported in the diagram of *Figure 10*.

Figure 9. L6564H 100 W TM PFC demonstration board: efficiency vs output power

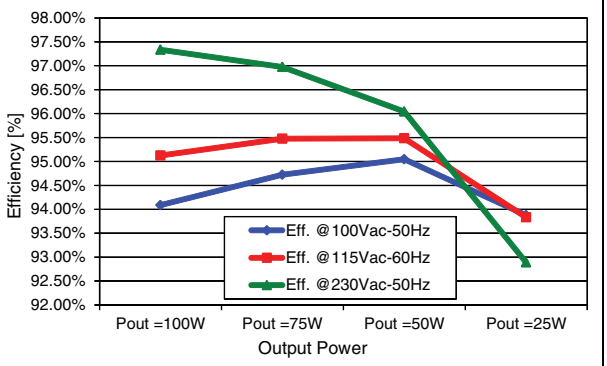
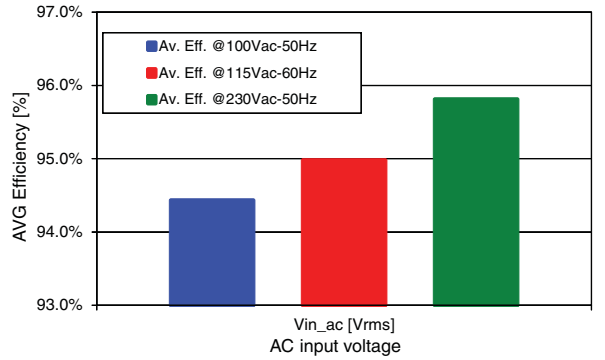
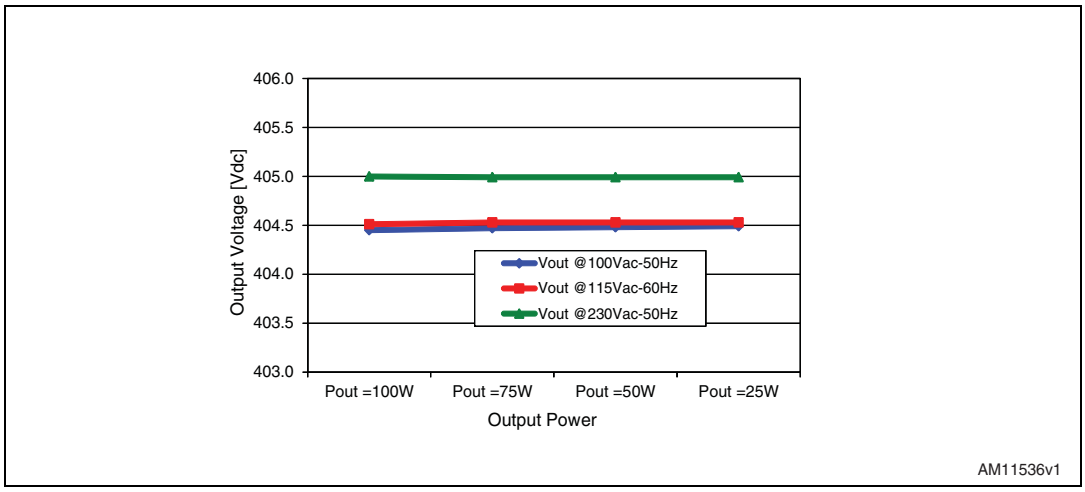


Figure 10. L6564H 100 W TM PFC demonstration board: average efficiency acc. to ES-2



The measured output voltage at different line and static load conditions is reported in the diagram of *Figure 11* on the right. As can be seen, the voltage is very stable over all the input voltage and output load range.

Figure 11. L6564H 100 W TM PFC demonstration board: static V_{out} regulation vs output power

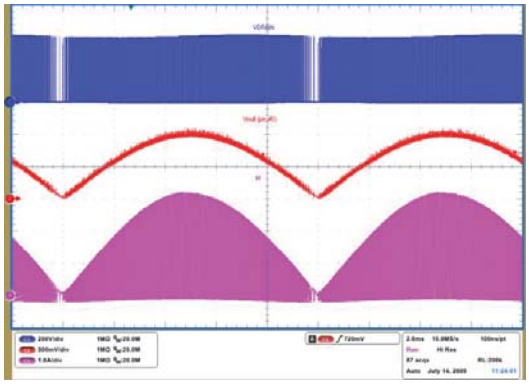


4.2 Inductor current in TM and L6564H THD optimizer

In the following figures the waveforms relevant to the inductor current at different voltage mains are reported: as seen in *Figure 12* and *11*, the peak inductor current waveform over a line half-period follows the MULT (pin #3) at both input mains voltages and therefore the line current is in phase with the input AC voltage, giving low distortion of the current waveform and high power factor. On both the drain voltage traces, close to the zero-crossing points of the sine wave, it is possible to note the action of the THD optimizer embedded in the L6564H. It is a circuit that minimizes the conduction dead-angle occurring to the AC input current near the zero-crossings of the line voltage (crossover distortion). In this way, the

THD (total harmonic distortion) of the current is considerably reduced. A major cause of this distortion is the inability of the system to transfer energy effectively when the instantaneous line voltage is very low. This effect is magnified by the high frequency filter capacitor placed after the bridge rectifier, which retains some residual voltage that causes the diodes of the bridge rectifier to be reverse-biased and the input current flow to temporarily stop. To overcome this issue the device forces the PFC pre-regulator to process more energy near the line voltage zero-crossings as compared to that commanded by the control loop. This results in both minimizing the time interval where energy transfer is lacking and fully discharging the high-frequency filter capacitor after the bridge. Essentially, the circuit artificially increases the ON-time of the power switch with a positive offset added to the output of the multiplier in the proximity of the line voltage zero-crossings. This offset is reduced as the instantaneous line voltage increases, so that it becomes negligible as the line voltage moves toward the top of the sinusoid. Furthermore, the offset is modulated by the voltage on the VFF pin so as to have little offset at low line, where energy transfer at zero-crossings is typically quite good, and a larger offset at high line where the energy transfer gets worse. To get the maximum benefit of the THD optimizer circuit, the high-frequency filter capacitors after the bridge rectifier should be minimized, compatible with EMI filtering needs. A large capacitance, in fact, introduces a conduction dead-angle of the AC input current, therefore reducing the effectiveness of the optimizer circuit.

Figure 12. L6564H 100 W TM PFC demonstration board: Vds and inductor current at 100 V_{ac}-50 Hz-full load



CH1: Q1 Drain voltage
CH2: MULT voltage - Pin # 3
CH4: L2 inductor current

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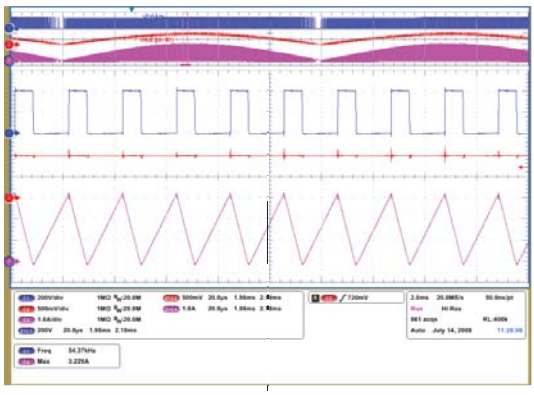
Figure 13. L6564H 100 W TM PFC demonstration board: zoom of Vds and inductor current at 100 V_{ac}-50 Hz-full load



CH1: Q1 Drain voltage
CH2: MULT voltage - Pin # 3
CH4: L2 inductor current

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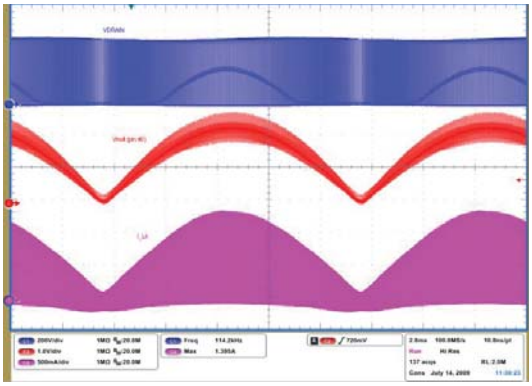
In *Figure 13* and *Figure 14* the detail of the waveforms at switching frequency allows the operating frequency and the current peak at top of the input sine wave during operation at 100 V_{ac} and 230 V_{ac} to be measured. Multiplier waveform has been captured as referenc.

Figure 14. L6564H 100 W TM PFC demonstration board: Vds and inductor current at 230 V_{ac}-50 Hz-full load



CH1: Q1 Drain voltage
CH2: MULT voltage - Pin # 3
CH4: L 2 inductor current

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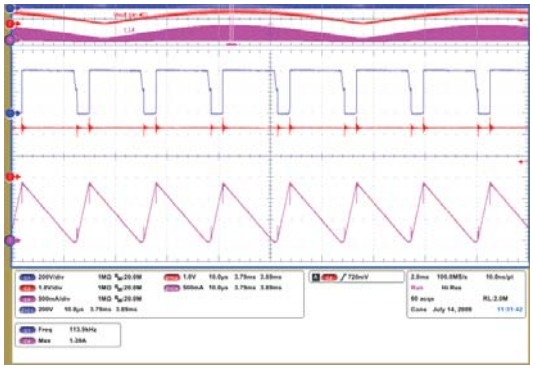
Figure 15. L6564H 100 W TM PFC demonstration board: zoom of Vds and inductor current at 230 V_{ac}-50 Hz-full load

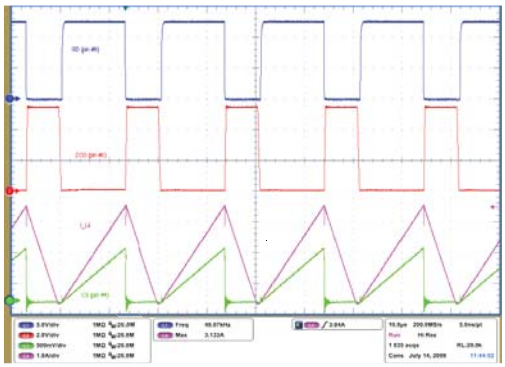


CH1: Q1 Drain voltage
CH2: MULT voltage - Pin # 3
CH4: L 2 inductor current

AM11509v1

In *Figure 16* and *Figure 17* the detail of the waveforms at switching frequency allows the operation of the transition mode control to be seen: once the inductor has transferred all the energy stored, a falling edge on the ZCD pin (pin #11) is detected and it triggers a new ON-time by setting the gate drive high. As soon as the current signal on the CS pin (pin #4) has reached the level programmed by the internal multiplier circuitry according to the input mains instantaneous voltage and the error amplifier output level, the gate drive is set low and MOSFET conduction is stopped. A following OFF-time transfers the energy stored in the inductor into the output capacitor and to the load. At the end of the current conduction a new demagnetization is detected by the ZCD that provides for a new ON-time of the MOSFET.

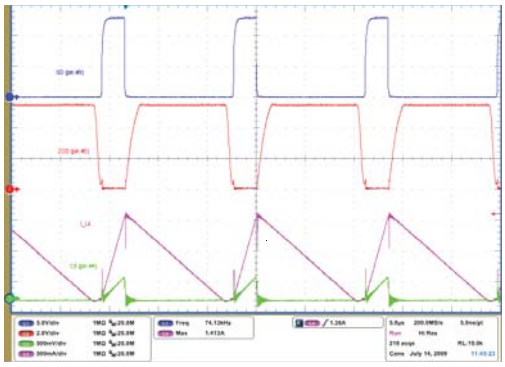
Figure 16. L6564H 100 W TM PFC demonstration board: Vds, ZCD and inductor current at 100 V_{ac}- 50 Hz-full load



CH1: GD - Pin # 13
CH2: ZCD - Pin # 11
CH3: CS - Pin # 4
CH4: L 2 inductor current

AM11510v1

Figure 17. L6564H 100 W TM PFC demonstration board: Vds, ZCD and inductor current at 230 V_{ac}- 50 Hz-full load



CH1: GD - Pin # 13
CH2: ZCD - Pin # 11
CH3: CS - Pin # 4
CH4: L 2 inductor current

AM11511v1

4.3 Voltage feed-forward and brownout function

The power stage gain of PFC pre-regulators varies with the square of the RMS input voltage. As does the crossover frequency FC of the overall open-loop gain because the gain has a single pole characteristic. This leads to large trade-offs in the design. For example, setting the gain of the error amplifier to get fc = 20 Hz @ 264 V_{ac} means having fc 4 Hz @ 88 V_{ac}, resulting in a sluggish control dynamics. Additionally, the slow control loop causes large transient current flow during rapid line or load changes that are limited by the dynamics of the multiplier output. This limit is considered when selecting the sense resistor to let the full load power pass under minimum line voltage conditions, with some margin. But a fixed current limit allows excessive power input at high line, whereas a fixed power limit requires the current limit to vary inversely with the line voltage.

Voltage feed-forward can compensate for the gain variation with the line voltage and allow all of the above-mentioned issues to be overcome. It consists of deriving a voltage proportional to the input RMS voltage, feeding this voltage into a squarer/divider circuit (1/V2 corrector) and providing the resulting signal to the multiplier that generates the current reference for the inner current control loop.

In this way a change of the line voltage causes an inversely proportional change of the half sine amplitude at the output of the multiplier (if the line voltage doubles the amplitude of the multiplier, output is halved and vice versa) so that the current reference is adapted to the new operating conditions with (ideally) no need to invoke the slow dynamics of the error amplifier. Additionally, the loop gain is constant throughout the input voltage range, which significantly improves dynamic behavior at low line and simplifies loop design.

In fact, with other PFC pre-regulators embedding the voltage feed-forward, deriving a voltage proportional to the RMS line voltage implies a form of integration, which has its own

time constant. If it is too small, the voltage generated is affected by a considerable amount of ripple at twice the mains frequency that causes distortion of the current reference (resulting in high THD and poor PF); if it is too large, there is a considerable delay in setting the right amount of feed-forward, resulting in excessive overshoot and undershoot of the pre-regulator output voltage in response to large line voltage changes. Clearly a trade-off was required. The L6564H realizes an innovative voltage feed-forward which, with a technique that makes use of just two external parts, overcomes this time constant trade-off issue whichever voltage change occurs on the mains, both surges and drops. A capacitor CFF and a resistor RFF, both connected from pin VFF (pin #5) to ground, complete an internal peak-holding circuit that provides a DC voltage equal to the peak of the rectified sine wave applied on the MULT pin (pin #3). In this way, in the case of sudden line voltage rise, CFF is rapidly charged through the low impedance of the internal diode; in the case of line voltage drop, an internal “mains drop” detector enables a low impedance switch which suddenly discharges CFF avoiding a long settling time before reaching the new voltage level. Consequently, an acceptably low steady-state ripple and low current distortion can be achieved without any considerable undershoot or overshoot on the preregulator output like in systems with no feed-forward compensation.

Figure 18. L6562A input mains surge 90 V_{ac} to 140 V_{ac}-no VFF input

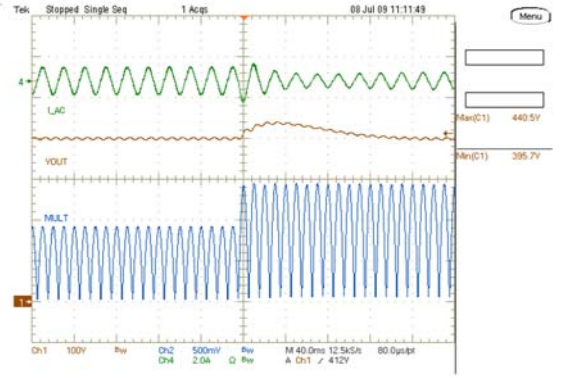
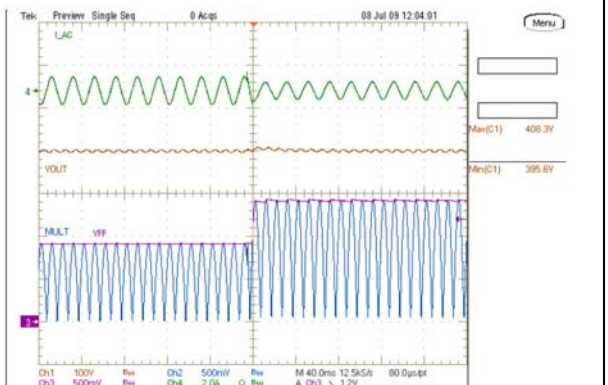


Figure 19. L6564H 100 W TM PFC demonstration board: input mains surge 90 V_{ac} to 140 V_{ac}



In *Figure 19* we see the behavior of the EVL6564H-100W demonstration board in the case of an input voltage surge from 90 to 140 V_{ac}: in the figure it is evident that the VFF function provides for the stability of the output voltage which is not affected by the input voltage surge. In fact, thanks to the VFF function, the compensation of the input voltage variation is very fast and the output voltage remains stable at its nominal value. The opposite is confirmed in *Figure 18*: the behavior of a PFC using the L6562A and delivering the same output power is shown: in the case of a mains surge, the controller cannot compensate it and the output voltage stability is guaranteed by the feedback loop only. Unfortunately, as previously mentioned, its bandwidth is narrow and therefore the output voltage has a significant deviation from the nominal value. The circuit has the same behavior in the case of mains surge at any input voltage, and it is not affected even if the input mains surge happens at any point of the input sine wave.

In *Figure 21* the circuit behavior in the case of mains dip is reported: as previously described, the internal circuitry has detected the decreasing of the mains voltage and it has activated the CFF internal fast discharge. As seen, in this case the output voltage changes but in few mains cycles it returns to the nominal value. The situation is different if the performance of a controller without the VFF function is still checked. In *Figure 20* the behavior of a PFC using the L6562A delivering similar output power is reported: in the case of a mains dip from 140 V_{ac} to 90 V_{ac} the output voltage variation is not very different but the output voltage requires a longer time to restore the original value. When performing tests with a wider voltage variation (e.g. 265 V_{ac} to 90 V_{ac}) the output voltage variation of a PFC without the voltage feed-forward fast discharging is much more emphasized.

Figure 20. L6562A input mains dip 140 V_{ac} to 90 V_{ac}-no VFF input

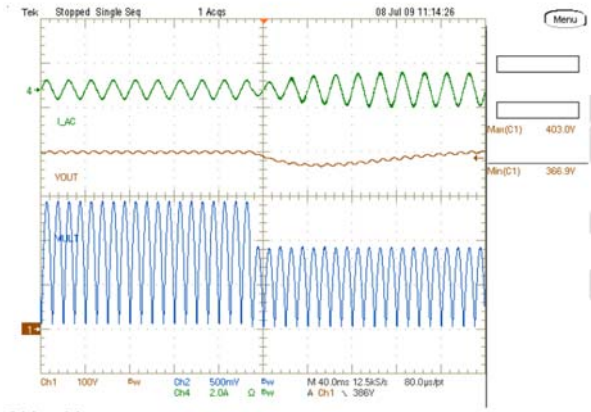
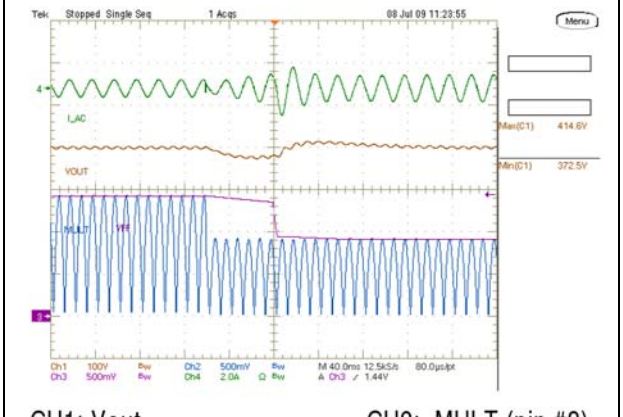


Figure 21. L6564H 100 W TM PFC demonstration board: input mains dip 140 V_{ac} to 90 V_{ac}



The fast discharge system allows to size the external RFF • CFF time constant on the VFF pin in order to minimize the ripple on the CFF capacitor. The effect of this improvement can be appreciated comparing the input current shape in a 100 W PFC board with a controller without fast discharge feature (*Figure 22*) in respect to the input current shape in the same board with the L6564H (*Figure 23*).

In *Figure 23* the input current of the L6564H has a better shape and the 3rd harmonic current distortion is not noticeable: this demonstrates the benefits of the new voltage feed-forward circuit integrated in the L6564H.

Figure 22. L6563 100 W TM PFC demonstration board: input current at 100 V_{ac}-50 Hz CFF=0.47 µF, RFF=390 kΩ

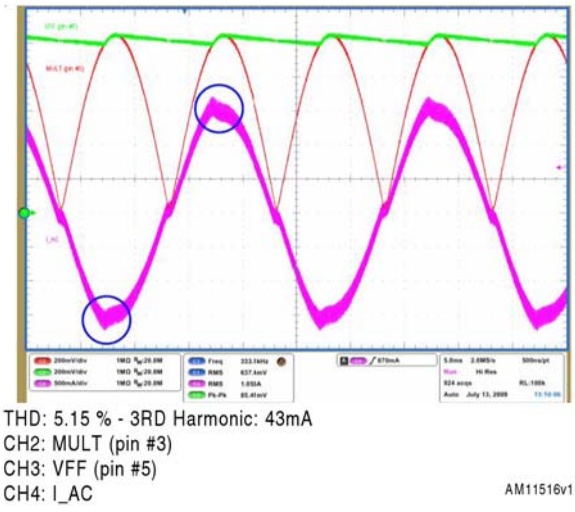
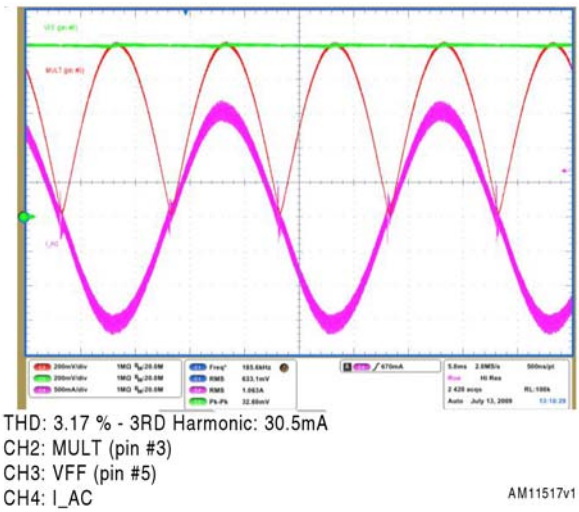
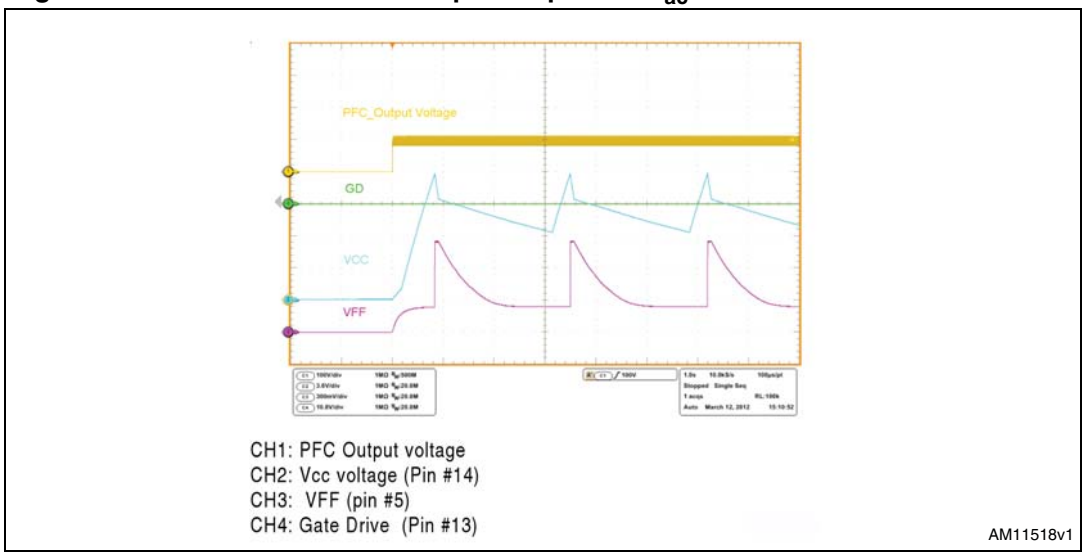


Figure 23. L6564H 100 W TM PFC demonstration board: input current at 100 V_{ac}-50 Hz CFF=1 µF, RFF=1 M



Another function integrated in the L6564H is the brownout protection, which is basically a not-latched shutdown function that must be activated when a mains undervoltage condition is detected. This abnormal condition may cause overheating of the primary power section due to an excess of RMS current. Brownout can also cause the PFC pre-regulator to work in open loop and this may be dangerous to the PFC stage itself and the downstream converter, should the input voltage return abruptly to its rated value. Another problem is the spurious restarts that may occur during converter power-down and that cause the output voltage of the converter not to decay to zero monotonically. For these reasons it is usually preferable to shut down the unit in case of brownout. Brownout thresholds are internally fixed at 0.88 V (typ.) for enabling operation and 0.8 V (typ.) for disabling the L6564H. Sensing of the input mains condition is done by an internal comparator connected to pin VFF (PIN #5) which delivers a voltage signal proportional to the input mains.

Figure 24. EVL6564H-100W startup attempt at 80 V_{ac}-60 Hz-full load



Because the brownout thresholds in the L6564H are internally fixed, the startup and shutdown threshold can be adjusted slightly modifying the resistor values used for the MULT pin. In *Figure 24* a startup tentative below the startup threshold is captured. As seen, at startup the brownout function does not allow the PFC startup even if the V_{CC} has reached the L6564H turn-on threshold.

In *Figure 25* and *26* the circuit waveforms during brownout protection operation are captured. In both cases the mains voltages were increased or decreased slowly: as can be seen, at turn-on or at turn-off there are no bouncing or starting attempts by the PFC converter.

Figure 25. EVL6564H-100W startup with slow input voltage increasing-full load

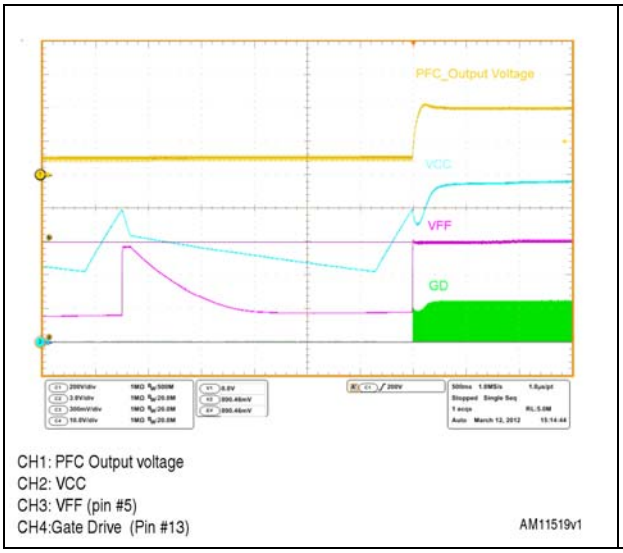
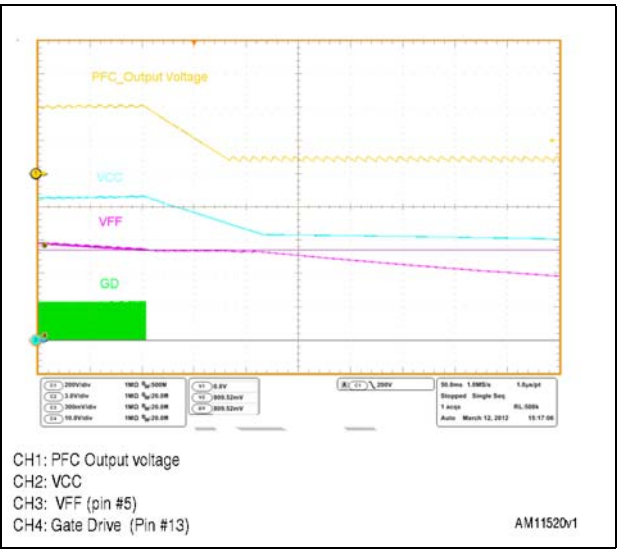


Figure 26. EVL6564H-100W turn-off with slow input voltage decreasing-full load



In *Figure 27* and *28* the waveforms during the startup of the circuit at mains plug-in are reported. Note that the V_{CC} voltage rises up to the turn-on threshold, and the L6564H starts

the operation. For a short time the energy is supplied by the V_{CC} capacitor, and then the auxiliary winding with the charge pump circuit takes over. At the same time, the output voltage rises from peak value of the rectified mains to the nominal value of the PFC output voltage. The good margin phase of the compensation network allows a clean startup, without any large overshoot.

Figure 27. EVL6564H-100W startup at 90 V_{ac}-60 Hz-full load

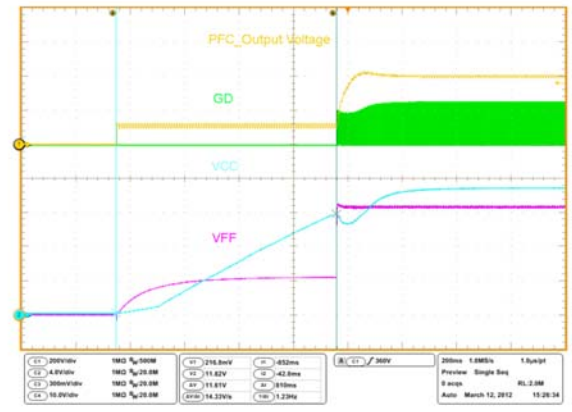
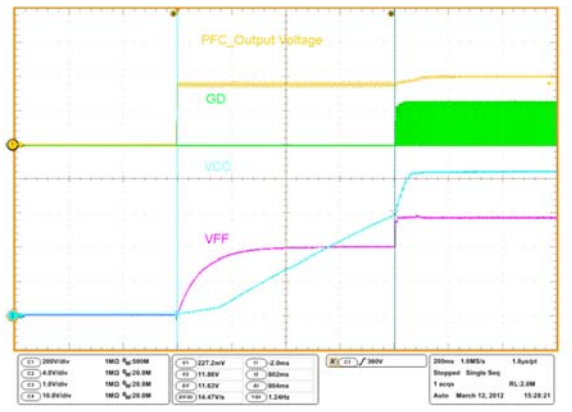


Figure 28. EVL6564H-100W startup at 265 V_{ac}-50 Hz-full load



4.4 PFC_OK pin and feedback failure (open loop) protection

During normal operation, the voltage control loop provides for the output voltage (Vout) of the PFC pre-regulator close to its nominal value, set by the resistors ratio of the feedback output divider. In the L6564H a pin of the device (PFC_OK, pin #6) has been dedicated to monitoring the output voltage with a separate resistor divider made up of R3, R6, R11 (high) and R15 (low), see *Figure 2*. This divider is selected so that the voltage at the pin reaches 2.5 V if the output voltage exceeds a preset value (Vovp), usually larger than the maximum Vout that can be expected, also including worst-case load/line transients.

For the EVL6564H-100W we have:

- Vo = 400 V
- Vovp = 434 V

Select:

- R3+R6+R11= 8.8 MΩ

then:

- R15 = 8.8 MΩ ·2.5/(434-2.5) = 51 kΩ

Once this function is triggered, the gate drive activity is immediately stopped until the voltage on the PFC_OK pin drops below 2.4 V. An example is reported in *Figure 29*.

Note that both feedback dividers connected to the L6564H pin #1 (INV) and pin #6 (PFC_OK) can be selected without any constraints. The unique criterion is that both dividers

must sink a current from the output bus which needs to be significantly higher than the current biasing the error amplifier and PFC_OK comparator.

The OVP function described above is able to handle “normal” overvoltage conditions, i.e. those resulting from an abrupt load/line change or occurring at startup. If the overvoltage is generated by a feedback disconnection, for instance, when one of the upper resistors of the output divider fails open, an additional circuitry detects the voltage drop of the INV pin. If the voltage on the INV pin is lower than 1.66 V and at the same time the OVP is active, a feedback failure is assumed. Therefore, the gate drive activity is immediately stopped, the device is shut down, its quiescent consumption is reduced below 180 µA and the condition is latched as long as the supply voltage of the IC is above the UVLO threshold. To restart the system it is necessary to recycle the input power, so that the V_{CC} voltage of the L6564H goes below 6 V and that of the PWM controllers goes below its UVLO threshold.

Note that this function offers a complete protection against not only feedback loop failures or erroneous settings, but also against a failure of the protection itself. Either resistor of the PFC_OK divider failing short or open, or a PFC_OK pin floating, results in shutting down the IC and stopping the pre-regulator. Moreover, the PFC_OK pin doubles its function as a not-latched IC disable: a voltage below 0.23 V shuts down the IC, reducing its consumption below 2 mA. To restart the IC simply let the voltage at the pin go above 0.27 V.

Figure 29. EVL6564H-100W load transient at 115 V_{ac}-60 Hz-full load to no load

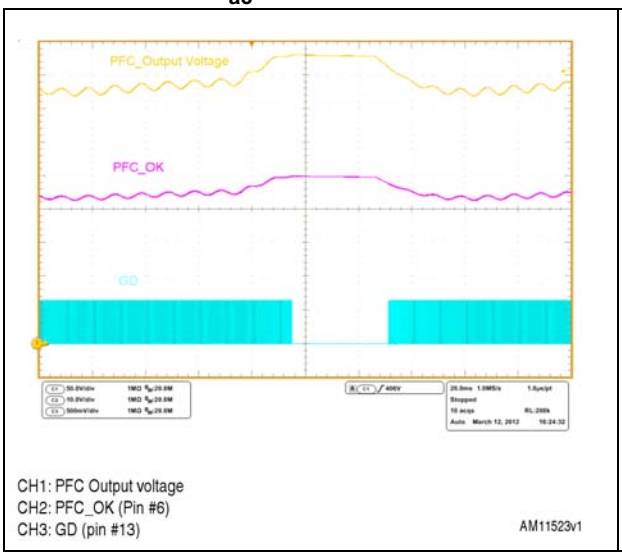
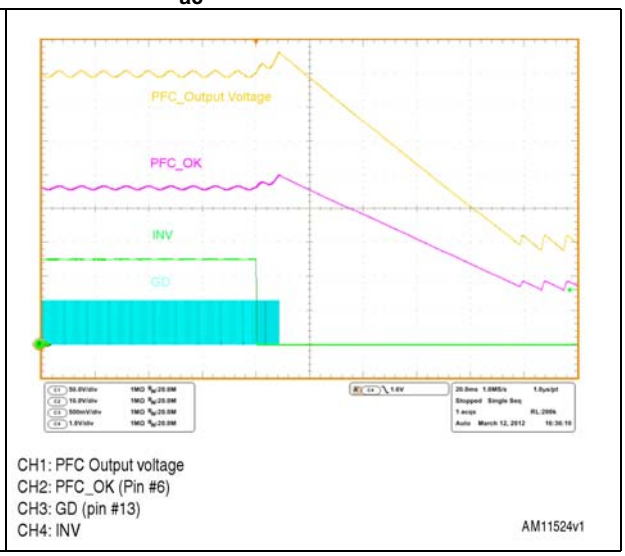


Figure 30. EVL6564H-100W open loop at 115 V_{ac}-60 Hz-full load



The event of an open loop is captured in *Figure 30*, note that the protection intervention latches the operation of the L6564H.

4.5 Power management and housekeeping functions

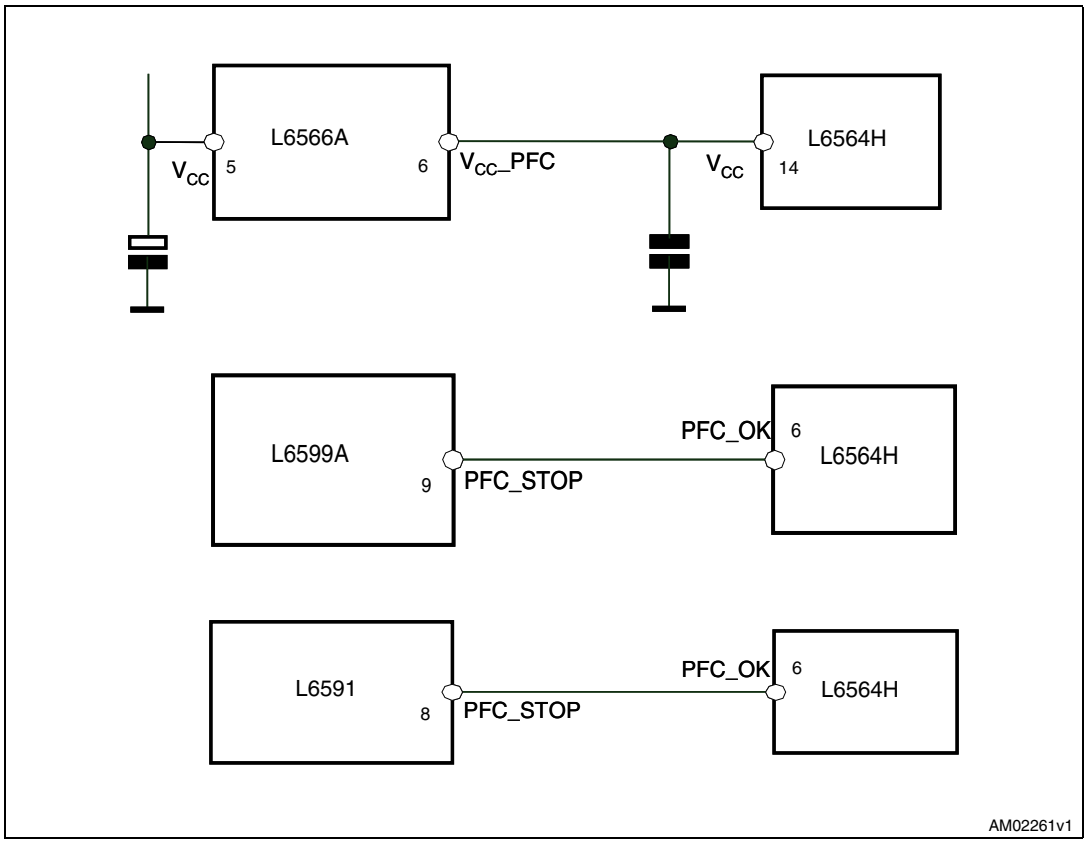
Differently from similar PFC controllers with more pins, the housekeeping functions of the L6564H are minimized but still there, and the device, in spite of the low pin count, still has some main functionalities that make it suitable to be implemented in high-end applications.

For example, in order to save power during light load operation or to put the converter in a safe condition after detecting a failure of the DC-DC converter, a communication line can be

established between the cascade converter and the PFC via the disable function included in the PFC_OK pin (pin #6). Needless to say, this operation assumes that the cascaded PFC converter stage works as the master (thanks also to the integrated brownout function) and the DC-DC stage as the slave or, in other words, that the PFC stage starts first, it powers both controllers and enables/disables the operation of the downstream converter stage. Several PWM controllers by STMicroelectronics have integrated some housekeeping functions for the D2D and offer the possibility to interface directly the L6564H with the downstream PWM controller via dedicated pins.

Should the residual consumption of the chip be an issue, it is also possible to cut down the supply voltage. In this case, such operation assumes that the cascaded DC-DC converter stage works as the master and the PFC stage as the slave or, in other words, that the DC-DC stage starts first, it powers both controllers and enables/disables the operation of the PFC stage. The EVL6564H-100W offers the possibility to test the disable function by connecting it to the cascaded converter of the DC-DC converter. The PFC_OK pin, V_{CC} and ground are available via the series resistors R30 and R31 (*Figure 2*).

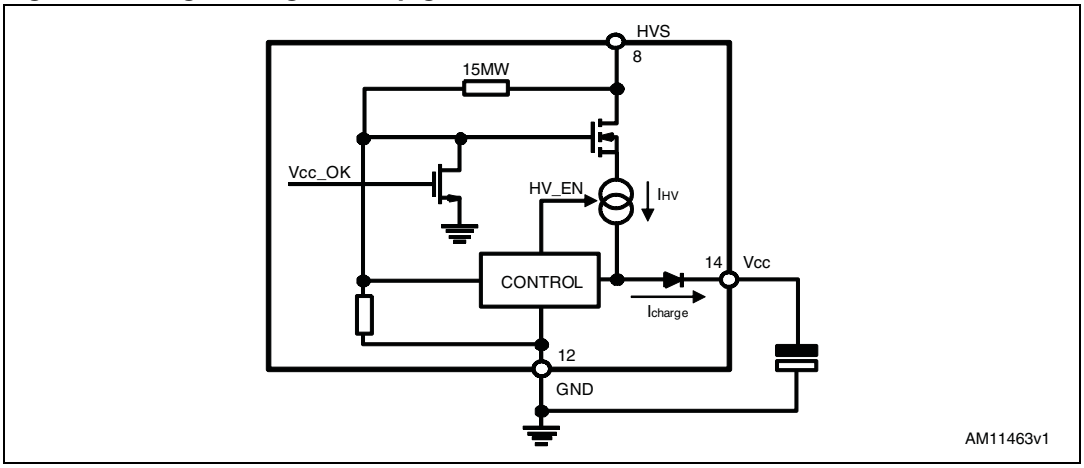
Figure 31. Interface circuits that let DC-DC converter controller IC disable the L6564H



5 High-voltage startup generator

Figure 32 shows the internal schematic of the high-voltage startup generator (HV generator). It is made up of a high-voltage N-channel FET, whose gate is biased by a 15 M resistor, with a temperature-compensated current generator connected to its source.

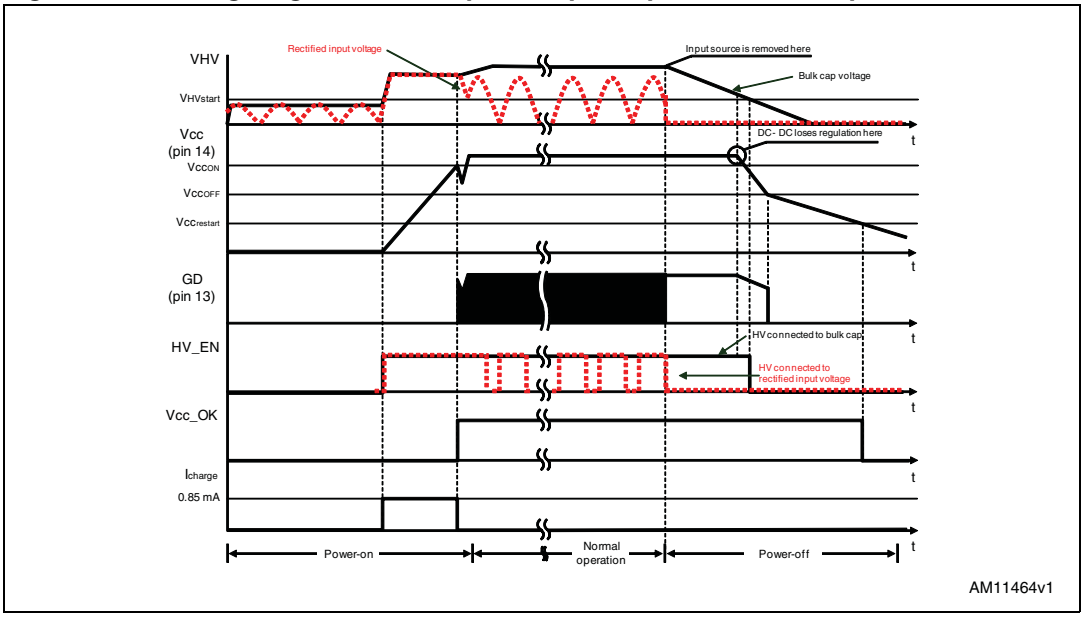
Figure 32. High-voltage startup generator: internal schematic



The HV generator is physically located on a separate chip, made with BCD™ offline technology able to withstand 700 V, controlled by a low-voltage chip, where all of the control functions reside.

With reference to the timing diagram of *Figure 33*, when power is first applied to the converter, the voltage on the bulk capacitor (Vin) builds up and, at about 80 V, the HV generator is enabled to operate (HV_EN is pulled high) so that it draws about 1 mA. This current, minus the device consumption, charges the bypass capacitor connected from pin V_{CC} (14) to ground and makes its voltage rise almost linearly.

Figure 33. Timing diagram: normal power-up and power-down sequences



As the V_{CC} voltage reaches the startup threshold (12 V typ.) the low-voltage chip starts operating and the HV generator is cut off by the V_{CC}_OK signal asserted high. The device is powered by the energy stored in the V_{CC} capacitor until the self-supply circuit (we assume that it is made with an auxiliary winding in the transformer of the cascaded DC-DC converter and a steering diode) develops a voltage high enough to sustain the operation. The residual consumption of this circuit is just the one on the 15 M resistor (10 mW at 400 V_{dc}), typically 50-70 times lower, under the same conditions, as compared to a standard startup circuit made with external dropping resistors.

At converter power-down the DC-DC converter loses regulation as soon as the input voltage is so low that either peak current or maximum duty cycle limitation is tripped. V_{CC} then drops and stops IC activity as it falls below the UVLO threshold (9.5 V typ.). The V_{CC}_OK signal is de-asserted as the V_{CC} voltage goes below a threshold V_{CC}restart located at about 6 V. The HV generator can now restart. However, if Vin < VHVstart, HV_EN is de-asserted too and the HV generator is disabled. This prevents converter restart attempts and ensures monotonic output voltage decay at power-down in systems where brownout protection (see the relevant section) is not used.

If the device detects a fault due to feedback failure, the internal V_{CC}restart is brought up to over the V_{CC}Off (turn-off threshold). As a result, shown in *Figure 34*, the voltage at pin V_{CC}, oscillates between its turn-on and turn-off thresholds until the HV bus is recycled and drops below the startup threshold of the HV generator.

The high-voltage startup circuitry is capable of guaranteeing a safe behavior in the case of short-circuit present on the DC-DC output when the V_{CC} of both controllers are generated by the same auxiliary winding. *Figure 39* shows how the PFC manages the V_{CC} cycling and the associated power transfer. At short-circuit the auxiliary circuit is no longer able to sustain the V_{CC} which starts dropping; on reaching its V_{CC}Off threshold the IC stops switching, reduces consumption and drops more until the V_{CC}restart threshold is tripped. Now, the high-voltage startup generator restarts and when the V_{CC} again crosses its turn-on threshold, the IC starts switching. In this manner the power is transferred from mains to PFC output only for a short time for each trep cycle.

Figure 34. High-voltage startup behavior during latch-off protection

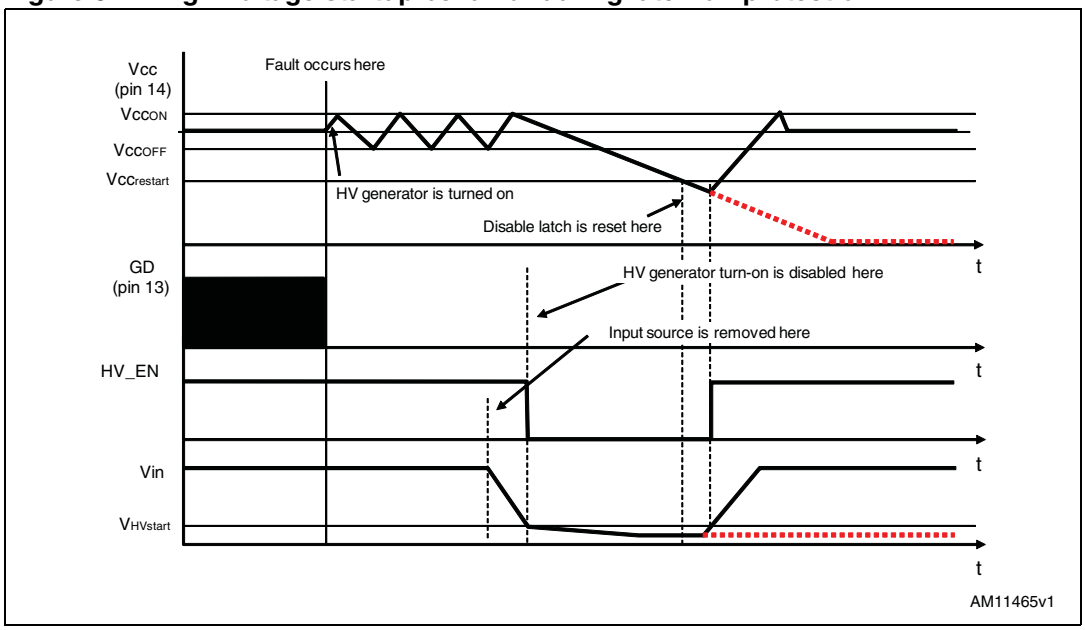
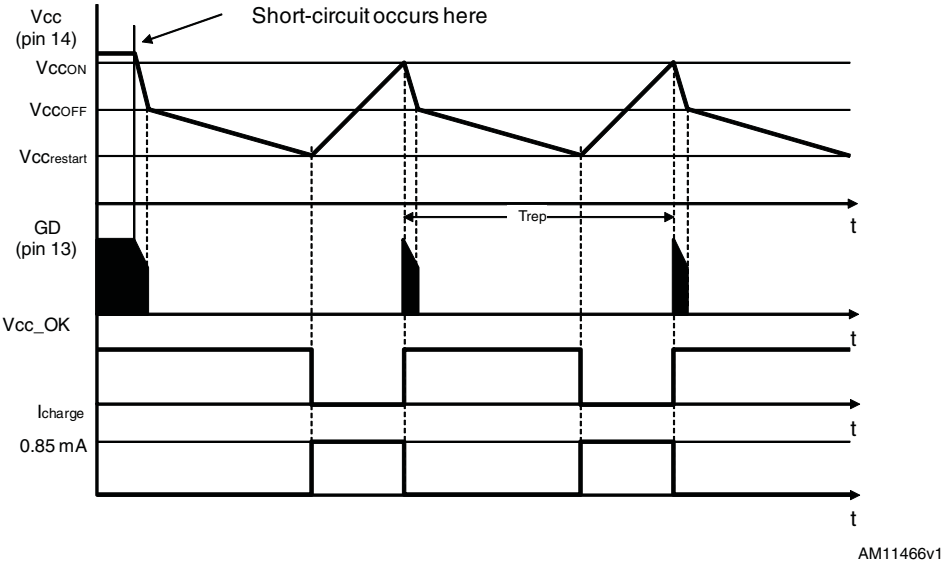


Figure 35. High-voltage startup managing the DC-DC output short-circuit



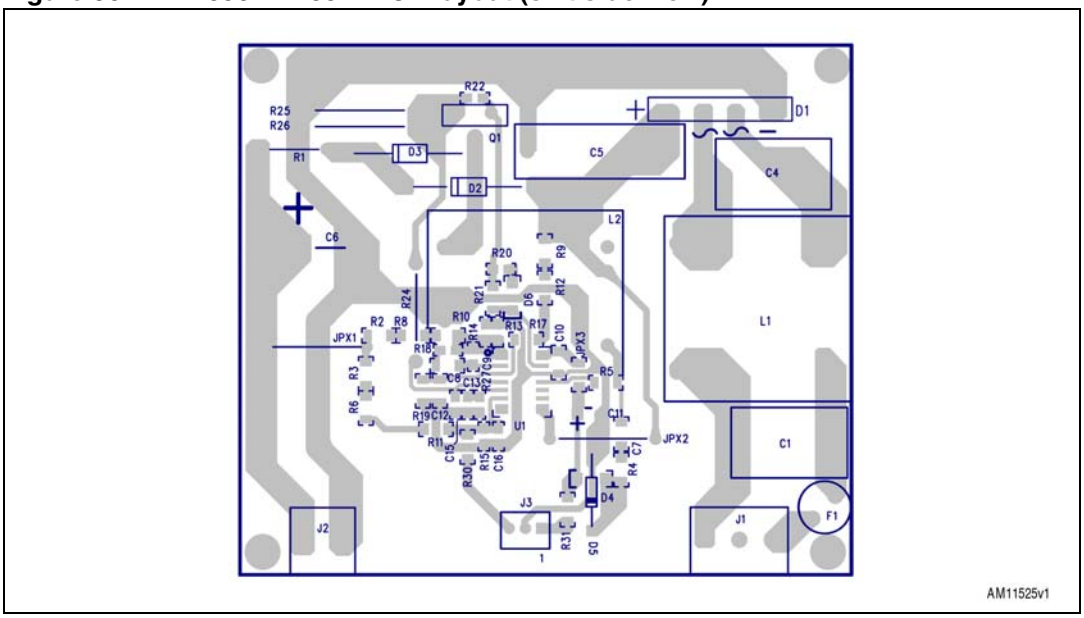
6 Layout hints

The layout of any converter is a very important phase in the design process needing attention by the design engineers. Even though the layout phase may sometimes seem time consuming, a good layout certainly saves time during the functional debugging and the qualification phases. Additionally, a power supply circuit with a correct layout needs smaller EMI filters or less filter stages and so allows a consistent cost saving.

Converters using the L6564H do not need any special or specific layout rule to be followed; just the general layout rules for any power converter must be applied carefully. Basic rules are listed here below, they can be used for other PFC circuits having any power level, working either in transition mode or with a fixed-off-time control.

1. Keep power and signal RTN separated. Connect the return pins of the component carrying high current such as input filter, sense resistors, and output capacitor as close as possible. This point is the RTN star point. A downstream converter must be connected to this return point.
2. Minimize the length of the traces relevant to the boost inductor, MOSFET drain, boost rectifier and output capacitor.
3. Keep signal components as close as possible to each L6564H relevant pin. Keep the tracks relevant to the pin #1 (INV) net as short as possible. Components and traces relevant to the error amplifier must be placed far from traces and connections carrying signals with high dV/dt like the MOSFET drain.
4. Please connect heatsinks to power GND.
5. Add an external shield to the boost inductor and connect it to power GND.
6. Connect the RTN of signal components including the feedback, PFC_OK and MULT dividers close to the L6564H pin #12 (GND).
7. Connect a ceramic capacitor (100÷470 nF) to pin #14 (V_{CC}) and to pin #12 (GND), close to the L6564H. Connect this point to the RTN star point (see rule 1).

Figure 36. EVL6564H-100W PCB layout (smt side view)



7 EMI filtering and conducted EMI pre-compliance measurements

The following figures show the peak measurement of the conducted noise at full load and nominal mains voltages for both mains lines. The limits shown in the diagrams are EN55022 class-B which is the most popular regulation for domestic equipment using a two-wire mains connection.

It is also useful to remember that, typically, a PFC produces a significant differential mode noise with respect to other topologies and therefore, if an additional margin with respect to the limits is required, it is suggested to try to increase the across-the-line (X) capacitors or the capacitor after the rectifier bridge C5. This is more effective and cheaper than increasing the size of the common mode filter coil which would only filter the differential mode noise by the leakage inductance between the two windings.

To recognize if the circuit is affected by common mode or differential mode noise it is sufficient to compare the spectrum of phase and neutral line measurements: if the two measurements are very similar, the noise is almost totally common mode. If there is a significant difference between the two measurement spectrums, their difference represents the amount of differential mode noise. Of course, to obtain a reliable comparison the two measurements must be done in the same conditions. If the peak measurement is used (like in the following figures), some countermeasures must be used, such as synchronizing the sweep of the spectrum analyzer with the input voltage. This is necessary with TM PFC having a switching frequency that is modulated along the sine wave.

Because the differential mode produces the common mode noise by the magnetic field induced by the current, decreasing the differential mode consequently limits the second one.

Figure 37. EVL6564H-100W conducted emission peak measurement at 100 V_{ac}-50 Hz-full load-phase wire

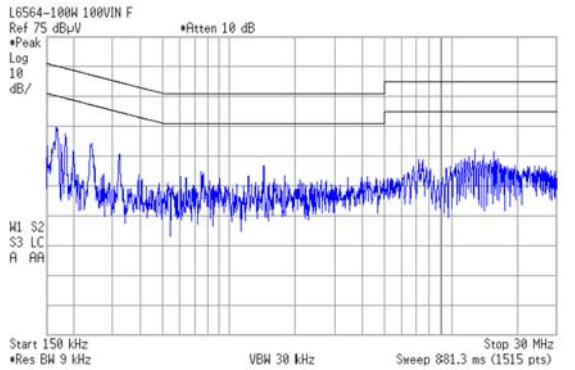


Figure 38. EVL6564H-100W conducted emission peak measurement at 100 V_{ac}-50 Hz-full load-neutral wire

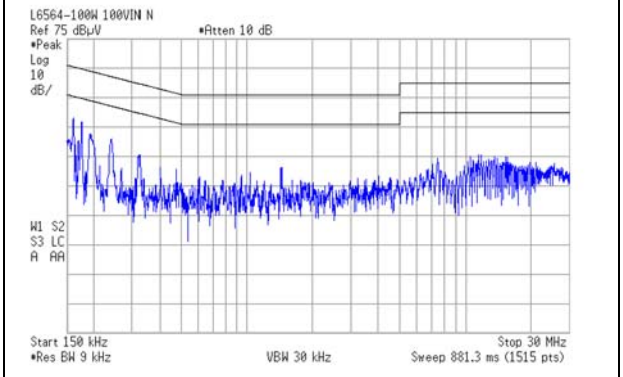


Figure 39. EVL6564H-100W conducted emission peak measurement at 230 V_{ac}-50 Hz-full load-phase wire

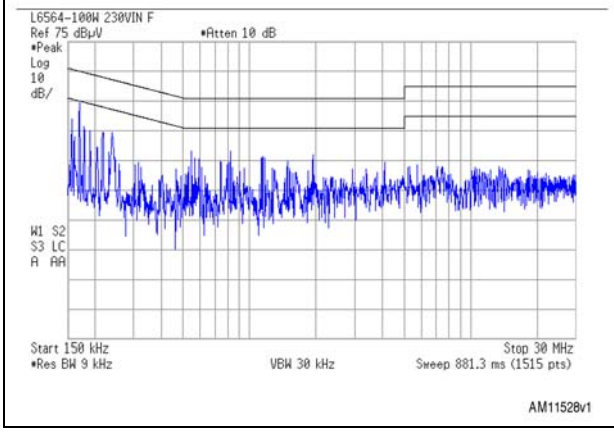
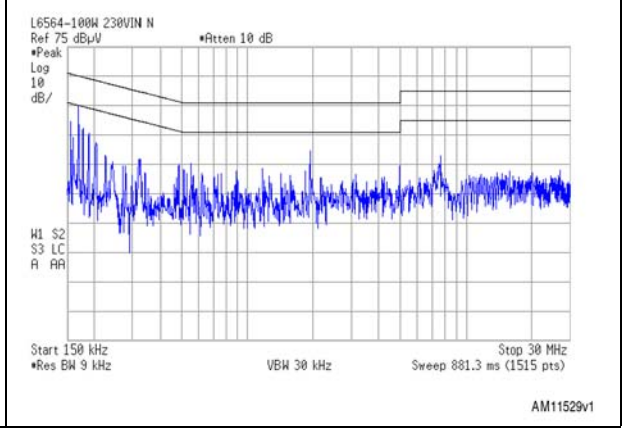


Figure 40. EVL6564H-100W conducted emission peak measurement at 230 V_{ac}-50 Hz-full load-neutral wire



As can be seen in the figures, in all test conditions there is a good margin of the measurements with respect to the limits. The measurements have been done in peak detection to speed up the sweep, which otherwise take a long time. Please note that the harmonic measurements done in quasi-peak or average as required by the regulation are much lower because of the jittering effect of the TM control that cannot be appreciated in peak detection.

8 PFC coil specification

8.1 General description and characteristics

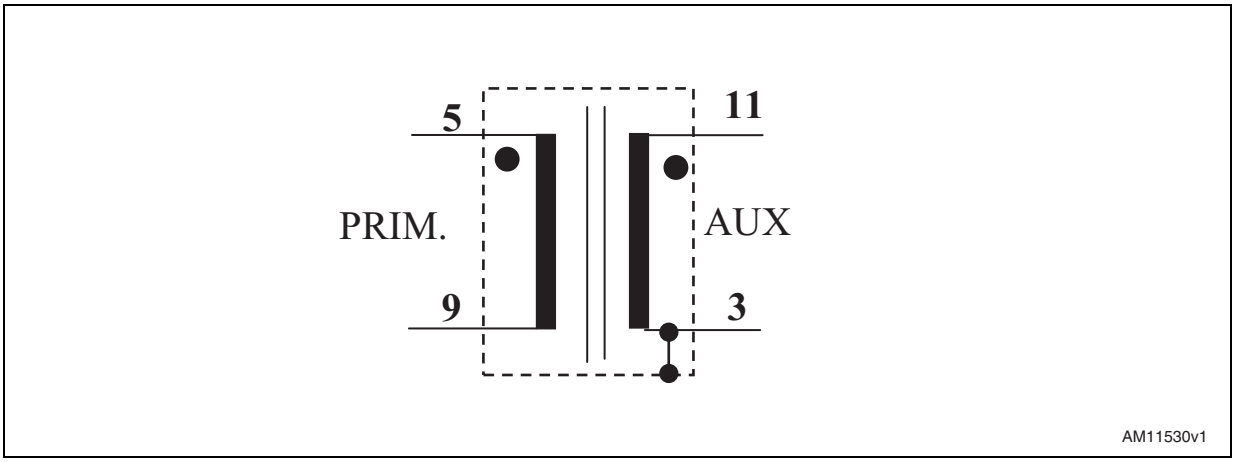
- Application type: consumer, home appliance
- Transformer type: open
- Coil former: vertical type, 6+6 pins
- Max. temp. rise: 45 °C
- Max. operating ambient temp.: 60 °C
- Mains insulation: n.a.
- Unit finishing: varnishing

8.2 Electrical characteristics

- Converter topology: boost, transition mode
- Core type: PQ26/20 - PC44
- Min. operating frequency: 40 KHz
- Typical operating frequency: 120 KHz
- Primary inductance: 520 H 10% @1 KHz - 0.25 V [(a)]
- Peak primary current: 4.2 Apk
- RMS primary current: 1.4 Arms

8.3 Electrical diagram

Figure 41. Electrical diagram



a. Measured between pins #5 & #9.

8.4 Winding characteristics

Figure 42. Winding characteristics

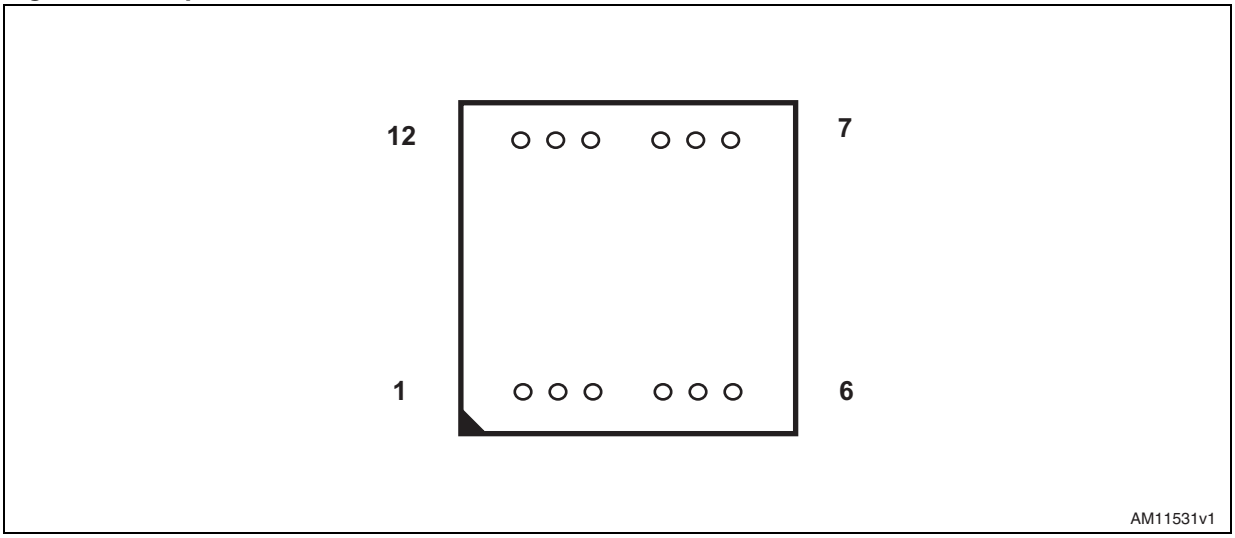
Pins:	Winding	Rms current	Number of turns	Wire type
5 - 9	Primary(1)	1.4 A_{RMS}	57.5 - fit	Multi-stranded #7 x ϕ 0.20 mm
11 - 3	AUX(2)	0.05 A_{RMS}	5.5 - spaced	ϕ 0.28 mm

1. Primary winding external insulation: 2 layers of polyester tape.
2. Aux. winding is wound on top of primary winding. External insulation with 2 layers of polyester tape.

8.5 Mechanical aspect and pin numbering

- Maximum height from PCB: 21.5 mm
- Coil former type: vertical, 6+6 pins
- TDK P/N: BPQ26/20-1112CP
- Pins #1, 2, 4, 6, 7, 10, 12 are removed - pin 8 is for polarity key.
- External copper shield: Not insulated, wound around the ferrite core and including the coil former. It must be well adherent to the ferrite. Height is 8 mm. Connected to pin #3 by a soldered, solid wire.

Figure 43. Top view



8.6 Unit identification

Manufacturer: TDK

Manufacturer P/N: SRW2620PQ-X22V102

9 References

– L6564H datasheet
– AN2761 application note
– AN3009 application note

10 Revision history

Table 3. Document revision history

Date	Revision	Changes
05-Sep-2012	1	Initial release.

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