AN4130
Application note

STEVAL-ILL045V1: 120 V A19 dimmable high power factor 9 W LED driver using the HVLED815PF

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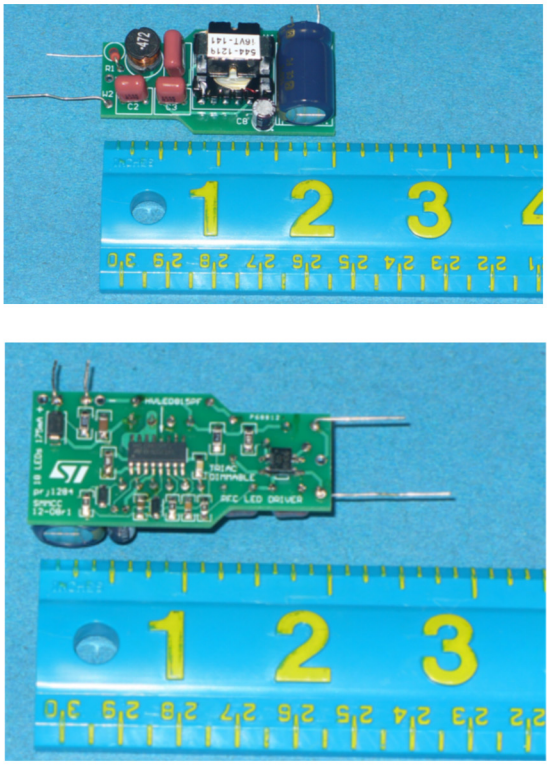
Introduction

The STEVAL-ILL045V1 demonstration board showcases ST's new HVLED815PF LED driver chip. It solves the problem of low-cost drive circuitry for LED replacements for 40 W incandescent or equivalent compact-fluorescent lamps.

The HVLED815PF is a new integrated power controller using primary-side control to achieve LED current regulation within +/-5%. (It also has primary-side voltage regulation, used here for open load protection.) The device incorporates an 800 V avalanche-rated FET and fits in a standard SO-16 package. An internal startup circuit eliminates the need for external rapid-start circuitry.

The PFC-flyback power converter operates in transition mode for highest efficiency and best use of components. With the addition of a few extra components the HVLED815PF draws near-sinusoidal input current from the AC line. The circuit regulates LED current over a wide range of line voltage and LED string voltage, and is dimmable with standard Triac-based dimmers.

Figure 1. Images top and bottom



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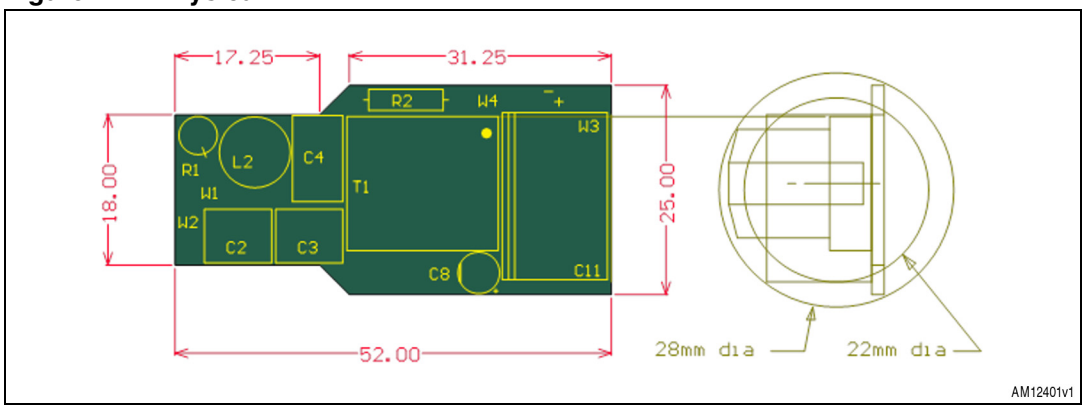
1 Features

The demonstration board features are:

- +/- 5% primary-side current regulation, no optocoupler
- Low component count - 25 parts, including the EMI filter
- Only 1 tight-tolerance component
- High efficiency, >86%
- High power factor >0.98 and low THD, <20% over 90 V to 132 V range
- Fits in 28 mm tubing, 52 mm overall length
- 9 W output, for light equal to 40-60 W incandescent
- Dimmable with common Triac dimmer.

Figure 2. Physical



2 Theory of operation

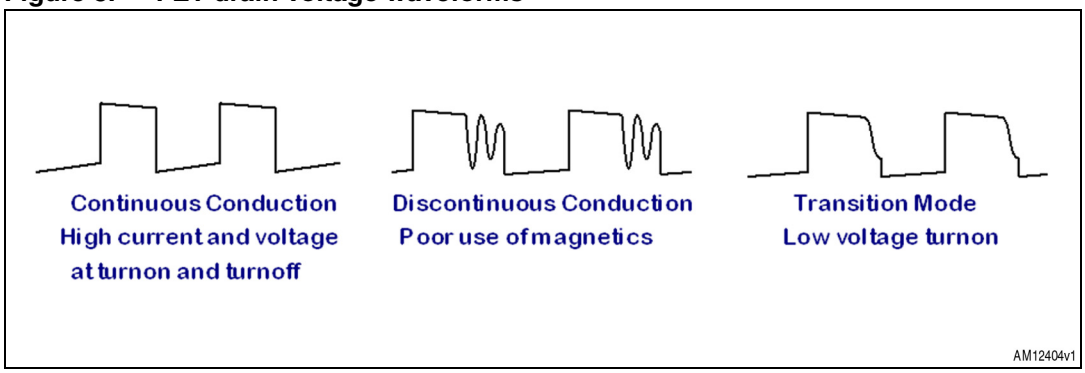
2.1 Transition-mode flyback

Flyback power converters operate by storing energy from the primary side in an inductor's air gap, and discharging the energy into a load on the secondary side. The converter can run in two modes:

1. Discontinuous conduction, where there is a deadtime between discharge and charge cycles.
2. Continuous conduction, where the discharge cycle is ended by starting the charge cycle before all the stored energy is delivered to the load.

Neither mode fully utilizes the magnetic structure of the inductor. However, if the recharge cycle is started just after the discharge cycle ends, the natural ringing of the inductor and stray capacitance can be used to reduce turn-on voltage stress on the switch. Transition mode converters can be very efficient as a result, having greatly reduced turn-on loss - the switch does not have to discharge its own and stray capacitance from a high voltage.

Figure 3. FET drain voltage waveforms



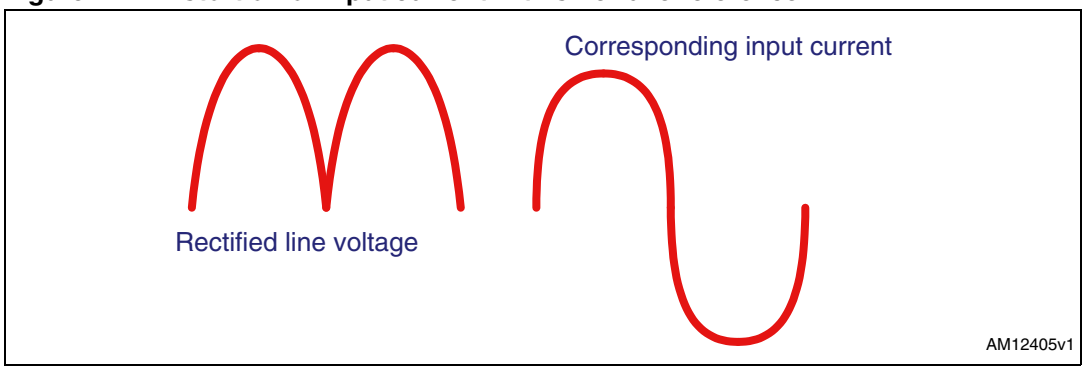
Operating frequency is a function of source and load voltages, and load current. If the source voltage varies, the operating frequency varies. This makes the transition mode converter very popular in low-cost commercial applications, where the varying frequency, due to input voltage ripple, spreads noise over a wide spectrum, reducing the noise at any one frequency. Conducted EMI tests can be easier to pass.

2.2 PFC-flyback

In the PFC-flyback converter the input voltage is the rectified line voltage, with almost no filtering. Converter input voltage goes to zero when the line voltage crosses zero.

It's common practice to use the rectified line voltage as a reference for the peak current in the flyback converter switch. This does not result in sinusoidal input current, but it's close enough. The duty cycle change with input voltage still distorts the waveform. This is discussed in detail in ST's AN1059 application note.

Figure 4. Distortion of input current with sinewave reference



2.3 Non-isolated flyback

In this circuit the transformer secondary shares part of the primary winding. The lack of isolation means that the burden of electrical safety rests on the LED thermal mounting. The LEDs must be isolated from human contact.

Electrical stress on the power conversion components is lower than a corresponding isolated flyback converter. Leakage inductance in the transformer is lower, because the secondary occupies the same space as part of the primary, and the remaining primary is very close to the secondary - interwinding insulation is not required. Reduced leakage inductance results in less overshoot in the FET drain voltage, so a lower voltage FET can be used safely. The HVELD815PF used here has an 800 V FET - too much for the US 120 V application but ideal for European line voltage.

2.4 Primary-side control

A PFC-flyback converter usually uses a PFC controller chip such as ST's L6562AT with an external FET and a feedback loop. The secondary side voltage and/or current are monitored, compared to a reference on the secondary side, and a control signal sent to the primary side with an opto-isolator. This signal is multiplied by a reference waveform (the rectified line voltage) and used to control peak switch current.

ST has developed a primary-side control circuit that eliminates the need for the secondary-side components. Voltage is monitored on the housekeeping winding at the end of the flyback converter discharge cycle, just as the secondary current reaches zero. Secondary current is set by measuring duty cycle and adjusting peak primary current, to provide a calculated secondary average current. But the circuit cannot work with a multiplier, so another method of shaping the peak switch current waveform must be found.

2.5 Using the HVLED815PF current limit for power factor correction

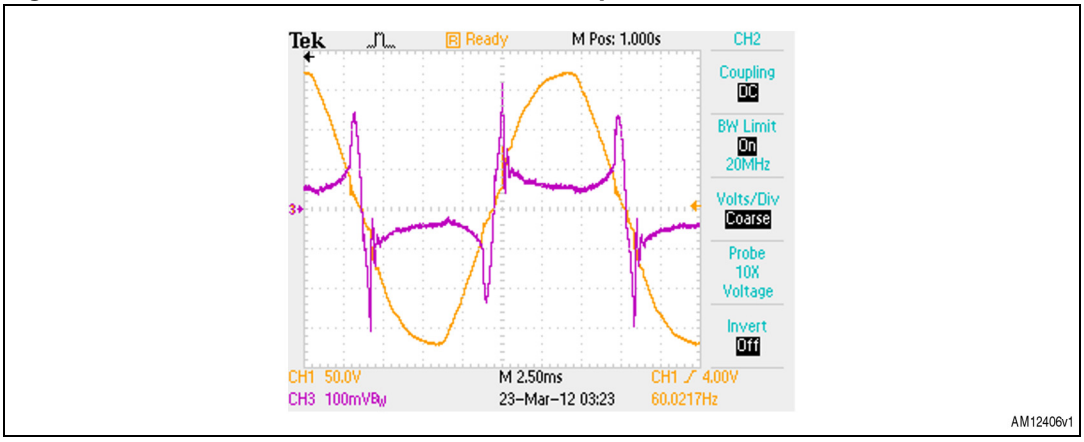
2.5.1 Average current regulation

The HVLED815PF does an excellent job of regulating output current in a DC input flyback supply. It calculates the peak current at which to shut off the driving FET by continuously looking at the duty cycle. The error between desired duty cycle and actual duty cycle appears as a current on the ILED pin - a capacitor on this pin integrates the error to zero over time. Since the voltage on this pin, divided by 2, directly sets the current at which the FET switch turns off, the output current is regulated.

In DC-input flyback power supplies very small capacitors are used on the ILED pin for quick response to changing loads or input voltage. The capacitor on this pin can be much larger if the load voltage does not change rapidly. LED current can be regulated more slowly, averaging out the error over several cycles of input voltage. A 4.7 µF low-voltage ceramic capacitor is used here.

The average LED current is kept constant even if the input voltage waveform is grossly distorted, such as a rectified sinewave, as occurs in the PFC-flyback topology. The input current waveform, however, is truly ugly. Note the magenta trace in the figure below.

Figure 5. Current distortion with sinewave input



Where:

- Yellow = line voltage
- Magenta = line current.

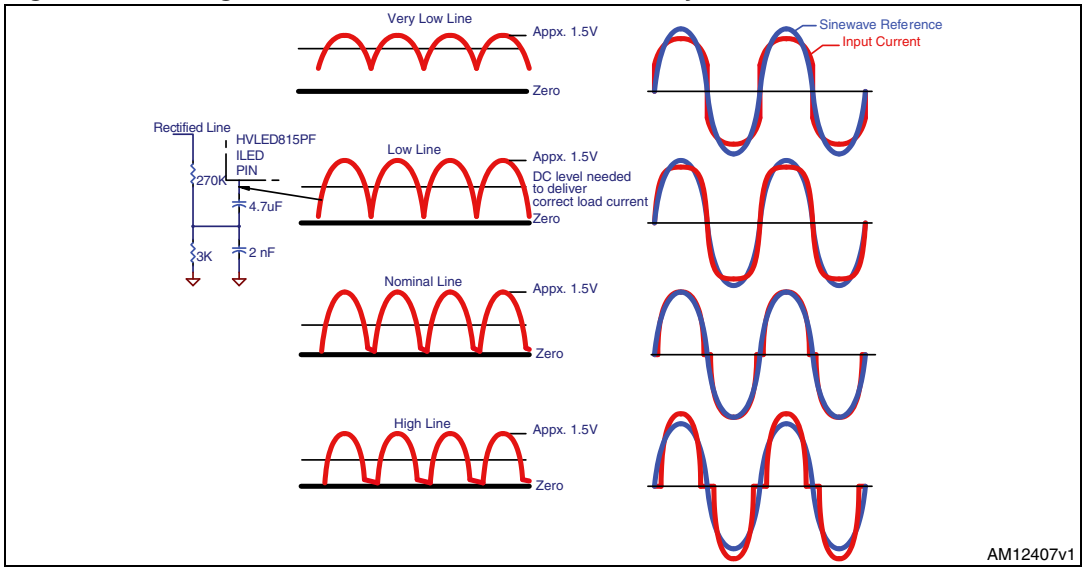
The peak FET shut-off current remains at the same level throughout the AC half cycle, but the duty cycle of the converter changes. (FET ON-time increases at lower input voltage - it takes longer to reach the same current if the converter input voltage is lower). The resulting input current waveform is VERY rich in harmonics (THD is in the range of 130%), though power factor is actually pretty good.

2.5.2 Adding an AC component to the current regulator

If an AC signal is injected into the ILED pin, the instantaneous FET peak current can be controlled, while the average output current (a DC level) remains regulated. The figure below shows the injection of a small fraction of the line voltage into the bottom of the ILED capacitor. The change in the input current waveform is dramatic. But it is best for only one

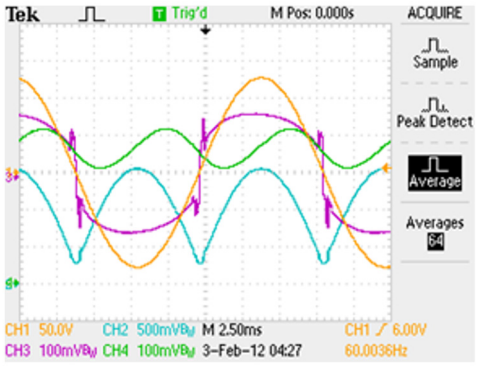
line voltage, and is a compromise for all others. But it's “good enough”. The small capacitor across the lower resistor is only there to keep switching noise out of the circuit.

Figure 6. Voltage and current waveforms with AC injection



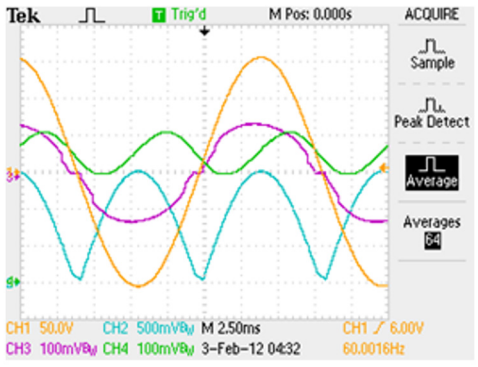
The current waveform at the “nominal line” above actually has the lowest harmonic content due to the input current distortion inherent in the PFC-flyback converter. The HVLED815PF clamps the voltage on the ILED pin between about 0.2 V on the low end, and at about 1.5 V on the high end. If the injected waveform wants to swing below 0.2 V, the peak current in the FET is set to zero, so no input current flows. The scope images in *Figure 7*, *8*, and *9* show how well the AC injection works.

Figure 7. Waveforms with 90 V input



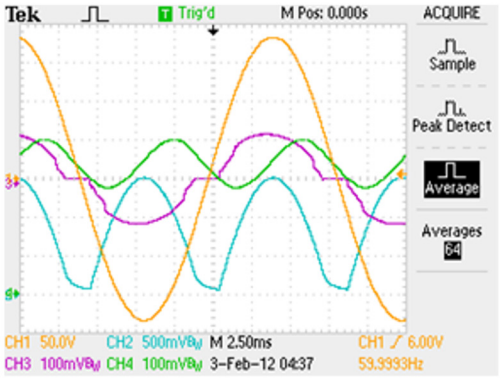
Trace colors:
Yellow = line voltage
Magenta = line current, 50 mA/div ref -3div
Blue = voltage at I_{LED} pin, ref -3 div
Green = LED current, 50 mA/div ref -3div

Figure 8. Waveforms with 110 V input



Trace colors:
Yellow = line voltage
Magenta = line current, 50 mA/div ref -3div
Blue = voltage at I_{LED} pin, ref -3 div
Green = LED current, 50 mA/div ref -3div

Figure 9. Waveforms with 130 V input



Where:

- Yellow = line voltage
- Magenta = line current, 50 mA/div ref -3div
- Blue = voltage at I_{LED} pin, ref -3 div
- Green = LED current, 50 mA/div ref -3div.

Power factor is excellent over the designed line voltage range of 90 V to 132 V, well above 0.98.

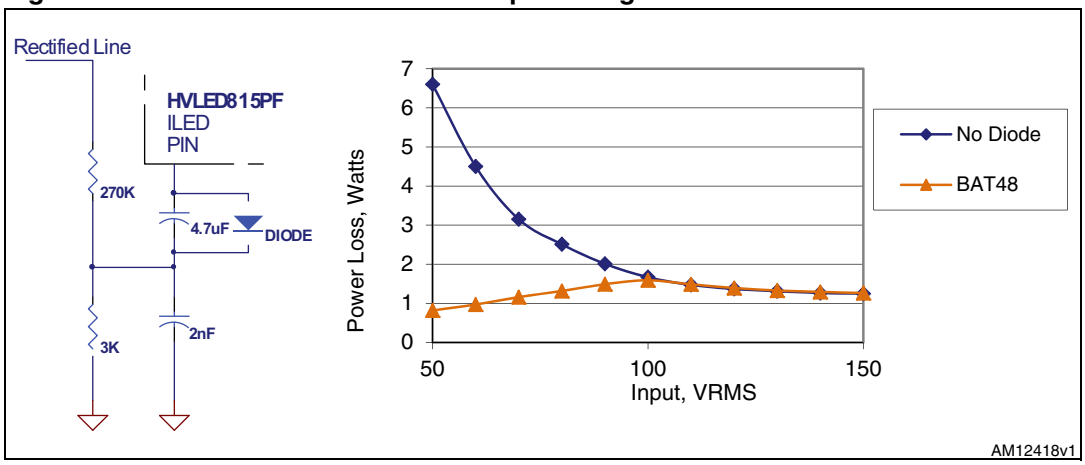
Total harmonic distortion reaches a minimum at one line voltage. Over the range, THD is less than 20%.

2.6 Diode clamp to limit input current

Since the peak FET current is directly controlled by the voltage on the ILED pin, a diode clamp can be added to limit the voltage increase to reasonable levels. The graph below shows the results for two conditions - no diode, and a Schottky diode having about 0.3 V forward drop, placed across the DC filter capacitor.

The HVLED815 attempts to provide regulated power even if low line voltage makes that task difficult. It raises the voltage on the ILED pin to fairly high levels if the line voltage is reduced. Losses in the unit rise dramatically with decreasing line voltage as the input current increases.

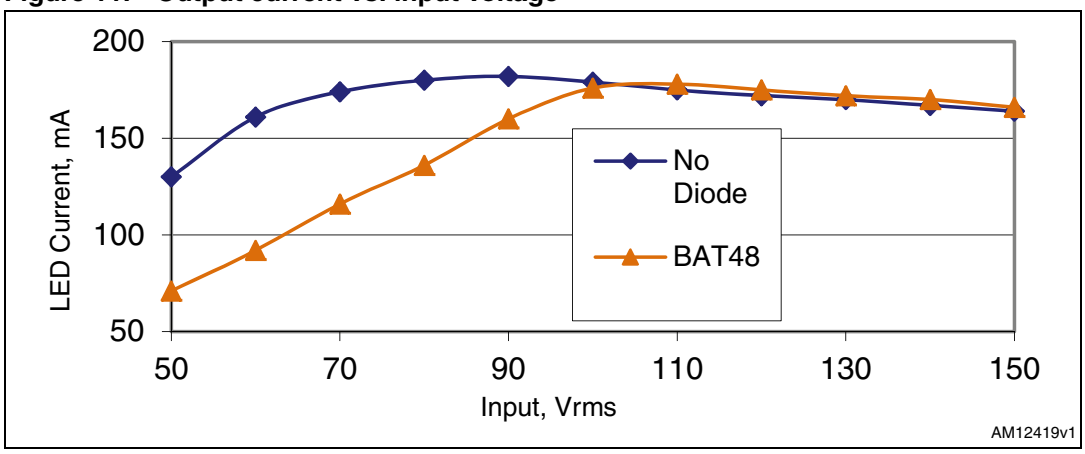
Figure 10. Power loss vs. sinusoidal input voltage



The input current increase can now be limited to a reasonable value. There are two consequences of this addition:

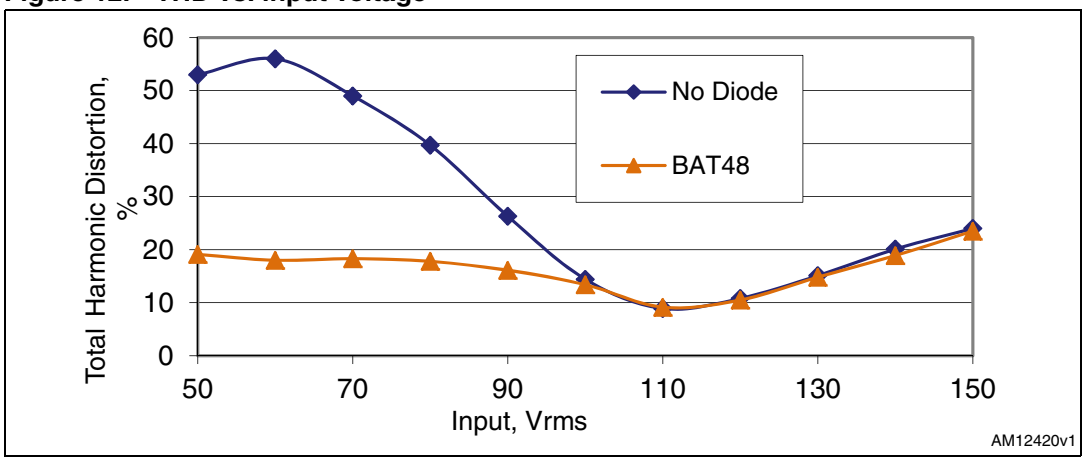
Line regulation is lost at low input voltages (the ILED pin cannot rise to regulate current).

Figure 11. Output current vs. input voltage



Harmonic distortion is greatly reduced at low line voltage.

Figure 12. THD vs. input voltage



The scope shots below show the result on the input current waveform.

Figure 13. 70 Vrms input, no diode

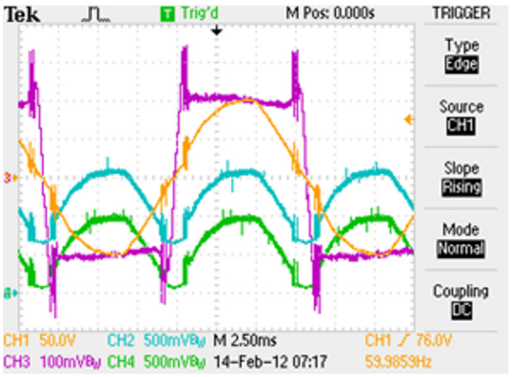
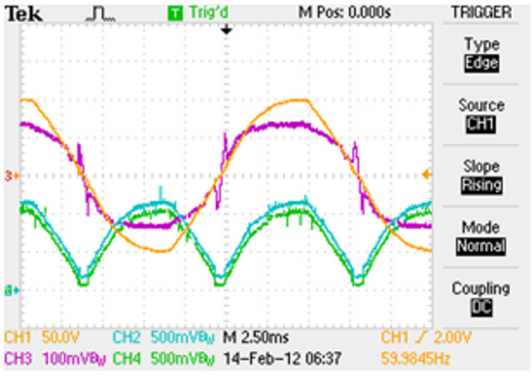


Figure 14. BAT48, ~0.3 V drop



Where:

- Yellow = line voltage
- Magenta = line current, 50 mA/div ref -3div
- Blue = Voltage at I_{LED} pin, ref -3 div
- Green = Voltage at bottom of 4.7 µF cap on I_{LED} pin.

2.7 Diode clamp effects on dimming

The diode-improved waveform also helps when the circuit is dimmed with a Triac, especially at low conduction angles. The ILED pin voltage is not allowed to rise. Note how high the ILED pin voltage (green trace) has risen in the first image, compared to the second, as the chip attempts to regulate the average output current. The voltage on that pin directly controls the peak FET current.

Figure 15. 40 Vrms dimmed input, no diode

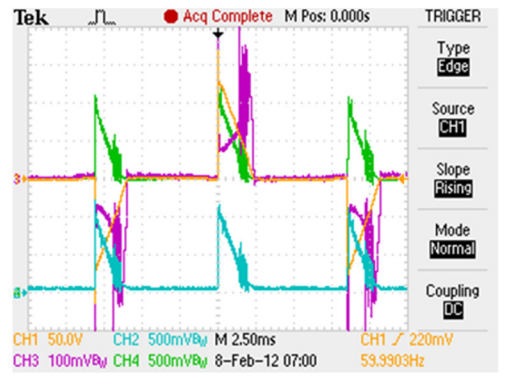
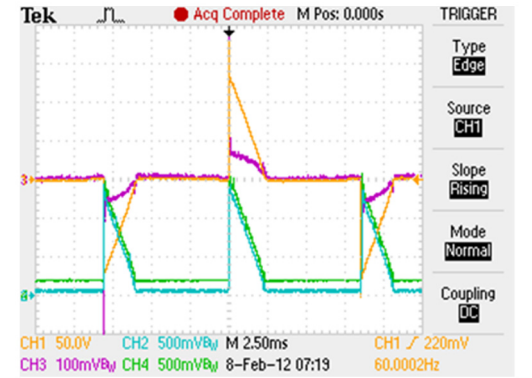


Figure 16. 40 Vrms dimmed input, BAT48 diode



Where:

- Yellow = line voltage
- Magenta = line current, 50 mA/div ref -3div
- Blue = Voltage at I_{LED} pin, ref -3 div
- Green = Voltage at bottom of 4.7 µF cap on I_{LED} pin.

Dissipated power is also reduced at low conduction angles due to the lower RMS input current:

Figure 17. Power loss vs. dimmed RMS line voltage (120 V line)

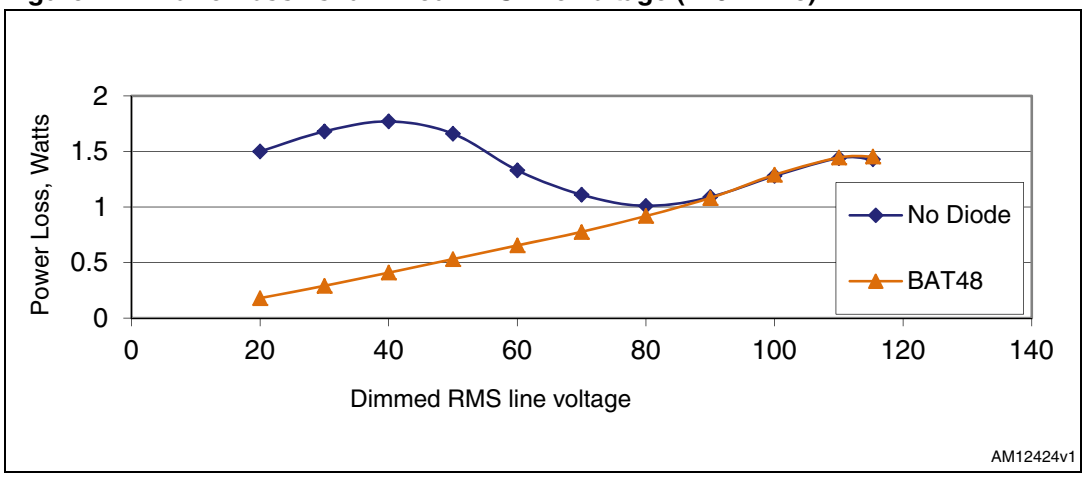
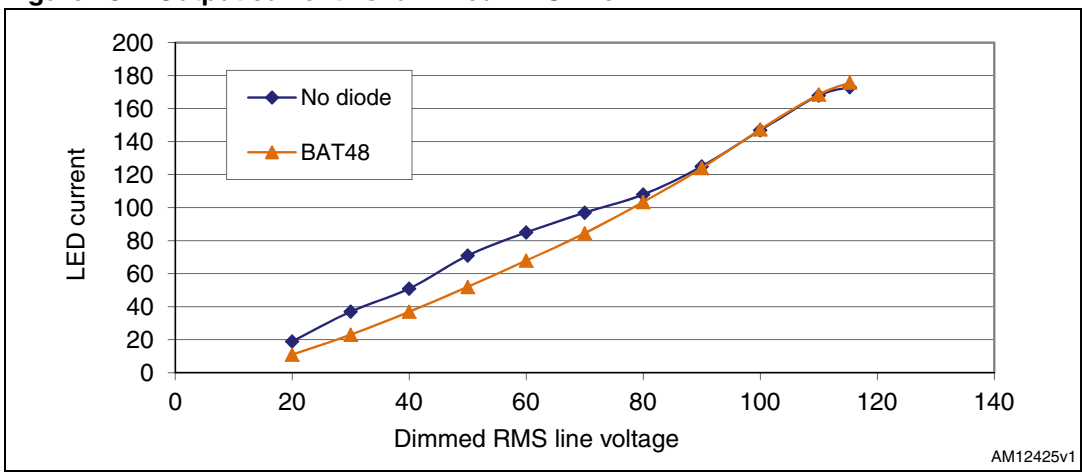


Figure 18. Output current vs. dimmed RMS line



Note that the dimming curve for the Schottky diode unit is much smoother and slightly lower at the low end. This allows the unit to meet the requirements of NEMA SSL 6-2010, as shown in *Figure 25*.

3 Power converter performance

3.1 LED current vs. line voltage and load voltage

Figure 19. LED current vs. line voltage with 18 series LED load

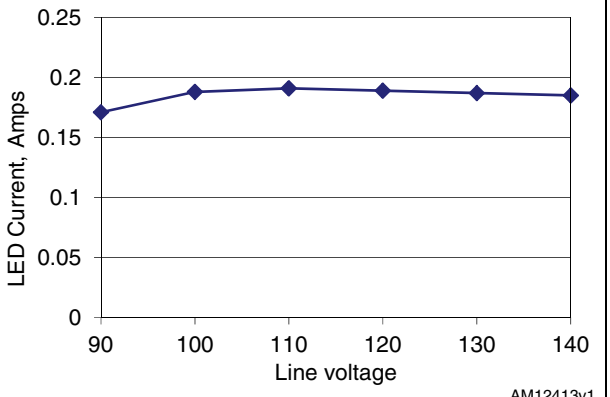
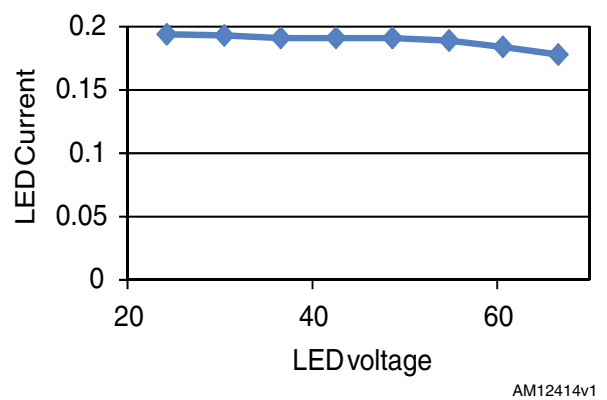


Figure 20. LED current vs. LED voltage at 120 V In



Nominal (18 LEDs) voltage is 54-56 V. Performance is excellent over a very wide range of load conditions, even with the AC injection.

3.2 Efficiency and power dissipation

Figure 21. Efficiency vs. line voltage

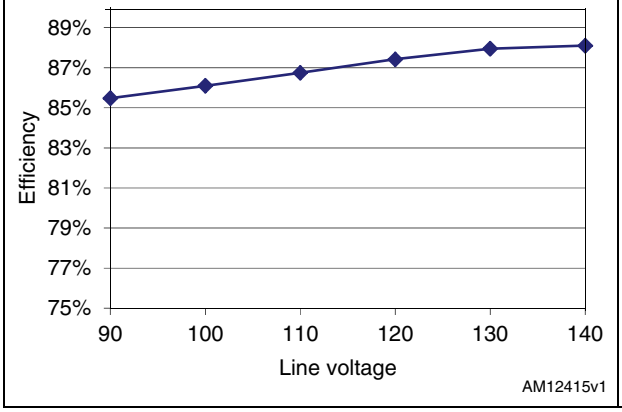
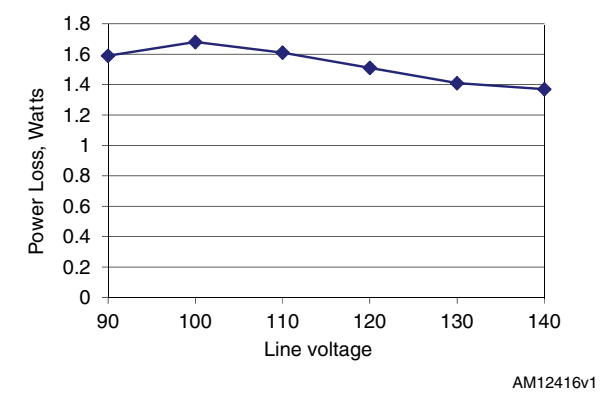


Figure 22. Power loss vs. line voltage



As expected, efficiency drops off at low voltage. The rather high $R_{DS(on)}$ of the HVLED815PF and the input filter series resistances increase I^2R loss due to higher required input current.

3.3 Power factor and total harmonic distortion

Figure 23. Power factor vs. line voltage

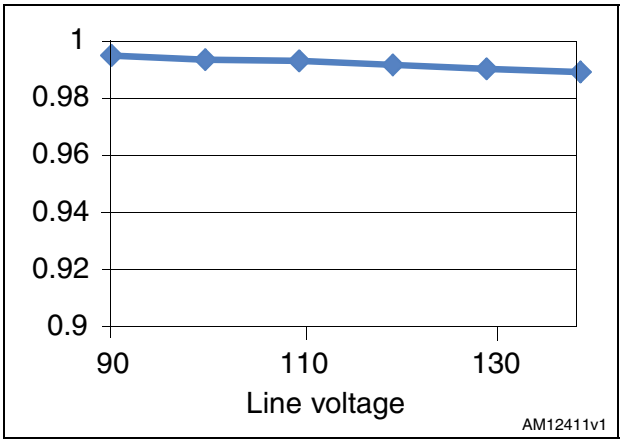
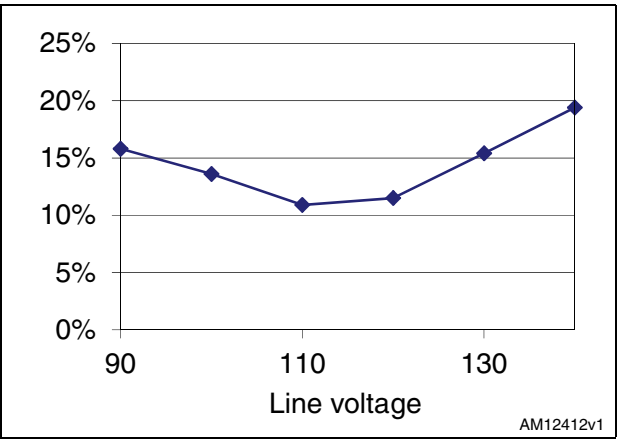
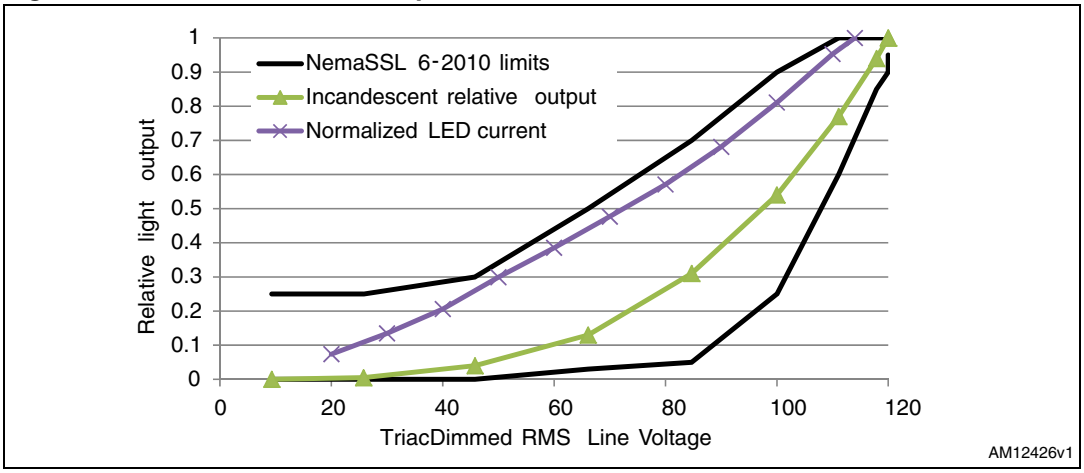


Figure 24. THD vs. line voltage



3.4 Dimming

Figure 25. Relative dimmed output



3.5 Conducted EMI

The conducted emissions plot for the two input lines are virtually identical. The plots are the maximum (peak hold) of 10 scans for peak power.

Figure 26. Conducted EMI, line 1

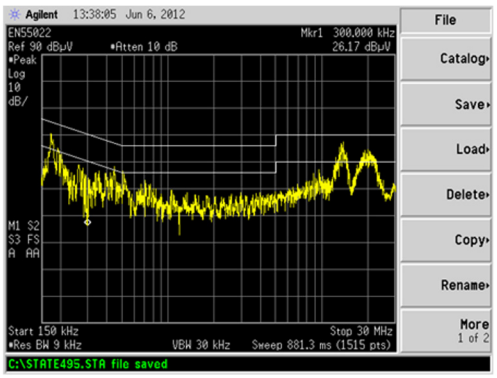
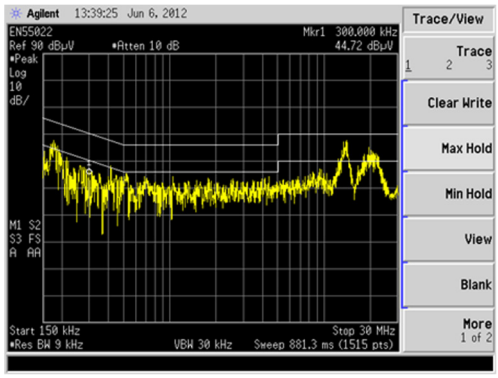
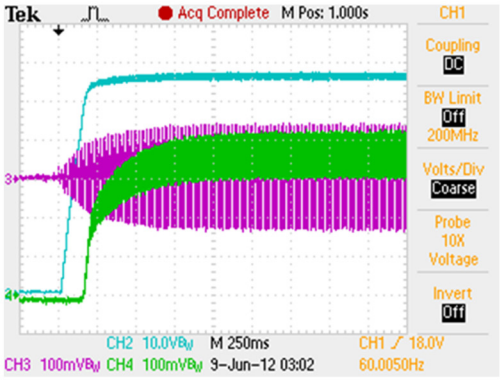


Figure 27. Conducted EMI, line 2



3.6 Startup

Figure 28. Unit startup



Where:

- Yellow = (not shown) line voltage, triggers scope
- Magenta = line current
- Blue = LED voltage
- Green = LED current.

The unit produces usable light in about 0.15 seconds, and nearly full output in about 0.5 seconds.

3.7 Component stress

3.7.1 Thermal

The unit was mounted above the bench in free air with the narrow end (AC input) down. Temperatures were recorded after 45 minutes of operation.

The dimmed temperatures were taken with a Triac dimmer feeding the unit. The dimmer was adjusted to the point where the power analyzer reported greatest loss. Undimmed input voltage was 120 Vrms. Dimmed input voltage was 108 Vrms, and conduction angle about 150 degrees.

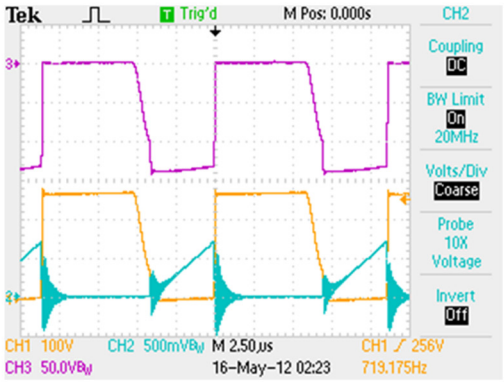
Table 1. Component thermal stress

Thermal stress	Undimmed	Dimmed
Efficiency	87.6%	85.7%
Power loss	1.41 W	1.56 W
Ambient	23.9c	24.9c
R1	36.7c	50.3c
R2	50.8c	73.2c
BR1	46.6c	50.6c
L2	42.1c	46.6c
U1	66.5c	78.1c
T1	56.3c	60.2c
D3	56.2c	58.7c
C11	41.9c	43.8c

3.7.2 Electrical

The plot below was taken near the peak of line voltage, where both voltage and current stresses are greatest.

Figure 29. Component electrical stress



Where:

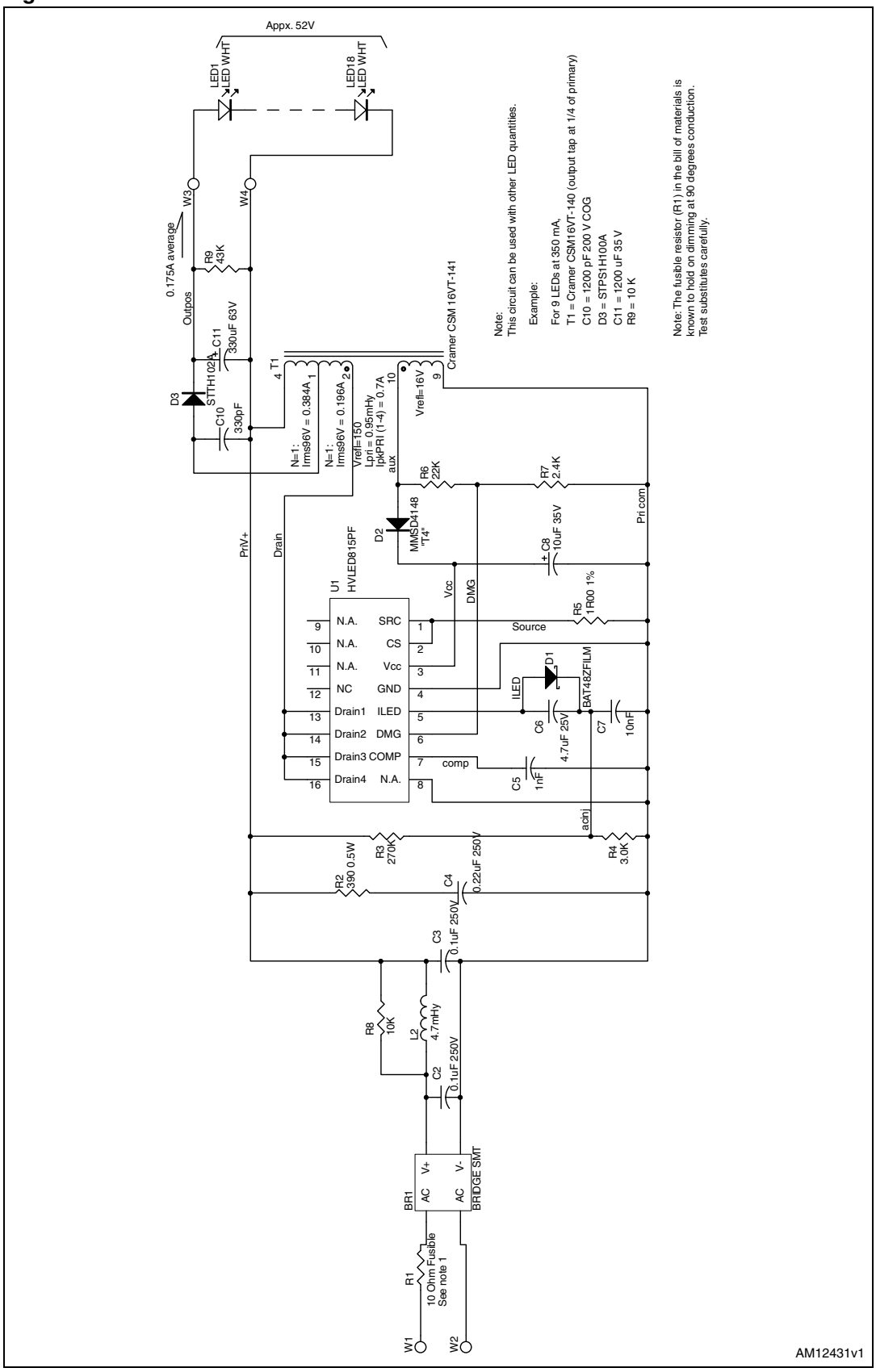
- Yellow = drain voltage
- Magenta = diode voltage
- Blue = drain current.

Note the VERY small overshoot in the drain voltage and diode voltage waveforms. This is due to the transformer's low leakage inductance, about 0.6 microhenries. The current ringing is due to the snubber capacitor on the secondary side resonating with the leakage inductance at FET turn-on and turn-off. The circulating current loop on the PC board is very small and is only weakly coupled to the AC line, so it does not cause an EMI problem.

3.8 Summary

Performance is excellent for an LED driver of this size and simplicity. The added bonuses of dimmability and power factor correction compel consideration of this design.

Figure 30. Schematic



4 Design guidance

This section, like any power design, proceeds from output to input. Please refer to the schematic on the previous page.

4.1 The load

The converter design is optimized for a string of 18 LEDs, about 54 Vdc at a current of 175 mA.

4.2 Preload resistor (R9)

While the unit's dimmed output current lies inside the NEMA limits, performance can be improved by adding a light preload. This reduces efficiency, but the unit's operation is much more stable at low conduction angles.

The reason is that most dimmers rely on line voltage to set the Triac firing delay after the zero crossing. At low conduction angles the delay is strongly dependent on line voltage. The slightest variation is visible, because the LED light output reacts very quickly to current changes, much more quickly than do incandescent lamps, where the filament is a thermal reservoir that slows the lamp’s response to changes in the dimmed RMS input voltage.

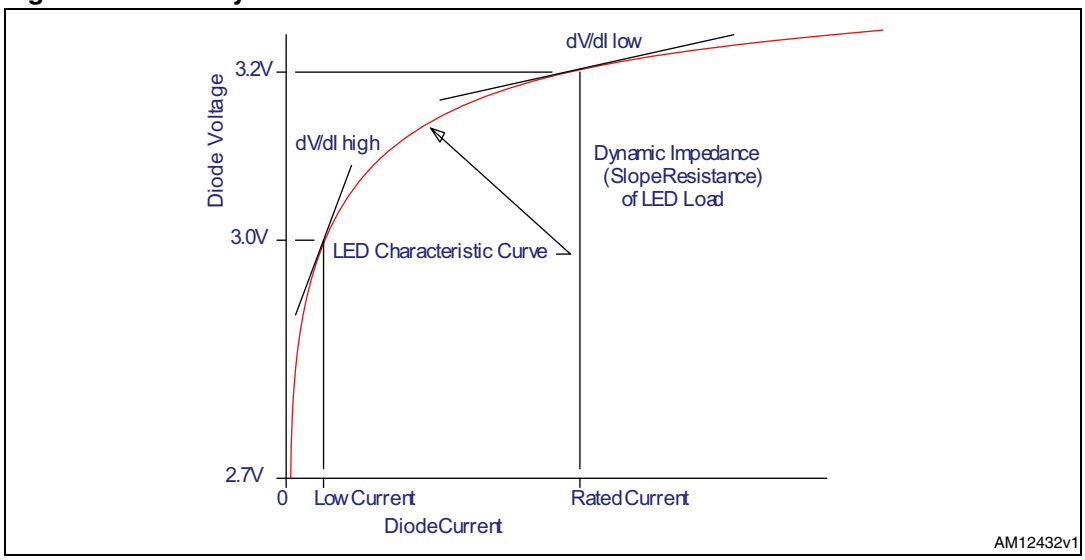
The preload resistor is also required for the open-load protection to work. Without it, the output voltage climbs until the leakage current in the output filter capacitor limits it. This causes no short-term damage, but should be avoided.

4.3 Output filter capacitor (C11)

4.3.1 LED ripple current

LEDs require more filtering than normal loads. LEDs are diodes, and their impedance is a function of the current through them. Typically, an LED has a dynamic impedance, or slope resistance, of about 1/10 of the ratio of DC voltage to DC current.

Figure 31. LED dynamic resistance vs. current



For a small voltage change the current change is about 10 times as large as for a resistive load.

A 1 W white LED (~3.2 V at ~350 mA) has a slope resistance of about 1 Ω at full power. As the current is reduced, the LED impedance rises accordingly, inversely proportional to the current. But the capacitor's impedance determines the ripple voltage - the LED current ripple percentage does not increase as the unit is dimmed.

4.3.2 Allowable ripple current in LEDs

At the converter switching frequency the output filter capacitor takes almost all the ripple current. The ESR of the capacitor is dominant at that frequency, and is orders of magnitude lower than the LED impedance. High frequency ripple in the LEDs is not a concern.

At twice the line frequency (120 Hz) LED ripple can have an effect on people even if it can't be directly observed. It's common practice in the lighting industry to limit the optical ripple to about 10% RMS of the total light, and NEMA SSL6-2010 requires a statement of ripple percentage on the packaging if this is exceeded. So LED current ripple must be kept below 10%.

At 120 Hz capacitive reactance dominates the shunting impedance - ESR can be ignored. Because of the low LED impedance the filter capacitors must reduce RMS ripple voltage to about 1% of the LED string voltage.

Equation 1

$$C = \frac{0.707 \cdot 100 \cdot I_{LED}}{2\pi \cdot 120Hz \cdot V_{string}}$$

For this design, with (18) 3.2 V LEDs at 175 mA, the capacitance should be about 284 µF. The value used was 330 µF.

4.4 Diode selection (D3)

4.4.1 Speed

D3 must be a fast-recovery part, but because of the transition-mode topology the recovery requirements are modest. Current in the diode reverses slowly, and the diode is completely turned off well before the FET turns on. Parts with Trr up to about 70 ns are suitable.

4.4.2 Reverse voltage

The diode must support the reflected line voltage and output voltage plus a small spike from leakage inductance. A standard 200 V fast-recovery diode was used. A high-voltage Schottky diode would also work, with a slight gain in efficiency and slightly increased cost.

4.4.3 Current rating

This is a low-stress application for the diode. The 1-amp rating of ST's STTH102A is probably too much, but the part is inexpensive, and it works well.

4.5 Snubber capacitor selection (C10)

The current at FET turn-off continues to flow in the leakage inductance of the transformer, resulting in a primary-side voltage spike. Common practice is to use an RCD clamp or an RC snubber to dissipate this energy as heat.

The snubber can be moved to the secondary side of the transformer if leakage inductance is low. The primary voltage can be caught on-the-rise by an R-C network placed across the secondary winding or the diode. This avoids the need for high-voltage diodes and capacitors on the primary side.

Experiments with relatively low values of capacitor and resistor determined that for a narrow range of capacitor values the primary overshoot at FET turn-off was greatly reduced. It was also discovered that the resistor is not needed if the secondary side capacitor is properly selected. Criteria for selection have not been determined.

The 800 V rating of the HVLED815PF's FET doesn't hurt either. It's certainly too much for a 120 V line.

4.6 Transformer design (T1)

4.6.1 Operating frequency

Higher operating frequency reduces the size of the transformer. Operating frequency can be increased up to the point where EMI filtering requirements become the limiting factor. An operating frequency just below 150 kHz puts the second harmonic inside the conducted EMI band, but the harmonics are smaller and easier to filter than the fundamental. Placing the fundamental at 120-135 kHz at the nominal line voltage peak is a good compromise, considering component tolerances.

4.6.2 Primary inductance

Assume the FET ON-time takes up half the cycle time.

Equation 2

$$L \cong \frac{V_{in\ PEAK}}{I_{PEAK} \cdot 2 \cdot 135KHz} = 132V \cdot 1.414 / (0.7A \cdot 2135000) = 988uH$$

A value of 950 µH was selected because additional time is required for the resonant drain voltage fall time of the transition-mode converter.

4.6.3 Primary peak current

This is set by the required output power, which is limited by I^2R loss in the internal FET on-resistance, to about 10 W. For this design, at US mains voltage, the peak current is about 0.7 amps.

4.6.4 Reflected voltage

For PFC-flyback transition-mode power converters on US 120 V lines the best reflected voltage choice is 110 to 130 V. This range gives the best converter efficiency. Copper losses can be spread more or less equally between the primary and secondary windings, and the FET turn-on losses from discharging circuit capacitance are quite low.

A turns ratio of 2:1 primary: secondary was selected for the 18-LED load, placing reflected voltage at about 112 V at full undimmed output.

4.6.5 Leakage inductance

This should be as low as possible - energy stored here does not contribute to LED power and must be dissipated as heat. Using part of the primary winding as the secondary greatly reduces leakage inductance, but does not entirely eliminate it.

4.6.6 Auxiliary winding turns ratio

The operating voltage for the HVLED815PF depends on the LED voltage and the turns ratio. The LED winding (secondary) voltage reflects to the flyback voltage on all windings. The turns ratio from the secondary to the auxiliary winding determines the auxiliary voltage, both for voltage regulation (open load protection) and for the Vcc power supply.

Sufficient voltage must be available to power the HVLED815PF at low dimmer settings. Usually the lowest LED voltage where light is visible is around 2.8 V. The reflected voltage on the auxiliary winding under these conditions must be greater than the HVLED815PF's V_{ccOFF} max.

4.6.7 Final transformer specification

Winding ratios, primary inductance, peak currents, and other specifications are shown on the schematic. The vendor's specification sheet appears later in this note.

4.7 DMG pin (R6, R7)

This single pin performs several functions; voltage limiting, zero current detection, and correction for line voltage changes. Its operation is discussed thoroughly in the relevant datasheet and is only summarized here. The internal circuit is also used in ST's HVLED805 and Altair chips. The datasheets and application notes for these parts offer additional insight into the pin operation.

Design begins with compensation for the internal comparator's propagation delay. At high line voltage the slope of FET current vs. time is higher, so for the same comparator reference voltage the current overshoots more than at low line. This is compensated by adding an offset proportional to line voltage to the comparator's reference input. R6, in conjunction with an internal resistor, RFF, of about 45 Ω, decreases the peak current trip point proportional to the line voltage. The values in the demo unit slightly overcompensate line voltage.

The two resistors form a divider that normally sets the converter output voltage. The LED driver uses constant-current mode - the constant-voltage circuit is used only for overvoltage protection, such as an open load situation. On the positive swing of the output and auxiliary windings the divided voltage is measured at the end of the transformer discharge time, and compared to an internal 2.5 V reference by a transconductance op amp. The Vout setting should equal the output filter capacitor's voltage rating.

The third function, zero current detection, uses the voltage at the DMG pin to measure the duty cycle of the output diode conduction period. This is used for the internal current regulator - the duty cycle measured here determines the FET cutoff current, indirectly controlling output current. The divider's resistor values have very little effect on this function.

During product development, it is helpful to separate the functions. Choose a value for R7 that sets the overvoltage protection level very high (2X expected), and adjust R6 to give the flattest current limit vs. line voltage characteristic. When the value for R6 is set, pick the value for R7 to give the correct overvoltage protection.

4.8 Filter capacitor for Vcc

The dimming requirement sets a minimum size for this capacitor. During the dimmer's non-conducting period the line is not present for the internal startup circuit to take over, so the stored energy in this part is used to keep the chip alive.

At low conduction angles the capacitor is barely topped off, and it must hold the Vcc voltage above the shut-off threshold for a half cycle. At the same time, the LEDs are operating on very low current, and the reflected voltage is smaller than normal, and LED dependent.

The capacitor value therefore depends on the turns ratio of the auxiliary winding to the output winding, the LED voltage at minimum conduction angle, and the shut-off threshold.

A small 10 µF low-voltage ceramic was tried, but the voltage coefficient of capacitance was so high the part did not work in the dimming mode. Capacitance was too low to maintain power to the chip between dimmed line pulses. High-K ceramic capacitance falls off dramatically, well below the rated voltage. A 10 µF electrolytic was then selected - it works well.

4.9 COMP pin capacitor

Because the HVLED815PF is used only in current limit mode when driving LEDs, the usual loop stability compensation network is not needed. Voltage limiting is used only when the LED string is open (think of bench testing…) and the comp pin capacitor needs to be small so that overvoltage response is quick. 1 nanofarad is a good value.

4.10 Current sense resistor

This resistor value is determined by the average LED current desired and turns ratio of the transformer, according to a formula, as follows:

Equation 3

$$I_{LED}=\frac{n}{2}\cdot\frac{V_{CLED}}{R_{SENSE}}$$

where n is the transformer turns ratio, V_{CLED} the internal reference, and R_{SENSE} the current sensing resistor. Internally, V_{CLED} is 0.2 V.

This is the ideal situation. In fact, because the transformer is not the ideal transformer, imperfect coupling makes the actual turns ratio less than the designed value. Also the voltage feed-forward compensation and demagnetizing time further reduce the actual LED current from the calculated number. Typically, the coefficient K is around 0.85~0.9. Therefore the formula to determine the resistor is:

Equation 4

$$R_{SENSE}=K\cdot\frac{n}{2}\cdot\frac{V_{CLED}}{I_{LED}}$$

For this demo board, with turns ratio of 2 and a 1.00 Ω, 1% current sensing resistor, we get the LED current around 180 mA. For different designs, tweaks may be needed, but once the final values are selected, repeatability from unit to unit is excellent.

4.11 AC injection divider (R3, R4)

In the US, line current total harmonic distortion must be kept below 20% of the 60 Hz fundamental.

The input current is already distorted due to the use of a sinusoidal peak current envelope. Input current harmonic distortion actually improves slightly when the line current goes to zero for a short time around the voltage zero crossing. The distortion minimum only occurs at one input voltage, increasing as the line voltage is moved away from that point. The average of the injected AC waveform (not the RMS value) should be set approximately equal to the DC level required to give the correct current to the LEDs. At nominal line the average injected voltage is close to 0.95 V - the RMS voltage is 1.111 times the average, or 1.05 V, peak voltage is about 1.45 V. Again, tweaking may be necessary, but repeatability between units is excellent once the values are selected.

There are two limits on the impedance of the network:

- Loss in the divider (mostly the upper resistor), which affects efficiency
- Impedance at the ILED pin should be much lower than that of the internal duty cycle calculation circuitry.

An upper divider resistance of 270 kΩ keeps resistive loss low:

Equation 5

$$P = \frac{V^2}{R} = 120 \cdot 120/270{,}000 = 53\text{mW}$$

The efficiency reduction for this loss is 0.053 W/9.8 W = 0.54%.

The impedance looking into the ILED pin of the HVLED815PF is approximately 1.5 V/ 10 µA = 150 K. This varies with duty cycle - it is lower as the line voltage is increased.

The injected voltage needed at the divider tap should be just sufficient enough to shut off the FET at the line zero crossing. The average of this voltage should therefore be equal to the average of an equivalent DC-input converter supplying the LEDs. The actual value of the lower resistor is determined experimentally to give the best compromise between high line and low line THD.

With the 270 kΩ upper divider resistor and the impedance of the ILED pin in parallel, a 3 kΩ resistor gives good results. THD is acceptable across the 90 V to 132 V voltage range. The divider values are not critical - 5% resistors are adequate.

A small capacitor across the lower divider resistor smooths the current pulses from the duty cycle measurement circuitry and helps keep switching noise out of the system. This should be in the range of 10 nanofarads for the switching frequency used in the demo.

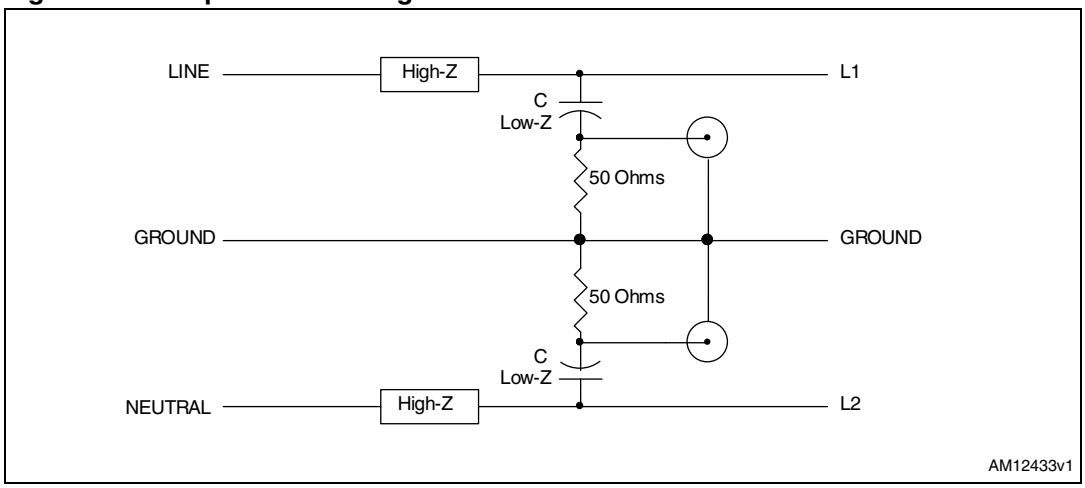
4.12 EMI filter design

In the US, conducted noise is measured between 150 kHz and 30 MHz. Low frequency noise is the most difficult to filter. The operating frequency was selected so that the fundamental is just below the measurement band, and the second harmonic frequency is as high as possible.

The noise injected into the line can be broken into two components, differential mode and common mode. We consider only differential mode noise in this non-isolated design. Good layout minimizes common-mode noise.

Conducted emission testing is done with a standard line impedance simulation network (LISN). A simplified diagram is shown below.

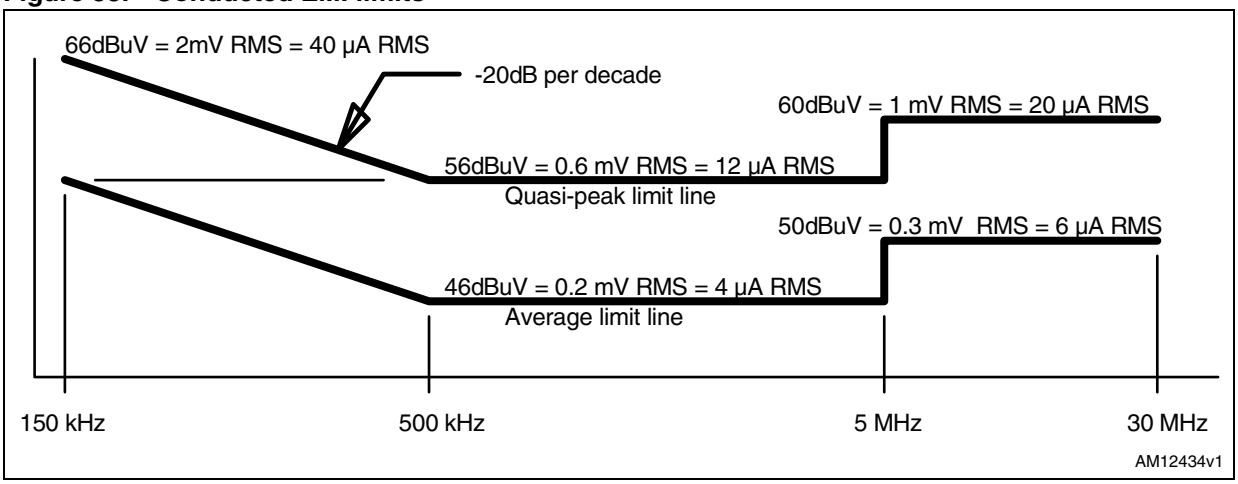
Figure 32. Simplified LISN diagram



Differential impedance in the noise spectrum (150 kHz to 30 MHz) is 100 Ω line-to-line, 50 Ω line-to-ground.

We design for peak noise at the FCC limit at 150 kHz. The design leaves some margin due to the frequency selection. Peak-to-peak of the 2 mVrms limit is about 6 mV per line relative to ground.

Figure 33. Conducted EMI limits



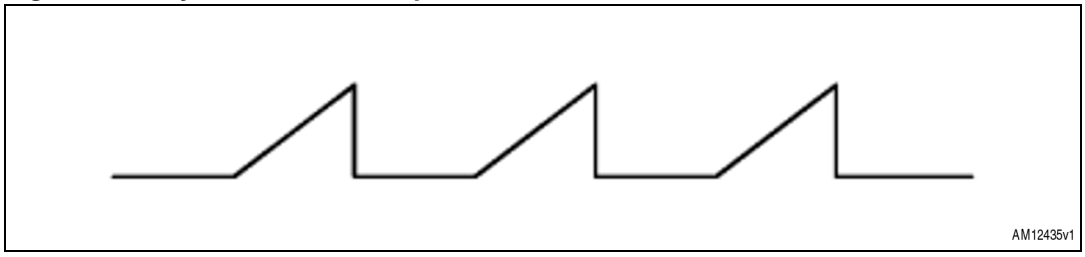
The typical differential filter consists of 4 components. Starting at the noise source, these are:

- Shunt capacitor on the converter input (C3)
- Series inductor (L1)
- Shunt capacitor across line (C2)
- Line impedance (in the LISN, about 100 Ω line-to-line at measurement frequencies).

4.12.1 Supporting the flyback input current

First we consider the differential current drawn by the converter. The input current waveform at line peak is sketched below:

Figure 34. Flyback converter input current waveform



The peak current is about 0.7 A, and the ON-time is about 3.5 microseconds. The charge that must be delivered by the capacitor directly across the converter each cycle is about:

Equation 6

$$Q = \frac{It}{2} = 0.7A \text{ x } 3.5e\text{-}6seconds/2 = 1.2 \text{ microcoulombs}$$

The capacitance needed was determined experimentally - 0.1 µF is a good starting point at this power level.

So, ripple voltage for the 0.1 µF capacitor is about:

Equation 7

$$V = \frac{Q}{C} = \frac{1.2uC}{0.1uF} = 12Vp - p$$

4.12.2 Shunting the HF noise

Next we examine the input capacitor. We use 0.1 µF here as well.

Values as small as 0.047 µF can be made to work, but the inductor value must increase to keep the noise on the AC line low enough. The resulting inductors either become physically large, or the resistive loss in the winding affects efficiency.

4.12.3 Limiting the noise current

At 150 kHz, the 0.1 µF capacitor has a reactance of about 10 Ω This reactance shunts away 90% of the noise current from the LISN, leaving only about 10% to the input. So 12 Vp-p must be reduced to about 12 mVp-p (half the noise appears on each line terminal relative to ground).

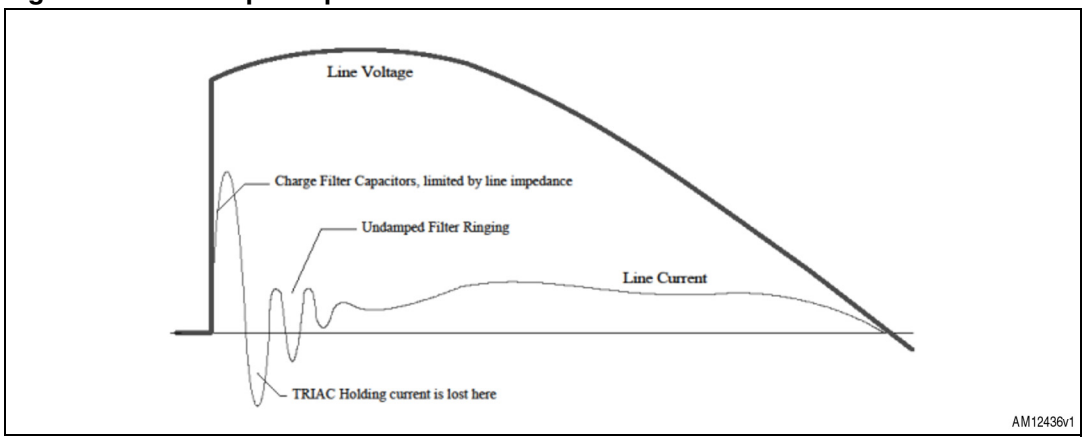
The inductor must have a reactance of at least 1000 Ohms at 150 KHz. It was found experimentally that a 4.7 mHy part worked well. The selected inductor has about 5.5 W of DC resistance, so I2R loss is relatively low.

4.13 EMI filter and dimming

4.13.1 Damping the input filter

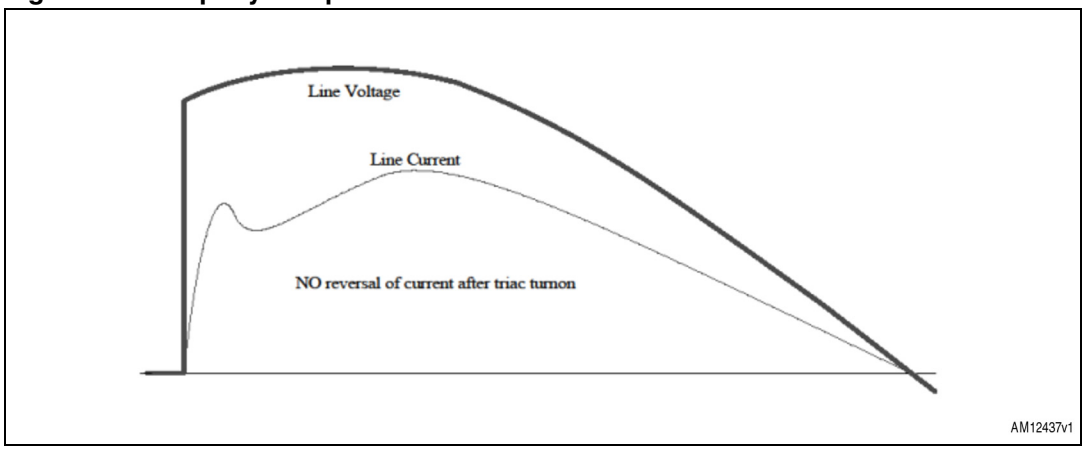
When the unit is dimmed a large transient voltage appears on the filter input capacitor:

Figure 35. Undamped input filter waveforms with Triac dimmer



To maintain Triac holding current, the ringing must be damped. The best way to do this is to add an R-C network across the filter output, where the network impedance is highest. Ideally, the input current waveform should look like this:

Figure 36. Properly damped waveforms



Actually, some high-frequency ringing can be tolerated, if the current reversal time is less than the turn-off time of the Triac, about 20 microseconds. The input filter, however, would ring at about:

Equation 8

$$f = \frac{1}{2\pi\sqrt{LC}} = 0.159/(4.7\text{mHy} \cdot 0.1\text{uF})^{0.5} = 7330\ \text{Hz}$$

so current reversal time would be in the 70 microsecond range. Damping is required.

The filter's output impedance is high, the impedance at the line end is low. In fact, the line end of the network is much less than the 100 Ω of the LISN at the ringing frequency, almost

insignificant for the damping function. So the ringing network primarily consists of the filter inductor and the converter input capacitor.

The typical damping network across a current-sink load would consist of a capacitor and a resistor in series. The minimum capacitor value would be 3 times the filter capacitance (3X C1, use 0.33 µF), and a resistor of:

Equation 9

$$Z = \sqrt{\frac{L}{C}} = (4.7\text{mHy}/0.33\text{uF})^{0.5} = 119\ \Omega.$$

However, power dissipation in the damping resistor can be a problem. If the dimmer is set to 90 degrees conduction, the input voltage comes on at the peak of the line waveform. The damping resistor must charge the damping capacitor 120 times a second to the peak line voltage. For each transient, the energy dissipated in the resistor is slightly less than:

Equation 10

$$E = 0.5CV^2 = 0.5 \cdot 0.33uF \cdot 2 \cdot 120V^2 = 4.7\text{mJ}$$

$$4.7\text{mJ} \cdot 120 = 0.57\text{W}.$$

Other damping mechanisms exist, however, so the damping network does not need to be so large. Reducing the size of the capacitor would allow the use of a 1/2 W resistor.

The PFC-flyback converter, unlike a regulating converter, has a POSITIVE input resistance near the filter's resonant frequency. The input current it draws increases when the line voltage increases, short term. This contributes some damping. The effective resistance can be calculated from line voltage and input power. Input power is about 11 W. At nominal line the input resistance is:

Equation 11

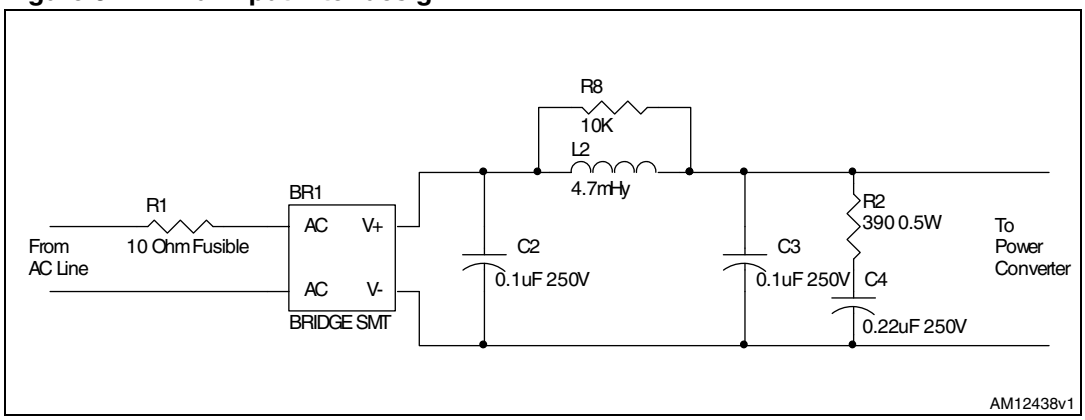
$$R = \frac{V^2}{P} = 14400/11 = 1310\ \Omega$$

Note that this resistance rises and falls as the square of the line voltage.

Some additional damping is provided by the winding resistance of the inductors and the fusible resistor. It was found experimentally that the ringing could be completely damped with a series R-C network of 0.22 µF and 390 Ω

The final filter design is shown below:

Figure 37. Final input filter design



The actual transient input waveforms are shown below for different scales:

Figure 38. Input transient at 200 mA/div, 2.5 ms/div

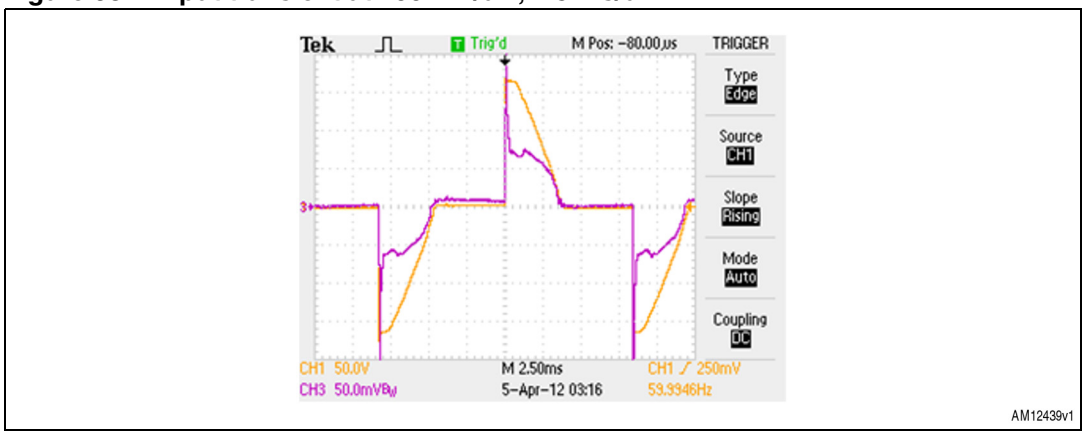


Figure 39. Input transient at 500 mA/div, 500 µs/div

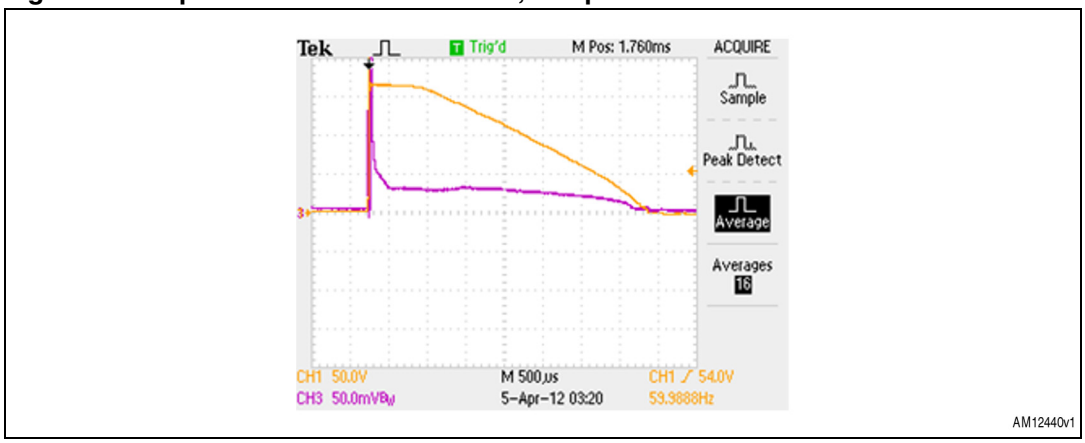
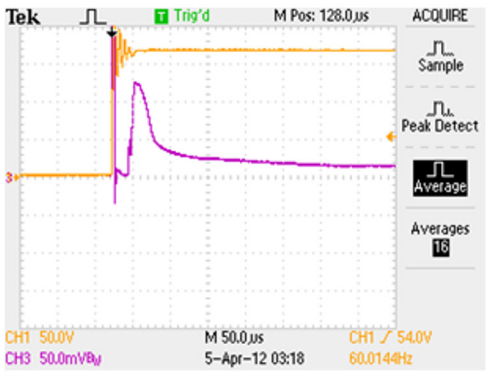


Figure 40. Input transient at 1 A/div, 50 µs/div



Where:

- Yellow = Triac dimmed line voltage
- Magenta = line current, scale below.

The rather high current spike at the leading edge is due to the input capacitor charging through the fusible resistor. A small inductor may be added to soften this if space permits, but it does no harm.

Even if Triac dimming is not required, the damper should be used. The EMI filter can ring up the supply voltage to very high levels at turn-on if it is not present, and instability has been seen without the damper under normal operating conditions.

5 Bill of materials

Table 2. BOM

Designator	Comment	Description	Footprint	Manufacturer	Vendor
BR1	BRIDGE SMT	1 A DIP BRIDGE	RH0x	Diodes Inc RH06-T	Digi-Key RH06DICT-ND
C2, C3	0.1 µF 250 V	Capacitor	BoxSDLWH5-0.5-8-6.3-11.2	Panasonic ECQ-E2104KB	Digi-Key P10967-ND
C4	0.22 µF 250 V	Capacitor	BOXSDLWH7.5-0.6-10.3-6-10.8	Panasonic ECQ-E2224KB	Digi-Key P10971-ND
C5	1 nF	Capacitor	0805	0805 X7R	
C6	4.7 µF 25 V	Capacitor	0805	Taiyo Yuden TMK212BJ475KG-T	Digi-Key 587-1782-1-ND
C7	10 nF	Capacitor	0805	0805 X7R	
C8	10 µF 35 V	Capacitor	CEV5MMP	Nichicon UPW1V100MDD6	Digi-Key 493-1850-ND
C10	330 pF	Capacitor	1206	AVX 12062A331JAT2A	Digi-Key 478-1433-6-ND
C11	330 µF 63 V	Capacitor	CEH12dx20L	Panasonic EEU-FC1J331	Digi-Key P10349-ND
D1	BAT48ZFILM	Schottky diode	SOD-123	ST BAT48ZFILM	
D2	MMSD4148	Signal diode 150-200 mA 100 V 4 ns	SOD-123	MMSD4148	
D3	STTH102A	Diode	SMA	ST STTH102A	
L2	4.7 mHy	Inductor	INDUC9MMVERT	Wurth 744 772 472 or 744 745 2 472	Digi-Key 732-3790-ND or 732-3084-ND
R1	10 Ω fusible	Resistor	resaxvert0.5w	Vishay/BC Components NFR0100001009JR500	Digi-Key PPC10CCT-ND
R2	390 0.5 W	Resistor	RES0.5	VISHAY NFR25H0003900JR500	Digi-Key PPC390BCT-ND
R3	270 kΩ	Resistor	1206	1206 5%	
R4	3.0 kΩ	Resistor	0805	0805 5%	
R5	1R00 1%	Resistor	1206	1206 1%	
R6	22 kΩ	Resistor	0805	0805 5%	
R7	2.4 kΩ	Resistor	0805	0805 5%	
R8	10 kΩ	Resistor	1206	1206 5%	
R9	43 kΩ	Resistor	1206	1206 5%	

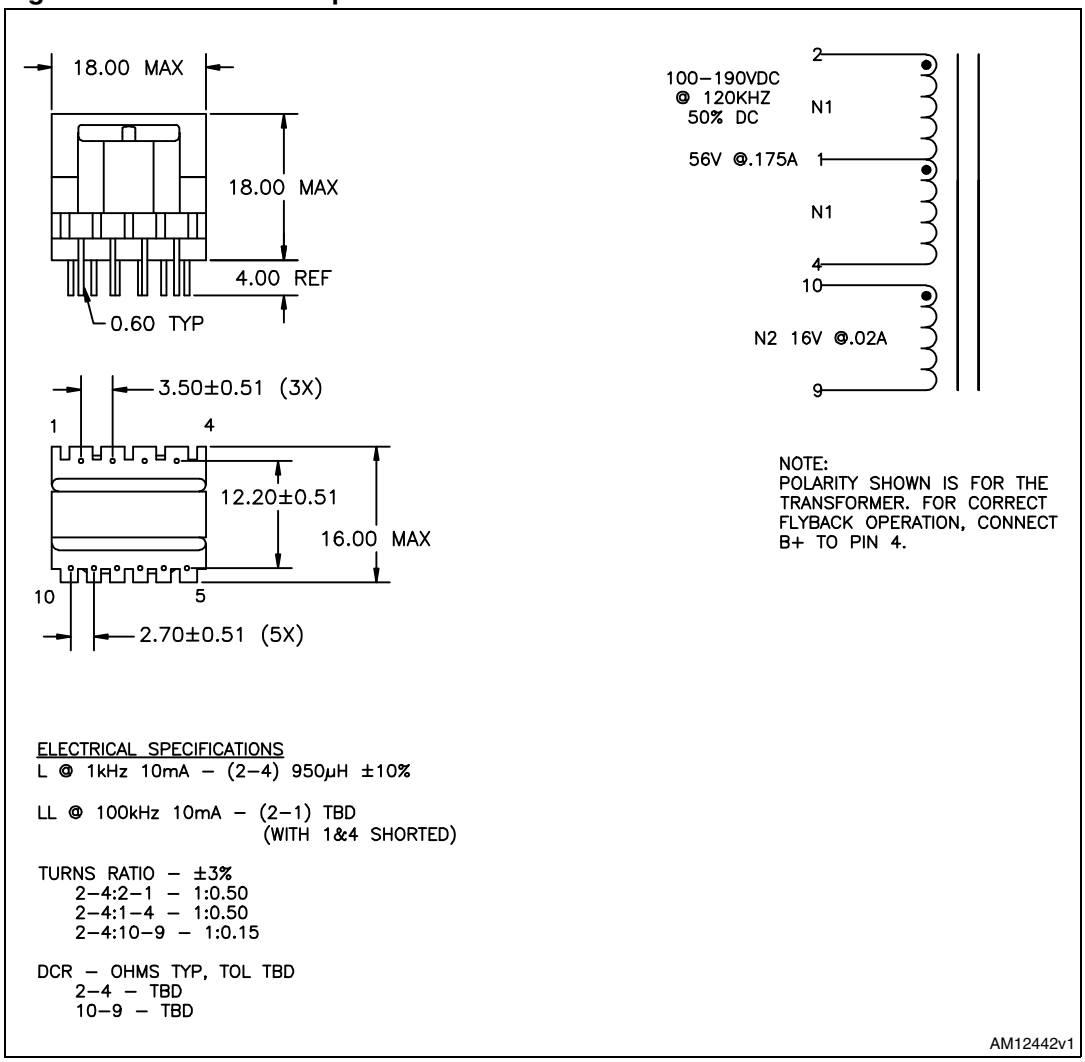
Table 2. BOM (continued)

Designator	Comment	Description	Footprint	Manufacturer	Vendor
T1	Cramer CSM 16VT-141	Cramer CSM2010 S-P Dual Sec	CRAMER CVP11	Cramer CSM 16VT-141	
U1	HVLED815PF	LED driver PFC	SO-16 - no pad pin 12	ST HVLED815PF	

6 Transformer specifications

For 18 LEDs (matches bill of materials and performance report).

Figure 41. Transformer specification for 18-LED load



7 Extensions and modifications

7.1 Lower output voltage, higher current

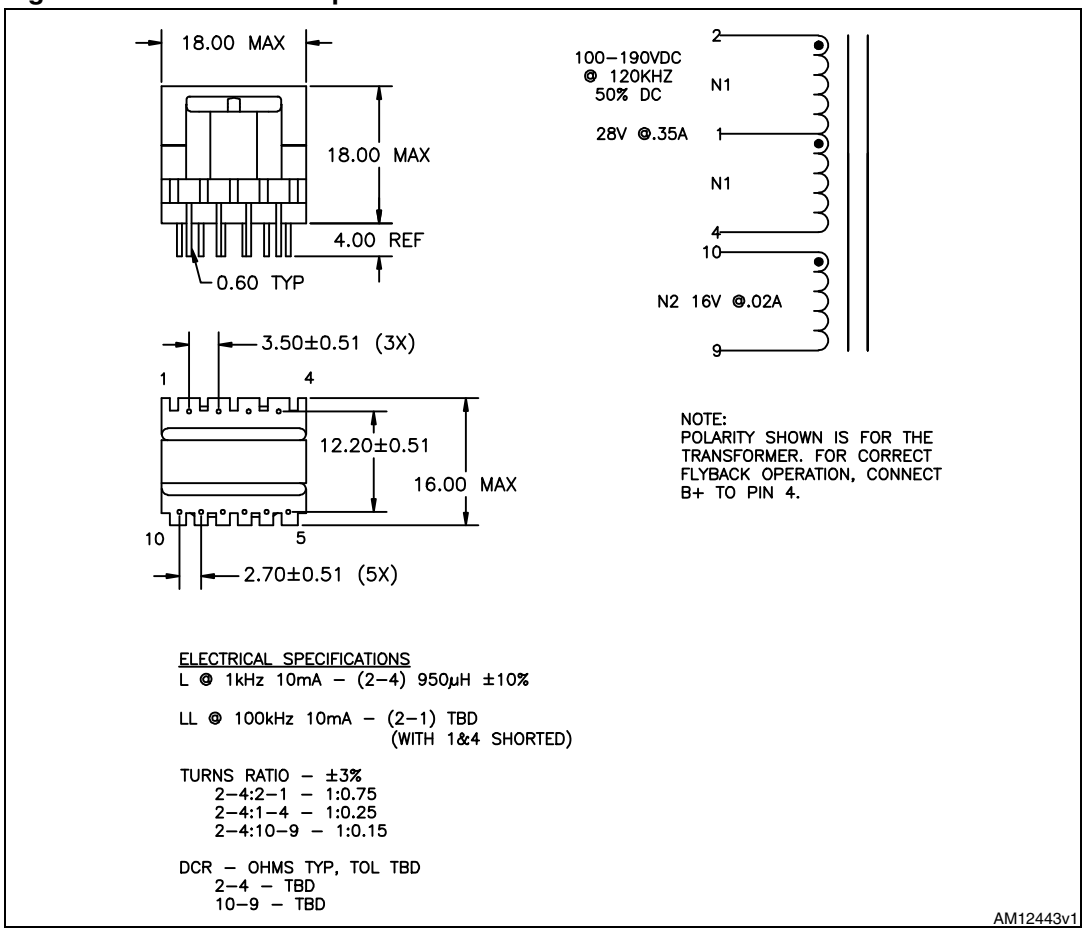
Components are listed below for a version to drive 9 LEDs at twice the current, 350 mA. Some other changes must also be made to the secondary side:

- Change snubber capacitor C10 to a high-quality part of four times the value, such as a 1200 pF COG ceramic rated for 200 V.
- Change diode D3 to a 150 V Schottky type such as ST's STPS1150 to reduce voltage drop. Efficiency is reduced if this change is not made.
- Change the output capacitor to one having 4 times the capacitance and half the voltage rating, 1000-1200 µF at 35 V. This maintains the ripple current near the same percentage of LED current as the original design.
- Change the preload resistor to one having ¼ the original resistance.
- Change the power transformer to Cramer CSM 16VT-140 (specification below). This transformer has the primary tap ¼ of the way down from the positive rail, giving half the turns ratio of the CSM 16VT-141.

There are no changes needed on the primary side.

The transformer specification for the 9-LED design is shown in *Figure 42*.

Figure 42. Transformer specification for 9-LED load



7.2 Higher line voltage

This is almost a wide-range design, dimmable at 90 V-130 V, and operable from 90 V to 305 V. The only thing preventing this is the voltage rating of capacitors and the output diode. The HVLED815PF's internal FET is rated for 800 V, a good design margin for European 230 V lines and US 277 V lighting circuits. The design is not sensitive to input frequency. AC injection divider (R3-R4) is adjusted, reasonable harmonic distortion (THD) performance can be expected from 180 V to 305 V.

At higher input voltage the surge limiting resistor R1 should be coordinated with the single-cycle surge rating of the input bridge. Triac dimming at higher input voltage requires redesign of the input filter.

8 PC layout

Figure 43. Top placement

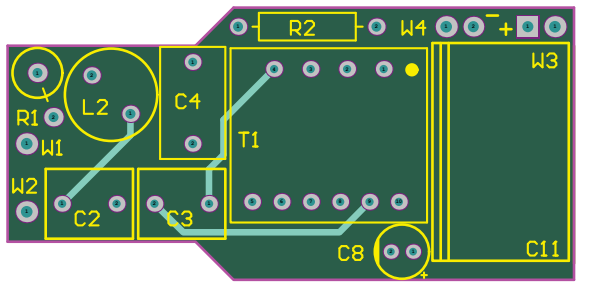


Figure 44. Top copper

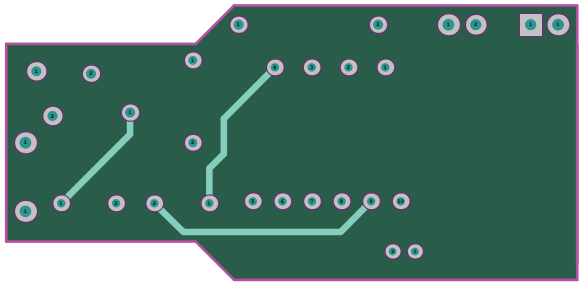


Figure 45. Bottom placement

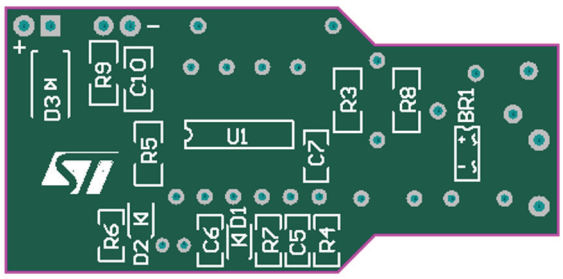
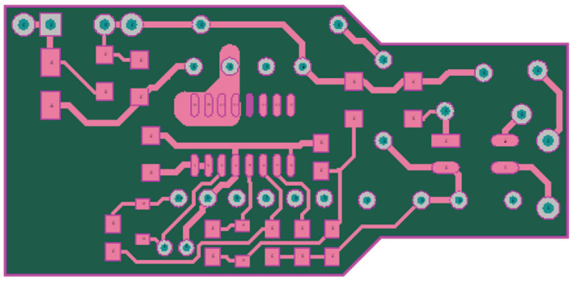


Figure 46. Bottom layer



9 References

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2. DB1534 EVLALTAIR05T-5W, “ALTAIR05T-800 5 W wide range CV-CC optoless adapter demonstration board”, rev 1, data brief.
3. HVLED805, “Off-line LED driver with primary-sensing”, rev 1, datasheet.
4. AN3360, “3.2 W LED Power Supply based on HVLED805”, rev 2, application note.
5. HVLED815PF, “Off-line LED driver with primary-sensing”, rev 1, datasheet.
6. US Patent 5,729,443 “Switched Current Regulator with Improved Power Switch Control Mechanism” Pavlin (1998)
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8. AN1059, “Design Equations of High-Power-Factor Flyback Converters based on the L6561”, rev 1, application note
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10. AN2838, “35 W Wide-Range High Power Factor Flyback Converter Demonstration Board using the L6562A”, rev 1, application note
11. AN4129, “9W Triac dimmable, high power factor, Isolated LED driver based on HVLED815PF (for US Market)”, rev 1, application note.

10 Revision history

Table 3. Document revision history

Date	Revision	Changes
03-Sep-2012	1	Initial release.

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