AN4149
Application note

Designing a CCM PFC pre-regulator based on the L4984D

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Introduction

Two methods of controlling power factor corrector (PFC) pre-regulators based on boost topology are currently in use: the fixed-frequency (FF) PWM and the transition mode (TM) PWM (fixed on-time, variable frequency).

With the first method the boost inductor works in a continuous conduction mode (CCM) and employs average current-mode control, a relatively complex technique requiring sophisticated controller ICs (e.g. the L4981A/B from STMicroelectronics) and a considerable component count.

The second one uses the more simple peak current-mode control and makes the inductor work on the boundary between continuous and discontinuous mode, which is implemented with cheaper controller ICs (e.g. the L6562A, L6563x and L6564x from STMicroelectronics), and much fewer external parts, making it far more cost efficient. For a given power throughput, TM operation involves higher peak currents compared to FF-CCM (see the figures below).

Figure 1. Line and inductor currents in CCM PFC

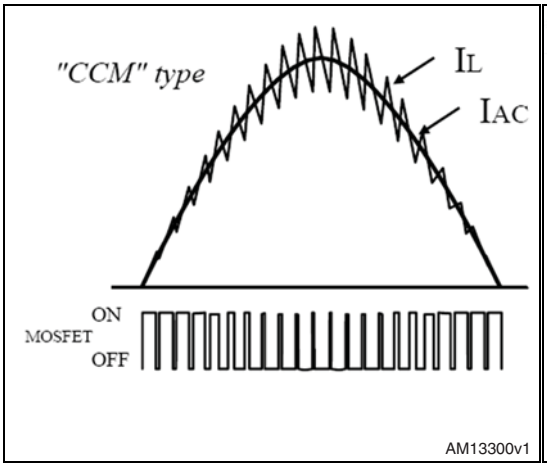
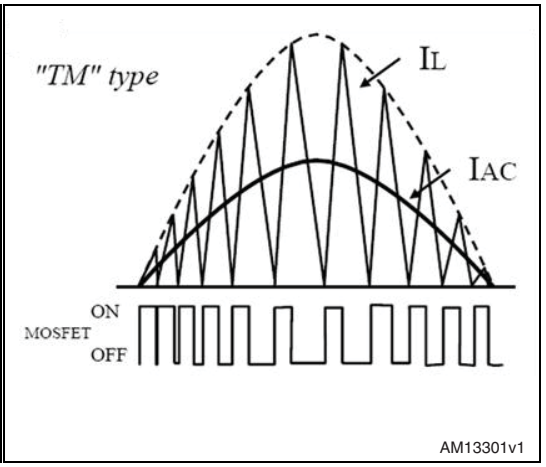


Figure 2. Line and inductor currents in TM PFC



This demonstration, consistent with the above-mentioned cost considerations, suggests the use of TM in a lower power range, while FF-CCM is recommended for higher power levels. In the power range of around 150-300 W, assessing which approach gives the better cost/ performance trade-off needs to be done on a case-by-case basis, considering the cost and stress of both power semiconductors and magnetic components, but also of the EMI filter.

At the same power level, the switching frequency component to be filtered out in a TM system is twice the line current, whereas it is typically 1/3 or 1/4 in a CCM system. In this document the CCM using a fixed-off-time (FOT) control mode, fully integrated in the controller, is proposed, coupling simplicity and low port count similar to a TM control. The design procedure is explained too.

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Fixed-frequency PWM is not the only alternative when CCM operation is desired. An additional approach that couples the simplicity and affordability of TM operation with the high-current capability of CCM operation can be a solution to the problem.

Fixed-frequency PWM modulates both switch ON and OFF times (their sum is constant by definition), and a given converter operates in either CCM or DCM depending on the input voltage and the loading conditions. Exactly the same result can be achieved with FOT approach: a conventional "peak" current mode control, where the ON-time T_{ON} of the external power switch is determined by the peak inductor current reaching the programmed value and the OFF-time T_{OFF} is determined by a special Fixed-off-time (FOT) modulator in such a way that the resulting switching period is constant as long as the boost converter is operated in CCM (i.e. the current in the boost inductor remains greater than zero in a switching cycle).

In *Figure 3* a block diagram of an FOT-controlled CCM PFC pre-regulator is shown. An error amplifier (VA) compares a portion of the boosted output voltage V_{out} with a reference VREF and generates an error signal V_C proportional to their difference, a DC voltage by hypothesis, which is fed into an input of the multiplier block and multiplied by a portion of the rectified input voltage V_{MULT}.

The multiplier output (VCSREF) is a rectified sine wave whose amplitude is proportional to that of V_{MULT} and to V_C, and is used as a reference for PWM modulation. The multiplier output is fed into the inverting input of a PWM comparator that, on the non-inverting input, receives the voltage VCS from the sense resistor Rsense, proportional to the current flowing through the switch M (typically a MOSFET) and the inductor L during the ON-time of M.

When the two voltages are equal, the comparator resets the PWM latch and M is turned off. As a result, the multiplier output determines the peak current through the switch and the inductor, and as, it is a rectified sinusoid, the inductor peak current is also enveloped by a rectified sinusoid.

When VCSREF and VCS are equal the PWM latch output Q going high activates the timer that, after a predetermined time in which T_{OFF} has elapsed, sets the PWM latch, therefore turning the switch on and starting another switching cycle.

If T_{OFF} is such that the inductor current does not fall to zero, the system operates in CCM. For the CCM PFC controller, please refer to *Figure 4*.

To understand how T_{OFF} needs to be modulated to achieve a fixed switching frequency independent of the instantaneous line voltage and the load, it is useful to consider the V·s balance equation for the boost inductor under the assumption of CCM operation:

Equation 1

$$T_{ON}\, Vpk \sin\theta = T_{OFF}\left(Vout - Vpk \sin\theta\right)$$

where Vpk is the peak line voltage, V_{out} is the regulated output voltage, and θ is the instantaneous phase angle of the line voltage. Solving for T_{ON} we get:

Equation 2

$$T_{ON} = \left(\frac{Vout}{Vpk \sin\theta} - 1\right) T_{OFF}$$

then, the switching period T_{SW} will be:

Equation 3

$$T_{sw} = T_{ON} + T_{OFF} = \left(\frac{Vout}{Vpk \sin\theta} - 1 \right) T_{OFF} + T_{OFF} = \frac{Vout}{Vpk \sin\theta} T_{OFF}$$

In the end, if T_{OFF} is changed proportionally to the instantaneous line voltage, i.e. if:

Equation 4

$$T_{OFF} = K_t Vpk \sin\theta$$

then T_{SW} will be equal to $Kt \cdot V_{out}$ and, since V_{out} is regulated by the voltage loop, also T_{SW} (and $f_{SW}=1/T_{SW}$) will be fixed. This result is based on the sole assumption that the instantaneous line voltage and the output load are such that the boost inductor operates in CCM.

Figure 3. Block diagram of an FOT-controlled PFC preregulator

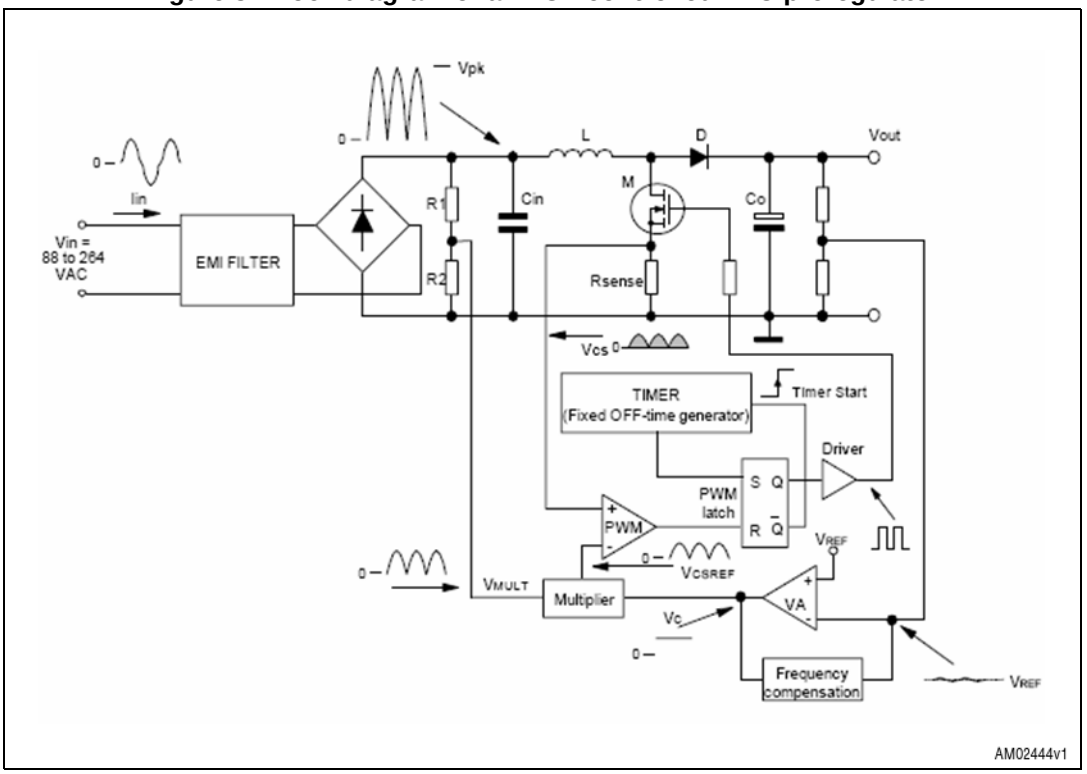


Figure 4. Line-modulated FOT modulator internal block diagram

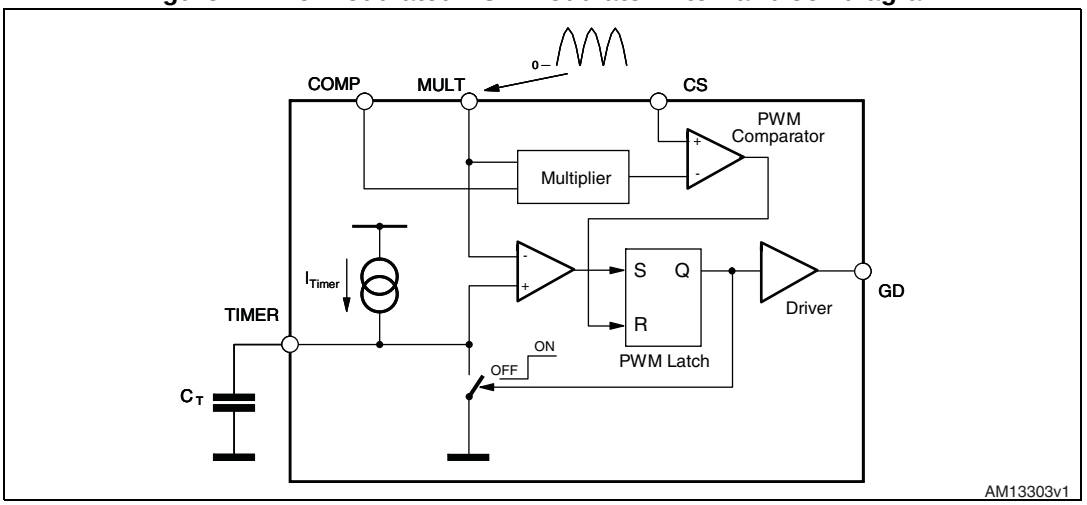
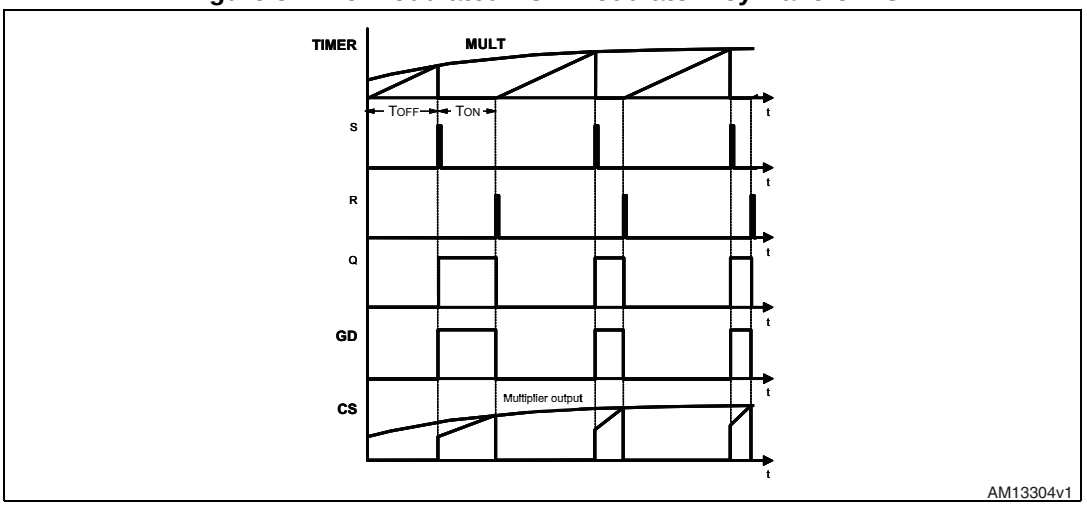


Figure 5. Line-modulated FOT modulator key waveforms



With reference to the block diagram (*Figure 4*) and the relevant key waveforms in *Figure 5*, an OFF-time proportional to the instantaneous line voltage is achieved by charging the capacitor C_T with a constant current I_{TIMER}, accurately fixed internally and temperature compensated, while the MOSFET is off and commanding MOSFET's turn-on (and resetting C_T at zero) as the voltage across C_T equals that on the pin MULT. The voltage on this pin is:

Equation 5

$$V_{MULT} = K_P \, Vpk \, sin\theta$$

where K_P is the divider ratio of the resistors biasing pin MULT. As a result:

Equation 6

$$T_{OFF} = \frac{C_T}{I_{TIMER}} K_P \, Vpk \, sin\theta \quad \rightarrow \quad K_t = \frac{C_T}{I_{TIMER}} K_P$$

and the switching frequency will be:

Equation 7

$$f_{sw} = \frac{1}{T_{sw}} = \frac{I_{TIMER}}{K_P\, C_T\, Vout} = \frac{1}{K_t\, Vout}$$

The timing capacitor C_T, therefore, will be selected with the following design formula:

Equation 8

$$C_T = \frac{I_{TIMER}}{K_P\, Vout\, f_{sw}}$$

V_{out} and f_{sw} are design specifications, K_P is chosen so that the voltage on pin MULT is within the multiplier's linearity range (0 to 3 V) and I_{TIMER} is specified in the "Electrical characteristics" section of the L4984D datasheet.

Along a line half-cycle, T_{OFF} goes all the way from nearly zero to the maximum on the sinusoid peak. It is important to check that the OFF-time occurring on the peak of the sinusoidal voltage at minimum input voltage is greater than the minimum programmable value:

Equation 9

$$T_{OFF\,min} = \frac{C_T}{I_{TIMER}} K_P\, Vpk_{min} > 1.2\,\mu s$$

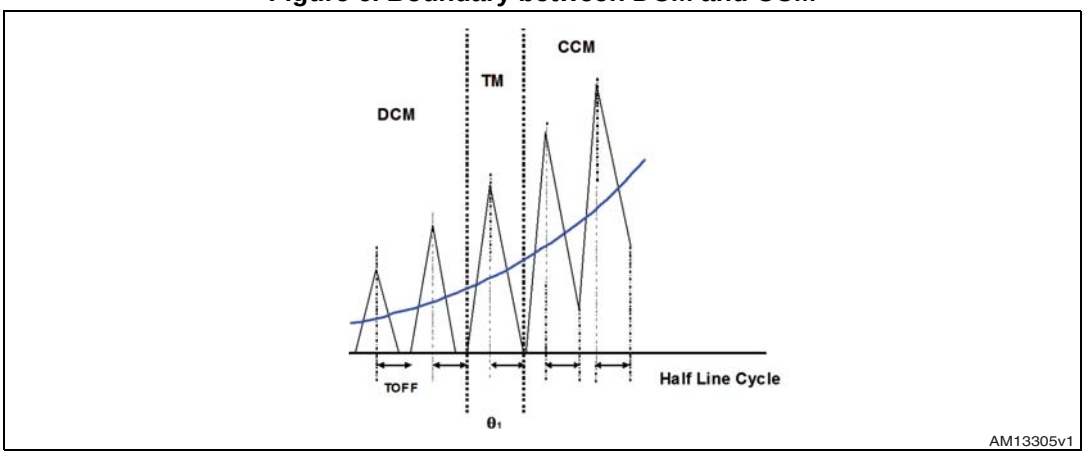
This constraint limits the maximum programmable frequency at:

Equation 10

$$f_{sw.max} = 833\frac{Vpk_{min}}{Vout} \qquad [KHz]$$

As the line RMS voltage is increased and/or the output load is decreased the boost inductor current tends to become discontinuous starting from the region around the zero-crossings. As a result, in the DCM regions the switching frequency is no longer constant and tends to increase.

Figure 6. Boundary between DCM and CCM



However, the frequency rise is significantly lower as compared to that of a transition-mode (TM) operated boost PFC stage, as illustrated in *Figure 7* and *8* .

Figure 7. Typical frequency change along a line half-cycle in a boost PFC operated in LM FOT

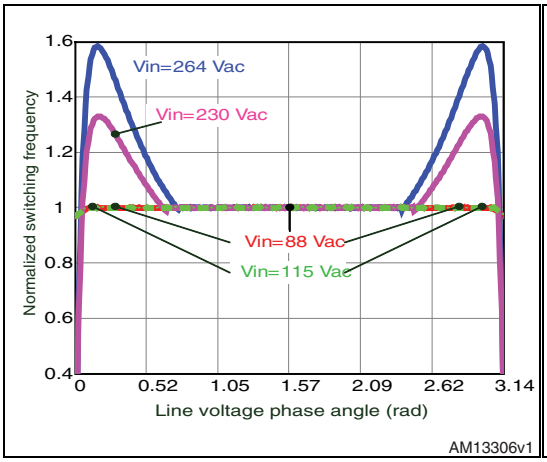
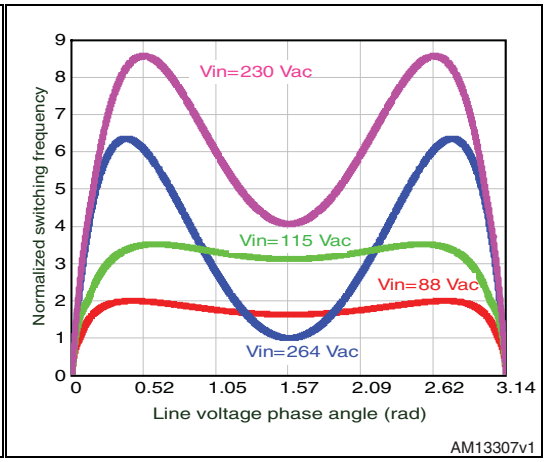


Figure 8. Typical frequency change along a line half-cycle in a boost PFC operated in TM



Due to the peak current vs. average current error which becomes much worse at low current levels (especially in DCM), the current that the boost PFC pre-regulator draws from the power line will not be exactly sinusoidal but will be affected by a distortion that will be lower as the current ripple in the boost inductor is smaller as compared to its peak value.

Figure 9 and *10* show some theoretical waveforms, relevant to full load condition, in a line cycle at different input voltages.

Figure 9. LM FOT controlled boost PFC: current waveforms (line current)

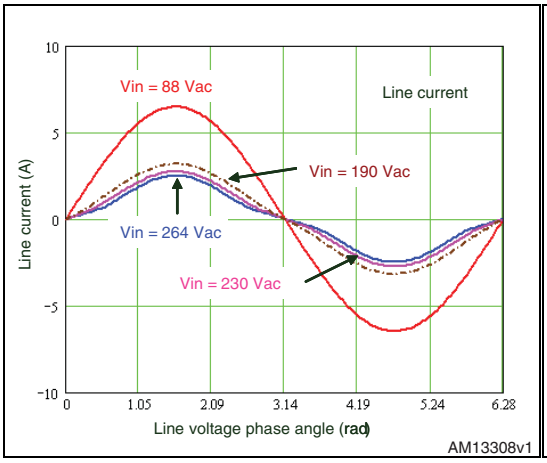
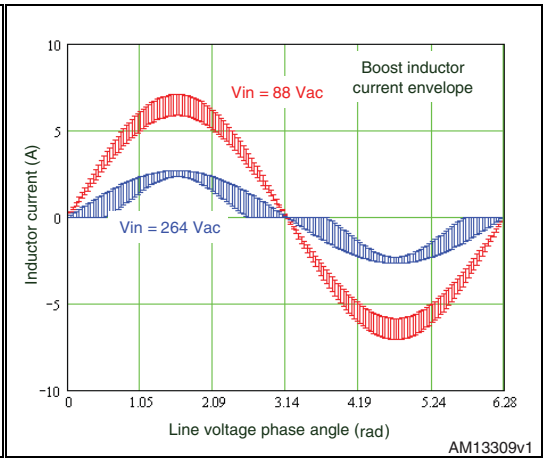


Figure 10. LM FOT controlled boost PFC: current waveforms (boost inductor current envelope)

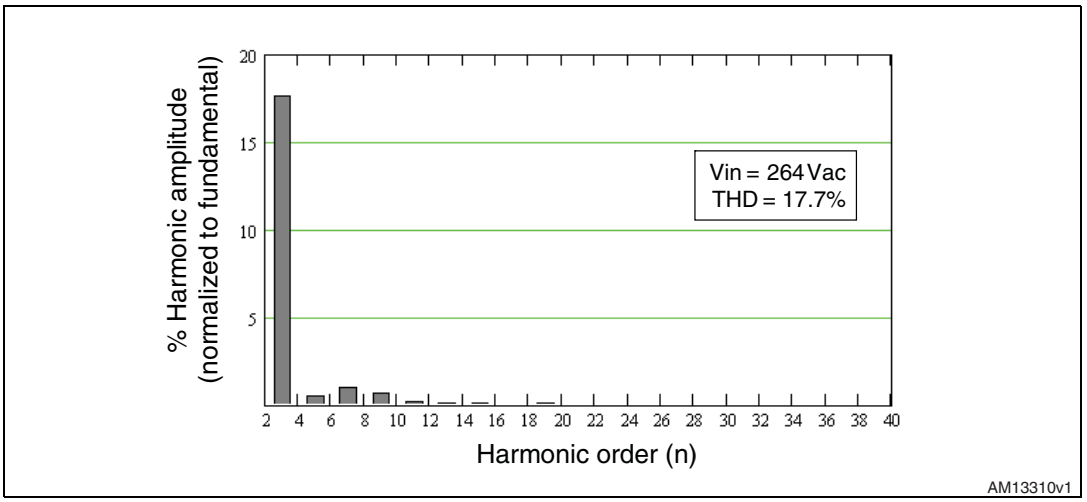


In *Figure 9* the line (input) current waveform is shown for different line voltages, while *Figure 10* illustrates the envelope of the inductor current at minimum and maximum line voltage.

The input current waveform relevant to V_{in} = 88 V_{ac} shows no visible sign of distortion; the operation of the boost inductor is CCM throughout the entire line cycle as shown by the

inductor current envelope. The brown waveform is relevant to V_{in}=190 V_{ac}, which is the condition where CCM operation no longer occurs at zero-crossings (this voltage value, for a given power level, depends on the inductance value of the boost inductor); a certain degree of distortion is already visible. The waveform relevant to V_{in} = 264 V_{ac} shows the highest degree of distortion and the largest portion of the line cycle where the boost inductor operates in discontinuous mode (DCM). However, its harmonic content, shown in *Figure 9* and *10*, is still so low that is not an issue for EMC compliance. Almost all the distortion is concentrated in the third harmonic, whose amplitude is 17% of the fundamental one, while the THD is 17.7%.

Figure 11. Line-modulated, FOT controlled boost PFC: input current harmonic contents



The compliance with conducted EMI emission regulations is also facilitated by the voltage ripple appearing across the output capacitor C_O , at twice the line frequency f_L, which has peak amplitude ΔV_{out} proportional to the output current I_{OUT}. As a consequence, f_{sw} is not constant but is modulated at $2f_L$, spreading the spectrum of the electrical noise injected back into the power line. The relative frequency change due to the output voltage ripple is:

Equation 11

$$\frac{\Delta f_{sw}}{f_{sw}} = \frac{\frac{\Delta Vout}{Vout}}{1+\frac{\Delta Vout}{Vout}}$$

where ΔV_{out} can be found with the following expression:

Equation 12

$$\Delta Vout = \frac{Iout}{4\pi f_L Cout}$$

2 Designing a CCM FOT-controlled PFC

2.1 Input specification

The following is a possible design procedure for a CCM FOT-controlled PFC using the L4984D. This first part is a detailed specification of the operating conditions of the circuit that is needed for the calculations of the design steps in the following sections.

In this example a 350 W wide-input range mains PFC circuit has been considered. Some design criteria are also given.

Mains voltage range (V_{acrms}) :

Equation 13

$$V_{AC\,min} = 90V \qquad V_{AC\,max} = 265V$$

Minimum mains frequency:

Equation 14

$$f_l = 47Hz$$

Rated output power (W):

Equation 15

$$P_{out} = 350W$$

Typically the output for a boost PFC output voltage is 400 V_{dc} as it has to be higher than the maximum rectified input voltage:

Equation 16

$$\sqrt{2} \cdot V_{AC\,max}$$

In cases where the maximum AC input voltage V_{ACmax} is higher than 265 V, as typical in ballast applications, the output voltage must be set higher accordingly. As a rule of thumb the output voltage must be set 6 or 7% higher than the maximum input voltage peak.

Regulated DC output voltage (V_{dc}):

Equation 17

$$V_{out} = 400V$$

The target efficiency and PF are set for the following calculations based on the operating condition of the PFC, here at minimum input voltage and maximum load. An efficiency of 92%, at minimum input voltage and maximum load, could be a starting point for a typical PFC.

Expected efficiency (%):

Equation 18

$$\eta = \frac{P_{out}}{P_{in}} = 92\%$$

Expected power factor:

Equation 19

$$PF = 0.99$$

Because of the narrow loop voltage bandwidth of the E/A to reject the ripple at twice the line frequency on the E/A output, the PFC output may experience overvoltage at startup or during load transients. In order to protect the controller from excessive output voltage that can overstress the output components and the load, in the L4984D a pin (PFC_OK, pin #6) has been dedicated to monitor the output voltage with a separate resistor divider. The divider is selected so that the voltage at the pin reaches 2.5 V if the output voltage exceeds a preset value (V_{OVP}) larger than the maximum V_{out} that can be expected, also including worst-case load/line transients.

Maximum output voltage (V_{dc}):

Equation 20

$$V_{OVP} = 430\,V$$

The output voltage has a ripple V_{out} at twice the line frequency ($2f_L$), and whose amplitude is proportional to the load and depends on the impedance of the output capacitor. The ripple amplitude determines the AC current flowing into the output capacitor and the ESR. The value of the maximum output voltage ripple accepted should be below a certain level to keep the output voltage far from the V_{OVP} limit during normal operating conditions, to increase hold-up time, and to reduce the AC losses on the output capacitor. The peak-to-peak voltage ripple V_{out} is usually selected in the range between 2-8% of the output voltage. Here a ratio of 5% is chosen for the output voltage ripple, that is 20 V.

Maximum output low frequency ripple (peak-to-peak):

Equation 21

$$\Delta V_{out} = 20V$$

The desired ripple on the output voltage is not the only parameter used to select the bulk capacitor. The hold-up time, if requested, should also be taken into account. The hold-up time is defined as the duration of time that a power supply's output will remain above a minimum level in case of mains dips.

The hold-up time (t_{Hold}) is measured from the time when the line voltage disappears to the time when the output voltage reaches the required minimum voltage value (V_{outmin}). A hold-up time of 10-20 ms is often required for today’s offline power supplies. Values of 300 V and 15 ms for the minimum output voltage after line drop and hold-up time, respectively, are chosen here:

Minimum output voltage after line drop (V_{dc}):

Equation 22

$$V_{out\,\min} = 300\,V$$

Hold-up time (ms):

Equation 23

$$t_{Hold} = 15ms$$

The design will be done on the basis of a maximum admitted ripple factor K_r , that is the ratio of the maximum peak-to-peak current ripple amplitude to the inductor peak current, at minimum line voltage and rated load. In the continuous conduction mode converters, the acceptable current ripple factor is typically fixed in a range between 20% and 35%. Low values for the K_r keep the peak-to-peak ripple current and the input current distortion low, but lead to larger inductor physical size. Choosing higher values for K_r , the inductor size can be smaller, but the input current distortion is increased. For this design, the maximum specified current ripple factor is chosen equal to 27%, as a trade-off between the inductor size and the input current distortion.

Ripple factor:

Equation 24

$$K_r = 0.27$$

In order to properly select the power components of the PFC and size the heat sinks, the maximum operating ambient temperature around the PFC circuitry must be known. Please note that this is not the maximum external operating temperature of the entire equipment, but it is the local temperature at which the PFC components are working. The power dissipation leading to a temperature rise combined with the ambient temperature must not result in any temperature exceeding the operating temperature rating of the components.

Maximum ambient temperature (°C):

Equation 25

$$T_{ambx} = 50°C$$

2.2 Operating conditions

The first step is to define the main parameters of the circuit, using the specifications given in *Section 2.1*.

Rated DC output current:

Equation 26

$$I_{out} = \frac{P_{out}}{V_{out}} \qquad I_{out} = \frac{350W}{400V} = 0.875A$$

Maximum input power:

Equation 27

$$P_{in} = \frac{P_{out}}{\eta} \qquad P_{in} = \frac{350\,W}{92} \cdot 100 = 380.4W$$

The maximum value of the RMS current circulating in the boost cell at the minimum line voltage of the selected range is equal to:

Maximum RMS input current:

Equation 28

$$I_{in} = \frac{P_{in}}{VAC_{\min} \cdot PF} \qquad I_{in} = \frac{380.4W}{90Vac \cdot 0.99} = 4.27A$$

In order to describe the energy and relevant equations concerning a boost PFC, the ratios of the voltage inputs of the boost converter to the regulated output voltage are defined. In particular k_{min} and k_{max} refer to the ratio of the minimum and the maximum input voltage to the output voltage, respectively.

Equation 29

$$k_{\min} = \sqrt{2}\frac{VAC_{\min}}{V_{out}} \qquad k_{\max} = \sqrt{2}\frac{90Vac}{400V} = 0.32$$

$$k_{\max} = \sqrt{2}\frac{VAC_{\max}}{V_{out}} \qquad k_{\max} = \sqrt{2}\frac{265Vac}{400V} = 0.94$$

Combining equation 28 and equation 29 the maximum line peak current can be found.

Maximum line peak current:

Equation 30

$$I_{PK\max} = \frac{2 \cdot P_{in}}{k_{\min} \cdot V_{out}} \qquad I_{PK\max} = \frac{2 \cdot 380.4W}{0.32 \cdot 400V} = 5.98A$$

Maximum inductor peak current:

Equation 31

$$IL_{PK\max} = \frac{\sqrt{2} \cdot P_{in}}{V_{AC\min} \cdot PF} \cdot \left(1 + \frac{K_r}{2}\right) \qquad IL_{PK\max} = \frac{\sqrt{2} \cdot 380.4W}{90V \cdot 0.99} \cdot \left(1 + \frac{0.27}{2}\right) = 6.85A$$

Inductor peak-to-peak ripple current :

Equation 32

$$\Delta IL_{PK\max} = K_r \cdot IL_{PK\max} \qquad \Delta IL_{PK\max} = 0.27 \cdot 6.85A = 1.85A$$

In order to calculate the losses of the switches, the RMS current flowing through the MOSFET and through the boost output diode are found.

Maximum RMS switch current:

Equation 33

$$ISW_{rms} = \frac{P_{in}}{\sqrt{2} \cdot V_{AC\,\min} \cdot PF} \cdot \sqrt{2 - \frac{16 \cdot k_{\min}}{3\pi}}$$

$$ISW_{rms} = \frac{380.4W}{\sqrt{2} \cdot 90V \cdot 0.99} \cdot \sqrt{2 - \frac{16 \cdot 0.318}{3\pi}} = 3.65A$$

Maximum RMS diode current:

Equation 34

$$ID_{rms} = \frac{P_{in}}{\sqrt{2} \cdot V_{AC\,\min} \cdot PF} \cdot \sqrt{\frac{16 \cdot k_{\min}}{3\pi}}$$

$$ID_{rms} = \frac{380.4W}{\sqrt{2} \cdot 90V \cdot PF} \cdot \sqrt{\frac{16 \cdot 0.32}{3\pi}} = 2.22A$$

It is worth reminding that the accuracy of the equations developed here is quite good at low line voltage and worsens at high line and as the power throughput is reduced. As the current stresses of the switches are calculated at maximum load and minimum line voltage, the previous expressions are acceptable for design purposes.

2.3 Power section design

2.3.1 Bridge rectifier

The input rectifier bridge can use standard slow recovery, low-cost devices. Typically a 600 V device is selected in order to have good margin against mains surges. An NTC resistor limiting the current at turn-on is required to avoid overstressing the bridge diodes.

The rectifier bridge power dissipation can be calculated starting from the input RMS current and the input average current through the bridge diodes.

Equation 35

$$\bar{I}_{in\_rms\_bridge} = \frac{\sqrt{2} \cdot I_{in}}{2} = \frac{\sqrt{2} \cdot 4.36A}{2} = 3.02A$$

Equation 36

$$\bar{I}_{in\_avg\_bridge} = \frac{\sqrt{2} \cdot I_{in}}{\pi} = \frac{\sqrt{2} \cdot 4.36A}{\pi} = 1.92A$$

The power dissipated on a D15XB60 bridge can be estimated combining equation 35 and equation 36 with the threshold voltage (V_{th}) and dynamic resistance (R_{diode}) of a single diode of the bridge, the values of which can be found in the datasheet of the diode.

Equation 37

$$P_{bridge} = 4 \cdot R_{diode} \cdot \bar{I}^{2}_{inrms} + 4 \cdot V_{th} \cdot \bar{I}_{in\_avg}$$

$$P_{bridge} = 4 \cdot 0.025\Omega \cdot (3.02A)^{2} + 4 \cdot 0.7V \cdot 1.92A = 6.29W$$

From this number and the given maximum ambient temperature T_{ambx} the total maximum thermal resistance required to keep the junction temperature below 125 °C is:

Equation 38

$$R_{th} = \frac{125°C - T_{ambx}}{P_{bridge}} \qquad R_{th} = \frac{125°C - 50°C}{6.29W} = 11.92\frac{°C}{W}$$

2.3.2 Input capacitor

The input filter capacitor, C_{in}, is placed across the output of the bridge diodes. This capacitor must smooth the high-frequency ripple and must sustain the maximum instantaneous input voltage. In a typical application an EMI filter is placed between the mains and the PFC circuit. In this application the EMI filter is reinforced by a differential mode Pi-filter after the bridge to reject the differential noise coming from the whole switching circuit. The design of the EMI filters (common mode and differential mode) is not described here.

For wide-range operation the minimum value of the input filter capacitor can be calculated as follows, using a practical formula based on the output power that the PFC delivers at full load:

Equation 39

$$C_{in} = 2.5 \cdot 10^{-3} \cdot \frac{\mu F}{W} \cdot P_{out} \qquad C_{in} = 2.5 \cdot 10^{-3} \cdot \frac{\mu F}{W} \cdot 350W = 875nF$$

The maximum value of this capacitor has to be not much higher than the minimum value to avoid the distortion of the input mains current, due to the residual voltage retained by the capacitor that causes the diodes of the bridge rectifier to be reverse-biased and the input current flow to temporarily stop. The selected value for the input filter capacitor of this design is 1 µF.

2.3.3 Output capacitor

The output bulk capacitor (C_O) selection depends on the regulated DC output voltage, the output power, the RMS current into the capacitor, the output voltage ripple and hold-up time (if requested).

The value of the output capacitor to meet the output voltage ripple requirements can be defined using the following expression (equation 40). ΔV_{out} has to be intended as twice the mains frequency peak-to-peak voltage ripple, function of the capacitor impedance and the peak capacitor current. The contribution of the ESR (equivalent series resistance) is neglected here as the capacitive reactance is dominant.

Equation 40

$$C_o \geq \frac{I_{out}}{2\pi \cdot f_l \cdot \Delta V_{out}} = \frac{P_{out}}{2\pi \cdot f_l \cdot V_{out} \cdot \Delta V_{out}} \qquad C_o \geq \frac{350W}{2\pi \cdot 47Hz \cdot 400V \cdot 20V} = 148.1\mu F$$

where f_l is the minimum line frequency. Although ESR usually does not affect the output ripple, it should be taken into account for power loss calculation. The total capacitor RMS ripple current, including the mains frequency and switching frequency components, is:

Equation 41

$$I_{Crms} = \sqrt{ID^2{}_{rms} - I^2{}_{out}} \qquad I_{Crms} = \sqrt{(2.22A)^2 - (0.87A)^2} = 2.04A$$

Reading the ESR value of the datasheet of the output capacitor chosen, the power losses associated to this ripple current can be easily calculated by:

Equation 42

$$P_{Crms} = I_{Crms}{}^2 \cdot ESR$$

If the PFC stage has to guarantee a specified hold-up time, the calculation of the output capacitor is different. The value of the capacitor when the line voltage drops out, needed to deliver the output power for a certain time (t_{Hold}) until the output voltage reaches the required minimum voltage value (V_{outmin}), depends on the load and the value of the ripple. When V_{outmin} is reached, a 'power fail' is detected, stopping the downstream system supplied by the PFC. The worst case for the hold-up time is at minimum input voltage and full load, with the line drop starting at the valley of the sine-varying ripple of the output voltage.

Equation 43

$$C_o = \frac{2 \cdot P_{out} \cdot t_{Hold}}{\left(V_{out} - \frac{\Delta V_{out}}{2}\right)^2 - V^2_{out\,\min}} \qquad C_o = \frac{2 \cdot 350W \cdot 15ms}{(400V - 10V)^2 - (300V)^2} = 169\mu F$$

Considering a 20% tolerance on the electrolytic capacitors, a value of 200 µF has been chosen, using two capacitors of commercial value of 100 µF placed in parallel. The actual hold-up time and ripple voltage with the selected value are:

Actual hold-up time:

Equation 44

$$t_{Hold} = \frac{C_o \cdot \left[\left(V_{out} - \frac{\Delta V_{out}}{2}\right)^2 - V^2_{out\,\min}\right]}{2 \cdot P_{out}}$$

$$t_{Hold} = \frac{200\mu F \cdot \left[(400V - 10V)^2 - (300V)^2\right]}{2 \cdot 350W} = 18ms$$

Peak-to-peak output voltage ripple:

Equation 45

$$\Delta V_{out} = \frac{I_{out}}{2 \cdot \pi \cdot f_l \cdot C_o} \qquad \Delta V_{out} = \frac{0.87A}{2 \cdot \pi \cdot 47\,Hz \cdot 200\mu F} = 14.81V$$

2.3.4 Boost inductor

As indicated in the specs in *Section 2.1: Input specification*, the maximum current ripple factor K_r , that is the ratio of the maximum peak-to-peak current ripple amplitude to the

inductor peak current at minimum line voltage and rated load, is 27%, as a trade-off between the inductor size and the stress on the switches.

This choice led to the inductor peak-to-peak ripple current (IL_{PK}) equal to 1.89 A (equation 32).

The value of the inductance L required for the boost inductor can be calculated starting from the volt-second balance of the inductor. The minimum value of L is then a function of the duration of the OFF-time, the voltage across the inductor during T_{OFF}, and the inductor peak-to-peak ripple current.

Equation 46

$$L = \frac{V_{out} - \sqrt{2} \cdot V_{AC}}{\Delta IL_{pk}(V_{AC})} \cdot T_{OFF}(V_{AC})$$

The latter expression should be calculated at low line and the value found is the minimum inductance value of the PFC inductor. To find the value of L, first T_{OFF} needs to be calculated.

In a fixed-off-time control using the L4984D, the off-time (T_{OFF}) is changed proportionally to the instantaneous line voltage in order to make the switching frequency (f_{SW}) constant. The switching frequency is determined by a capacitor connected between the TIMER pin and ground, charged by an accurate internal generator (I_{TIMER}) of 156 µA (typ.), during the OFF-time, generating a voltage ramp.

When the voltage ramp equals the voltage on the MULT pin, connected through a resistive divider to the rectified mains to get a sinusoidal voltage reference, the OFF-time of the power MOSFET is terminated, the gate driver (GD) pin is driven high and the ramp resets at zero. The timing capacitor C_T is then selected with the following formula:

Equation 47

$$C_T = \frac{I_{TIMER}}{k_p \cdot V_{out} \cdot f_{SW}}$$

where f_{sw} is the switching frequency and k_p the maximum required divider ratio, calculated considering the maximum value of the multiplier input, that is, the voltage measured on the MULT pin at maximum mains voltage. According to the datasheet of the L4984D, the linear operating range is between 0 to 3 V, so the maximum value of the multiplier input ($V_{MULTmax}$) is equal to 3 V.

The maximum required divider ratio k_p can be now found as:

Equation 48

$$k_p = \frac{V_{MULT\ max}}{\sqrt{2} \cdot VAC_{max}} = \frac{3.00V}{\sqrt{2} \cdot 265Vac} = 8 \cdot 10^{-3}$$

The switching frequency chosen for this design is around 70 kHz, so the capacitor on the TIMER pin needed to obtain the desired frequency is (equation 47):

Equation 49

$$C_T = \frac{156\,\mu A}{8 \cdot 10^{-3} \cdot 400\,V \cdot 70\,kHz} = 695\ pF$$

A commercial value of 680 pF has been selected. An NP0 capacitor has to be used.

Now T_{OFF} can be finally calculated. Along a line half-cycle, T_{OFF} varies from nearly zero to the maximum value, occurring at the MULT peak voltage. To calculate the boost inductor the value at the MULT peak should be considered, found simply from the product of the maximum required divider ratio k_p and the peak of the rectified input voltage at low mains voltage (Vpkmin).

The maximum OFF-time at V_{ACmin} is then:

Equation 50

$$T_{OFF}(V_{AC\,\min}) = \frac{680\,pF}{156\,\mu A} \cdot 8 \cdot 10^{-3} \cdot \sqrt{2} \cdot 90V = 4.4\,\mu s$$

The value of the inductance L required for the boost inductor at V_{ACmin} can now be calculated with equation 46.

Equation 51

$$L(VAC_{\min}) = \frac{V_{out} - \sqrt{2} \cdot V_{AC\,\min}}{\Delta IL_{pk}(V_{AC\,\min})} \cdot T_{OFF}(V_{AC\,\min})$$

$$L(VAC_{\min}) = \frac{400V - \sqrt{2} \cdot 90V}{1.85\,A} \cdot 4.4\,\mu s = 654\,\mu H$$

The value chosen for the inductor is 700 µH.

2.3.5 Power MOSFET selection and power dissipation calculation

The selection of the MOSFET concerns mainly $R_{DS(on)}$, that should be low in order to minimize conduction losses, without increasing the switching losses due to the MOSFET 's equivalent output capacitance C_{oss}. To achieve high efficiency both $R_{DS(on)}$ and C_{oss} have to be taken into account, and the trade-off between cost vs. performance must also be considered.

The MOSFET breakdown voltage is needed, considering the PFC nominal output voltage and adding some margin (20%) to guarantee reliable operation. Therefore, a minimum voltage rating of 500 V ($1.2 \cdot V_{out}$ = 480 V) is selected.

In this 350 W CCM PFC application, two STF21N65M5 (placed in parallel) have been chosen, to improve robustness against surges and burst tests, and 650 V MOSFETs have been chosen, having a good balance between R_{DSon} and C_{oss}. In order to calculate the contribution of the MOSFETs to the total efficiency of the system, the power losses have been calculated, which are mainly the sum of the conduction, switching and capacitive losses.

The conduction losses at maximum load and minimum input voltage are calculated by:

Equation 52

$$P_{cond}(VAC) = RDS_{on} \cdot (ISW_{rms}(VAC))^2$$

Because normally in a MOSFET datasheet $R_{DS(on)}$ is given at ambient temperature (25 °C), in order to properly calculate the conduction losses at 100 °C (typical MOSFET junction operating temperature), a factor K_{TEMP} between 1.5 to 2, which can be found in the device datasheet, should be taken into account. In the case of the STF21N65M5, looking at the normalized ON resistance vs. temperature graph, a factor of 1.7 should be considered at 100 °C.

Equation 53

$$R_{DSon\_@100°C} = \frac{RDS_{on\_@25°C}}{Num\_of\_paralleled\_MOSFETs} \cdot K_{TEMP} = \frac{0.179\,\Omega}{2} \cdot 1.7 = 0.152\,\Omega$$

where the RDS_{on} value is divided by two since two MOSFETs are placed in parallel. The maximum RMS switching current, at minimum V_{AC}, has been found from equation 33. Now, from equation 52 and equation 53, and considering that two MOSFETs in parallel have been used, the maximum conduction losses at low line and full load can be calculated as:

Equation 54

$$P_{cond}(VAC) = R_{DSon\_@100°C} \cdot (ISW_{rms}(VAC))^2$$

$$P_{cond}(90V) = 0.152\,\Omega \cdot (3.65\,A)^2 = 2.02\,W$$

The switching losses are difficult to predict as they depend on the particular switching waveform, determined by many factors (driving current, gate resistors, MOSFET gate internal resistance, Vth, gate charge, total capacitance on the drain node including parasitic capacitances etc.). A good approximation to determine the generic switching losses due to the MOSFET commutation occurring at turn-on and turnoff can be basically expressed by:

Equation 55

$$P_{sw}(VAC) = \frac{1}{2} \cdot V_{DS} \cdot I_D \cdot (t_{rise} + t_{fall}) \cdot f_{sw}$$

where V_{DS} is the drain-to-source of the MOSFET, I_D the average drain current and t_{rise} and t_{fall} refer to the rising and the falling edge of V_{DS} . To estimate the rising and falling times of the drain voltage, datasheet values of the switching performance of the MOSFET can be used.

First the average rising times of the drain voltage can be calculated considering the total drain node capacitance and the average value of the peak current flowing through the inductor.

The exact value of the MOSFET's C_{OSS} is indicated in the datasheet looking at the graph representing C_{OSS} vs. V_{DS}. At V_{DS} equal to 400 V, C_{OSS} is 40 pF. This value should be multiplied by two as two MOSFETs have been used in parallel, and adding a rough 100pF of all other contributions, C_D can be found:

Equation 56

$$C_D = 2 \cdot C_{OSS} + C_{stray} = 2 \cdot 40\,pF + 100\,pF = 180\,pF$$

Then the average rising time of the drain voltage is:

Equation 57

$$t_{rise} = \frac{C_D \cdot V_{DS}}{I_D} = \frac{C_D \cdot V_{DS}}{\frac{1}{\pi} \cdot \int_0^{\pi} IL_{pk\,max}} \approx 17\,ns$$

However, the average falling time depends on the driving current I_G (limited by the resistor placed on the gate), the MOSFET's total gate charge Q_G and the driving voltage V_{dr}, supposed here equal to V_{CC} (for example, 15 V) applied for simplicity. In the resistor calculation the intrinsic gate resistance should also be considered. In the case of the STF21N65M5, R_G is 2.5 Ω which has to be added to the externally placed resistor R_{Gext} (3.3 Ω in this design).

Equation 58

$$t_{Cfall} = \frac{Q_G}{I_G} = \frac{Q_G}{\frac{V_{dr}}{R_{Gext} + R_G}} = \frac{50\,nC}{\frac{15V}{3.3\Omega + 2.5\Omega}} \approx 19ns$$

Finally, the MOSFET's switching losses can be estimated with equation 55:

Equation 59

$$P_{SW}(90V) = \frac{1}{2} \cdot 400V \cdot 4.36\,A \cdot (17\,ns + 19ns) \cdot 70\,kHz = 2.2W$$

To estimate the capacitive losses, that is, the losses due to the discharge of the total drain capacitance through the MOSFET at turn-on, this simple expression can be considered:

Equation 60

$$P_{cap}(VAC) = \frac{1}{2} \cdot C_D \cdot V_{DS}^{\,2} \cdot f_{sw}(VAC)$$

$$P_{cap}(90V) = \frac{1}{2} \cdot 180\,pF \cdot (400V)^2 \cdot 70\,kHz = 1W$$

The MOSFET total losses at minimum input voltage (V_{ACmin}) is the sum of the three previous losses from equation 54, equation 55, and equation 60:

Equation 61

$$P_{loss}(VAC) = P_{cond}(VAC) + P_{sw}(VAC) + P_{cap}(VAC)$$
$$P_{loss}(90V) = 2.02W + 2.2W + 1W = 5.23W$$

From equation 61, using the data relevant to the MOSFET selected, it can be observed that the maximum total losses, occurring at V_{ACmin} and full load, is around 5 W. From this number and the given maximum ambient temperature, the total maximum thermal resistance required to keep the MOSFET's junction temperature below 125 °C is:

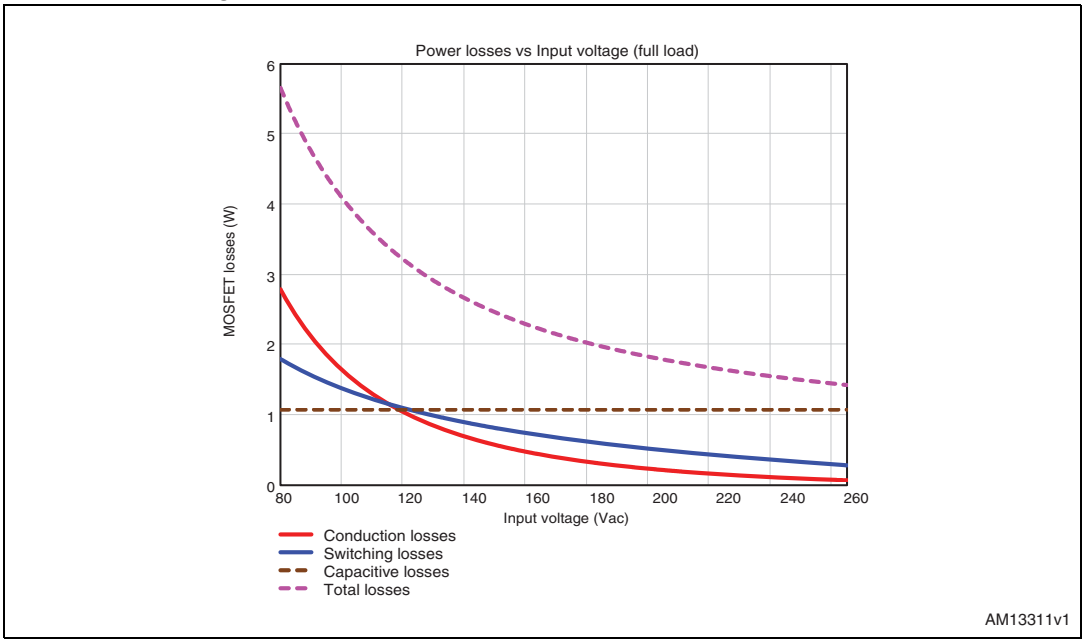
Equation 62

$$R_{th} = \frac{125°C - T_{ambx}}{P_{loss}(VAC)} \qquad R_{th} = \frac{125°C - 50°C}{5.23W} = 14.3\frac{°C}{W}$$

As the result of equation 62 is much lower than the junction-ambient thermal resistance given in the MOSFET datasheet for the selected device package (62.5 °C/W), a heatsink must be used.

Figure 12 shows the trend of the total losses on the line voltage for the two selected STF21N65M5 MOSFETs.

Figure 12. Total MOSFETs losses in the 350 W FOT PFC



2.3.6 Boost diode selection

Following criteria similar to those used for the calculation of the MOSFET losses, the output rectifier can be properly selected. A minimum breakdown voltage of $1.2 \cdot (V_{out})$ and a minimum current rating higher than $5 \cdot I_{out}$ (equation 26) can be considered for an initial rough selection of the rectifier. The correct selection is then confirmed by the thermal calculation, as the diode junction temperature must be below 125 °C.

Since this circuit operates in the continuous current mode, reverse recovery is experienced by the diode, and the MOSFET at turn-on has to carry also the boost diode minority carrier charge. Then, to minimize the recovery losses, an ultra-fast diode with low t_{rr} (reverse recovery time, the time required to deplete the stored charge) and Q_{rr} (reverse recovery charges, the charge that must be dissipated on the MOSFET) or a SiC rectifier has to be selected.

In this 350 W application the STTH8S06 (600 V, 8 A) has been selected and shows very fast reverse recovery time, 12 ns typical (measured for IF =1 A). The rectifier AVG (equation 26) and RMS (equation 33) current values, the V_{th} (rectifier threshold voltage) and R_d (dynamic resistance) given in the datasheet allow calculating the rectifier losses.

From the STTH8S06 datasheet, V_{th} is 1.2 V, and R_d is 0.087 Ω, the conduction losses are equal to:

Equation 63

$$P_{diode} = V_{th} \cdot I_{out} + R_d \cdot ID^2{}_{rms} \qquad P_{diode} = 1.2V \cdot 0.87\,A + 0.087\,\Omega \cdot (2.22\,A)^2 = 1.48W$$

Since the converter is working in continuous conduction mode the losses in the MOSFETs due to the recovery of the boost diode have to be taken into account. The energy loss due to the reverse recovery effect of the diode is:

Equation 64

$$E_{rr} = V_R \cdot Q_{rr}$$

Where V_R is the reverse voltage across the output diode, when it stops conducting, that is 400 V, and Q_{rr} the reverse recovery charges, the charge that must be dissipated through the MOSFET. On the datasheet the graph of Q_{rr} vs. dI_F/dt is represented. Following the $0.5 \times I_{F(AV)}$ curve at T_j = 125 °C a value of 80 nC is found assuming the typical case of 200 A/us.

Then the recovery energy is:

Equation 65

$$E_{rr} = 400V \cdot 80\,nC = 32\,\mu J$$

And the reverse recovery losses are:

Equation 66

$$P_{rr} = E_{rr} \cdot f_{sw} = 32\,\mu J \cdot 70\,kHz = 2.24W$$

If a single heatsink for the MOSFETs and diode is used, the maximum total losses of the switches should be considered:

Equation 67

$$P_{switch} = P_{loss}(90V) + P_{diode}(90V) + P_{rr} = 5.84W + 1.48W + 2.24W = 9.56W$$

From this number and the given maximum ambient temperature, the total maximum thermal resistance required can be found as:

Equation 68

$$R_{th} = \frac{125°C - T_{ambx}}{P_{switch}} \qquad R_{th} = \frac{125°C - 50°C}{9.56W} = 7.85\frac{°C}{W}$$

In this design in order to keep the junction MOSFET temperature below 100 °C (around 90 °C measured on the package) and to ensure a higher degree of reliability, the thermal resistance has been chosen equal to:

Equation 69

$$R_{th} = \frac{100°C - 50°C}{9.57W} = 5.23\frac{°C}{W}$$

3 L4984D biasing circuitry

The following sections describe the selection of the circuitry around the L4984D.

3.1 Feedback and OVP

Pin 1 (INV): this pin is connected both to the inverting input of the E/A and to the OVP circuitry. A resistive divider has to be connected between the boost regulated output voltage and this pin. The internal reference on the non-inverting input of the E/A is 2.5 V (typ.), the output voltage (V_{out}) of the PFC pre-regulator is set at the nominal value by the resistor ratio of the feedback output divider. R_{outH} and R_{outL} will be then selected considering the desired nominal output voltage and the desired output power dissipated on the output divider.

For example for a 25 mW output divider dissipation:

Equation 70

$$R_{outH} = \frac{(V_{out} - 2.5V)^2}{25mW} \qquad R_{outH} = \frac{(400V - 2.5V)^2}{25mW} = 6.320M\Omega$$

Please note that for R_{outH} a resistor with a suitable voltage rating (> 400 V) is needed, or more resistors in series have to be used. Here three 2.2 MΩ resistors in series have been selected.

Equation 71

$$\frac{R_{outH}}{R_{outL}} = \frac{V_{out}}{2.5V} - 1 \qquad \frac{R_{outH}}{R_{outL}} = \frac{400V}{2.5V} - 1 = 159$$

Equation 72

$$R_{outL} = \frac{V_{out}}{159} \qquad R_{outL} = \frac{6.6M\Omega}{159} = 39.7k\Omega$$

For R_{outL} a value of 160 kΩ in parallel to a 56 kΩ has been selected.

Pin 2 (COMP): this pin is the output of the E/A that is fed to one of the inputs of the multiplier. A feedback compensation network is placed between this pin and INV. It has to be designed in with a narrow bandwidth in order to avoid that the system rejects the output voltage ripple (100 Hz) that would bring high distortion of the input current waveform. A theoretical criterion to define the compensation network value is to set the E/A bandwidth (BW) below 20 Hz. The compensated two-pole feedback network selection for this 350 W FOT PFC has been described in detail in *Section 4: FOT PFC boost control loop*.

Pin 6 (PFC_OK - Feedback failure protection): PFC_OK pin has been dedicated to monitor the output voltage of a separate resistor divider. This divider is selected so that the voltage at the pin reaches 2.5 V if the output voltage exceeds a preset value (Vovp), usually larger than the maximum V_{out} that can be expected, also including worst-case load/line transients. For a maximum output voltage V_{outmax} of 430 V and selecting a 50 µA current flowing in to the divider:

Equation 73

$$R_L = \frac{V_{REF\_PFC\_OK}}{I_{divider}} \qquad R_L = \frac{2.5V}{50\mu A} = 50k\Omega$$

By selecting a commercial value of 56 kΩ:

Equation 74

$$R_H = R_L \cdot \left(\frac{V_{OUT\_MAX}}{V_{REF\_PFC\_OK}} - 1 \right) \qquad R_H = 56k\Omega \cdot \left(\frac{430V}{2.5V} - 1 \right) = 9.623M\Omega$$

Three resistors 3.3 MΩ in series provide the calculated value for the PFC_OK high resistor. Notice that both feedback dividers connected to the L4984D pin #1 (INV) and pin #6 (PFC_OK) can be selected without any constraints. The unique criterion is that both dividers have to sink a current from an output bus which needs to be significantly higher than the current biasing the error amplifier and the PFC_OK comparator. The OVP function handles "normal" overvoltage conditions, i.e. those resulting from an abrupt load/line change or occurring at startup. In case the overvoltage is generated by a feedback failure, for instance when the upper resistor of the output divider (R1) fails open, eventually the error amplifier output (COMP) will saturate high and the voltage on its inverting input (INV) will drop from its steady-sate value (2.5 V).

An additional comparator monitors the voltage on pin INV, comparing it against a reference located at 1.66 V. When the voltage on pin PFC_OK exceeds 2.5 V and, simultaneously, the voltage on pin INV falls below 1.66 V, the FFD function is triggered: the gate drive activity is immediately stopped, the device is shut down and its quiescent consumption reduced. This condition is latched and in order to restart the L4984D it is necessary to recycle the input power, so that the V_{cc} voltage falls below 6 V ($VCC_{restart}$).

The pin PFC_OK doubles its function as a non-latched IC disable: a voltage below 0.23 V shuts down the L4984D, reducing its consumption below 2.2 mA. To restart simply let the voltage on the pin rise above 0.27 V. Note that these functions offer complete protection against not only feedback loop failures or erroneous settings, but also against a failure of the protection itself. Either resistor of the PFC_OK divider failing short or open or a pin PFC_OK floating will result in shutting down the L4984D and stopping the pre-regulator.

3.2 Current sense resistor

Pin 4 (CS): The pin #4 is the inverting input of the current sense comparator. Through this pin, the L4984D senses the instantaneous inductor current, converted in a proportional voltage by an external sensing resistor (R_S). As this signal crosses the threshold set by the multiplier output, the PWM latch is reset and the power MOSFET is turned off. The threshold is defined by:

Equation 75

$$V_{CS} = V_{CS\_OFFSET} + k_m \cdot \frac{(V_{COMP} - 2.5V) \cdot V_{MULT}}{V_{FF}^2}$$

where:

- V_{CS} (multiplier output) is the reference for the current sense (V_{CS_OFFSET} is its offset).
- k_m=0.23 (typ.) is the multiplier gain.
- V_{COMP} is the voltage on pin 2 (E/A output).
- V_{MULT} is the voltage on pin 3.
- V_{FF} is the second input to the multiplier for $1/V^2$ function. It compensates the control loop gain dependence on the mains voltage. The voltage at this pin is a DC level equal to the peak voltage on pin MULT (pin 3).

The sense resistor value (R_S) can be calculated as follows. For the 350 W PFC it will be:

Equation 76

$$R_s < \frac{0.84V}{7.0A} = 0.12\Omega$$

Where:

- I_{Lpk} is the maximum peak current in the inductor, calculated with
- $V_{csm\ in}$ = 0.84 V is the minimum value of the L4984D current sense reference clamp ($V_{CSclamp}$ in the datasheet).

According to the result, three parallel resistors of 0.33 Ω with 1 W of power rating have been selected.

Because the internal current sense clamping sets the maximum current that can flow in the inductor, the maximum peak of the inductor current will be calculated considering the maximum $V_{csclamp}$ admitted on the L4984D:

Equation 77

$$IL_{pkx} = \frac{0.93V}{0.11\Omega} = 8.45A$$

The calculated IL_{pkx} will be the value at which the boost inductor shall not saturate and it will be used for calculating the inductor number of turns and air gap length. The power dissipated by R_S is given by:

Equation 78

$$P_s = R_s \cdot ISW_{rms}^2 \qquad P_s = 0.11\Omega \cdot (3.73)^2 = 1.53W$$

3.3 Mult divider and VFF

Pin 3 (MULT): the MULT pin is the second multiplier input. It will be connected, through a resistive divider, to the rectified mains to get a sinusoidal voltage reference.

Figure 13. Multiplier characteristics family for V_{FF} = 1 V

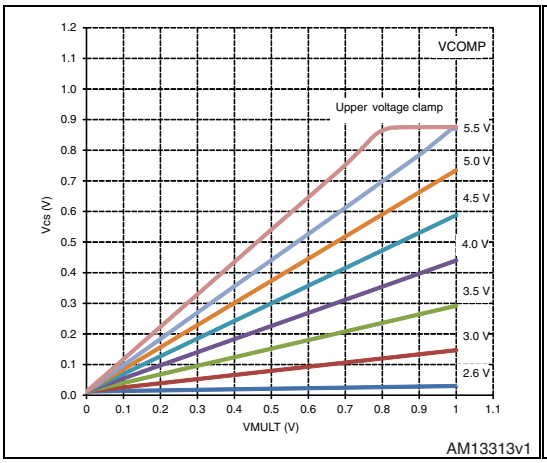
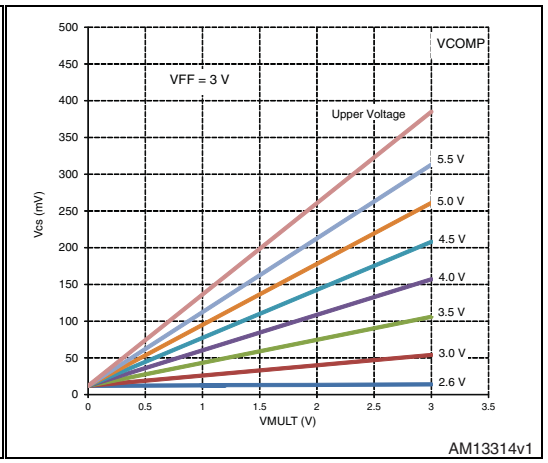


Figure 14. Multiplier characteristics family for V_{FF} = 3 V



A complete illustration is given by the diagrams of *Figure 13* and *Figure 14* which show the typical multiplier characteristics family. The linear operation of the multiplier is guaranteed within the range 0 to 3 V of V_{MULT} and the range 0 to 0.82 V (typ.) of V_{CS}, while the minimum guaranteed value of the maximum slope of the characteristics family (typ.) is:

Equation 79

$$\frac{dV_{CS}}{dV_{MULT}} = 1.4\frac{V}{V}$$

The voltage on the MULT pin is used also to derive the information on the RMS mains voltage for the V_{FF} compensation and the brownout function:

Pin 5 (VFF): the power stage gain of PFC pre-regulators varies with the square of the RMS input voltage. This applies as well to the crossover frequency fc of the overall open-loop gain because the gain has a single pole characteristic. This leads to large trade-offs in the design. For example, setting the gain of the error amplifier to get fc = 20 Hz at 264 Vac means having fc about 4 Hz at 88 Vac, resulting in sluggish control dynamics. Additionally, the slow control loop causes large transient current flow during rapid line or load changes that are limited by the dynamics of the multiplier output. This limit is considered when selecting the sense resistor to let the full load power pass under minimum line voltage conditions, with some margin. But a fixed current limit allows excessive power input at high line, whereas a fixed power limit requires the current limit to vary inversely with the line voltage.

Voltage feed-forward can compensate for the gain variation with the line voltage and allow overcoming all of the above-mentioned issues. It consists of deriving a voltage proportional to the input RMS voltage, feeding this voltage into a squarer/divider circuit ($1/V^2$ corrector) and providing the resulting signal to the multiplier that generates the current reference for the inner current control loop.

In this way a change of the line voltage will cause an inversely proportional change of the half sine amplitude at the output of the multiplier (if the line voltage doubles, the amplitude of the multiplier output will be halved and vice versa) so that the current reference is adapted to the new operating conditions with (ideally) no need for invoking the slow dynamics of the error amplifier. Additionally, the loop gain will be constant throughout the input voltage range, which improves significantly dynamic behavior at low line and simplifies loop design.

Actually, with other PFC embedding the voltage feed-forward, deriving a voltage proportional to the RMS line voltage implies a form of integration, which has its own time constant. If it is too small, the voltage generated will be affected by a considerable amount of ripple at twice the mains frequency that will cause distortion of the current reference (resulting in high THD and poor PF). If it is too large, there will be a considerable delay in setting the right amount of feed-forward, resulting in excessive overshoot and undershoot of the pre-regulator's output voltage in response to large line voltage changes. Clearly a trade-off was required.

The L4984D implements an innovative voltage feed-forward which, with a technique that makes use of just two external parts, overcomes this time constant trade-off issue whichever voltage change occurs on the mains, both surges and drops. A capacitor C_{FF} and a resistor R_{FF}, both connected from the pin VFF (pin #5) to ground, complete an internal peak-holding circuit that provides a DC voltage equal to the peak of the rectified sine wave applied on pin MULT (pin #3). In this case following values have been selected:

Equation 80

$$C_{FF} = 1\mu F \qquad R_{FF} = 1M\Omega$$

In this way, in case of sudden line voltage rise, C_{FF} will be rapidly charged through the low impedance of the internal diode. In case of line voltage drop, an internal "mains drop" detector enables a low impedance switch which suddenly discharges C_{FF} avoiding a long settling time before reaching the new voltage level. Consequently, an acceptably low steady-state ripple and low current distortion can be achieved without any considerable undershoot or overshoot on the preregulator's output like in systems with no feed-forward compensation. This pin is internally connected to a comparator in order to provide the brownout (AC mains undervoltage) protection. A voltage below 0.8 V shuts down (does not latch~~ed~~) the L4984D and brings its consumption to a considerably lower level. The L4984D restarts as the voltage at the pin rises above 0.88 V. These data have to be considered during the MULT divider selection, setting the minimum operating voltage.

Please find here following the procedure to set properly the operating point of the multiplier and the divider resistor values. Supposing a 60 uA (I_{MULT}) current flowing into the multiplier divider, the lower resistor value can be calculated:

Equation 81

$$R_{multL} = \frac{V_{MULT\,max}}{I_{MULT}} = \frac{3.00V}{60\mu A} = 50k\Omega$$

A commercial value of 51 kΩ for the lower resistor is selected. The upper resistor value can now be calculated:

Equation 82

$$R_{multH} = \frac{1-k_p}{k_p} \cdot R_{multL} = \frac{1-8\cdot 10^{-3}}{8\cdot 10^{-3}} \cdot 56k\Omega = 6.944M\Omega$$

In this application example a R_{multH} = 6.9 MΩ and a R_{multL} = 51 kΩ have been selected. Please note that for R_{multH} a resistor with a suitable voltage rating (> 400 V) is needed, or more resistors in series will have to be used.

The voltage on the multiplier pin with the selected component values re-calculated at minimum line voltage is 0.93 V and at maximum line voltage is 2.74 V, so the multiplier will work correctly within its linear region. Finally, depending on the MULT resistors the brownout functions also have to be checked, calculating the V_{START} and V_{STOP} voltages:

Equation 83

$$V_{START} = \frac{0.88V}{\sqrt{2}} \cdot \frac{R_{multH} + R_{multL}}{R_{multL}} \qquad V_{START} = \frac{0.88V}{\sqrt{2}} \cdot \frac{6.9M\Omega + 56k\Omega}{56k\Omega} = 77.29V$$

Equation 84

$$V_{STOP} = \frac{0.80V}{\sqrt{2}} \cdot \frac{R_{multH} + R_{multL}}{R_{multL}} \qquad V_{STOP} = \frac{0.80V}{\sqrt{2}} \cdot \frac{6.9M\Omega + 51k\Omega}{51k\Omega} = 70.2V$$

Start and stop PFC voltages are suitable for correct operation by the PFC; the MULT divider has to be set considering these two voltages, in order to disable the PFC with an anomalous input low mains voltage that could cause an overheating of the PFC due to the higher input mains current. In order to set the required voltage startup threshold reiterations could be required by selecting MULT resistors and checking the actual PFC start voltage.

3.4 Gate driver (GD) and VCC pins

Pin 8 (GND): this pin acts as the current return both for the signal internal circuitry and for the gate drive current. When laying out the printed circuit board, these two paths should run separately.

Pin 9 (GD): is the output of the driver. The pin is able to drive an external MOSFET with 600 mA source and 800 mA sink capability.

The high-level voltage of this pin is clamped at about 12 V to avoid excessive gate voltages in case the pin is supplied with a high V_{cc}. To avoid undesired switch-on of the external MOSFET because of some leakage current when the supply of the L4984D is below the UVLO threshold, an internal pull-down circuit holds the pin low. The circuit guarantees 1.1 V maximum on the pin (at I_{sink}=2mA), with $V_{cc} > V_{CC\_ON}$. This allows omitting the "bleeder" resistor connected between the gate and the source of the external MOSFET used for this purpose.

Pin 10 (V_{CC}): is the supply of the device. This pin will be externally connected to the startup circuit (usually, one resistor connected to the rectified mains) and to the self-supply circuit. Whatever the configuration of the self-supply system, a capacitor will be connected between this pin and ground. To start the L4984D, the voltage must exceed the startup threshold (12 V typ.). Below this value the device does not work and consumes around 65 µA (typ.) from V_{CC}. This allows the use of high value startup resistors (in the hundreds of kΩ), which reduces power consumption and optimizes system efficiency at low load, especially in wide-range mains applications. When operating, the current consumption (of the device only, not considering the gate drive current) rises to a value depending on the operating conditions but never exceeding 6 mA. The device keeps on working as long as the supply voltage is over the UVLO threshold (13 V max). If the V_{CC} voltage exceeds 22.5 V, an internal Zener

diode, 20 mA rated, will be activated in order to clamp the voltage. Please remember that during normal operation the internal Zener will not have to clamp the voltage, because in that case the power consumption of the device will increase considerably and its junction temperature will also increase. The recommended operating condition for safe operation of the device is below the minimum clamping voltage of the pin.

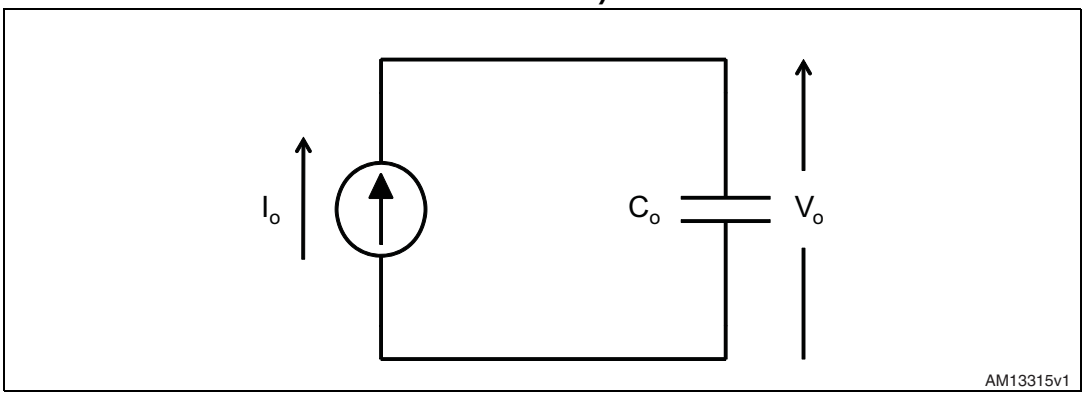
4 FOT PFC boost control loop

In order to find a compensation network ensuring stability over a large variety of operating conditions and to prevent dangerous oscillations of the output voltage as a result of load changes, it is necessary to have a correct understanding of the control loop of FOT PFC systems.

The loop gain of PFC pre-regulators must have a very low crossover frequency (f_c) so as to keep V_{COMP} (error amplifier output) fairly constant over a given line cycle, filtering twice the line frequency ripple on the output of the error amplifier, in order to ensure low THD (total harmonic distortion). As a rule of thumb, f_c should not exceed 20 Hz.

The small signal model of a PFC stage with a constant power load (the regulated DC-DC converter) can be represented as a controlled current source delivering power to the output capacitor.

Figure 15. Small signal model of a PFC stage with a constant-power load (DC-DC converter)



The current generator:

$$\hat{i}_o$$

is controlled by the small-signal AC control voltage:

$$\hat{v}_c$$

and the system acts as a pure integrator and the resulting control-to-output transfer function is:

Equation 85

$$\frac{\hat{v}_o}{\hat{v}_c} = G(j\omega) = \frac{G_o}{j\omega}$$

where the unity gain factor G_o is given by the following expression regardless of the control method and the characteristics of the control IC:

Equation 86

$$G_o = \frac{P_{out}}{V_{out} \cdot (V_C - V_{C0}) \cdot C_o}$$

In the previous expression V_c is the error signal of the voltage control loop (voltage on the COMP pin for the L4984D), that is, the output of the error amplifier, and V_{CO} the "zero-power" level of the control voltage, that is, the burst mode threshold of COMP voltage (2.4 V, typ.).

The effective control voltage V_{comp} - V_{C0}, can be expressed for the L4984D starting from the expression of the variation of signal out from the modulator with respect to the E/A output (COMP) change, using the formula indicated in the datasheet of the L4984D (equation 87).

Equation 87

$$V_{CS} = V_{CS\_OFFSET} + k_m \cdot \frac{(V_{COMP} - 2.4V) \cdot V_{MULT}}{V_{FF}^2}$$

Where k_m is the small signal multiplier gain assumed here equal to the large single gain k_m (typ. 0.304). From this expression, replacing:

Equation 88

$$V_{CS} = R_S \cdot I_{Lpk} \qquad V_{FF} = \sqrt{2} \cdot V_{AC} \cdot K_p$$

and rewriting equation 31 which describes the maximum inductor peak current as:

Equation 89

$$IL_{pk} = \frac{\sqrt{2} \cdot I_{out} \cdot V_{out}}{\eta \cdot V_{AC} \cdot PF} \cdot \left(1 + \frac{K_r}{2}\right)$$

the effective control voltage V_{comp}-V_{CO} can be found:

Equation 90

$$V_{COMP} - V_{C0} = \frac{2 \cdot R_S \cdot K_p \cdot P_{in}}{K_m} \cdot \left(1 + \frac{K_r}{2}\right)$$

Then this expression can be used to find the unity gain factor (equation 86):

Equation 91

$$G_o = \frac{k_m}{2 \cdot \eta \cdot V_{out} \cdot R_S \cdot k_p \cdot \left(1 + \frac{K_r}{2}\right) \cdot C_o}$$

$$G_o = \frac{0.23}{2 \cdot 0.92 \cdot 400V \cdot 0.11\Omega \cdot k_p \cdot \left(1 + \frac{0.27}{2}\right) \cdot 200 \cdot \mu F} = 955.7$$

Looking at *Figure 16*, related to the gain and the phase of the control-to-output transfer function, it is possible to notice that it has just one pole at the origin. The gain falls with a slope -20 dB/dec and the phase shift is -90 ° at all frequencies.

It can also be noted that the crossover frequency is much higher than the one required for a PFC (lower than 20 Hz). To make the gain roll off at low frequency (so as to cross the 0 dB axis at low frequency) and to boost the phase in the neighborhood of the crossover frequency (so as to increase phase margin), type II compensation is usually used, which adds a pole-zero couple.

Figure 16. Bode plots of the control-to-output transfer function

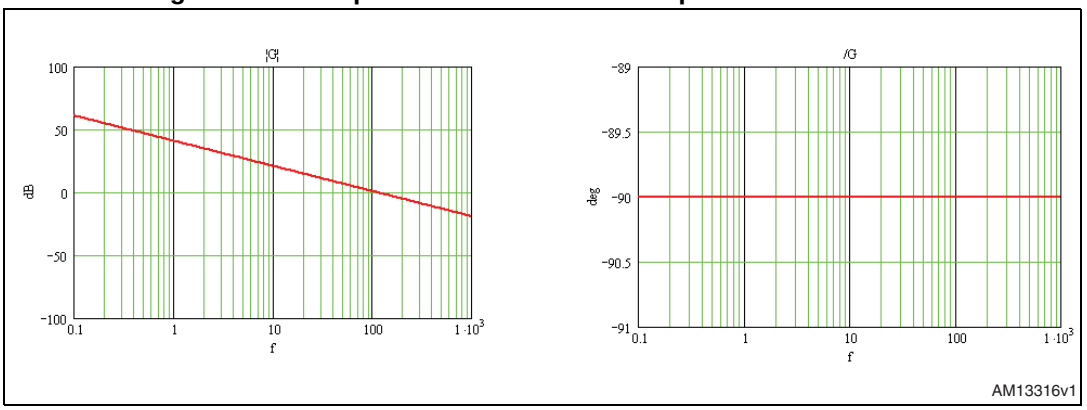
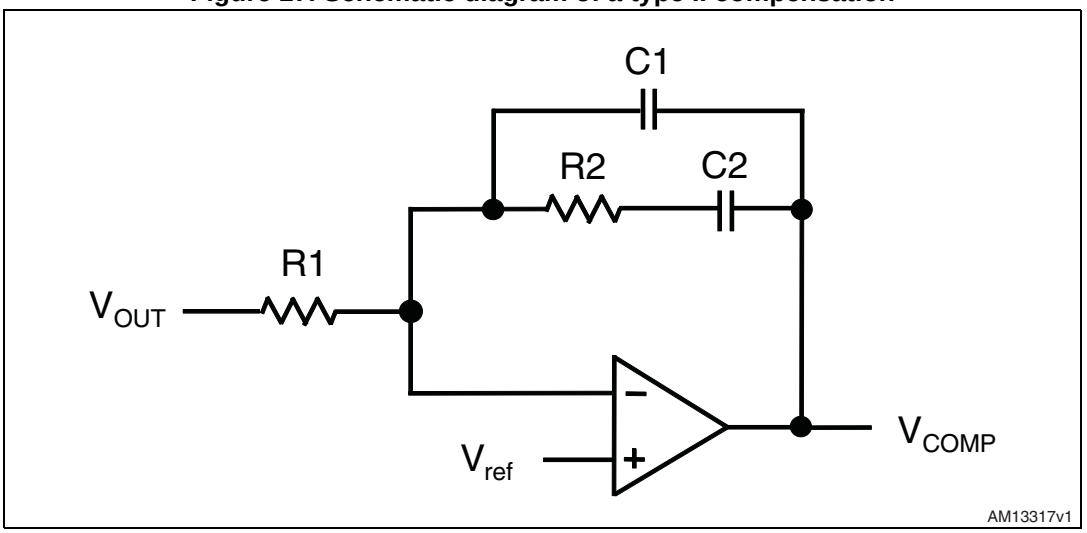


Figure 17. Schematic diagram of a type II compensation



The transfer function of the compensated error amplifier is:

Equation 92

$$G_{EA}(s) = \frac{1}{R_{INV\_H} \cdot C_1} \cdot \frac{1 + \frac{1}{s \cdot R_2 \cdot C_2}}{s \cdot \left(1 + \frac{C_1 + C_2}{s \cdot R_2 \cdot C_1 \cdot C_2}\right)}$$

In order to calculate the values of the components of the compensation network, the Venable K-Factor calculation is used, starting from the amount of phase margin needed at the crossover frequency and the desired maximum 3rd harmonic distortion level D_3.

Phase margin is defined as the difference between 180 ° and the actual phase lag at the frequency where the open-loop gain is unity. The higher the phase margin, the more over-damped the system is. As rule of thumb, to ensure fast transient response with a good level of ringing, a phase margin of 60 ° has to be chosen.

$$D_3 = 2\% \qquad \Phi_m = 60°$$

The Venable K-factor is defined as:

Equation 93

$$K = \frac{1 + \sin\left(\frac{\pi}{180} \cdot \phi_m\right)}{\cos\left(\frac{\pi}{180} \cdot \phi_m\right)} = 3.732$$

The required E/A gain (at $2f_L$) in order to keep the distortion below the desired maximum 3rd harmonic distortion (D_3) is:

Equation 94

$$H_{2f} = \frac{2 \cdot D_3 \cdot (V_{COMP} - V_{C0})}{\Delta V_{out}/2} = \frac{2 \cdot D_3 \cdot \frac{2 \cdot R_S \cdot k_p \cdot P_{in}}{k_m} \cdot \left(1 + \frac{K_r}{2}\right)}{\Delta V_{out}/2}$$

$$H_{2f} = \frac{2 \cdot 0.02 \cdot \frac{2 \cdot 0.011\Omega \cdot 8 \cdot 10^{-3} \cdot 380.4W}{0.23} \cdot \left(1 + \frac{0.27}{2}\right)}{14.81V/2} = 0.018$$

while the unity frequency gain is:

Equation 95

$$H_0 = \frac{4\pi \cdot f_{LINE\_min} \cdot H_{2f}}{K^2} \qquad H_0 = \frac{4\pi \cdot 47Hz \cdot 0.018}{3.732^2} = 0.763$$

The frequency of the zero and the pole of the compensation network can be found with the following two expressions, where G_0 is the unity gain factor (equation 91).

Equation 96

$$z = \frac{1}{2\pi} \cdot \sqrt{\frac{G_o \cdot H_o}{K}} \qquad z = \frac{1}{2\pi} \cdot \sqrt{\frac{955.7 \cdot 0.763}{3.732}} = 2.2Hz$$

Equation 97

$$p = \frac{K}{2\pi} \cdot \sqrt{G_o \cdot H_o \cdot K} \qquad p = \frac{3.732}{2\pi} \cdot \sqrt{955.7 \cdot 0.763 \cdot 3.732} = 30.9Hz$$

Then the values of the components can be calculated as follows.

Feedback parallel capacitor:

Equation 98

$$C1 = \frac{1}{H_o \cdot R_{outH}} \cdot \frac{z}{p} \qquad C1 = \frac{1}{0.763 \cdot 6.6M\Omega} \cdot \frac{2.2Hz}{30.9Hz} = 14.1nF$$

A value of 22 nF has been selected for the parallel feedback capacitor.

Feedback series capacitor:

Equation 99

$$C2 = C1 \cdot \left(\frac{p - z}{z} \right) \qquad C2 = 22nF \cdot \left(\frac{30.9Hz - 2.2Hz}{2.2Hz} \right) = 287nF$$

A value of 220 nF has been selected for the series feedback capacitor.

Feedback series resistor:

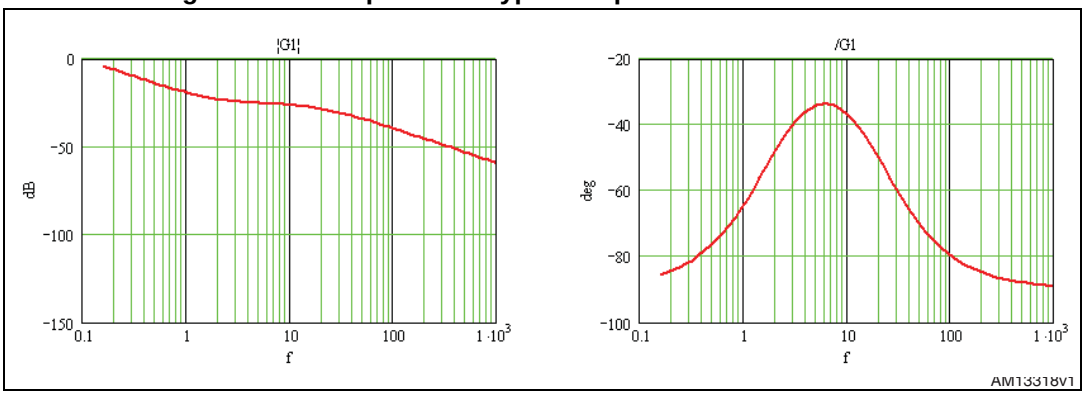
Equation 100

$$R_2 = \frac{1}{2\pi \cdot z \cdot C_2} \qquad R_2 = \frac{1}{2\pi \cdot 2.2Hz \cdot 220nF} = 328.8k\Omega$$

A value of 330 kΩ has been selected for the series feedback resistor.

The gain and the phase of the transfer function of the type II amplifier are represented in the bode plots in *Figure 19*.

Figure 18. Bode plots of a type II amplifier's transfer function



The closed-loop transfer function is the product of the control-to-output transfer function (equation 85) and the E/A transfer function (equation 92):

Equation 101

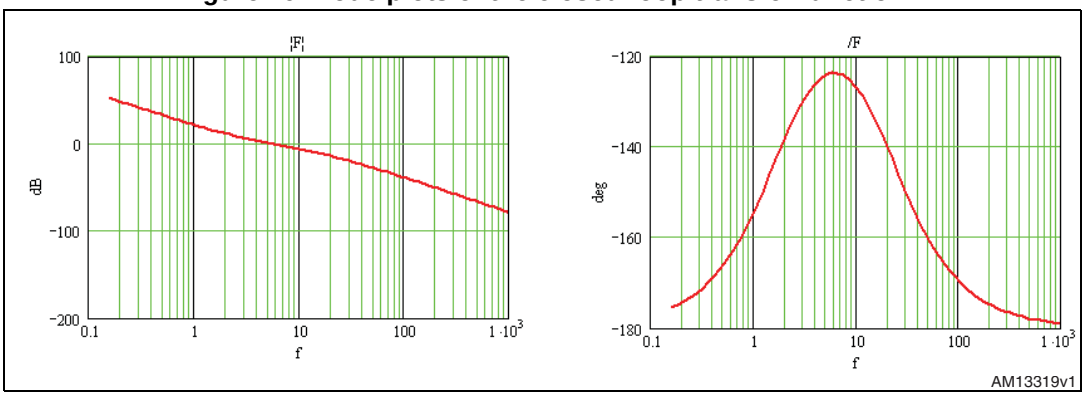
$$D3 = \frac{H_{2fL} \cdot \Delta V_{out}/2}{V_{COMP} - V_{C0}} \cdot \frac{100}{2}$$

$$D3 = \frac{H_{2fL} \cdot \Delta V_{out}/2}{\frac{2 \cdot R_S \cdot k_p \cdot P_{in}}{k_m} \cdot \left(1 + \frac{K_r}{2}\right)} \cdot \frac{100}{2}$$

$$D3 = \frac{0.011 \cdot 14.81/2}{\frac{2 \cdot 0.011\Omega \cdot 8 \cdot 10^{-3} \cdot 380.4W}{0.23} \cdot \left(1 + \frac{0.27}{2}\right)} \cdot \frac{100}{2} = 1.286$$

The gain and the phase of the closed-loop transfer function is represented in the Bode plots in *Figure 20*.

Figure 19. Bode plots of the closed-loop transfer function



Finally all the parameters describing the actual closed-loop transfer function are calculated.

Crossover frequency:

Equation 102

$$f_c = \left| root\left(\left|F\left(2\pi f - 1, f\right)\right|\right) \right|$$

$$f_c = 5.9Hz$$

Phase margin:

Equation 103

$$\Phi = 180° + \Phi F\left(2 \cdot \pi \cdot f_c\right)$$

$$\Phi = 56.4°$$

E/A gain at $2f_L$:

Equation 104

$$H_{2fL} = \left| H\left(4 \cdot \pi \cdot f_{LINE\_min}\right) \right| = 0.011$$

From equation 90 and equation 104 the actual 3rd harmonic distortion can be found:

Equation 105

$$D3 = \frac{H_{2fL} \cdot \Delta V_{out}}{V_{COMP} - V_{ref}} \cdot \frac{100}{2} = 1.253$$

The comparison between *Figure 20* and *Figure 21* shows the practical difference between two different configurations of compensation network. In the first case, where the series resistor R2 is such to move the "phase boost" far from the crossover frequency, the phase margin is very low (around 22 °) then the system is underdamped, experiencing large overshoots and ringings. In the second case where the phase margin is around 56 ° the response of the system to the load variation is fast and without ringing, thus with limited deviations.

Figure 20. 115 V_{ac} step load (50 % to 100 %): improper compensation

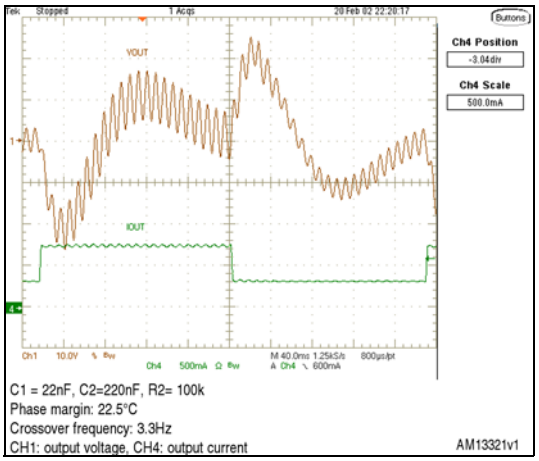
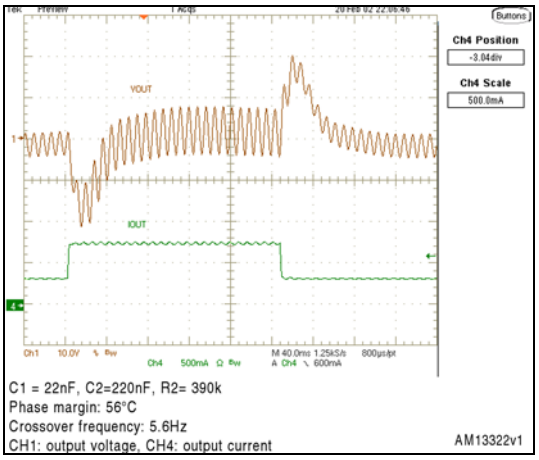


Figure 21. 115 V_{ac} step load (50 % to 100 %): good compensation

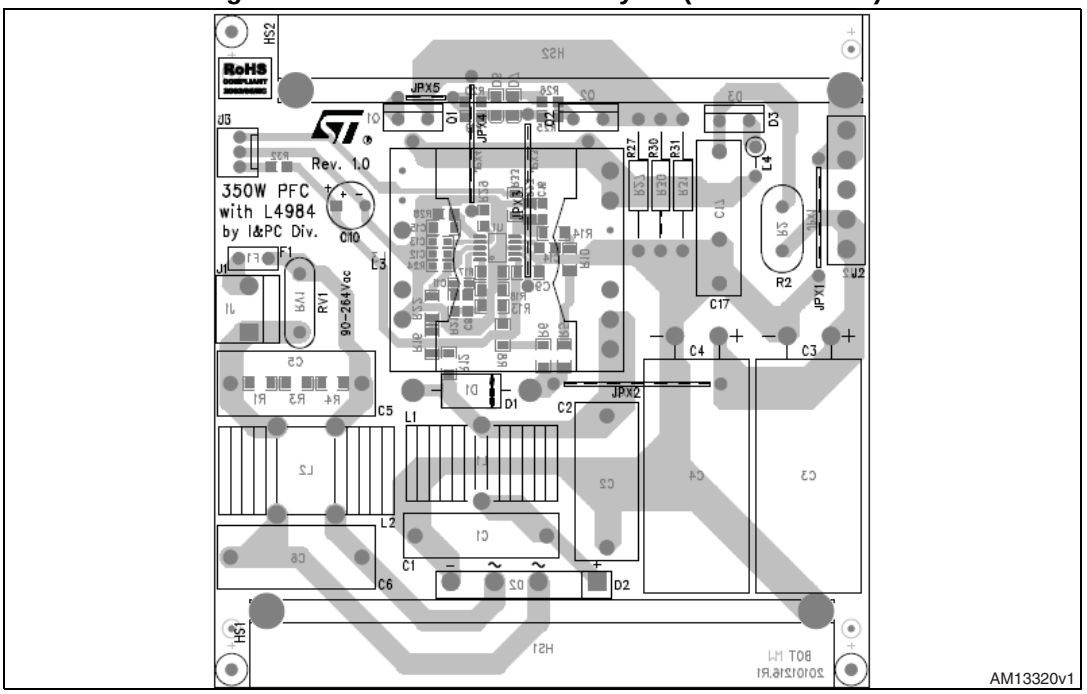


5 Layout hints

The layout of any converter is a very important phase in the design process which is sometimes neglected by the designers. Even if the layout phase sometimes looks to be time-consuming, a good layout undoubtedly saves time during the functional debugging and the qualification phases. Additionally, a power supply circuit with a correct layout needs smaller EMI filters or less filter stages, allowing consistent cost saving.The L4984D does not need any special attention to the layout, just requiring that the general layout rules for any power converter be carefully applied. Basic rules are listed here below, using the EVL4984-350W PCB layout as a reference (*Figure 23*).

- Keep the power and signal RTN separated. Connect the return pins of the components carrying high current such as the input filter, sense resistors or output capacitors as close as possible. This point is the RTN star point. A downstream converter must be connected to this return point.
- Minimize the length of the traces relevant to the boost inductor, MOSFET's drain, boost rectifier and the output capacitor.
- Keep signal components as close as possible to each relevant pin of the L4984D. Specifically, components and traces relevant to the error amplifier have to be placed far from traces and connections carrying signals with high dV/dt, such as the MOSFET's drain.
- Connect heatsinks to power GND.
- Add an external shield to the boost inductor and connect it to power GND.
- Please connect the RTN of the signal components including the feedback, PFC_OK and MULT dividers close to pin 8 (GND) of the L4984D.
- Connect a ceramic capacitor (100÷470 nF) close to pin #10 (V_{CC}) and to pin #8 (GND) of the L4984D. Connect this point to the RTN star point (see rule 1).

Figure 22. EVL4984-350W PCB layout (SMT side view)



6 Design example using the L4984D-CCM PFC excel spreadsheet

An excel spreadsheet has been created for a quick and easy reference in order to design a boost CCM PFC pre-regulator using the L4984D.

Figure 22 shows the first sheet already precompiled with the input design data used in *Section 2.1*.

Figure 23. Excel spreadsheet design specification input table

Design Specs:	Parameter	Value	Unit [ ]
Mains Voltage Range	VacMin	90	VACrms
Mains Voltage Range	VacMax	265	VACrms
Min.Mains Frequency	fl	47	Hz
Regulated Output Voltage	Vout	400	Vdc
Rated Output Power	Pout	350	W
Max. Output Low Frequency Ripple	Δ Vout	10	Vpk-pk
Holdup Capability	Thold	17	ms
Min. Output Voltage after Line drop	VoutMin	300	Vdc
Expected Efficiency	η	90	%
Expected Power Factor	PF	0.99	---
Max inductor current ripple to peak ratio (@VACmin,Pout_max)	Kr	0.3	---
Maximum Ambient Temperature	Tambx	50	°C
Switching frequency	fs	70	kHz

AM13323v1

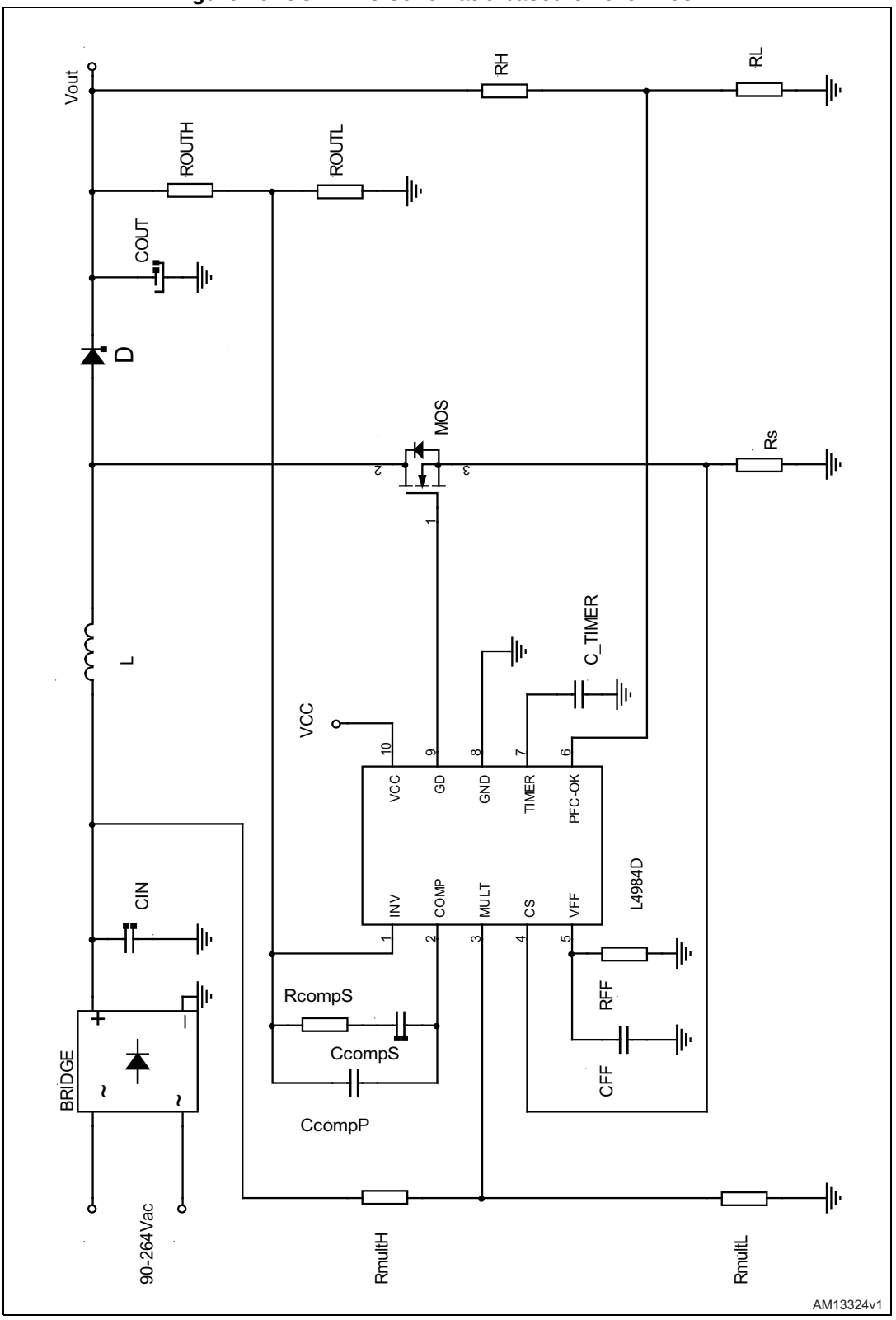
Figure 24. Other design data

Other Design Data:	Parameter	Value	Unit [ ]
Maximum Magnetic Flux Density	Bmax	0.25	T
Ripple Voltage Coefficient	r	0.05	---
Timer pin source current	Itimer	156	uA

AM13325v1

The spreadsheet generates a complete list of parts of the PFC schematic represented in *Figure 25 on page 39* including the power dissipation calculation of the power components, following the calculation procedure described in this document .

Figure 25. CCM PFC schematic based on the L4984D



The bill of material for *Figure 25: CCM PFC schematic based on the L4984D* is automatically compiled by the excel spreadsheet. It summarizes all selected components and some pertinent data.

Figure 26. Excel spreadsheet BOM

350 W FOT PFC BASED ON L4984D
BILL OF MATERIAL

		Selected Value	Unit [ ]
BRIDGE RECTIFIER	*D15XB60*		
MOSFET P/N	*2 x STF21N65M5*		
DIODE P/N	*STTH8S06*		
Inductor	*L*	*700*	*µH*
Max peak Inductor current	*Ilpkx*	*7.91*	*A*
Pin 4 – CS Sense resistor	*Rsx*	*0.11*	*Ω*
Power dissipation	*Ps*	*1.53*	*W*
INPUT Capacitor	*Cin*	*1*	*µF*
OUTPUT Capacitor	*Cout*	*330*	*µF*
Pin 3 - MULT Divider	*Rmult L*	*100*	*kΩ*
	Rmult H	*12500*	*kΩ*
Pin 7 - TIMER capacitor	*CT*	*680*	*pF*
Switching frequency	*fs*	*72.26*	*kHz*
Pin 1 - Feedback Divider	*RoutH*	*6600*	*kΩ*
	RoutL	*41.5*	*kΩ*
Pin 6 - Output divider for PFC_OK	*RL*	*56*	*kΩ*
	RH	*9900*	*kΩ*
Pin 1,2 - Compensation Network	*CcompP*	*22*	*nF*
	CcompS	*220*	*nF*
	RcompS	*390*	*kΩ*
Voltage Feedforward	*CFF*	*1000*	*nF*
	RFF	*1000*	*kΩ*
IC Controller	*L4984D*		

7 References

- L4984D, CCM PFC controller", datasheet.
- A new continuous-time model for current-mode control with constant frequency, constant On-time and constant Off-time, in CCM and DCM", IEEE power electronics specialists conference record, San Antonio, Texas, pp. 382-389, 1990.
- Current mode control, venable technical paper #5, www.venableind.com.
- Fixed-Off-Time control of PFC pre-regulators", 10th European conference on power electronics and applications, EPE2003, Toulouse France, paper 382.
- A systematic approach to frequency compensation of the voltage loop in boost PFC pre-regulator", abstract.

8 Revision history

Table 1. Document revision history

Date	Revision	Changes
07-Mar-2013	1	Initial release.
06-Jun-2013	2	Updated title in cover page and *Figure 26: Excel spreadsheet BOM*. Minor text changes.