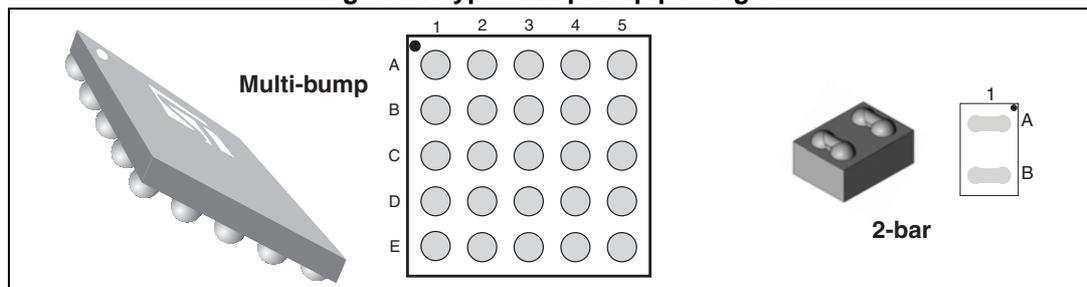

Flip Chip package description and recommendations for use

Introduction

This document provides package and usage recommendation information for 01005 Flip Chips.

The competitive market of portable equipment, notably the mobile phone market, is driven by a challenging development of highly integrated products. To allow manufacturers of portable equipment to reduce the dimension of their products, STMicroelectronics has developed packages with reduced size, thickness and weight in the form of the Flip Chip. The electrical performance of such components in Flip Chips is improved thanks to shorter connections than the ones in standard plastic packages (TSSOP, SSOP or BGA [Figure 1](#)).

Figure 1. Typical Flip Chip packages



The Flip Chip package family has been designed to fulfill the same quality levels and the same reliability performances as standard semiconductor plastic packages. This means these new Flip Chip packages should be considered as new surface mount devices which will be assembled on a printed circuit board (PCB) without any special or additional process steps required. In particular this package does not require any extra underfill to increase reliability performances or to protect the device. This package is compatible with existing adapted 01005 pick and place equipment for board mounting. Only lead-free, RoHS compliant Flip Chips are available in mass production.

This application note addresses the following topics:

- Product description
- Mechanical description
- Packing specifications and labeling description
- Recommended storage and shipping instructions
- Soldering assembly recommendations
- User responsibility and returns
- Changes
- Delivery quantity
- Quality

1 Product description

Flip Chips are manufactured with a wafer level process that STMicroelectronics has developed by attaching solder bumps on I/O pads of the active wafer side, thus allowing bumped dice to be produced. The I/O contact layout can be either matrix shape or set in periphery. No redistribution layer is used. This allows parasitic inductances coming from the redistribution metal tracks to be minimized.

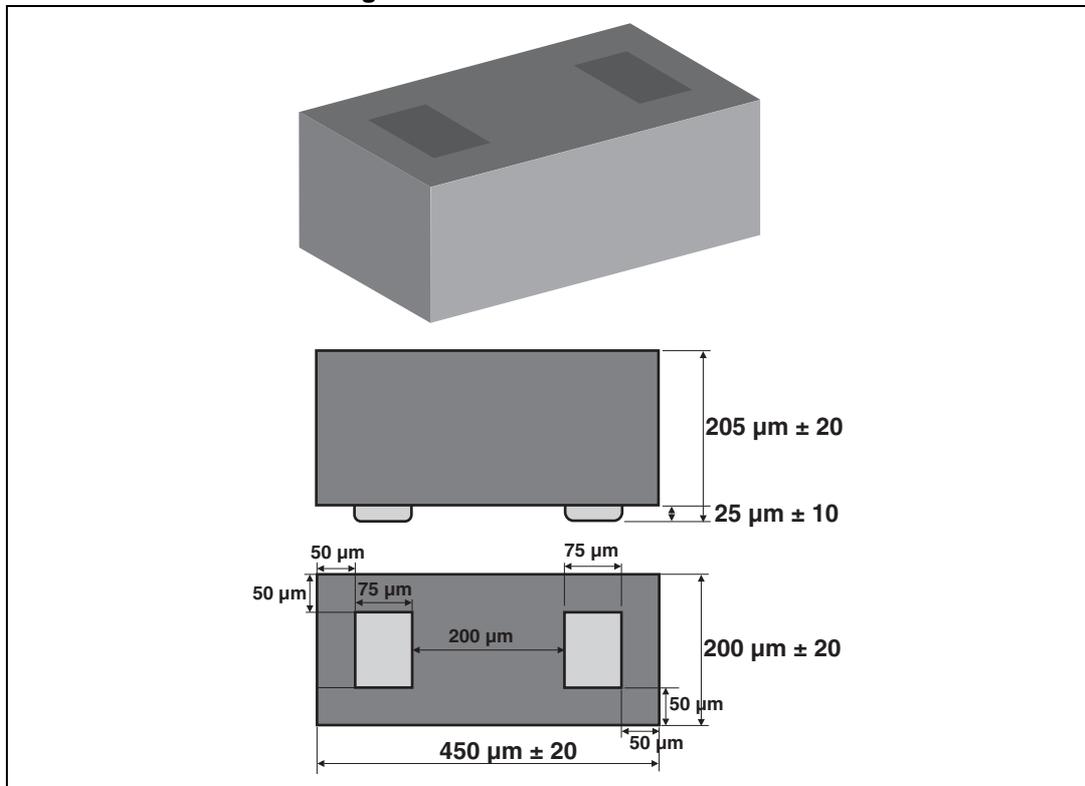
Lead-free bump composition is 98.25% Sn, 1.2% Ag, 0.5% Cu, 0.05% Ni. This is fully compatible with standard lead-free reflow processes. The bump dimension (25 μm bump height, shown [Figure 2](#)) allows the pick and place process to be compatible with existing equipment adapted to 01005 package (SIPLACE SX for example) and makes it also compatible with the PCB design rules used for standard ICs.

These components are delivered in tape and reel packing with the bumps turned down (placed on the bottom of the carrier tape cavity). The other face of the component is flat and allows picking as in the standard SMD packages.

Devices are 100% electrically tested before packing. The product references are marked on the flat side of the device.

2 Mechanical description

Figure 2. Mechanical dimensions



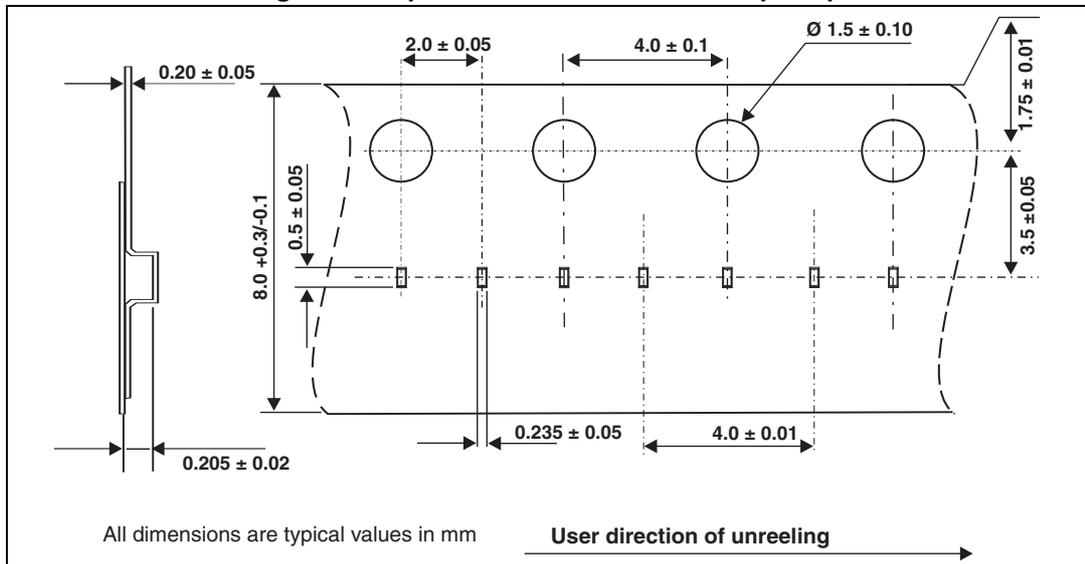
3 Packing specifications and labeling description

Flip Chips are delivered in tape and reel to be fully compatible with standard high volume SMD components. The features of tape and reel materials are in accordance with EIA-481-D, IEC 60286-3 and EIA 763 (783) standards. All features not specified in this section are in accordance with EIA-481-D, IEC 60286-3 and EIA 763 (783) standards.

3.1 Carrier tape

Flip Chips are placed in the carrier tape with their bump side facing the bottom of the cavity so that the components can be picked-up by their flat side. No flipping of the package is necessary for mounting on PCB. Carrier tape mechanical dimensions are shown in the example [Figure 3](#).

Figure 3. .Tape dimensions for 01005 Flip Chip



* A1 bump location varying with product layout

The cavities in the carrier tape have been designed to avoid any damage to the components. Specific hole is present to improve device stability during sealing and pick up.

The embossed carrier tape is in a black conductive material (surface resistivity within 10E5 and 10E11 ohm/sq). Use of this material protects the component against damage from electrostatic discharge and ensures the total discharge of the component prior to placement on the PCB. Conductivity is guaranteed to be constant and not affected by shelf life or humidity. The material will not break when bent and does not have any residue to rub off, powder, or flake.

3.2 Cover tape

The carrier tape is sealed with a transparent, antistatic (surface resistivity within 10E5 ohm/sq and 10E11 ohm/sq) polyester film cover tape with a heat activated adhesive. The cover tape tensile strength is higher than 10 N.

The peeling force of the cover tape is between 0.08 N and 0.5 N in accordance with the testing method EIA-481-D and IEC 60286-3. Cover tape is peeled back in the direction opposite to the carrier tape travel; the angle between the cover tape and the carrier tape is between 165 and 180 degrees and the test is done at a speed of 120 ± 10% mm/minute.

3.3 Reels

The sealed carrier tape with the Flip Chip is reeled on seven-inch reels (see [Figure 4](#) for reel mechanical dimensions). These reels are compliant with EIA-481-C standard. In particular, they are made of an antistatic polystyrene material. Color of the reel may vary depending on supplier.

Dice quantity per reel is 20000. In compliance with the IEC 60286-3, each reel contains a maximum of 0.1% empty cavities. Two successive empty cavities are not allowed. Each reel may contain components coming from 2 different wafer lots.

Each reel has a minimum leader of 400 mm and a minimum trailer of 160 mm (compliant with EIA 481-C and IEC 60286-3 standards). The leader makes up a portion of carrier tape with empty cavities and sealed by cover tape at the beginning of the reel (external side). The leader is affixed to the last turn of the carrier tape by using adhesive tape. The trailer is at the end of the reel and consists of empty, sealed cavities (see [Figure 5](#)).

Figure 4. Seven-inch reel mechanical dimensions

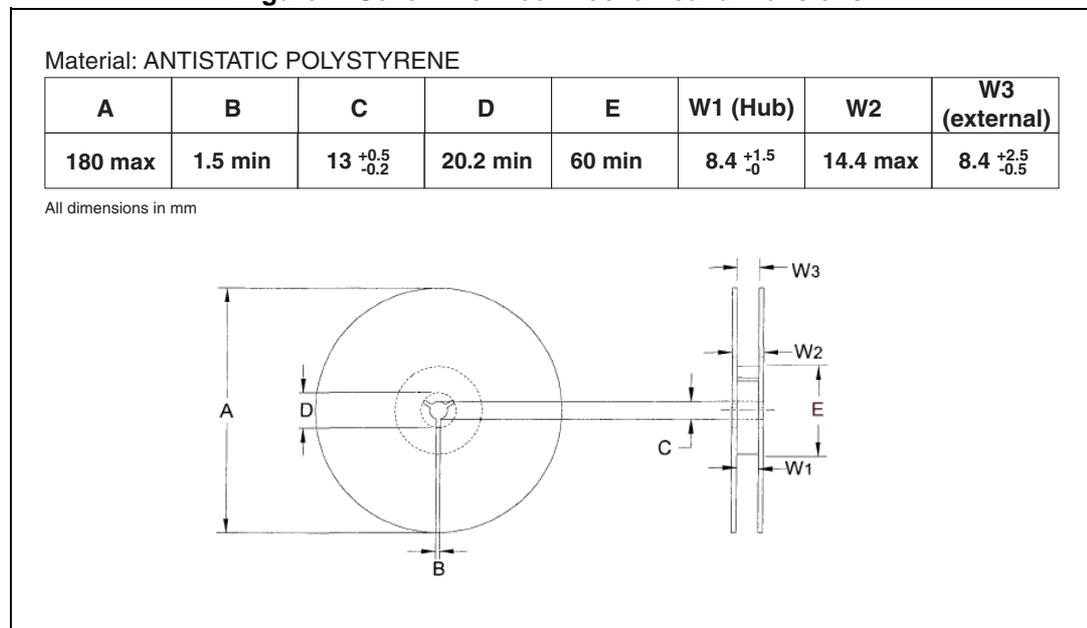
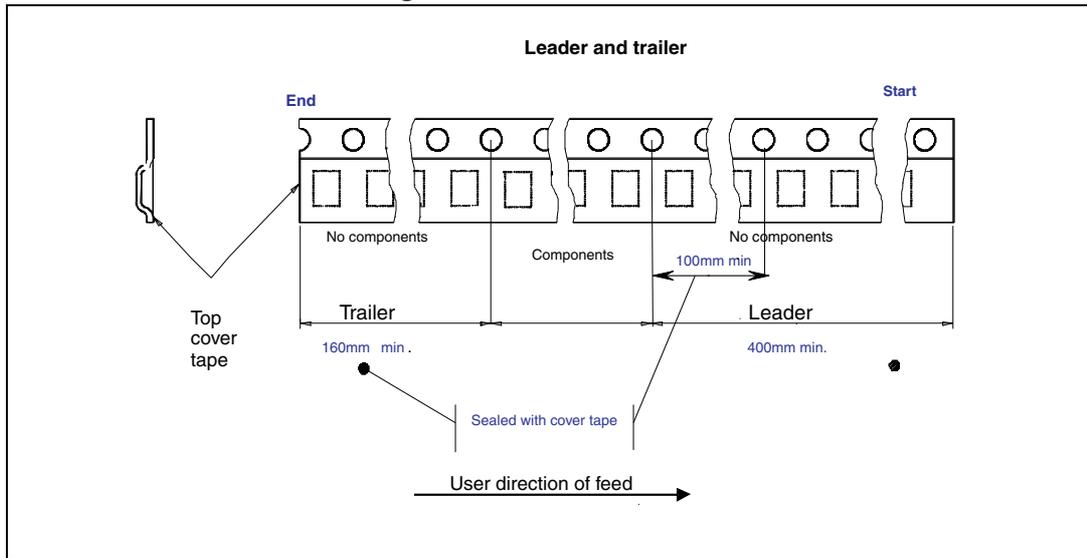


Figure 5. Leader and trailer



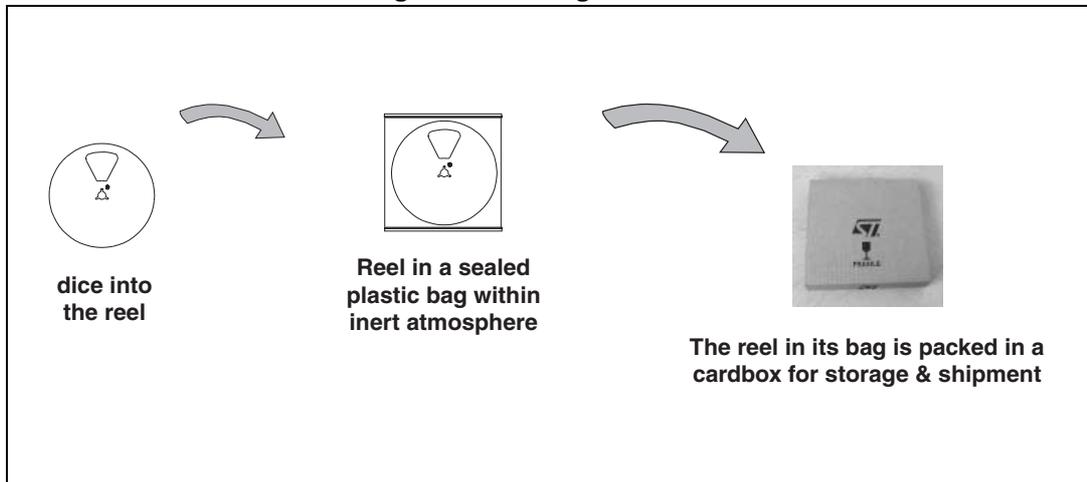
3.4 Final packing

Each reel is heat sealed under inert atmosphere in a transparent, recyclable and antistatic polyethylene bag (minimum of 4 mils material thickness).

Reels are then packed in cardboard boxes.

The complete description for packing is shown on [Figure 6](#).

Figure 6. Packing flow chart



3.5 Labeling

To ensure component traceability, labels are stuck on the reels and the cardboard box. The seven inch reels and the cardboard box are identified by labels including part number, shipped quantity and traceability references (*Figure 7* and *Table 1*).

The traceability is ensured for each production lot and each shipment lot through the labeling.

The trace code number printed on the labels ensures backward traceability from the lot received by the customer at each step of the process - in / out dates and quantity at diffusion, assembly, test and final store. Likewise, forward traceability is able to trace a lot history from the wafer fab to the customer's location.

Figure 7. Example of a reel label



Table 1. Parameter reel label

Field	Field type
Assembled in	Mandatory-Country of origin
Pb-free 2 nd . Level interconnect	As per JEDEC Standard JESD97
MSL	Mandatory for concerned products as defined in MPI Moisture Sensitivity Level as per JEDEC J-STD-020 Mandatory for SMD
Bag seal date	For MSL 2 and above, date of vacuum sealing of dry bag For MSL=1, "Not Moisture Sensitive" must be printed instead
PBT	Peak Package Body Temperature as JEDEC J-STD-020 Mandatory for the SMD
Category	Pb-free category as pr JEDEC Standard JESD97 Mandatory for concerned products as defined in MPI
Eco level	Mandatory for ECOLEVEL devices only as defined in MPI
Type	Mandatory First line: Not Required Second line: Raw line product name
Total qty	Mandatory - bulk quantity
Trace code	Mandatory- Traceability code with Wafer Fab Production Area Code
Bulk ID	Mandatory- Bulk ID Number, Start with A
Bar code	Mandatory-Bar code area

4 Recommended storage, shipping instructions and descriptions

Flip Chip reels are packed under inert N₂ atmosphere in a sealed bag. For shipment and handling, reels are packed in a cardboard box.

Components in a non opened sealed bag can be stored 6 months after shipment.

Components in tape and reel must be protected from exposure to direct sunlight.

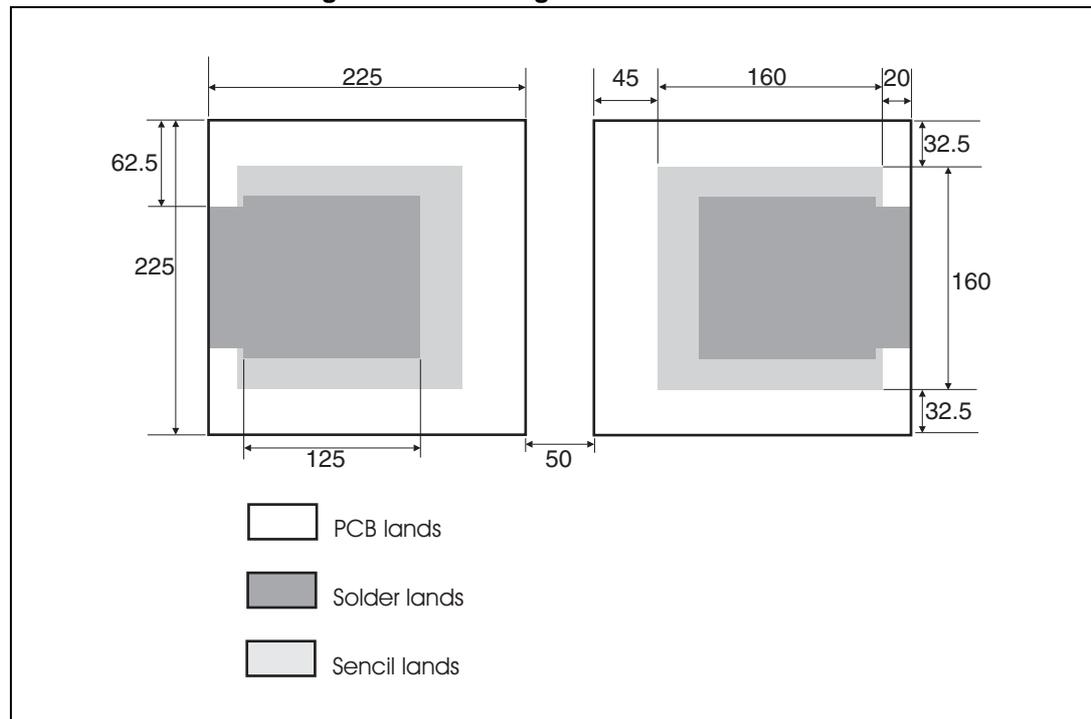
Moisture sensitivity level (MSL as per JEDEC J-STD-020C) is not applicable to Flip Chip devices since there is no plastic encapsulation and so no risk of moisture absorption and related possible package cracks.

5 Soldering assembly recommendations

5.1 PCB design recommendations for 01005 Flip Chip

For optimum electrical performance and highly reliable solder joints, STMicroelectronics recommends the PCB design guidelines listed below.(see [Figure 8](#))

Figure 8. PCB design recommendations



PCB pad finishing: Cu- Ni (2-6 μm) Au (0.2 μm max) or CuOSP (Organic Substrate Protection)

Note: A too thick gold layer finishing on the PCB pad is not recommended (low joint reliability).

5.2 PCB assembly guidelines

For Flip Chip mounting on the PCB, STMicroelectronics recommends the use of a solder stencil aperture of $160 \times 160 \mu\text{m}^2$ typical and a stencil thickness of $80 \mu\text{m}$. Use of solder paste type 4 minimum is recommended for optimal demolding (powder particle size $20\text{-}38 \mu\text{m}$ per IPC-J-STD-005 for example OM340 from Cookson). Flip Chips are fully compatible with the use of near eutectic 95.8% Sn, 3.5% Ag and 0.7% Cu solder paste with no clean flux. ST's recommendations for Flip Chip board mounting are illustrated on the soldering reflow profile shown in [Figure 9](#).

Figure 9. ST ECOPACK® recommended soldering reflow profile for Flip Chip mounting on PCB (definitions)

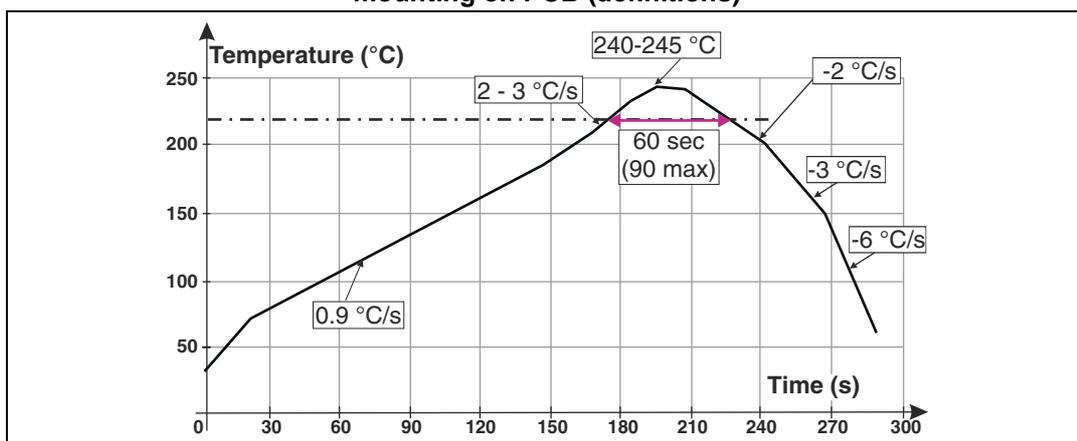


Table 2. ST ECOPACK® recommended soldering reflow profile for Flip Chip mounting on PCB (value)

Profile	Value	
	Typical	Max.
Temp. gradient in preheat (T = 70 – 180 °C)	0.9 °C/s	3 °C/s
Temp. gradient (T = 200 – 225 °C)	2 °C/s	3 °C/s
Peak temp. in reflow	240 - 245 °C	260 °C
Time above 220 °C	60 s	90 s
Temp. gradient in cooling	-2 to -3 °C/s	-6 °C/s
Time from 50 to 220 °C	160 to 220 s	

Dwell time (see [Table 2](#)) in the soldering zone (with temperature higher than 220 °C in [Figure 9](#)) has to be kept as short as possible to prevent component and substrate damages. Peak temperature must not exceed 260 °C. Controlled atmosphere (N₂ or N₂H₂) is recommended during the whole reflow, specially above 150 °C.

Flip Chips are able to withstand three times the previous recommended reflow profile to be compatible with a double reflow when SMDs are mounted on both sides of the PCB plus one additional repair.

A maximum of three soldering reflows are allowed for these lead-free packages (with repair step included).

The use of a no-clean paste is highly recommended to avoid any cleaning operation. To prevent any bump cracks, ultrasonic cleaning methods are not recommended.

For peak and place equipment, 01005 machine adapted is mandatory (SIPLACE SX for example) and placement accuracy has to be $20 \pm \mu\text{m}$ maximum. With more than $25 \mu\text{m}$ shift, there is high risk of bad soldering. Plastic nozzle are recommended for picking, to avoid backside chipping.

Regarding die size and weight, implementation of ionizers close to pick and place is recommended to avoid any ESD issue.

Rework of reels is not authorized by customer, regarding winding force issue.

6 Changes

STMicroelectronics reserves the right to implement minor changes of geometry and manufacturing processes without prior notice. Such changes will not affect electrical characteristics of the die, the pad layout or the maximum die size. However for confirmed orders, no variation will be made without customer's approval.

7 Quality

7.1 Electrical inspection

Products in Flip Chip are 100% electrically probed according to the critical parameters of the ST product specification. The last operation before packing is 100% electrical testing. The other parameters are guaranteed by technology, design rules and by continuous monitoring systems.

7.2 Visual inspection

A visual control is performed on all manufacturing lots according to the MIL-STD-883 method 2010.

8 Conclusion

Lead-free Flip Chip packages have been developed by STMicroelectronics for electronic applications where integration and performance are the main concerns of designers.

STMicroelectronics Flip Chips offer:

- Remarkable board space saving (package size equal to die size and total height less than 605 μm)
- Enhanced electrical performance (minimized parasitic inductance due to very short electrical paths and absence of redistribution layer)
- High reliability due to integration of a whole function traditionally based on discrete interconnected components.

Flip Chips are delivered in tape and reel and are fully compatible with other high volume SMD components (standard plastic packages or CSP/BGA packages) regarding existing pick and place equipment, standard solder reflow assembly equipment and standard PCB techniques.

9 Revision history

Table 3. Document revision history

Date	Revision	Changes
25-Jul-2014	1	First issue

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