Getting started with STM32F37/38xxx SDADC (sigma-delta ADC)

Introduction

The STM32F37/38xxx microcontrollers combine a 32-bit Arm® Cortex®-M4 core with a DSP and FPU instructions running at 72 MHz with advanced analog peripherals. The Cortex®-M4 core includes a precise 16-bit sigma-delta ADC.

This application note outlines the main features of the SDADC and shows how the SDADC can be used in some application cases: temperature measurement using PT100, pressure measurement using MPX2102A, wave recorder, and electrocardiogram (ECG) acquisition.

These application examples are implemented in C language and are available as part of the STM32F37/38xx DSP and standard peripherals library package (stm32f37x_dsp_stdperiph_lib) and the demonstration firmware package (stm32373c_eval_fw) of the STM32373C-EVAL evaluation board.

This document must be read in addition to the SDADC section in the reference manual *STM32F37xxx advanced Arm®-based 32-bit MCUs* (RM0313).

All values given in this document are guidance only. Refer to the related datasheet to get guaranteed and up-to-date values.

Table 1. Applicable products

Type	Products
STM32F37/38xxx	STM32F372C8, STM32F372CB, STM32F372CC, STM32F372R8, STM32F372RB, STM32F372RC, STM32F372V8, STM32F372VB, STM32F372VC STM32F373C8, STM32F373CB, STM32F373CC, STM32F373R8, STM32F373RB, STM32F373RC, STM32F373V8, STM32F373VB, STM32F373VC STM32F378CC, STM32F378RC, STM32F378VC STM32F382RC, STM32F382VC STM32F383CC, STM32F383RC, STM32F383VC

1 General information

This document applies to the STM32 Arm®-based microcontrollers.

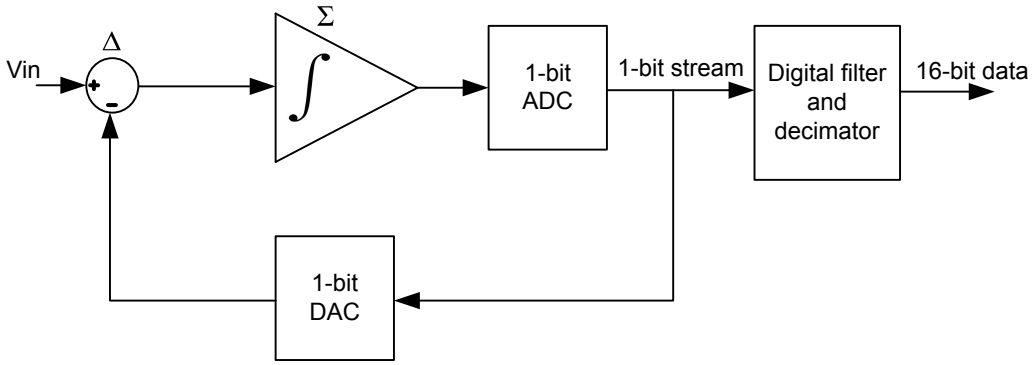
Note: Arm is a registered trademark of Arm Limited (or its subsidiaries) in the US and/or elsewhere.

2 Basics of sigma-delta converters

Sigma-delta converters, also known as oversampling converters, consist of two basic circuits: a modulator and a digital filter (see the figure below).

In the modulator, the input signal is added to the negative feedback signal from the digital-to-analog converter (DAC). The signal difference, after passing through the integrating circuit, reaches the input of the comparator (1-bit ADC), where it is compared to the reference voltage (the comparator works as a 1-bit quantizer). The input signal from the comparator (1-bit ADC) controls the 1-bit converter and reaches the input of the digital filter, that decreases flowability and transforms the 1-bit stream into 16-bit words. The used filter topology that ensures the low-pass stage is $Sinc^3$.

Figure 1. Block diagram of a sigma-delta analog-to-digital converter



3 16-bit SDADC overview

Main features

The STM32F37/38xxx devices include three embedded SDADC, that can be synchronized together. The main features of these SDADC are listed below:

- Effective number of bits (ENOB) equal to 14 bits
- 5 differential input pairs, or 9 single-ended inputs, or a combination
- High-performance data throughput:
  - 16.6 ksps input sampling rate when multiplexing between different channels
  - 50 ksps input sampling rate for single-channel operation
- Programmable gain: x0.5, x1, x2, x4, x8, x16 and x32
- Selectable reference voltage: V_{DDSD}, 1.22 V, 1.8 V and V_{REF}

3.1 Clock selection

The SDADC clock is supplied by SDADCCLK, that divides the system clock (SYSCLK) by a selectable prescaler: 2, 4, 6, 8, 10, 12, 14, 16, 20, 24, 28, 32, 36, 40, 44 and 48.

The typical operating frequency of SDADC is 6 MHz in fast-speed mode and 1.5 MHz in low-speed mode.

Example: If SYSCLK is set to 72 MHz, the SDADC divider must be set to the following SYSCLK typical frequency:

- Fast-speed mode: prescaler = 12 (72 MHz / 6 MHz)
- Low-speed mode: prescaler = 48 (72 MHz / 1.5 MHz)

3.2 Input modes

The SDADC has three possible input modes, that can be combined:

- Differential mode
- Single-ended offset mode
- Single-ended zero-reference mode

Differential mode

This mode is recommended when the sensors being used produce very small signals, with high susceptibility to noise. This is especially the case when using thermocouple and bridge type sensors (pressure sensors).

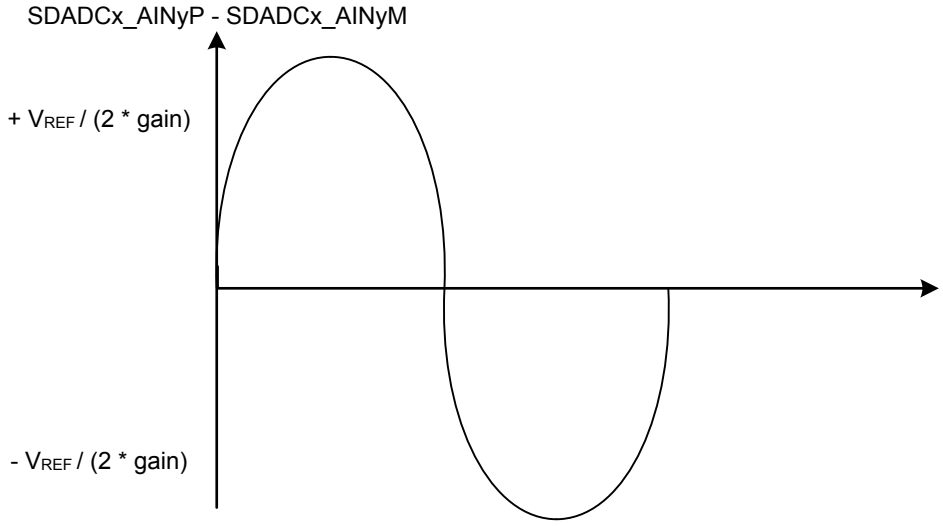
In differential mode, the SDADC converts the difference between SDADCx_AINyP and SDADCx_AINyM. The result can be either positive or negative depending on which input is at higher voltage.

Note: The SDADC can not measure negative voltages and the input voltage on each channel must stay within the electrical limits of the device.

The input range is [-V_{REF} / (2 * gain), + V_{REF} / (2 * gain)], and the conversion value is in the range [-32768, +32767].

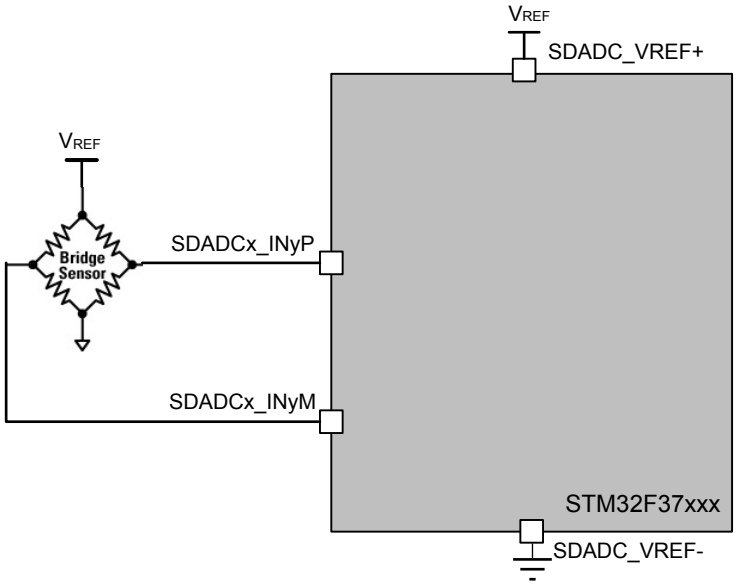
Example: For a 1.22 V reference voltage and a gain set to 1, the input range is +/- 0.61 V.
The formula is Vin = SDADCx_AINyP - SDADCx_AINyM = ReadData * V_{REF} / (2 * gain x 32768) with ReadData is two's complement read data from the SDADC data register: SDADCx_JDATAR or SDADCx_RDATAR.

Figure 2. Input signal range in differential mode



The figure below shows how to connect a bridge type sensor to the 16-bit SDADC. Both positive (SDADCx_AINyP) and negative (SDADCx_AINyM) inputs are connected to sensor outputs.

Figure 3. Typical connection of differential sensor to differential channels

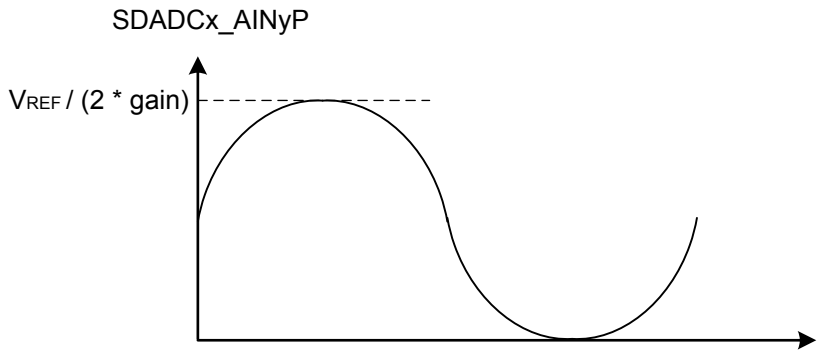


Single-ended offset mode

In this mode, the conversions are performed by connecting the negative input to 0 V internally, leaving the corresponding pin for the negative input (SDADCx_AINyM) free to be used for other purposes. The signal to be measured is applied to the positive input SDADCx_AINyP. This mode of operation is similar to differential mode, except that the output data is only from 0 to +32767, and not from –32768 to +32767.

Therefore half of the dynamic range is lost. Consequently the SNR (signal-to-noise ratio) is degraded. The formula is Vin = SDADCx_AINyP = ReadData * V_{REF} / (2 * gain * 32768)
with ReadData is two's complement read data from SDADC data register: SDADCx_JDATAR or SDADCx_RDATAR.

Figure 4. Input signal range in single-ended offset mode

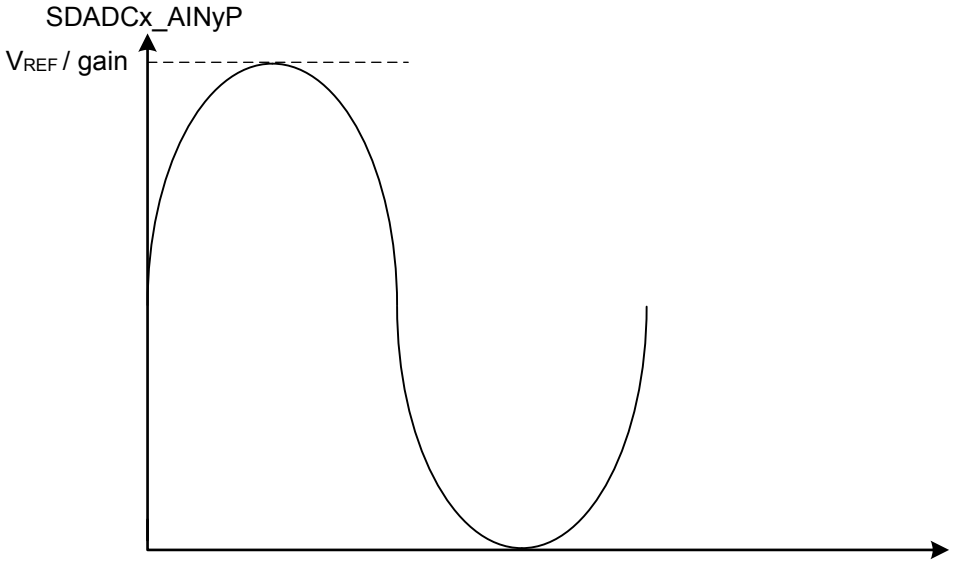


Single-ended zero-reference mode

In this mode, the signal is applied to the positive input SDADCx_AINyP, and the negative input is set to the signal reference (normally 0 V). This mode injects an input common mode of half scale to the ADC, thus maintaining the dynamic range the same as in differential mode (-32768 to +32767). In this mode, the injected common mode is dependent on gain variations.

The formula is Vin = SDADCx_AINyP = (ReadData + 32768) * V_{REF} / (gain * 65536)
with ReadData is two's complement read data from SDADC data register: SDADCx_JDATAR or SDADCx_RDATAR.

Figure 5. Input signal range in single-ended zero-reference mode



Note: When channel p (with an even p) is used in differential mode, the channel p+1 is automatically used as minus input (SDADCx_AINyM) and therefore channel p+1 can not be used in single-ended offset or zero-reference mode.

When the channel 4 is configured in differential mode, the channel 5 is automatically used as minus input. Therefore the channel 5 can not be used in single-ended offset or zero-reference mode.

3.3 SDADC voltage references

The SDADC reference voltage is selectable among the following sources:

- $V_{REFINT1}$: 1.2 V embedded reference voltage
- $V_{REFINT2}$: 1.8 V embedded reference voltage
- V_{DDSD}: SDADC analog supply voltage, from 2.2 V to 3.6 V
- V_{REFSD+}: external SDADC reference voltage, from 1.1 V to V_{DDSD}

The table below shows the voltage weights per bit (step size) using three possible references.

Table 2. Voltage step sizes

V_{REFSD+}	µV/bit
$V_{REFINT1}$ = 1.2 V	18.46
$V_{REFINT2}$ = 1.8 V	27.69
3.3 V	50.35

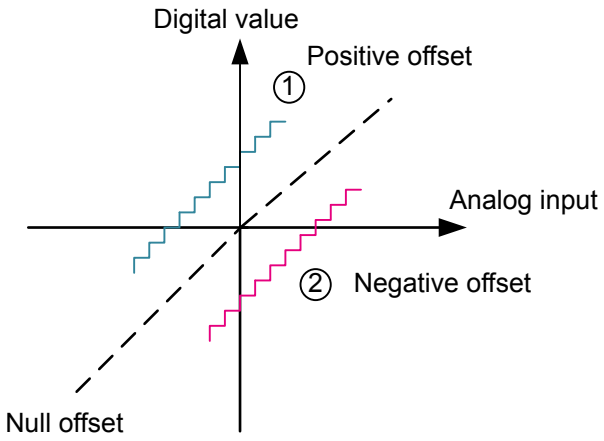
3.4 Calibration

In order to get the best performance from the SDADC, two parameters must be calibrated: offset and gain.

Offset calibration

The offset error is a constant value that is added to the ideal conversion value. The figure below illustrates the offset error.

Figure 6. Offset error in SDADC



The SDADC embedded in STM32F37/38xxx devices provides an automatic offset calibration without adding external components. Its principle can be summarized in the following steps:

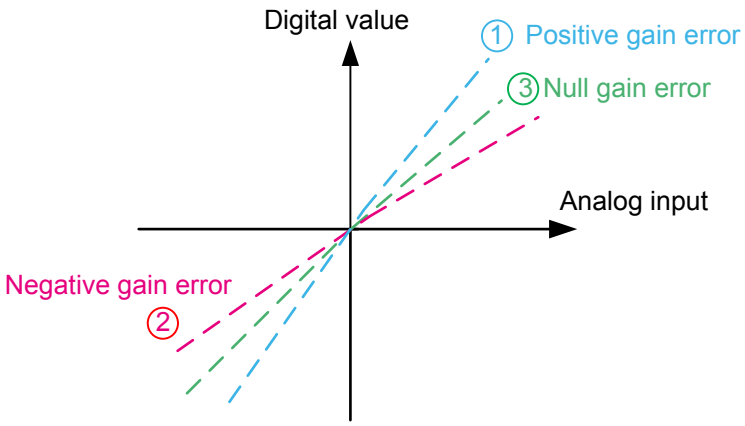
1. Shorts internally both channel inputs (positive and negative).
2. Performs conversion and stores the result in an internal register (configuration register).
3. Subtracts automatically the calibration value from the conversion value during standard conversion.

Note: It is recommended to run calibration at least once after SDADC configuration.

Gain calibration

As illustrated in the figure below, the gain error is the deviation of the SDADC transfer function from the ideal straight line. This gain error is due to the built-in programmable amplifier. According to the device datasheet, the typical analog gain error is -2.7%, which means there can be 884 counts (at maximum voltage) due to gain error. Reducing the gain error is then mandatory when performing accurate measurements.

Figure 7. Gain error in SDADC



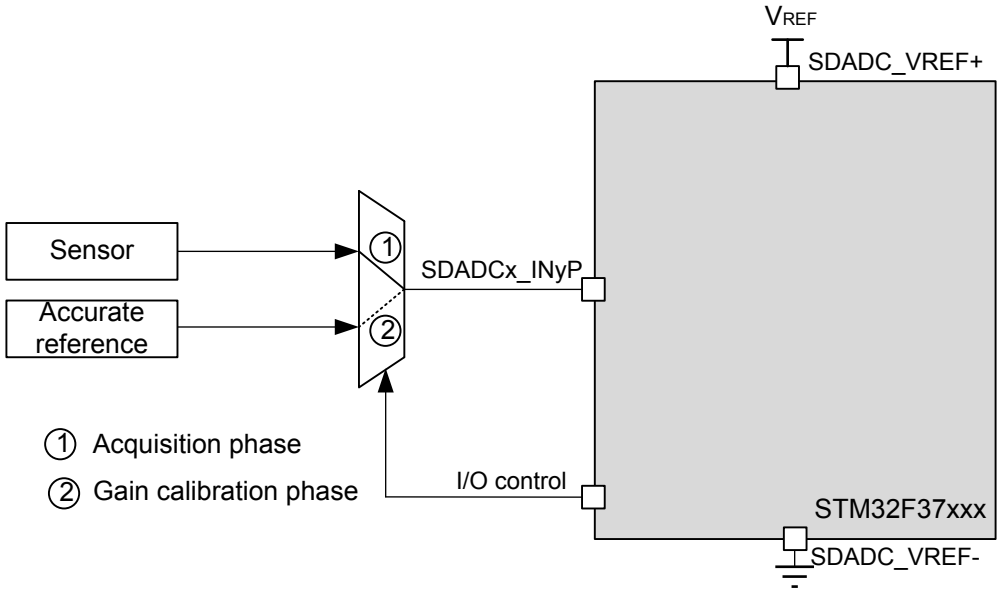
The following gain types are implemented in the SDADC:

- Analog gain: x1/2, x1, x2, x4, x8
- Digital gain: x16 and x32

Only the analog gains are considered in the gain calibration.

The gain calibration requires an external accurate reference (see the figure below). The accurate reference voltage (AccRef) is applied at the SDADC input and the SDADC output is checked.

Figure 8. Gain calibration using the accurate reference voltage



The gain is computed as follows: AccRef / (Output * V_{REF} / 65536).

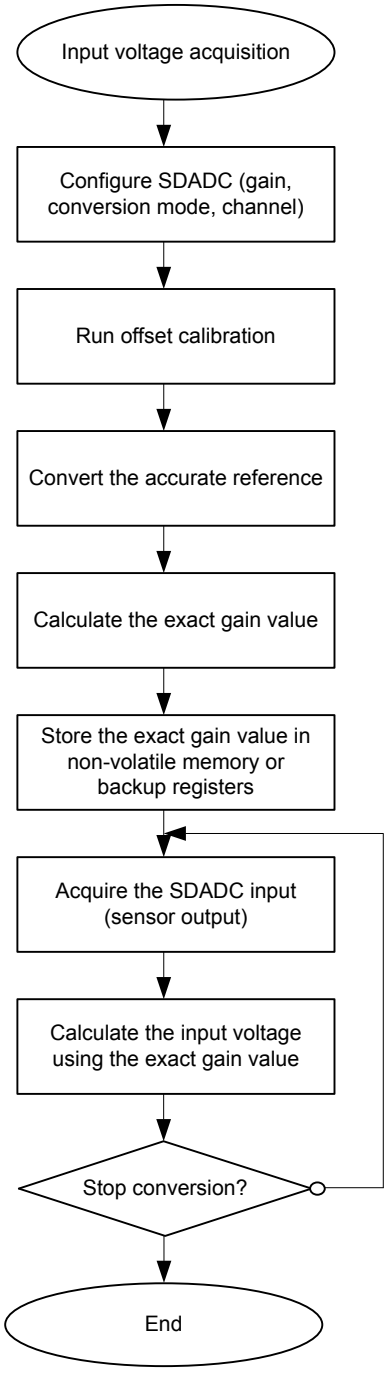
The computed gain can be stored in a non-volatile memory (Flash memory) and used during the acquisition phase

Note: Before running the gain calibration, it is mandatory to run offset calibration.

Software procedure for offset and gain calibration

The flowchart below shows a typical SDADC application using both offset and gain calibration.

Figure 9. SDADC software calibration sequence



3.5 Matching impedance

The impedance of the analog signal source, or series resistance (RAIN), between the source and the MCU pin, may lead to a voltage drop across it because of the current flowing into the pin.

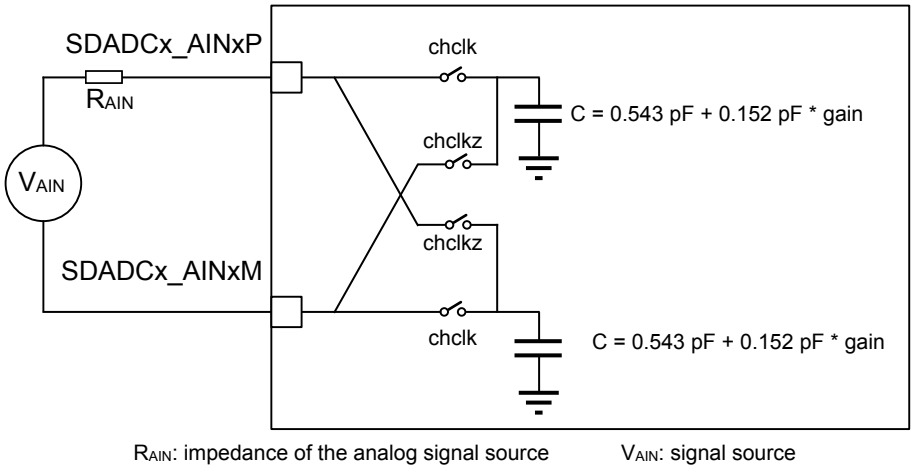
In the SDADC, the channel input impedance depends on:

- the SDADC clock
- the analog gain (0.5 - 8)

The figure below shows the equivalent input circuit for input channel where, Rin is the input impedance of the SDADC analog input. Rin can be calculated using the formula:

$$R_{in} = \frac{1}{2 \times f_{clk} \times C}$$

Figure 10. Equivalent input circuit for input channel



RAIN: impedance of the analog signal source VAIN: signal source

Table 3. Typical input impedance of SDADC input channel

Frequency (MHz)	Gain	Rin (kΩ)
1.5	0.5	540
6	0.5	135
6	8	47

3.6 Low-power modes

The 16-bit SDADC combines both high resolution and low power consumption, making the SDADC suitable for battery-powered products. If the SDADC is left powered-up continuously, it consumes 1.2 mA maximum (typically 800 µA). The following SDADC modes reduce the power consumption:

- Slow mode: the SDADC consumes 600 µA maximum but the sampling rate is limited to 12.5 Ksps maximum.
- Standby mode: the SDADC consumes 200 µA maximum but a stabilization time of 300 SDADC clock cycles (50 µs @ 6 MHz) is required each time the SDADC exits from Standby mode.
- Power-down mode: the SDADC consumes 2.5 µA maximum but a stabilization time of 600 SDADC clock cycles (100 µs @ 6 MHz) is required each time the SDADC exits from Standby mode.

4 Sigma-delta (SD) versus successive approximation register (SAR) analog-to-digital converters

Analog-to-digital converters come in different architectures to be able to address the needs of various applications. The main types available in the market are listed below:

- Successive approximation register (SAR) ADC

  These ADCs are frequently used in embedded systems, with sample rates of less than 5 Msps. Their resolution ranges from 8 to 16 bits. This type of ADC is used in industrial control applications.
- Sigma-delta ADC (SDADC)

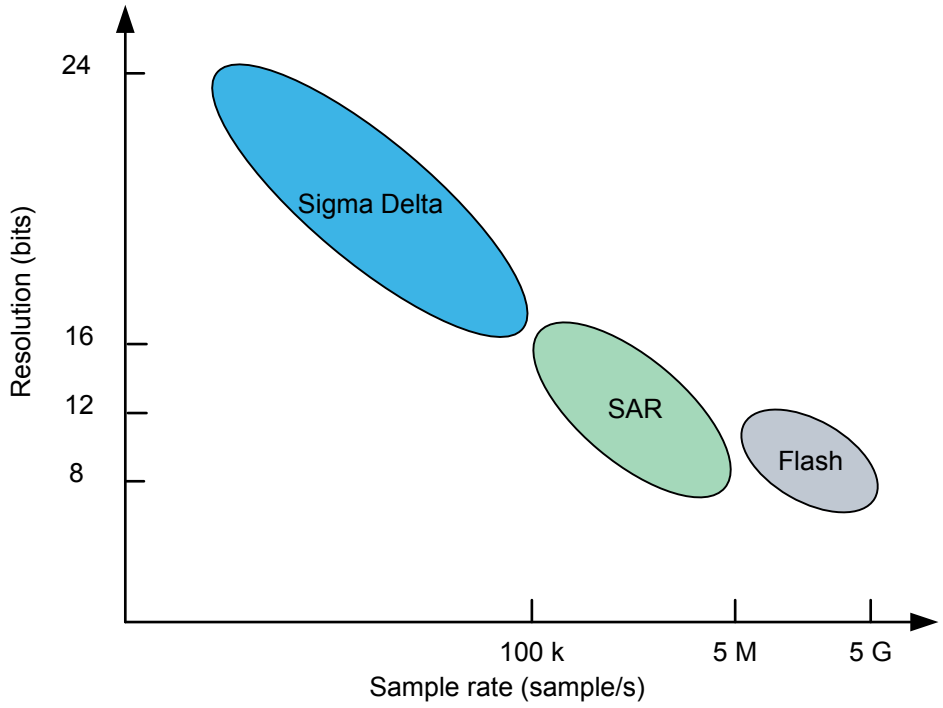
  These ADCs are used in lower-speed applications requiring high resolution. The resolution may attain 24 bits by oversampling, but the sampling rate is limited to only a few ksps.
- Flash ADC

  These ADCs are the fastest type of analog-to-digital converter. They are suitable for applications requiring a very high sampling rate. However, flash converters have low resolution (12 bits). This type of ADC is used in oscilloscopes.

The STM32F37/38xxx devices include two types of embedded ADCs: 12-bit SAR ADC and 16-bit SDADC.

The figure below gives an overview of the different ADC architectures, comparing their resolution and sampling rate.

Figure 11. ADC architecture versus resolution and sampling rate



The table below summarizes the differences between the two types of ADC.

Table 4. SDADC versus SAR ADC feature comparison

Feature	SDADC	SAR ADC
Maximum sampling rate	50 ksps(1)	1 Msps
Resolution	16 bits	12 bits
Input mode	Single-ended and differential	Single-ended
Embedded gains	0.5x to 32x	N/A
Number of channels	5 differential input pairs or 9 single-ended inputs	16 single-ended inputs
Number of instances	3 with synchro capability	1
Automatic offset calibration	Yes	
Analog watchdog	N/A	Yes
Trigger sources for regular conversion	• Software • Start of conversion of another SDADC	• Software • Embedded timers • External events
Trigger sources for injected conversion	• Software • Embedded timers • External events • Start of conversion of another SDADC	
Input range	Independent from V_{REF}, less than V_{REF}	[V_{REF-}, V_{REF+}]
Reference voltage	• 1.22 V • 1.8 V • V_{DDSD} • V_{REFSD+}	V_{REF+}
Input impedance(2)	47 kΩ to 540 kΩ	125 kΩ to 2500 kΩ

1. *The sampling rate is 50 ksps when selecting a single channel and 16.6 ksps when multiplexing between different channels.*
2. *For SDADC, the input impedance depends on the selected gain and the selected operating frequency (1.5 MHz or 6 MHz). For SAR ADC, the input impedance depends on used sampling frequency (0.05 - 1 MHz) and sampling capacitor (8pF).*

5 Application examples

This section presents how the 16-bit SDADC embedded in STM32F37/38xxx devices can be used in application examples such as temperature measurement, pressure measurement, three-phase power meter, or voice recorder.

5.1 Temperature measurement

This section details how to use a 16-bit SDADC to perform accurate temperature measurement using the PT100 sensor connected to PE7 on the STM32373C-EVAL evaluation board.

The application source code is available in folder `Project\STM32F37x_StdPeriph_Examples\SDADC` in *stm32f37x_dsp_stdperiph_lib* (STM32F37x DSP and standard peripherals library package) .

A current source circuit available on the STM32373C-EVAL board is used to provide a fixed 1 mA current (when V_{DD} = 3.3 V) to the temperature sensor PT100, that is connected to the SDADC1 channel 3P (PE7), through a reference resistor 1.8 kΩ labeled R33.

The SDADC is configured in single-ended offset mode. The input range is from 0 V to V_{REF} / (2 * gain).

In this application, the SDADC internal gain is set to 8, so the range is from 0 V to V_{REF} / 16.

The external reference V_{REF} (set to 3.3V on STM32373C-EVAL) is used as reference for the SDADC using JP17. The measurement ranges then between 0 V and V_{REF} / 16 = 0.20625 V. The conversion is performed in continuous mode with interrupts enabled on the end of the regular conversion.

The temperature is computed using the following formula:

$$Rpt100 = 100 + 0.385 \times T$$

$$then \quad T = \frac{(Rpt100 - 100)}{0.385}$$

$$Vpt100 = Rpt100 \times Ipt100 = Rpt100 \times \frac{V_{DD\_ANA}}{2 \times Rref}$$

$$then \quad Rpt100 = \frac{Vpt100 \times 1800 \times 2}{V_{DD\_ANA}}$$

$$and \quad T = \frac{1}{0.385} \times \left(\frac{(Vpt100 \times 1800 \times 2)}{V_{DD\_ANA}} - 100 \right)$$

where

- Rpt100 is the resistance of the PT100 sensor.
- Vpt100 is the voltage measured on PT100 sensor.
- Ipt100 is ~ 1mA current crossing the PT100 sensor.
- V_{DD_ANA} is the analog voltage.
- Rref is the reference resistor 1.8 kΩ labeled R33 on STM32373C-EVAL.

Table 5. Temperature sensor voltage range

Configuration	Temperature (°C)	Resistance (Ω)	Voltage (mV)
V_{DD} = 3.3 V and Rref = 1.8 KΩ	0	100	91.667
	20	107.7	98.725
	50	119.2	109.2667

The temperature measurement is performed in two steps:

1. Temperature sensor calibration

   This phase is performed with JP18 fitted in 2-3(REF) position. A 100 Ω resistor is connected to PE7 that is connected to V_{REF} through the reference resistor. The SDADC converter measures the analog voltage applied on PE7 and then computes the correction coefficient. This calibrates the gain. The PT100 is not connected in this phase.

2. Temperature measurement

   This phase is performed with JP18 fitted in 1-2 (PT100) position. The PT100 sensor is connected to PE7 that is connected to V_{REF} through the reference resistor. The SDADC converter measures the analog voltage applied on PE7 and then computes the temperature, that is given by the following formula:

$$\frac{CoeffCorrection \times \frac{AvrgRegularConvData}{SDADC\_GAIN} \times REFERNEC\_RESISTOR \times 2}{\frac{SDADCRESOL}{RESISTANCE\_COEFFICIENT}} - RESISTANCE\_ZERODEGRE$$

   where:

   – CoeffCorrection is the correction coefficient computed in phase 1.
   – AvrgRegularConvData is the average value of 256 samples.
   – SDADC_GAIN is the internal SDADC gain. In this example it is set to 8.
   – REFERENCE_RESISTOR is the reference resistor 1.8 kΩ labeled R33 on STM32373CEVAL.
   – SDADCRESOL is the sigma-delta converter: 2^{16} - 1.
   – RESISTANCE_ZERODEGRE is the resistance of the PT100 at 0 °C.
   – RESISTANCE_COEFFICIENT is the coefficient of the PT100 sensor.

5.2 Pressure measurement

This application example shows how to use the 16-bit SDADC to perform a pressure measurement, using the absolute pressure sensor MPX2102A, that is mounted on the STM32373C-EVAL evaluation board.

The application source code is available in the folder `Project\STM32F37x_StdPeriph_Examples\SDADC` in *stm32f37x_dsp_stdperiph_lib* (STM32F37x DSP and standard peripheral library package).

On the STM32373C-EVAL board, the MPX2102A sensor is connected to the SDADC1 channels 8P (PE8) and 8N (PE9). The MPX2102A sensitivity, when powered by 3.3 V, is:

3.3 V * 40 mV / 10 V = 13.2 mV / 1000 mB = 13.2 µV/mB.

To increase the sensitivity, an external 45.1 gain is applied, using the TVS632 operational amplifier that is available on the STM32373C-EVAL. The same operational amplifier is used to shift down the input voltage by 3.3 V / 10 = 0.33 V.

Table 6. Pressure sensor voltage range

Configuration	Pressure (HPA)	Differential voltage on sensor outputs (mV)	Differential voltage on SDADC inputs (mV)
V_{DD} = 3 V	800	10.56	146.256
	1000	13.2	265.32
	1200	15.84	384.384

Note: Refer to the user manual STM32373C-EVAL evaluation board (UM1564) for more details about how the MPX2102A is connected to PE8 and PE9.

The SDADC channel 8 is configured in differential mode. The external reference V_{REF} (set to 3.3 V on STM32373C-EVAL) is used as reference for SDADC. The conversion is triggered by the TIM19 timer with interrupt enabled on the end of the injected conversion.

The input voltage is calculated using the formula below:

$$inputvoltage = \left(InjectedConvData \times \frac{SDADC\_VREF}{SDADC\_RESOL \times SDADC\_GAIN}\right) + OFFSET\_VOLTAGE$$

where:

- InjectedConvData is the digital value read from SDADC data register.
- SDADC_VREF is the sigma-delta converter voltage reference, set externally to 3.3 V.
- SDADC_RESOL is the sigma-delta converter resolution: 2^{16} - 1.
- SDADC_GAIN is the internal SDADC gain (set to 4 in this example).
- OFFSET_VOLTAGE is the offset voltage added by the operational amplifier TVS632 (approximately 3.3 V / 10 = 0.33 V).

The pressure is calculated using the formula below:

$$\mathrm{Pr}\,essuremB = \frac{1000000 \times inputvoltage}{MPX2102\_SENSITIVITY \times EXTERNGAIN}$$

5.3 Wave recorder

This example shows how to use the 16-bit SDADC to record the human voice using the electric condenser microphone that is installed on the STM32373C-EVAL evaluation board.

The application source code is available in the file `Project\STM32373C-EVAL\src\waverecorder.c` in *stm32373c-eval_fw* (STM32373C-EVAL demonstration firmware package).

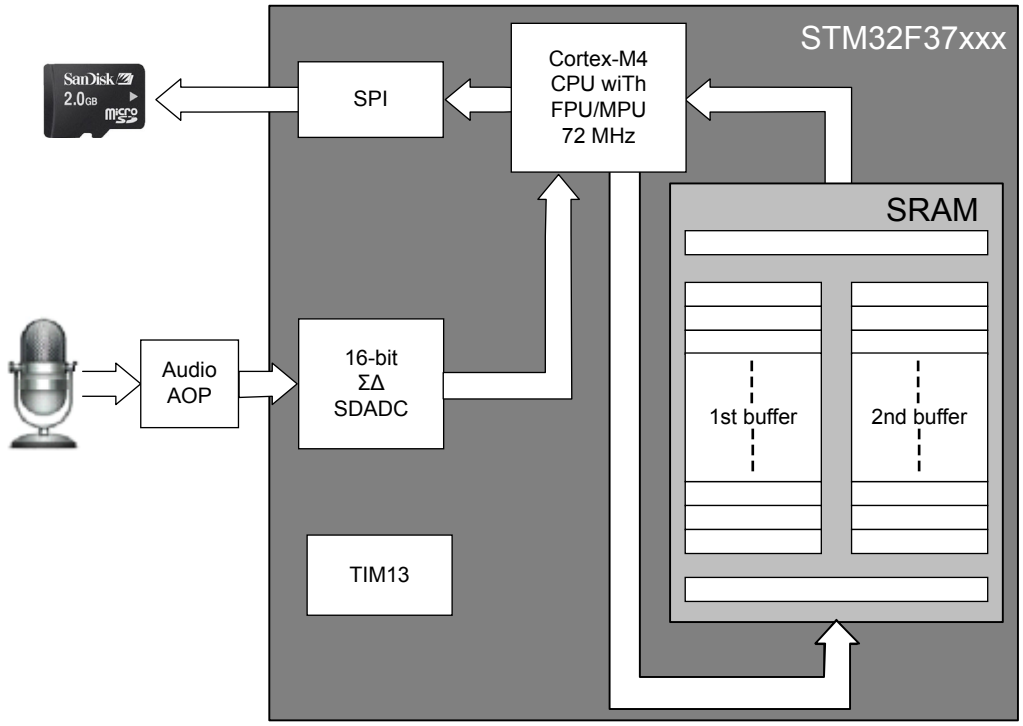
A microphone is connected to the SDADC1 channel 6 (PB0) through an audio amplifier/filter. The SDADC is configured in single-ended zero-reference mode, and the voice recording is triggered by TIM13 at a sampling rate of 8 kHz.

The wave-recorder application uses a ping-pong buffer: one buffer is actively being written in the microSD™ memory card, while the second buffer is filled with the new samples.

Writing access to the microSD™ memory card uses the open source file system FatFS.

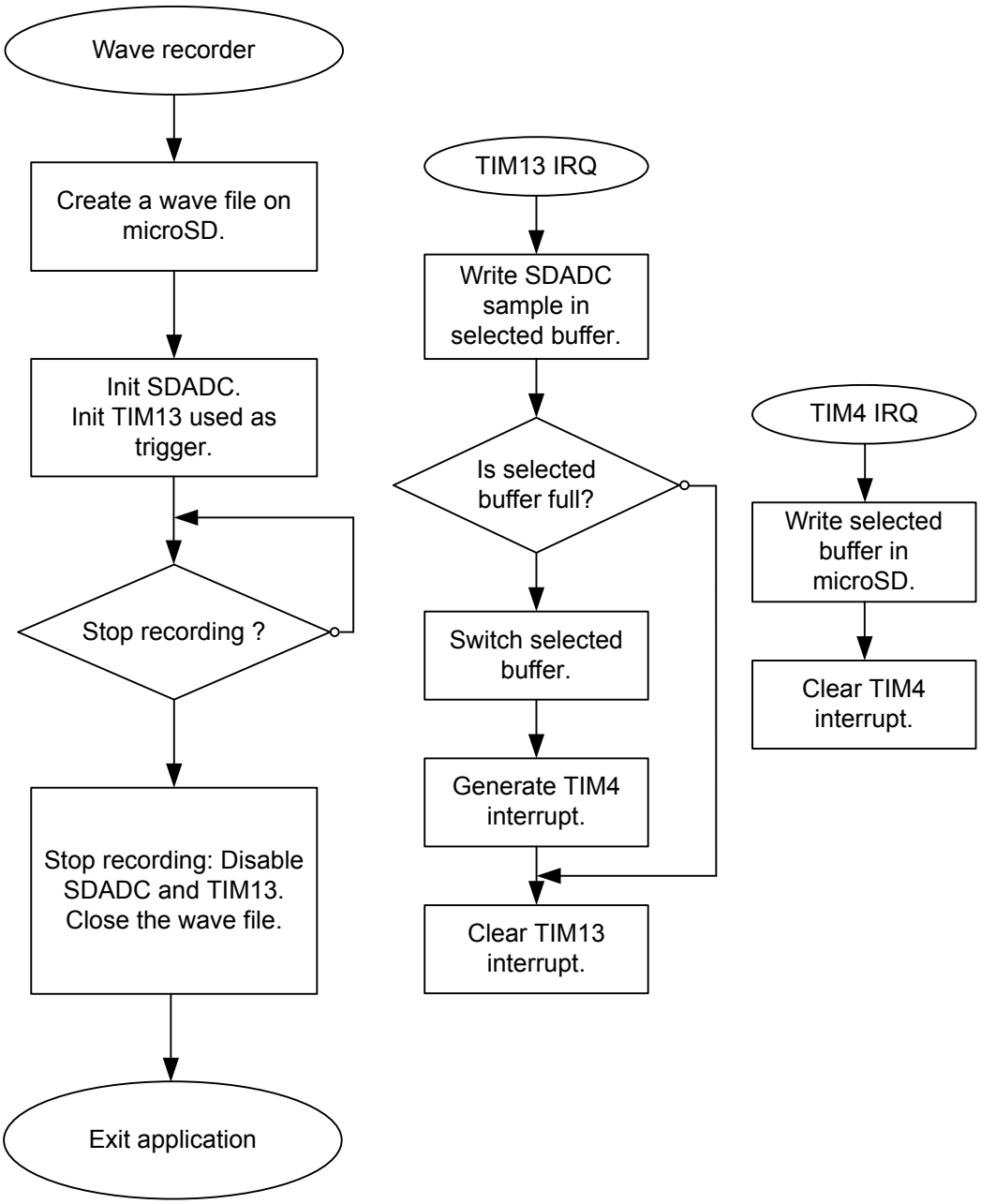
The figure below shows the block diagram of the voice recorder application.

Figure 12. Block diagram of the voice recorder



The flow chart of this application example is given in the figure below.

Figure 13. Flowchart of the wave recorder application



5.4 ECG acquisition

This example shows how to use the 16-bit SDADC to acquire a human ECG using two ECG electrodes TS1 and TS2 that are installed on the STM32373C-EVAL evaluation board.

The application source code is available in the file `Project\STM32373C-EVAL\src\applications.c` in *stm32373c-eval_fw* (STM32373C-EVAL demonstration firmware package).

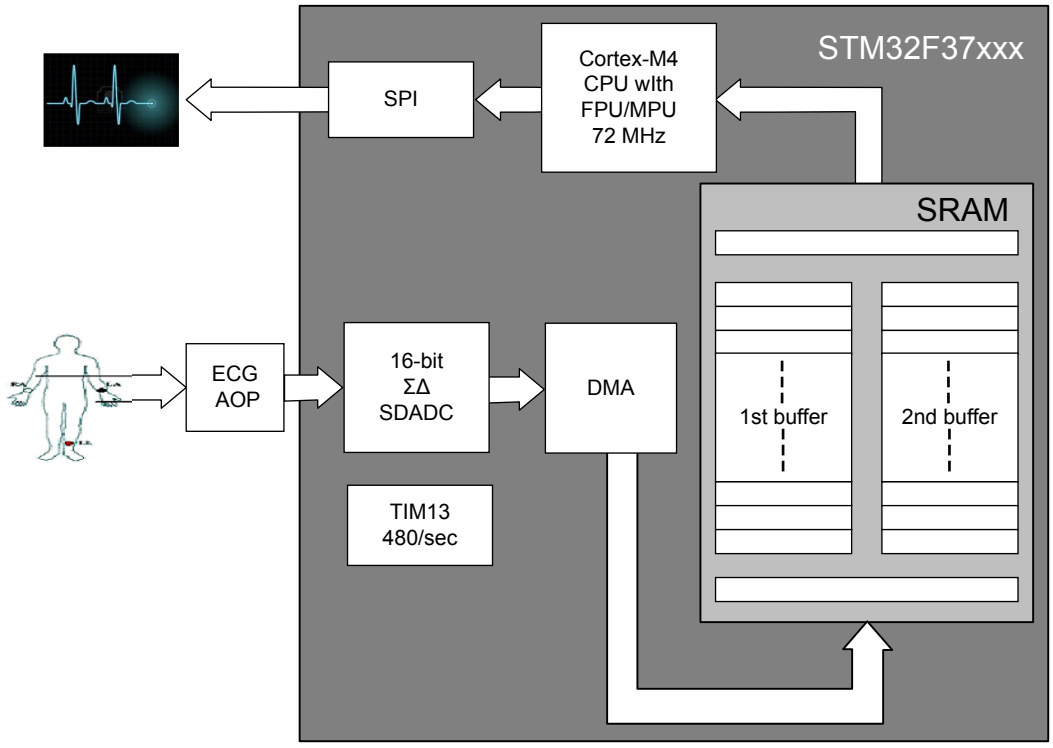
Two ECG electrodes, TS1 and TS2, are connected to the SDADC1 channel 0 (PE12) through an ECG amplifier/ filter. The SDADC is configured in single-ended zero-reference mode and the conversion is triggered by the TIM3 timer at a sampling rate of 480 Hz.

The ECG acquisition application uses a ping-pong buffer: one buffer is actively being filtered (using a bandpass filter) and then displayed on the LCD, while the second buffer is filled with the new ECG samples.

Note: ECG samples are filtered using the Arm DSP library.

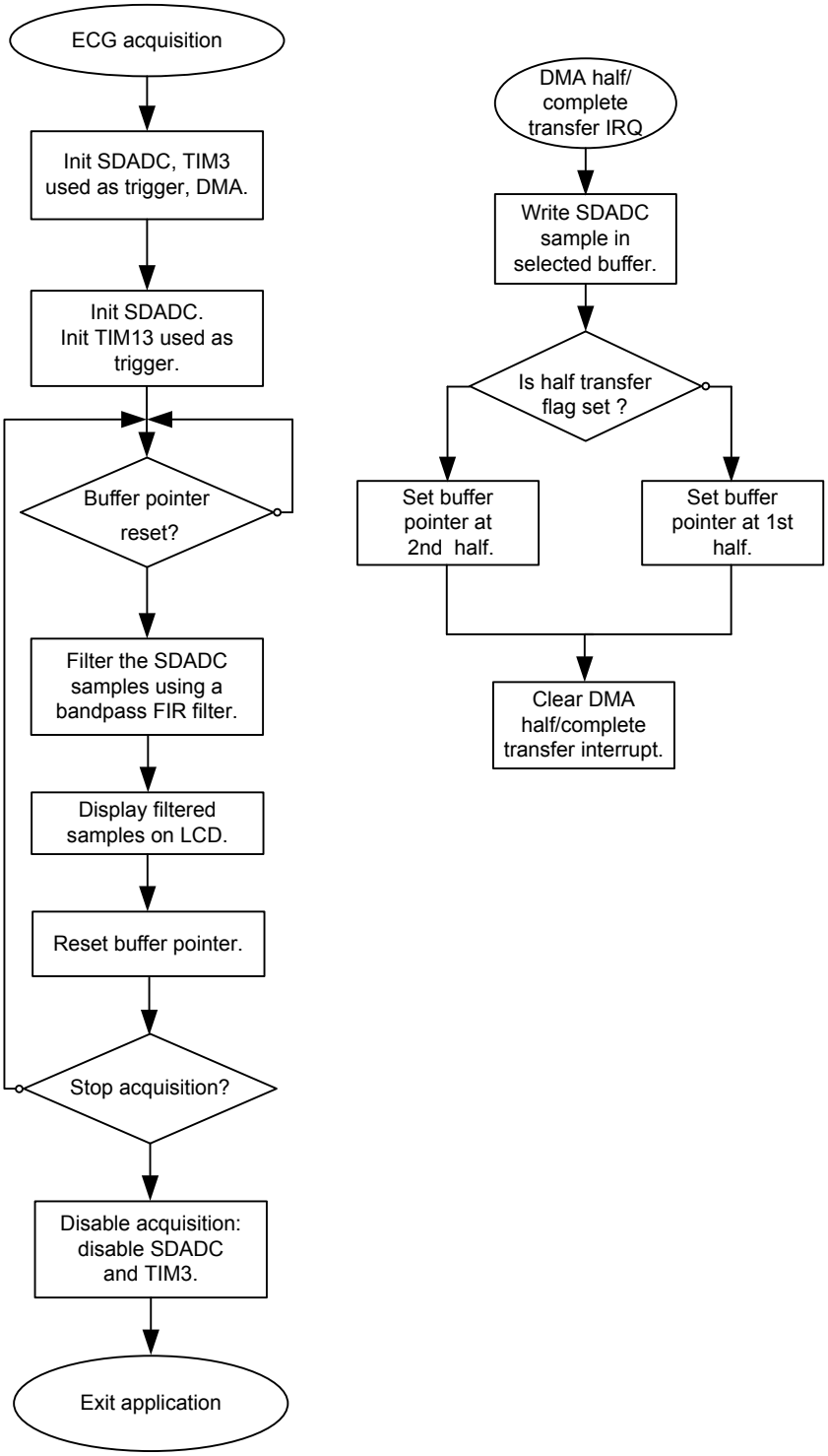
The figure below shows the block diagram of the ECG acquisition application.

Figure 14. Block diagram of the ECG acquisition application



The flowchart of this application is given in the figure below.

Figure 15. Flowchart of the ECG acquisition application



5.5 Power-meter application

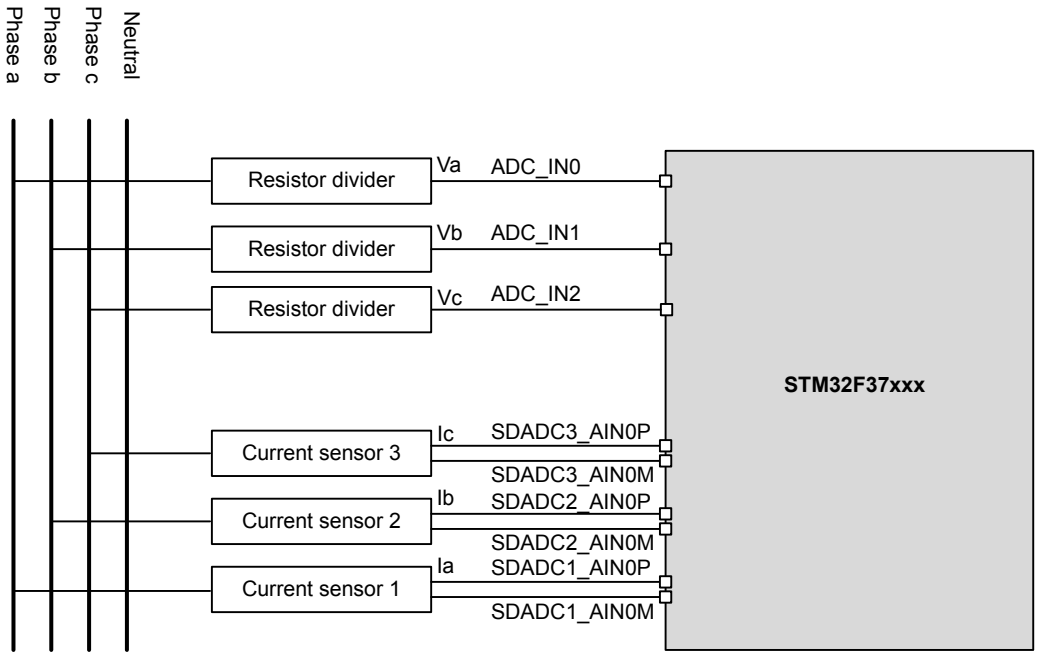
The analog-to-digital converter is the most important part of a power-meter application and the SDADC embedded in STM32F37/38xxx devices meets the requirements of this type of application. Typically, a class B power meter requires 1.5% current measurement accuracy, which means a 14-bit ENOB ADC.

For the voltage measurement, there are no strict requirements and therefore the SAR ADC can be used for voltage measurement synchronized with the SDADC that is used for measuring the current.

Another ADC constraining parameter is the sampling rate. For power-meter applications, a sampling rate of up to 12.8 ksps is sufficient for harmonic spectrum analysis.

As shown in the figure below, in the power-meter application, the phase measurement consists of measuring voltages: Va, Vb and Vc, in single-ended mode, using the SAR ADC while currents (Ia, Ib and Ic) are converted in differential mode using the SDADC. All are triggered by the same timer (for example TIM19).

Figure 16. Three phases of the power-meter application



Revision history

Table 7. **Document revision history**

Date	Version	Changes
13-Dec-2012	1	Initial release.
20-Jan-2021	2	Updated: • title and Introduction • new Section 1 General information • structure of Section 3 16-bit SDADC overview • [-32768,+32767] in Section 3.2 Input modes • Table 4. SDADC versus SAR ADC feature comparison

Contents

List of tables

List of figures