New generation of 650 V SiC diodes

Introduction

For many years ST has been a worldwide leader in high voltage rectifiers dedicated to energy conversion. During the last decade, electronic systems have followed a continuous trend towards higher power density and more energy savings driven by governments' environmental awareness. Power-supply designers are permanently confronted with stringent efficiency regulations (Energy Star, 80Plus, European Efficiency…). They are forced to consider the use of new power converter topologies and more efficient electronic components such as high-voltage silicon-carbide (SiC) Schottky rectifiers. To help them face this challenge, ST developed in 2008 a first family of 600 V SiC diodes. After having sold millions of pieces, ST's reliability and know-how is confirmed on these new components using wide band gap materials.

In hard-switching applications such as high end server and telecom power supplies, SiC Schottky diodes show significant power losses reduction and are commonly used. A growing use of those rectifiers is also recorded in solar inverters, motor drives, USP and HEV applications.

However, the high cost of this technology tends to drive designers to use it at high current-density levels (3 to 5 times higher than standard Si diodes), inducing more constraints on the diode. Indeed, the Silicon-carbide material features a positive thermal coefficient potentially leading to some instability and lower current-surge robustness than silicon diodes. ST decided to review the design and develop a second generation of SiC diodes offering an enhanced current capability while still featuring an attractive switching-off behavior. The peak reverse voltage was also increased to 650 V in order to ensure a safer operation in certain designs.

Typical applications (non-exhaustive list)

- Industrial high voltage AC/DC power management unit
- Desktop and PC power supply
- Server power supply
- Telecom power
- TV SMPS
- AC/DC power management unit, high voltage, and other topologies
- Uninterruptible power supply (UPS)
- Air conditioner PFC
- Photovoltaic applications (solar boost converter, inverter topology, micro-inverter…)
- On-board charger (OBC)
- EV (electrical vehicle) charging station

1 Features of the SiC diodes

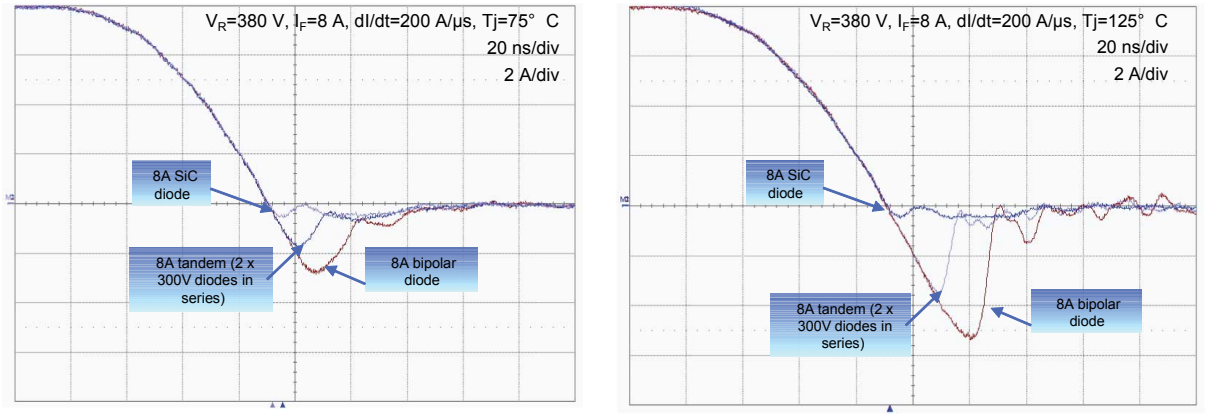
1.1 Turn-off behavior

1.1.1 Comparison with Si bipolar diode

The benefits brought by silicon-carbide diodes on the switching losses in the applications working in continuous-conduction mode (such as PFC applications) are already well known. The capacitive nature of the recovery current allows constant turn-off characteristics when the temperature increases. In contrast the turn-off behavior of bipolar diodes is characterized by a strong dependency on junction temperature, dI/dt slope and forward current level (see Figure 1.).

Thanks to their properties, SiC diodes allow significant reduction of power losses in the associated MOSFETs when switched-on. They also permit new optimization options for the power converter (for example, increasing the switching frequency and speed, lowering the size of passive components, snubber-circuits and EMI filters).

Figure 1. Switching behavior comparison between Si and SiC diodes for T_j = 75 °C and T_j = 125 °C



The capacitive recovery current is generated by the charge of the junction capacitance C_j under a certain reverse voltage and corresponds to a quantity of stored charges Q_C.

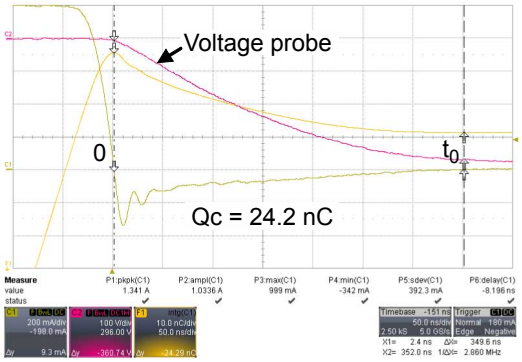
1.1.2 Capacitive charge (Q_C) measurement

Some confusion exists about the measurement conditions of Q_c. A comparison between the switch-off behavior and the integral of the current used to estimate Q_c is shown in Figure 2..

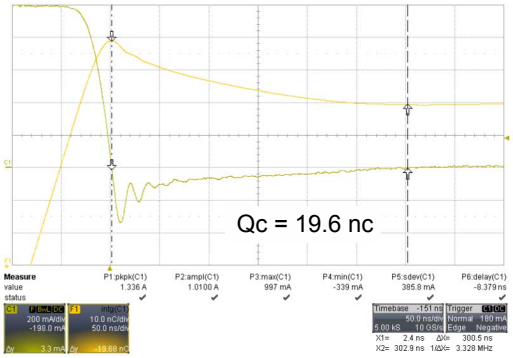
Figure 2.A and Figure 2.B show measurements at low forward current (I_F = 1 A) and low dI/dt slope (50 A/µs), with and without reverse voltage across the diode. A certain inaccuracy of the measurement of Q_c can be observed. It is linked to the probe, which features its own equivalent capacitance.

Figure 2.C shows a measurement at I_F = 2 A and a high dI/dt slope (200 A/µs) without any probe voltage. With such a high value of current-slope some oscillations appear. Taking into account the total capacitive current until t_0 when the reverse voltage reaches V_R, Q_c measured by the integral of the current is similar to the one in Figure 2.B.

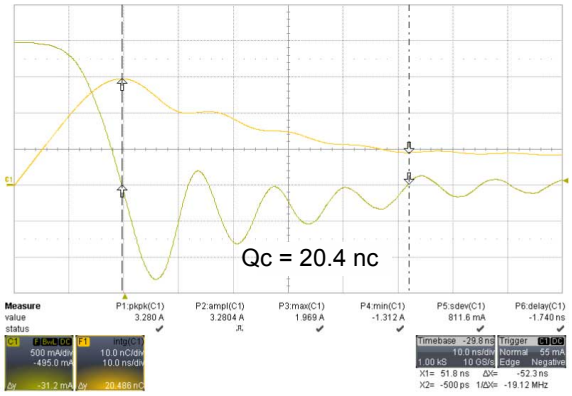
Figure 2. Q_c measurement of a 6 A SiC diode at I_F = 1 A, T_j = 25 °C, V_R = 400 V, dI/dt = 50 A/µs



A. With voltage probe



B. Without voltage probe



C. I_F = 2 A, dI/dt = 200 A/µs

To avoid false readings due to some measurement inaccuracy, a theoretical approach is preferred. The quantity of charge Q during a certain period of time [0-t0] is delimited by the reverse voltage variation V across the junction capacitance C_j between 0 and V_R and is given by the following formulas:

$$\int_0^{Q_c} dQ = \int_0^{t0} i(t)dt \quad (1)$$

With

$$i\left(t\right) = C_j \frac{dV(t)}{dt} \quad (2)$$

After simplification and introduction of the junction capacitance variation versus the reverse voltage $C_j(V)$, Q_c is defined by the following formula:

$$Q_c\left(V_R\right) = \int_0^{V_R} C_j\left(V\right) dV \quad (3)$$

This relation demonstrates that Q_c is defined by the integral of the junction capacitance C_j between 0 and V_R, the voltage reapplied on the diode. This theoretical approach allows the direct and accurate evaluation of Q_c, avoiding the inaccuracy introduced by potential measurement problems.

The strict expression of the energy stocked in the junction capacitor for a given reverse voltage can be determined by:

$$E_{Q_c}\left(V_R\right) = \int_0^{V_R} C_j\left(V\right) \times V \, dV \quad (4)$$

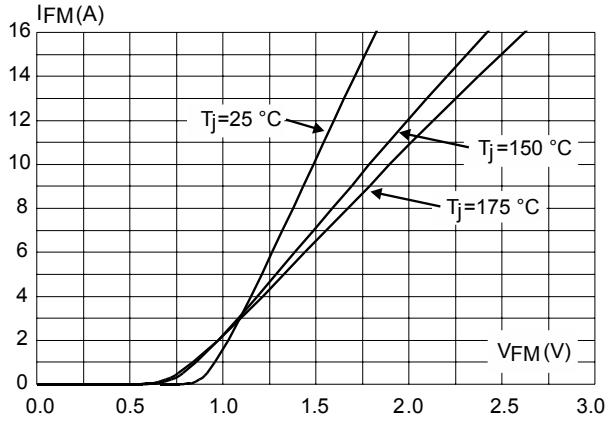
Due to the non-linearity of the junction capacitance versus the reverse voltage, this relation is different from the traditional energy formula ½ · C · V² (or ½ · Q · V), which is valid only when considering a constant capacitance.

1.2 Forward characteristics

Another main feature of SiC diodes is the variation of the forward voltage drop (V_F) with the junction temperature.

Figure 3. shows the forward current versus forward voltage drop characteristics for 3 different junction temperature levels. A crossing-point can be observed at a certain level of current IC. When the current is lower than this level, the temperature coefficient of the forward voltage drop (αV_F) is negative. When the current is higher, it becomes positive. The same crossing point exists for traditional silicon diodes, but it appears at a much higher current level (>10 times the nominal current). This is linked to the higher forward current density of SiC diodes.

Figure 3. ST's STPSC806 first generation: typical forward voltage drop versus forward current



As a consequence, the working area of SiC rectifiers usually corresponds to $\alpha V_F > 0$, which leads to an increase of the forward voltage drop with the junction temperature, meaning an increase of the conduction power losses, hence an increase of the temperature and so on. This electro-thermal mechanism results in a thermal runaway loop. The effect is explained in Section 2 .

1.3 Other characteristics

1.3.1 Low leakage current

The new generation of 650 V SiC diode offers some low leakage current values similar to the 600 V Si counterparts. Therefore the reverse power losses defined in PFC by the Eq. (5) stays negligible as showed in Table 1.

$$P_{REV}(T_j) = \delta_{av} \times V_R \times I_R(V_R, T_j) \quad (5)$$

With

$$\delta_{av} = 1 - \frac{2 \times \sqrt{2} \times V_{in}}{\pi \times V_{out}} \quad (6)$$

Table 1. Leakage current and reverse losses comparison in PFC at 90Vac between Si and SiC diode

Product	I_R at $V_R = V_{RRM}$	P_{rev} in PFC at V_{in} = 90 V, V_{out} = 400 V
	Typical / Maximum	Typical
STTH8R06D	35 / 400 µA at 125 °C	0.011
STPSC806D	150 / 1000 µA at 125 °C	0.047
STPSC8H065D	65 / 335 µA at 150 °C	0.02

1.3.2 “C” thermal coefficient

The “C” thermal coefficient represents the leakage current dependence on the junction temperature. The leakage current increases by an exponential law with the junction temperature. Knowing a reference point $I_R(V_R,T_{jRef})$ and the value of the thermal coefficient “C”, one can easily calculate the leakage current at a given temperature T_j using the following formula:

$$I_R\left(V_R, T_j\right) = I_R\left(V_R, T_{jRef}\right) \times e^{c\left(T_j - T_{jRef}\right)} \quad (7)$$

where V_R is the reverse voltage applied across the diode.

Each diode has its own coefficient that can be calculated using two points as follows:

$$c = \frac{1}{T_{jRef2} - T_{jRef1}} \times I_n\left(\frac{I_R\left(V_R, T_{jRef2}\right)}{I_R\left(V_R, T_{jRef1}\right)}\right) \quad (8)$$

If the SiC Schottky diodes have low leakage currents and they have also a smaller temperature dependence compared to the Si counterparts. As illustrated in Table 2., typically the “C” thermal coefficient should be around 2 times lower than the Si diodes.

Table 2. “C” thermal coefficient comparison between Si and SiC diode

Product	I_{R1} at V_R = 400 V, T_{j1}	I_{R2} at V_R = 400 V, T_{j2}	C coefficient
STTH8R06	8 µA at 125 °C	50 µA at 150 °C	0.070
STPSC8H065D	4 µA at 150 °C	8.5 µA at 175 °C	0.030

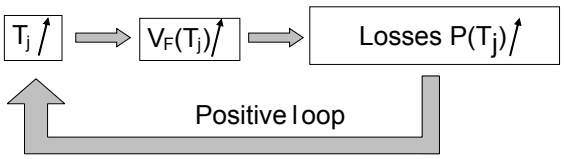
The feature of low dependence with the T_j is interesting to push back the limit of thermal runaway due to the power reverse losses. Regarding the stability criterion formula linked to P_{PREV} given by Eq. (9), the interest for the use at high T_j of small packages with high thermal resistance becomes certain.

$$\frac{dP_{REV}(T_j)}{dT_j} \leq \frac{1}{R_{th(j-a)}} \quad (9)$$

2 Forward thermal runaway

In some particular application conditions a thermal runaway loop can be triggered (see Figure 4.) and the thermal system of the diode may become unstable.

Figure 4. Thermal runaway loop



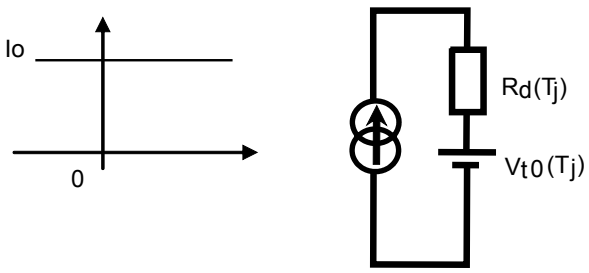
Two kinds of application conditions can be linked to the thermal runaway risk:

- the stationary regime during the regular working mode
- the critical transient phases.

2.1 Thermal runaway risk in regular working mode

During the regular operating mode, the average current in the diode can modeled with a constant current generator as shown in Figure 5.

Figure 5. Simple electrical model



The electrical model given by Eq. (10) , simulates the variation of the forward voltage drop versus the junction temperature for a given current I_0.

$$V_F(I_0, T_j) = V_{t0_{150°}} + \alpha V_{t0}(T_j - 150) + [R_d + \alpha R_d \times (T_j - 150)] \times I_0 \quad (10)$$

$$V_{t0}(T_j) = V_{t0_{150°}} + \alpha V_{t0}(T_j - 150) \quad (11)$$

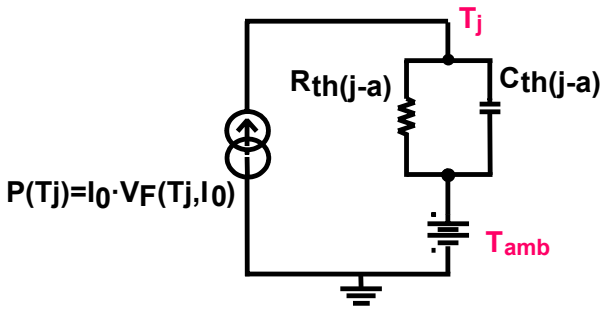
$$R_d(T_j) = R_{d_{150°}} + \alpha R_d(T_j - 150) \quad (12)$$

$V_{t0}(T_j)$ is the V_F value for a fixed T_j when I_F is null. The inverse function of $R_d(T_j)$ represents the straight slope between 2 forward current levels and the threshold voltage V_{t0} for a fixed T_j. (see AN604 Calculation of conduction losses).

αV_{t0} and αR_d are thermal coefficients. They represent the junction temperature impact on V_{t0} and R_d.

Using the electrical model previously defined, the conduction power losses $P(T_j)$ can be estimated. Using the analogy between thermal and electrical units, a simple electro-thermal model is described in Figure 6.. The thermal model is defined by the thermal resistance $R_{th(j-a)}$ and the thermal capacitance $C_{th(j-a)}$ junction to ambient.

Figure 6. Simple electro-thermal model



The resolution of the above electro-thermal system gives the $T_j(t)$ expression used to find the thermal runaway limit and to highlight the stability condition of the diode. The equation giving the conduction power losses versus T_j is the following:

$$P(T_j) = [V_{t0_{150°}} + \alpha V_{t0}(T_j - 150)] \times I_0 + [R_{d_{150°}} + \alpha R_d \times (T_j - 150)] \times I_0^2 \quad (13)$$

with

$$A = I_0 \times (V_{t0_{150°}} - 150 \times \alpha V_{t0}) + I_0^2 \times (R_{d_{150°}} - 150 \times \alpha R_d) \quad (14)$$

and

$$I_0 \times \alpha V_{t0} \times T_j + I_0^2 \times \alpha R_d \times T_j = (I_0 \times \alpha V_{t0} + I_0^2 \times \alpha R_d) \times T_j = B \times T_j \quad (15)$$

A simplified version is:

$$P(T_j) = A + B \times T_j \quad (16)$$

The global system equation is defined by:

$$T_j = T_{amb} + R_{th} \times \left(P(T_j) - C_{th} \times \frac{dT_j}{dt}\right) \quad (17)$$

Or again

$$T_j \times (1 - B \times R_{th}) + R_{th} \times C_{th} \times \frac{dT_j}{dt} = T_{amb} + A \times R_{th} \quad (18)$$

Solving the differential equation gives the stability condition on the junction temperature:

$$T_j(t) = \frac{R_{th} \times (A + T_{amb} \times B)}{B \times R_{th} - 1} \times e\left(\frac{B \times R_{th} - 1}{C_{th} \times R_{th}}\right) \times t - \frac{T_{amb} + A \times R_{th}}{B \times R_{th} - 1} \quad (19)$$

Due to the exponential function in the expression of $T_j(t)$, if B x R_{th} - 1 > 0 then the limit:

$$\lim_{t \to \infty} T_j(t) \to \infty \quad (20)$$

leads to the diode destruction if the current I_0 is not interrupted. Thus, the stability condition is given by:

$$B \times R_{th} - 1 < 0 \quad (21)$$

so

$$R_{th} < \frac{1}{B} \quad (22)$$

The detailed expression gives:

$$R_{th} < \frac{1}{\alpha V_{t0} \times I_0 + \alpha R_d \times {I_0}^2} \quad (23)$$

Note that the limit of thermal runaway can be directly found by:

$$\frac{dP_T(T_j)}{dT_j} \leq \frac{1}{R_{th(j-a)}} \quad (24)$$

Numerical application:

An application with an average current I0 = 6 A using the STPSC6H065 is considered here.

The V_{t0}, R_d value of the typical forward voltage curve versus forward current of the STPS6H065 datasheet are calculated between 3 A and 9 A and between 25 °C and 150 °C:

$V_{t0150°C}$ = 0.85 V, $R_{d150°C}$ = 0.175 Ω, αV_{t0} = -800 µV/°C, αR_d = 600 µΩ/°C.

So, the “B coefficient” is equal at 0.017 W/°C, and the critical R_{th}, beyond which the thermal runaway is reached, is R_{th} > 59.5 °C/W.

Considering the $R_{th(j-a)}$ of the TO-220 package in air to be around 60 °C/W, the stability condition will not be respected since $B \cdot R_{th(j-a)} - 1 > 0$ and thus the diode cannot be used without a heatsink for this value of current.

The diode must be mounted on its own heatsink, in choosing the R_{th} value checking $B \cdot R_{th(j-a)} - 1 < 0$ and respecting $T_j < T_{jmax}$. In this case of a stable condition,

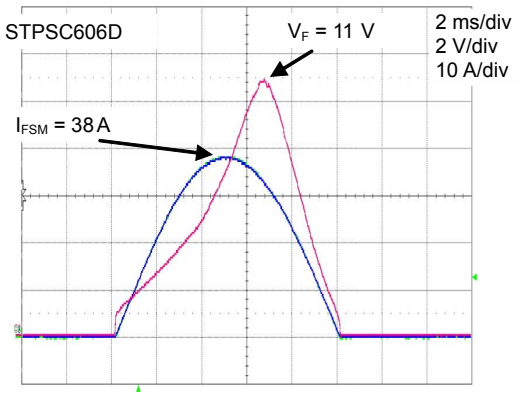
$$\lim_{t \to \infty} T_j(t) \to -\frac{T_{amb} + A \times R_{th}}{B \times R_{th} - 1} \quad (25)$$

if T_j targeted is 125 °C with T_{amb} = 40 °C, the heatsink should be chosen for an $R_{th(j-a)}$ value equal to 7.74 °C/W.

2.2 Thermal runaway risk in transient phase

The thermal runaway phenomenon can easily be observed with the short I_{FSM} test waveform by sensing the forward voltage drop. I_{FSM} is defined by a sine-wave of 10 ms shown in Figure 7. and is described in the datasheet as the non-repetitive maximum surge forward current.

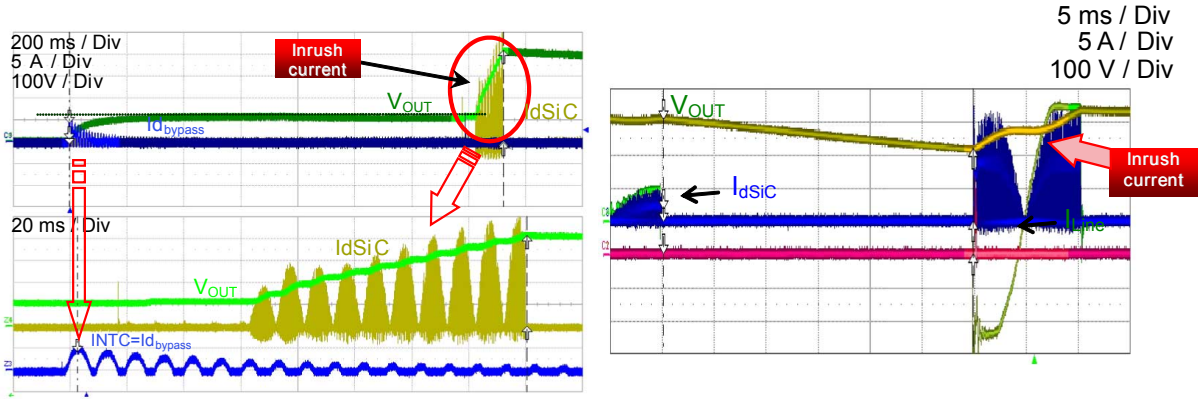
Figure 7. Thermal runaway phenomenon during an I_{FSM}-test waveform



In standard applications, the current waveforms are either shorter or longer and more complex due to the switching frequency. However the I_{FSM} parameter stays a reference that reflects the capability of the diode to sustain a surge current.

In an SMPS, during the transient phases such as the start-up phase, a power line drop-out, a lightning surge or a short circuit, experience shows that some high surge current stresses are applied to the diode. Examples are shown in Figure 8..

Figure 8. Inrush current proportional to dV_{out}/dt during a start-up phase and a power line drop-out



Unlike the regular operating mode, the current stress duration is generally lower than 1 s. In this case a thermal runaway phenomenon can be triggered and the advised limit to avoid the destruction of the diode is the T_{jmax} given in the datasheet.

The estimation of T_j during these transient conditions involves the transient thermal impedance:

$$\Delta T(t) = P(t) \times Zth'(t) = \int_0^t P(t)Zth'(t-\tau)d_\tau \quad (26)$$

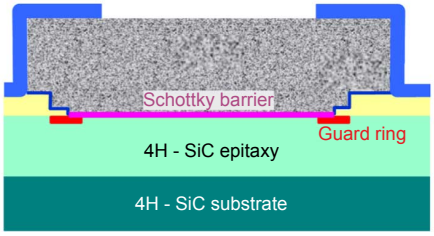
In most cases, the complexity of the current waveform implies that the above equation is solved with help of an electro-thermal model as shown in Figure 12.

To push back the thermal runaway limit and improve the capability of SiC diodes to withstand high current surges, a second generation of SiC diode has been developed by STMicroelectronics using a combination of a Schottky diode and a PN diode. This new technology is usually called Junction Barrier Schottky (JBS).

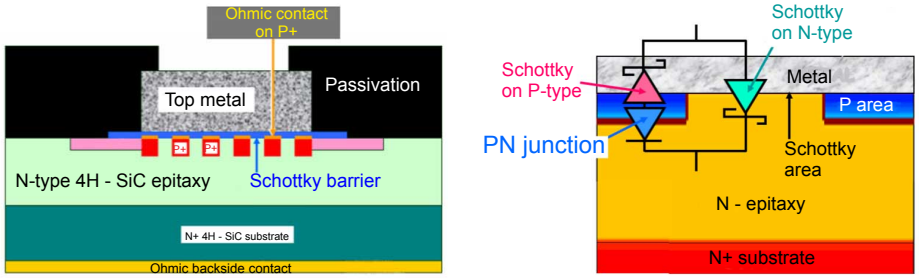
3 New 650 V JBS SiC diodes

3.1 Device structure

Figure 9. Comparison between a pure SiC Schottky structure with the JBS SiC structure



Schematic cross section of conventional SiC Schottky diode (1st generation device)



Schematic cross section of a JBS SiC diode (2nd generation device)

The 2nd generation SiC device is based on JBS (junction barrier Schottky) concept. At high forward voltage drops, this structure benefits from the injection of minority carriers by the PN junctions inserted within the main Schottky contact. Thus in case of surges current, modulation of resistivity induces a lower V_F and a smaller increase of T_j. Moreover, the PN grid supports the decrease the leakage current I_R and to increase the breakdown voltage V_{br} of the device. So, thanks to this new design, the robustness of device is drastically increased compared to standard Schottky diode.

3.2 Comparison between first and second generation of SiC diodes

3.2.1 Forward voltage comparison

The forward voltage characteristics of the first and the second generation are compared in Figure 10.. The dotted line network corresponds to the linear characteristics of the pure SiC Schottky diode. The positive thermal coefficient is evident. Those curves highlight the difficulties in characterizing the pure SiC Schottky diode at high current with constant junction temperature due to the overheating linked to the measurement. To limit this thermal effect, the tests are made with a short duration pulse t_p = 50 µs. The second generation of SiC diodes also presents a linear characteristic up to a certain level of current. A clamping effect linked to the JBS structure then appears at higher current. This effect happens when there is a bias of the merged PN junctions, roughly beyond 3 V, 10 A @ 175 °C; 3.5 V, 15 A at 125 °C; 4 V, 25 A at 75 °C…

Figure 10. Forward voltage comparison between pure Schottky SiC diode and JBS SiC diode

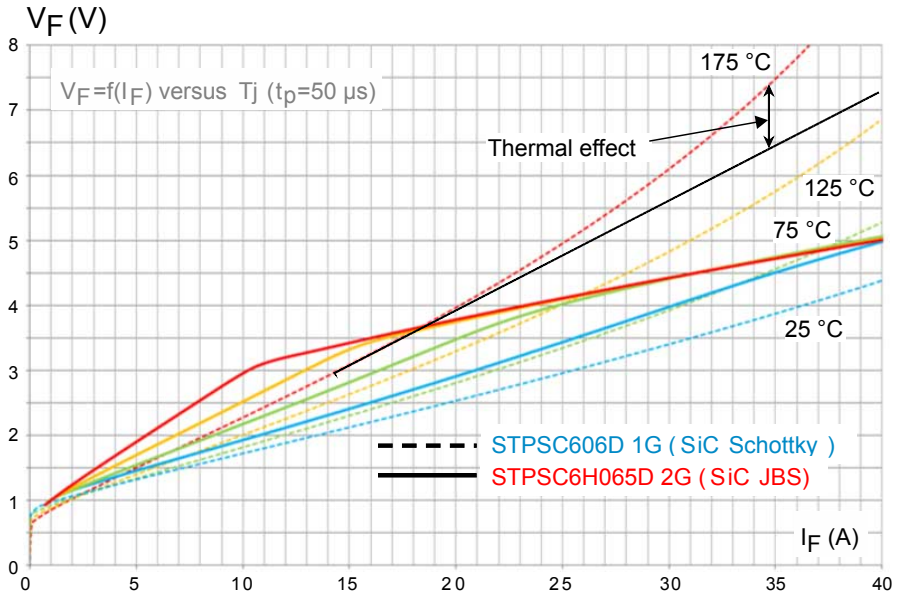
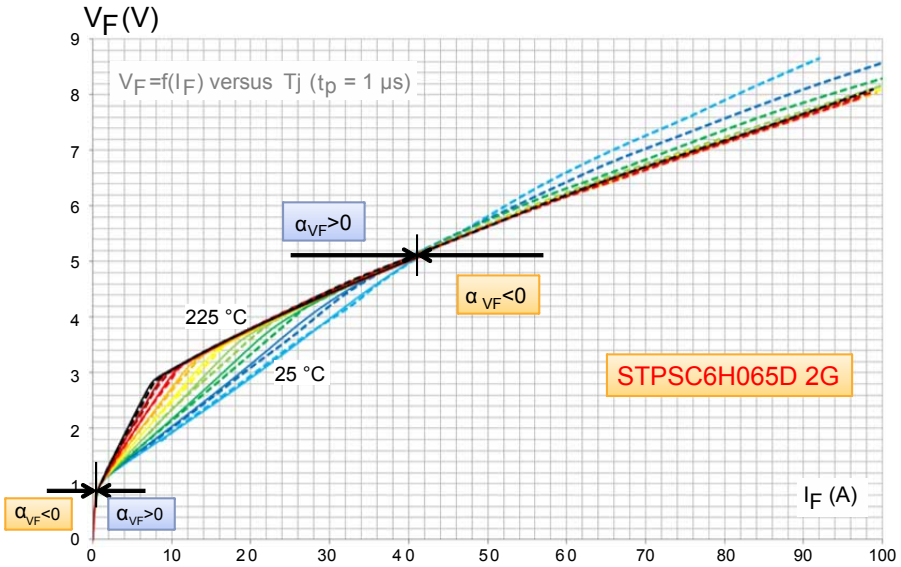


Figure 11. shows the characterization of the 2nd generation SiC diode up to 100 A with a pulse duration t_p = 1 µs. This network of curves highlights two crossing points. First, αV_F is negative below 1.5 A, then positive up to around 42 A, then once again negative. When the merged PN junction is biased, at high T_j (>125 °C) all the curves converge to one straight line giving a forward characteristics almost independent of the temperature.

Figure 11. Forward voltage characteristic of JBS SiC diode up to 100 A with t_p = 1 µS



The JBS structure clamps the forward voltage at high current and high T_j. This new technology thus avoids the thermal runaway phenomenon and the I_{FSM} value can go up to 9 or 10 times the nominal current rating.

3.2.2 I_{FSM} PSpice simulation: comparison between 1st and 2nd generation

The electro-thermal model simulates the variation of the forward voltage drop during a current spike and gives an estimate of the junction temperature. The electro-thermal model of a 2nd generation 6 A SiC diode is given in Figure 12.. The model is composed of an electrical model based on the typical forward characteristics shown in Figure 11. and a thermal model based on the typical transient thermal impedance junction-to-case curve given in the datasheet.

Figure 12. Electro-thermal model of the 6 A /650 V SiC G2 (STPSC6H065D) from STMicroelectronics

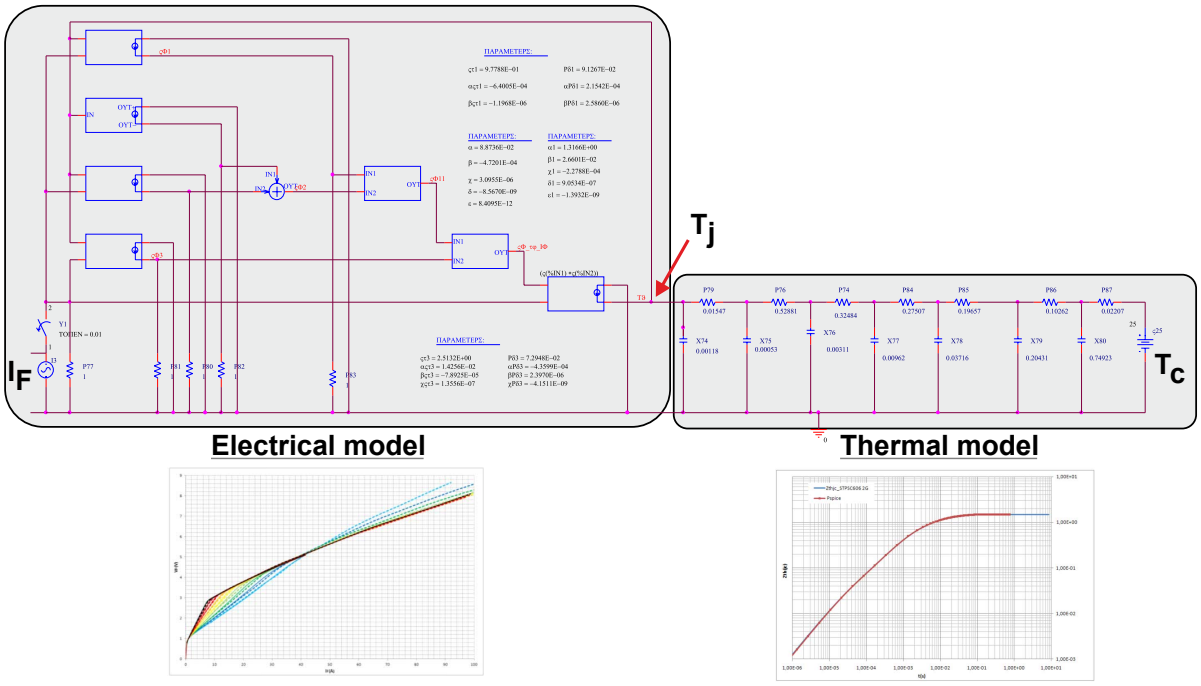
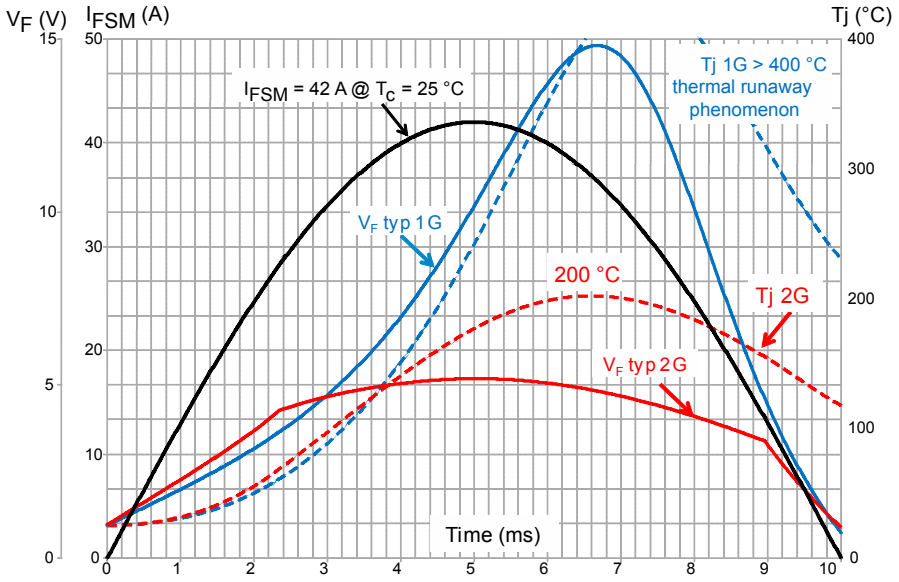


Figure 13. shows the result of a PSpice simulation for an I_{FSM} value of 42 A. With such a surge current, thermal instability is reached with the 1st generation device. The forward voltage drop and the junction temperature increase exponentially until the diode is destroyed. With the 2nd generation device, the JBS effect clamps the forward voltage drop and limits the increase of junction temperature.

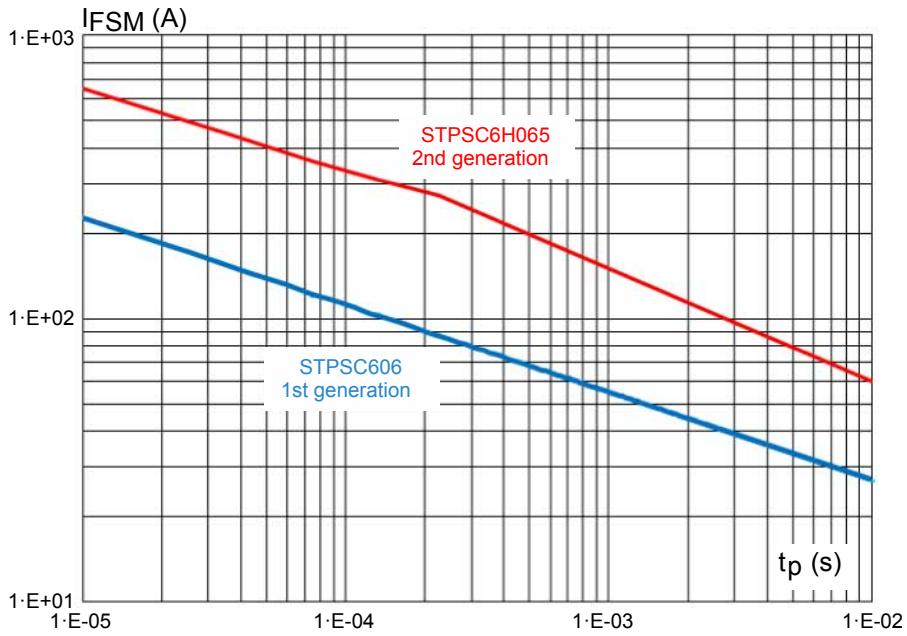
Figure 13. **Result of I_{FSM} PSpice simulation: comparison between 6 A / 650 V SiC 2nd generation (STPSC6H065D) and 6 A /600 V SiC 1st generation (STPSC606D)**



3.2.3 I_{FSM} datasheet comparison between SiC G2 and SiC G1

The non-repetitive IFSM curves versus pulse duration presented in Figure 14. come from the datasheet of the STPSC606 and the STPSC6H065. The graph, based on measurements, shows the improvement of the surge current capability with the second generation. Thanks to the JBS structure, the I_{FSM} values are more than doubled.

Figure 14. **Non repetitive I_{FSM} versus t_p comparison between 6 A SiC 1st generation and 6 A SiC 2nd generation**



Current stresses in the range of tens of microseconds are usually linked to the switching period. Such a surge current can also happen during lightning surge tests. Stresses in the range of tens of milliseconds are usually related to line-dropout tests.

Table 3. I_{FSM} with t_p = 10 ms and T_j = 25°C: comparison between first and second generation

I_{FSM}, sinusoidal, 10 ms, at 25 °C				
I_F (A)	4	6	8	10
SiC 1st generation	14	27	30	40
SiC 2nd generation	38	60	75	90

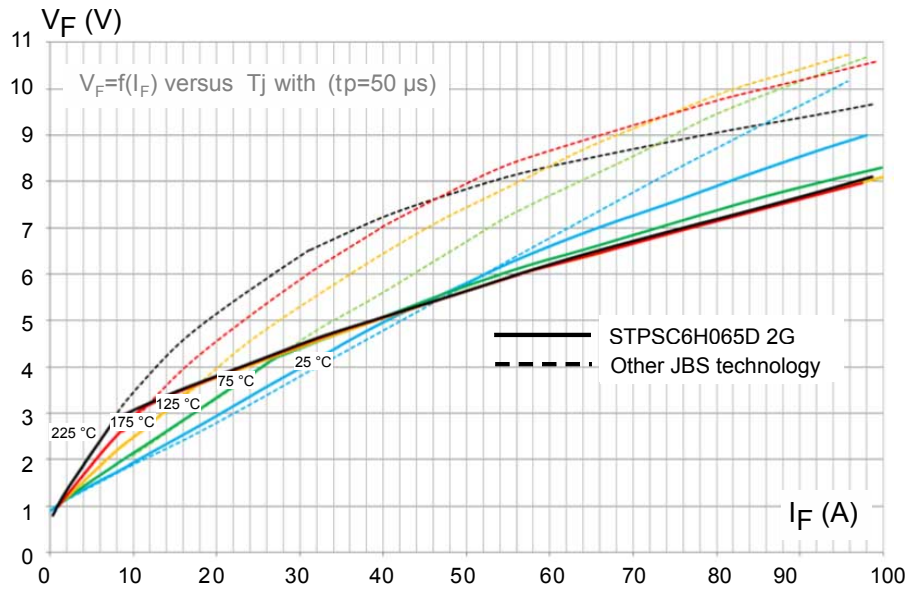
3.3 JBS structure trade-off: current surge capability versus Q_{rr}

The efficiency of the JBS structure to sustain a current spike is linked to the bias current level of the merged PN junction. This level characterizes “the JBS positioning”. Designing the diode with a higher bias current level leads to a higher forward voltage drop, and hence a higher T_j for the same surge. Likewise, the lower the bias current level, the lower the forward voltage drop at high current. However, the conduction of a PN junction implies some recovery charges (Q_{rr}) when the diode switches and turns off. This is linked to the minority carriers’ recombination, which does not happen in a conventional SiC Schottky structure. As a consequence, a trade off between I_{FSM} and Q_{rr} should be considered.

3.3.1 Forward characteristics comparison between ST’S SiC 2nd generation and other JBS designs

Figure 15. illustrates in dotted lines another dimensioning of the merged PN junction compared with ST’s design. The dotted lines present forward voltage drops around 2 volts higher than ST’s diode between 30 A and 70 A at 225 °C. On the other hand, this characteristic indicates that the carrier injection phenomenon (Qrr) should appear at higher forward current levels.

Figure 15. Forward voltage drop between STPSC6H065D and another JBS structure

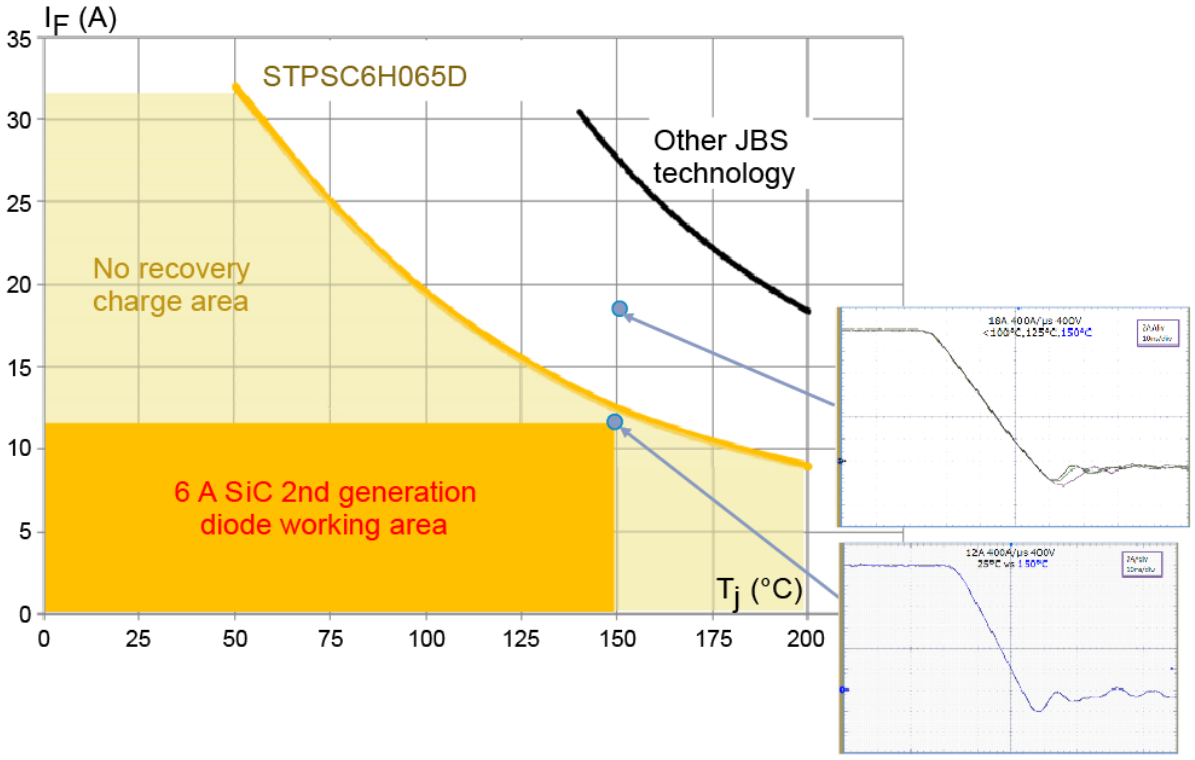


The characterization of the recovery charges for a given junction temperature versus the forward current allows the determination of the no recovery charges area.

3.3.2 No recovery charge area

Figure 16. illustrates the no-recovery-charges area for a 6 A SiC 2nd generation diode in the reference plan of forward current versus junction temperature. ST's STPSC6H065D SiC G2 was designed to be used without any recovery charges up to 2 x $I_{F(AV)}$ at 150 °C or again 3 x $I_{F(AV)}$ at 100°C. The 2 oscilloscope traces illustrate the switch-off behavior of the diodes at I_F = 12 A and I_F = 18 A for T_j = 150 °C. At I_F = 12 A, the behavior at 25°C and 150°C is stable confirming the absence of recovery charges. At I_F = 18 A, recovery charges start to appear between 100 °C and 125 °C and become more significant at 150 °C. The same characterization was made on a sample of diodes featuring another JBS technology (corresponding to the dotted lines in Figure 15.). This other JBS trade-off presents a larger no-recovery-charge area but compromises on the forward voltage drop, that is higher at high current levels.

Figure 16. Comparison of no recovery charge area between ST's 6 A SiC 2nd generation diode and another JBS technology



In a PFC, the peak current flowing through the diode can be estimated by:

$$I_{peak_{diode}} = \frac{\sqrt{2} \times P_{out}}{V_{in(\min)_{rms}} \times \eta} \quad (27)$$

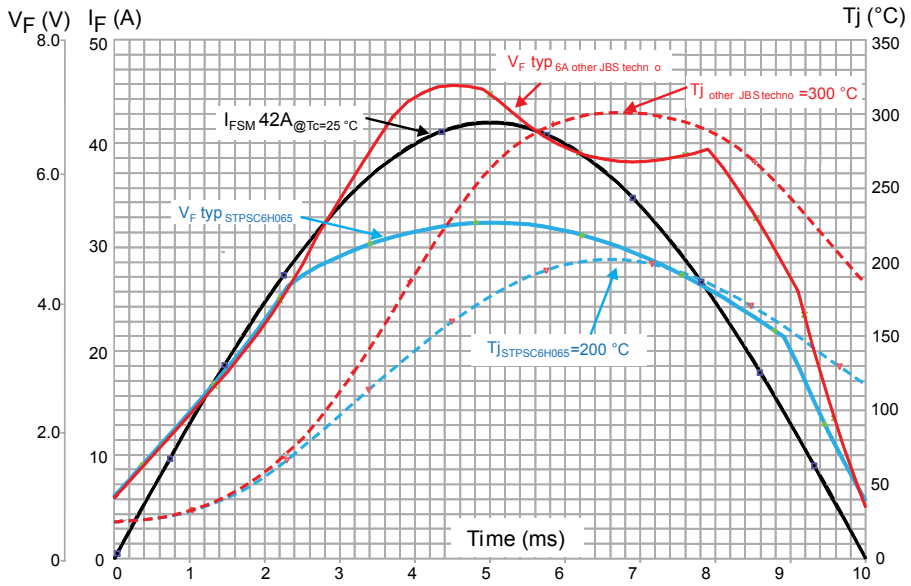
For example, in an 800 W server application with a PFC working at $V_{in(min)}$ = 90 V AC and an efficiency of 90%, the peak current reaches 14 A (it's the same for a 1600 W PFC application working at 180 V AC). In this application the choice of a 6 A SiC G2 working with a T_j around 125 °C is adapted.

3.3.3 PSpice electro-thermal simulation result

The interest of the dimensioning of the ST's JBS structure compared to another JBS positioning can clearly be highlighted with the electro-thermal simulation. Figure 17. and Figure 18. present the result of the PSpice simulation respectively for an IFSM waveform and a startup phase in a PFC application. The electrical model of the STPSC6H065D is compared to one of the other 6 A JBS technologies coupled with a thermal model similar to the one of the STPSC6H065D.

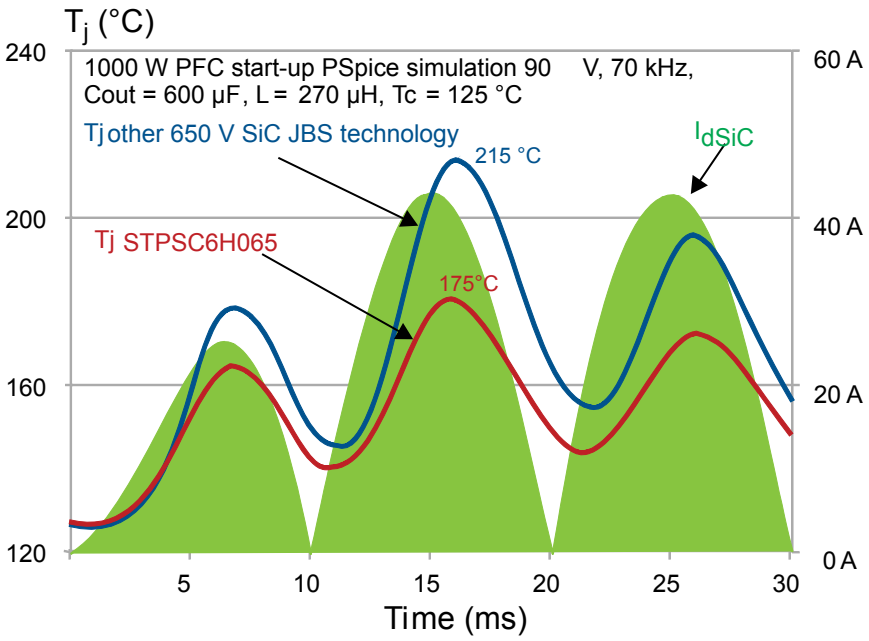
Figure 17. shows that the higher values of the forward characteristic of the other JBS technology in Figure 15. lead to a much higher Tj (+ 100°C) compared to ST's product during a 42 A IFSM spike.

Figure 17. I_{FSM} electro-thermal simulation with Tj comparison between ST's 6 A SiC G2 and another 6 A JBS technology



A second electro-thermal simulation was done during an SMPS start-up phase Figure 18.. It demonstrates once again the interest of correctly dimensioning the JBS structure.

Figure 18. Electro-thermal simulation of a PFC start-up phase with T_j comparison between ST's 6 A SiC 2nd generation and another 6 A JBS technology



The lower T_j observed through the electro-thermal simulation on ST's JBS structure contributes to the robustness of the ST's product in the application.

4 Efficiency measurement

Table 4. summarizes the key parameters for the 1st and 2nd generation of SiC diodes. If the JBS structure improves the surge current capability, it degrades somewhat the values of forward voltage drop at low current level.

Table 4. Comparison of key parameters between first generation and second generation of SiC diodes

Product	V_{RRM} (V)	I_{FSM}, (A) sinusoidal, 10 ms	V_F (V) at 6 A, 25 °C typical / maximum	V_F (V) at 6 A, 150 °C typical / maximum
6 A SiC, 1st gen STPSC606D	600	27	1.4/1.7	1.6/2.1
6 A SiC, 2nd gen STPSC6H065D	650	60	1.56/1.75	1.98/2.5

In a typical PFC application, the efficiency will be affected by less than 0.1% between the 1st and 2nd generation. A first approximation demonstrated by the following equations shows that the efficiency difference in a PFC could be estimated by $\Delta V_F/V_{OUT}$.

$$\frac{P_{cond}}{P_{out}} = \frac{V_{t0} \times I_{av} + R_d \times I_{rms}^2}{V_{out} \times I_{out}} \quad (28)$$

with

$$I_{av} = I_{out} = \frac{P_{out}}{V_{out}} \quad (29)$$

and

$$I_{rms} = \frac{P_{out}}{V_{inpk} \times \eta} \times \sqrt{\frac{16 \times V_{inpk}}{3 \times \pi \times V_{out}}} \quad (30)$$

then

$$\frac{P_{cond}}{P_{out}} = \frac{V_{t0} + k \times I_{av} \times R_d}{V_{out}} = \frac{V_F(k \times I_{av})}{V_{out}} \quad (31)$$

with

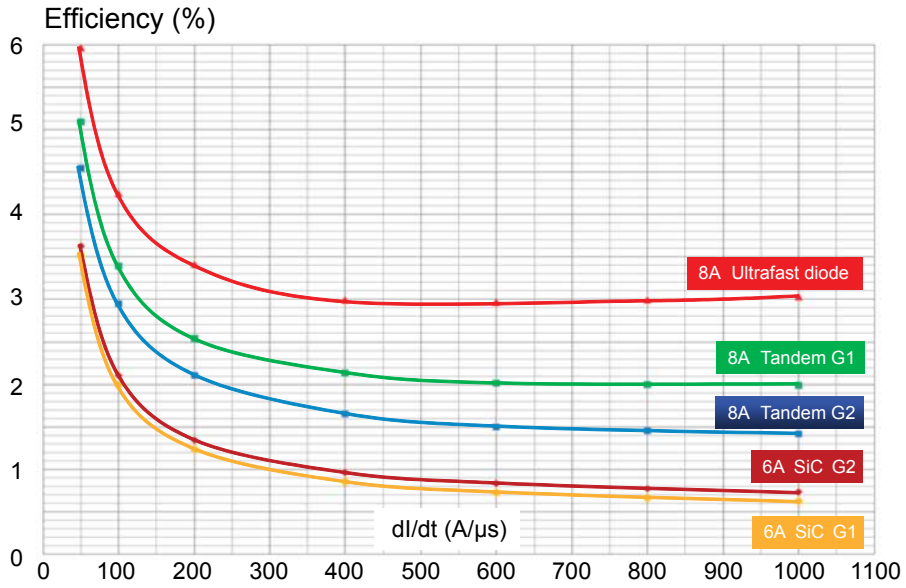
$$k = \frac{V_{out} \times 16}{3 \times \pi \times V_{inpk} \times \eta^2} \quad (32)$$

4.1 dI/dt optimization

The contribution of the SiC diode in the switching cell is essential. Its switching performance leads to new optimizations that can help to go a step forward in increasing the efficiency. It is well known that the MOSFET switching speed (dI/dt) is an important parameter to optimize the efficiency. The dI/dt slope (when the transistor turns on and when the diode turns off) can be easily changed by tuning the value of the gate resistor R_g of the transistor.

Figure 19. shows, the efficiency drop between SiC diodes and silicon diodes for different dI/dt slopes. This efficiency drop is defined by the total power losses due to the diode divided by P_{OUT}. The conduction power losses, the switch-off power losses in the diode and the switch-on power losses in the transistor due to the Q_{rr} of the silicon diodes are taken into account.

Figure 19. **Comparison of efficiency drop in a 500 W PFC with V_{IN} = 90 V F = 100 kHz, T_j = 125 °C**



With silicon bipolar rectifiers, there is an optimized dI/dt slope to reduce the power losses. When the slope increases, the switching time decreases but the reverse recovery current increases. For low dI/dt values, the impact of the switching time dominates, and for higher dI/dt the impact of Q_{rr} may become more important. Hence, the switching power losses due to the recovery charges (Q_{rr}) decrease with the increase of dI/dt until a certain point from which they start to increase again due to Q_{rr}. For those silicon diodes, the slope choice must also be made taking into account electromagnetic considerations (EMC) which sometimes impose a limitation of that slope.

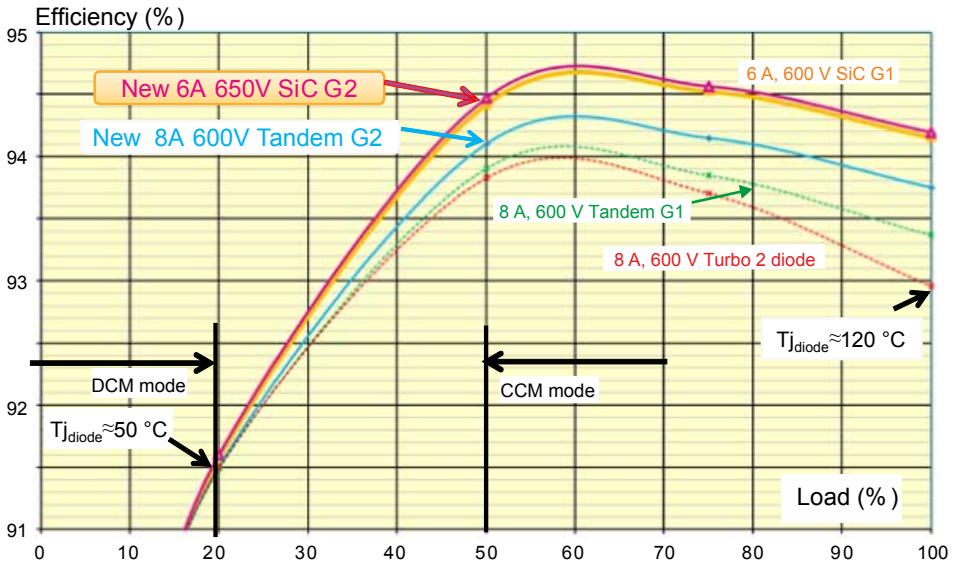
With SiC diodes, the power losses continue to decrease whenever dI/dt increases. Being naturally soft (due to capacitive nature of the recovery current), they offer the possibility to switch the transistor more quickly and thus increase the efficiency of the converter.

4.2 Example of efficiency measurements

Compared to the conventional ultrafast diode, using SiC diodes we can expect, an efficiency gain of between 1% and 2%.

An example of efficiency measurements in a 480 W PFC at V_{IN} = 115 V AC is presented in Figure 20.. The efficiency gain with the SiC diode compared to the conventional 600 V silicon diodes reaches 1.2%.

Figure 20. Typical efficiency measurement in a 480 W PFC at V_{IN} = 115 V, F_{sw} = 100 kHz, dI/dt = 600 A/µs



5 Conclusion

To keep its leadership in power rectifiers, ST developed a complete portfolio of silicon carbide diodes that are more and more popular in power converters thanks to their very high switching performance.

To help designers in their quest for more current density and helping them to reduce cost, STMicroelectronics developed a second generation of SiC Schottky rectifiers. The design of these new diodes provides increased robustness while not impacting their performance and blocks the effect of the positive thermal coefficient of the silicon carbide material. These new diodes have already proven to be very efficient in high-power SMPS.

To help designers reduce their time to market, STMicroelectronics developed a complete electro-thermal model of the diode. Combined with a model of the electrical circuit in which the SiC rectifier is used, the model can simulate all the worst case conditions of the transient phases of the power-supply. This way, power-supply designers can verify that the diode is completely safe in all conditions.

Supporting a wide range of applications, ST's SiC rectifiers are available in a variety of supported currents and packages, giving more flexibility on the power density/power dissipation trade-off.

Revision history

Table 5. **Document revision history**

Date	Version	Changes
30-May-2013	1	Initial release.
12-Jul-2018	2	Updated Section 4 .

Contents