AN4260
Application note

12 V, 150 mA non-isolated buck converter using the VIPER06XS, from the VIPer™ plus family

Introduction

This document describes the STEVAL-ISA115V1, a 12 V, 0.13 A power supply set in buck topology with the VIPer06XS, a new offline high voltage converter by STMicroelectronics, specifically developed for non-isolated SMPS.

The features of the device are:

- 800 V avalanche rugged power section
- PWM operation at 30 kHz with frequency jittering for lower EMI
- Limiting current with adjustable set point
- On-board soft-start
- Safe auto-restart after a fault condition and low standby power consumption

The available protection includes: thermal shutdown with hysteresis, delayed overload protection and open loop failure protection. All protection is auto-restart mode.

Figure 1. STEVAL- ISA115V1 product evaluation board

GIPG2305140928LM

Contents

List of figures

1 Adapter features

The electrical specifications of the evaluation board are listed in *Table 1*.

Table 1. Electrical specifications

Parameter	Symbol	Value
Input voltage range	V_{IN}	[90 V_{AC}; 265 V_{AC}]
Output voltage	V_{OUT}	12 V
Max. output current	I_{OUT}	0.15 A
Precision of output regulation	ΔV_{OUT_LF}	±5%
High frequency output voltage ripple	ΔV_{OUT_HF}	50 mV
Max. ambient operating temperature	T_{AMB}	60 °C

2 Circuit description

The converter schematic is given in *Figure 2*. The input section includes a resistor R1 for inrush current limiting, a diode D1 and a Pi filter (C1, L1, C2) for rectification and EMC suppression.

The FB pin is the inverting input of the internal transconductance error amplifier, internally referenced to 3.3 V. This allows the output voltage value to be set in a simple way through the R4-R5 voltage divider between the output terminal and the FB pin, according to the following equation:

Equation 1

$$V_{OUT} = 3.3V \cdot \left(1 + \frac{R5}{R4}\right)$$

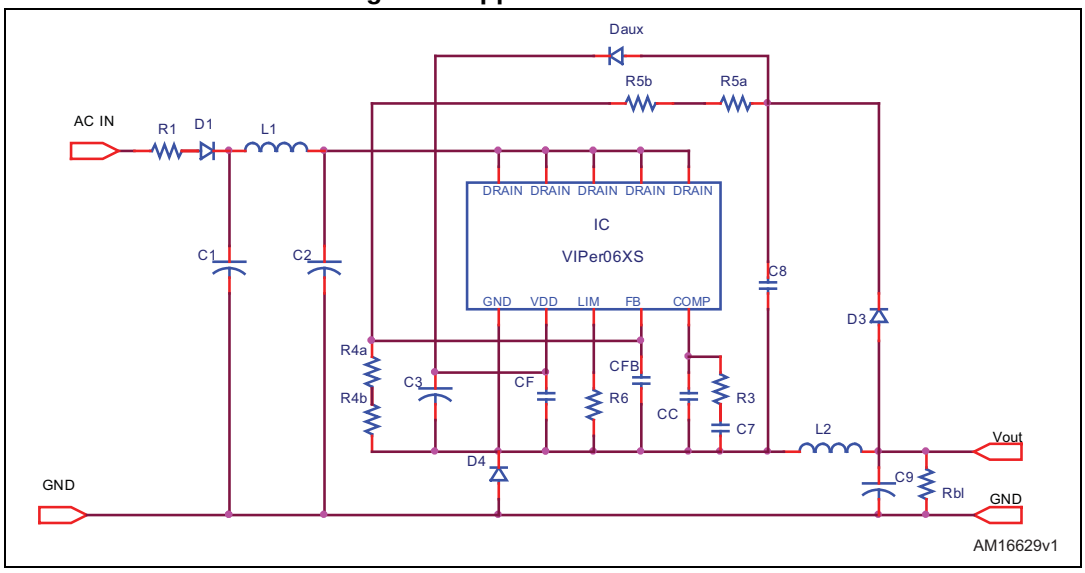
where R4 has been split into R4a and R4b; and R5 into R5a and R5b so to allow a better tuning of the output voltage value.

The compensation network is connected between the COMP pin (which is the output of the error amplifier) and the GND pin and is made up of Cc, R3 and C7.

The bleeder resistor Rbl provides about 1 mA minimum load, in order to avoid overvoltage when the output load is disconnected. Its value is a trade-off between output voltage increase and power consumption rise in no load.

At power-up the DRAIN pin supplies the internal HV startup current generator which charges the C3 capacitor up to V_{DDon} (13 V typical). At this point, the power MOSFET starts switching, the generator is turned off and the IC is powered by the energy stored in C3, waiting for V_{OUT} reaches its steady-state value. After that, the IC is supplied from the output through the diode Daux. This allows the system to reach very low values of standby consumption because, keeping the V_{DD} voltage always above the V_{DDCSon} threshold, prevents the HV startup generator from being turned on.

Figure 2. Application schematic



3 Bill of material

Table 2. Bill of material

Name	Value	Description	Footprint	Manufacturer
C1	4.7 µF, 400 V	Electrolytic capacitor		Saxon
C2	4.7 µF, 400 V	Electrolytic capacitor		Saxon
C3	2.2 µF, 25 V	Ceramic capacitor	SMD: 0805	Murata
CFB	n.c	Ceramic capacitor	SMD: 0805	
Cf	100 nF, 50 V	Ceramic capacitor	SMD: 0805	Murata
CC	n.c	Ceramic capacitor	SMD: 0805	
C7	22 nF, 25 V	Ceramic capacitor	SMD: 0805	Murata
C8	150 nF, 50 V	Ceramic capacitor	SMD: 0805	Murata
C9	100 µF, 25 V	Electrolytic capacitor		Rubycon, ZL series
D1	1N4007	High voltage rectifier	DO-41	Fairchild
D3	STTH1L06	High voltage ultra fast rectifier	SMB (SOD87)	ST
D4	STTH1L06	High voltage ultra fast rectifier	SMB (SOD87)	ST
Daux	1N4148	100 V, 0.15 A fast switch diode	SOD-123	Zetex
IC	VIPer06XS	High voltage converter	SSO-10	ST
L1	1 mH	Input filter inductor	SMD	Epcos
L2	RFB0810-152	1.5 mH power inductor		Coilcraft
R1	22 ohm, 1%	1 W resistor	SMD 2010	Panasonic
R3	1.2 kohm, 1%	1/4 W resistor	SMD: 0805	Panasonic
R4a	12 kohm, 1%	1/4 W resistor	SMD: 0805	Panasonic
R4b	0 ohm	1/4 W resistor	SMD: 0805	
R5a	0 ohm	1/4 W resistor	SMD: 0805	
R5b	33 kohm, 1%	1/4 W resistor	SMD: 0805	Panasonic
R6	not mounted	1/4 W resistor	SMD: 0805	
Rbl	10 kohm, 1%	1/4 W resistor	SMD: 0805	Panasonic

4 Layout

Figure 3. Layout (top)

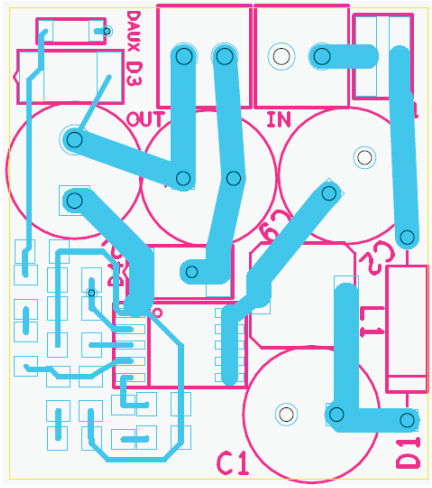
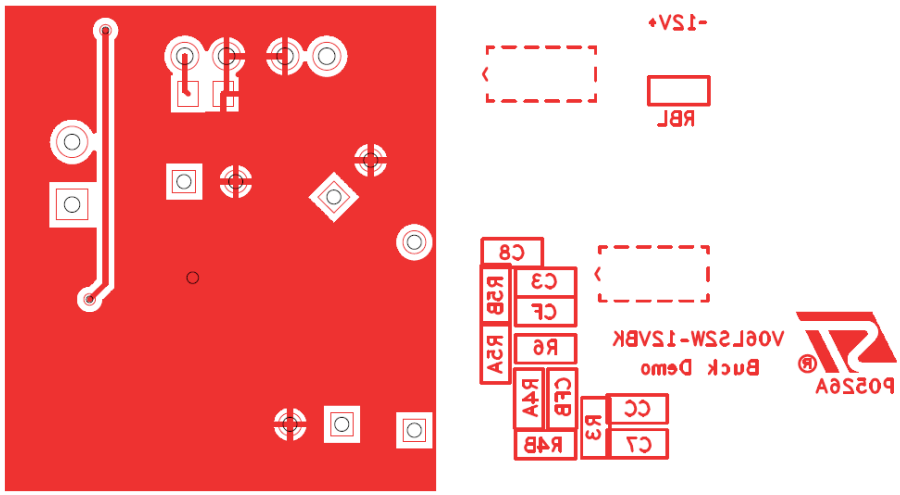


Figure 4. Layout (bottom)



5 Testing the board

5.1 Typical waveforms

GND voltage and the current across the inductor L2 (I_L2) in full load condition are shown for the two nominal input voltages in *Figure 5* and *Figure 6*, and for minimum and maximum input voltage in *Figure 7* and *Figure 8* respectively.

Figure 5. Waveforms at V_{IN} = 115 V_{AC}, full load

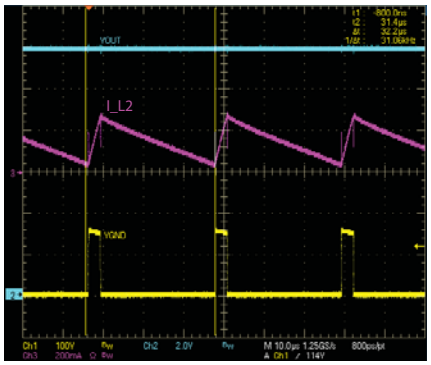


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Figure 6. Waveforms at V_{IN} = 230V_{AC}, full load

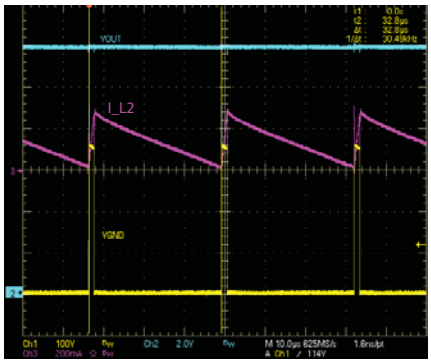

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Figure 7. Waveforms at V_{IN} = 80 V_{AC}, full load

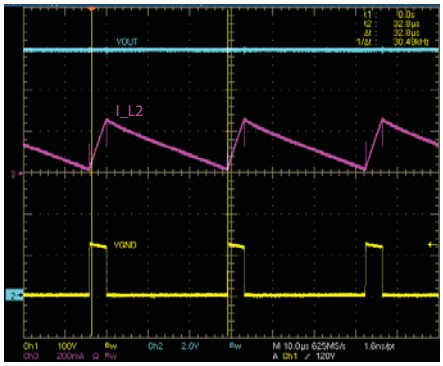

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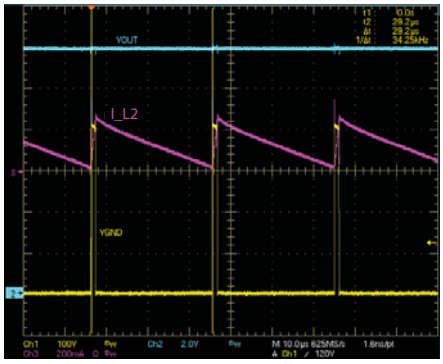
Figure 8. Waveforms at V_{IN} = 265 V_{AC}, full load



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5.2 Line/load regulation and output voltage ripple

The output voltage of the board has been measured in different lines and load conditions. The results are shown in *Figure 9* and *Figure 10*.

Figure 9. Line regulation

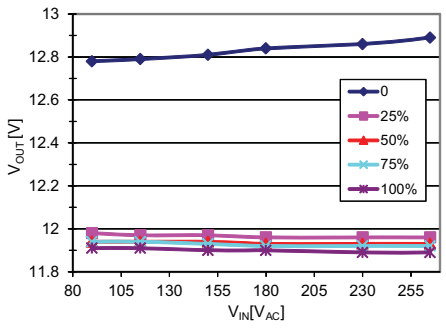

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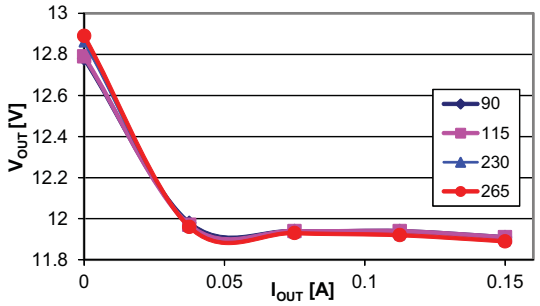
Figure 10. Load regulation



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The output voltage ripple in full load condition is shown in *Figure 11* at V_{IN} = 115 V_{AC} and in *Figure 12* at V_{IN} = 230 V_{AC}.

Figure 11. Output voltage ripple at 115 V_{AC}, full load

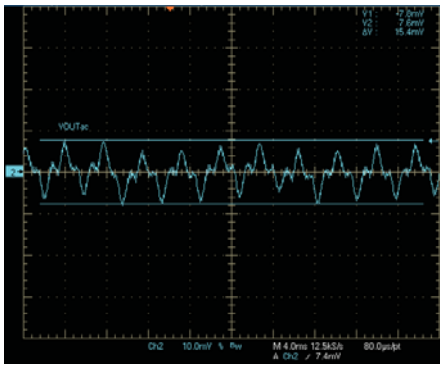

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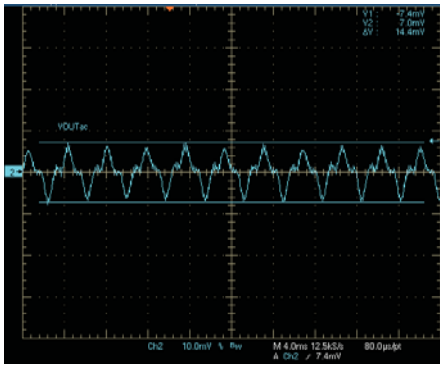
Figure 12. Output voltage ripple 230 V_{AC}, full load



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5.3 Burst mode and output voltage ripple

When the converter is lightly loaded, the COMP pin voltage decreases. As it reaches the shutdown threshold, V_{COMPL} (1.1 V, typical), the switching is disabled and no more energy is transferred to the secondary side. So, the output voltage decreases and the regulation loop makes the COMP pin voltage increase again. As it rises 40 mV above the V_{COMPL} threshold, the normal switching operation is resumed. This results in a controlled on/off operation (referred to as "burst mode") as long as the output power is so low that it requires a turn-on time lower than the minimum turn-on time of the VIPER06XS. This mode of operation keeps the frequency-related losses low when the load is very light or disconnected, making it easier to comply with energy saving regulations.

The figures below show the output voltage ripple when the converter is no/lightly loaded and supplied with 115 V_{AC} and with 230 V_{AC} respectively.

Figure 13. Output voltage ripple at 115 V_{AC}, no load

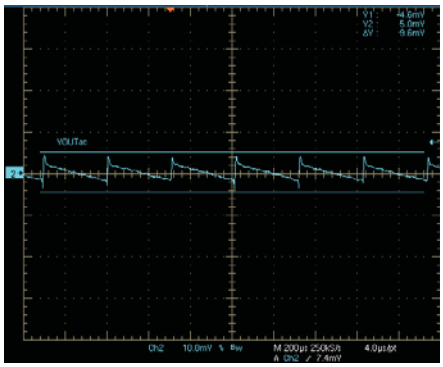

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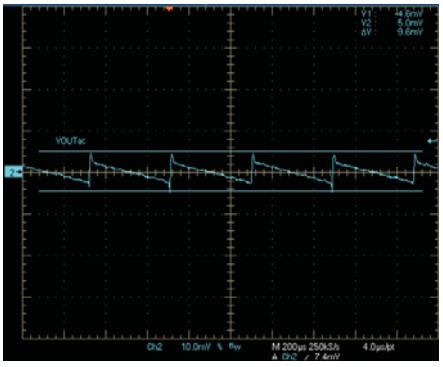
Figure 14. Output voltage ripple at 230 V_{AC}, no load



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5.4 Efficiency

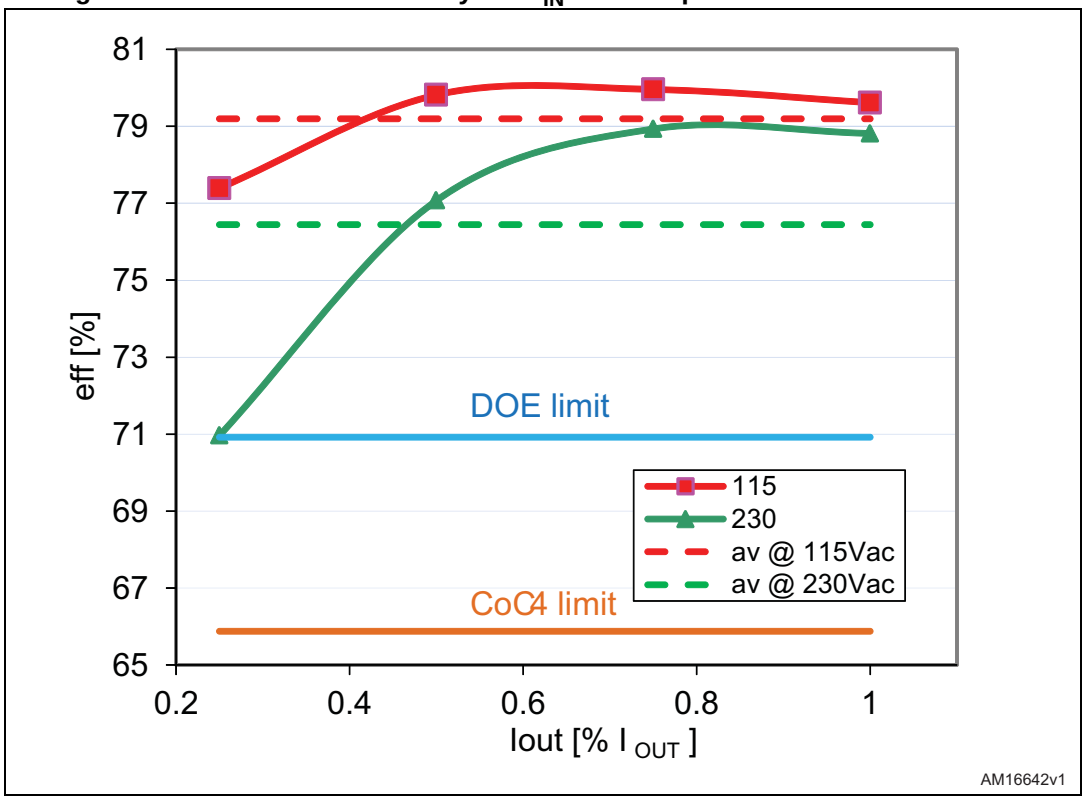
The active mode efficiency is defined as the average of the efficiencies measured at 25%, 50%, 75% and 100% of maximum load, at nominal input voltage (V_{IN} = 115 V_{AC} and V_{IN} = 230 V_{AC}).

External power supplies (the power supplies which are contained in a separate housing from the end-use devices they are powering) need to comply with the Code of Conduct, version 4 "Active Mode Efficiency" criterion, which states an active mode efficiency higher than 65.9% for a power throughput of 1.8 W.

Another standard to be applied to external power supplies in the coming years is the DOE (department of energy) recommendation, whose active mode efficiency requirement for the same power throughput is 70.9%.

The presented evaluation board is compliant with both standards, as per *Figure 15*, where the average efficiencies of the board at 115 V_{AC} (79.2%) and at 230 V_{AC} (76.4%) are plotted with dotted lines, together with the above limits. In the same figure the efficiency at 25%, 50%, 75% and 100% of load for both input voltages is also shown.

Figure 15. Active mode efficiency vs. V_{IN} and comparison with CoC4 and DOE



5.5 Light load performance

The input power of the converter has been measured in no load condition for different input voltages and results are reported in *Table 3*.

Table 3. No load input power

V_{IN} [V_{AC}]	P_{IN} [mW]
90	32
115	34
150	37
180	39
230	42
265	48

In version 4 of the Code of Conduct, the power consumption of the power supply when it is no loaded is also considered. The criteria to be compliant with are reported in *Table 4*:

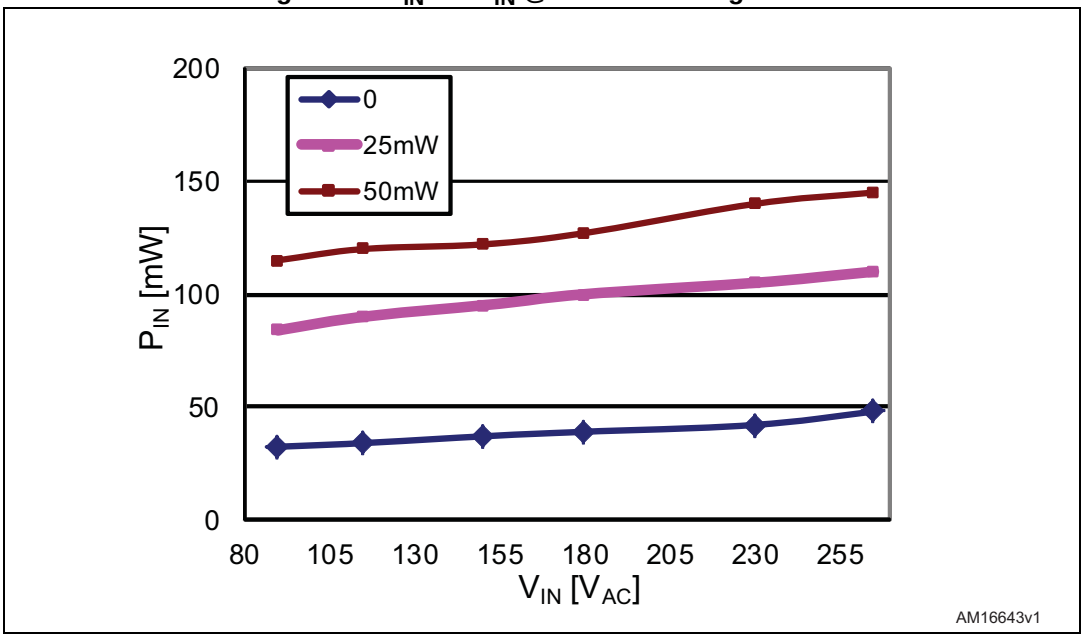
Table 4. Energy consumption criteria for no load

Nameplate output power	Maximum power in no load for AC-DC EPS
0 to ≤ 50 W	< 0.3 W
> 50 W < 250 W	< 0.5 W

The power consumption of the presented board is about six times lower than the limit fixed by version 4 of the Code of Conduct. Even though the performance seems to be disproportionally better than requirements, it is worth noting that often AC-DC adapter or battery charger manufacturers have very strict requirements about no load consumption and if the converter is used as an auxiliary power supply, the line filter is often the main line filter of the entire power supply that increases greatly the standby consumption.

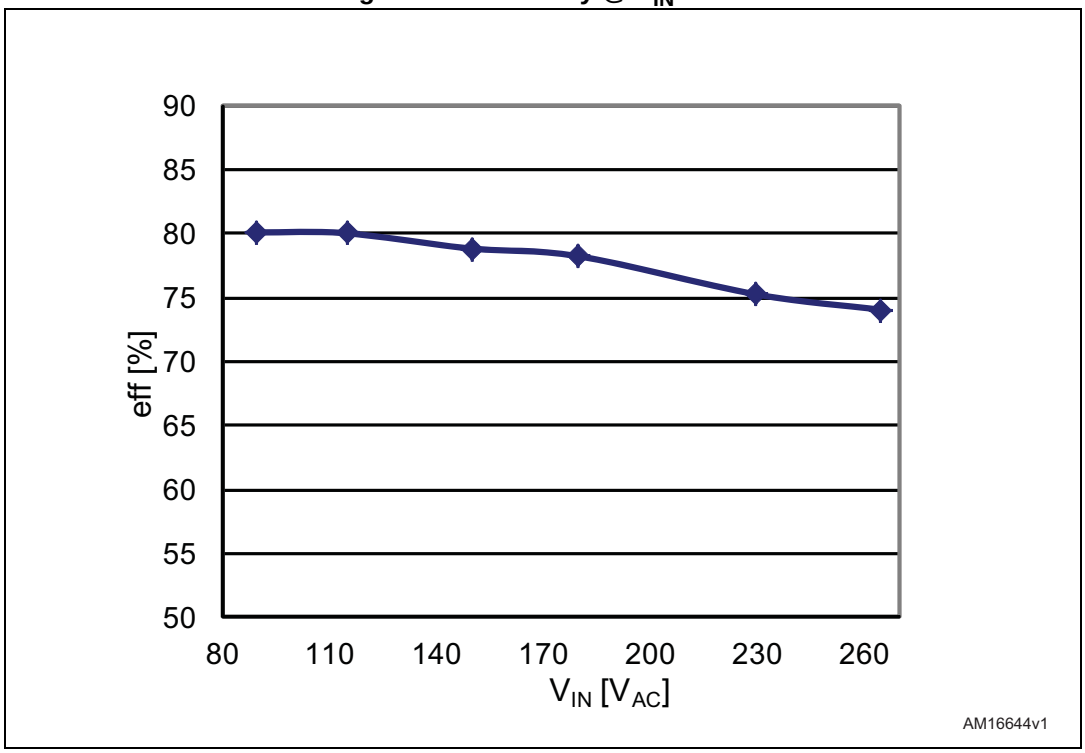
Even though version 4 of the Code of Conduct does not have other requirements regarding light load performance, in order to give a more complete overview, the consumption of the evaluation board in two other light load cases (P_{OUT} = 25 mW and P_{OUT} = 50 mW) has also been measured. The results versus line voltage are plotted in *Figure 16*, together with the no load measurements reported in *Table 3*.

Figure 16. P_{IN} vs. V_{IN} @ no load and light load



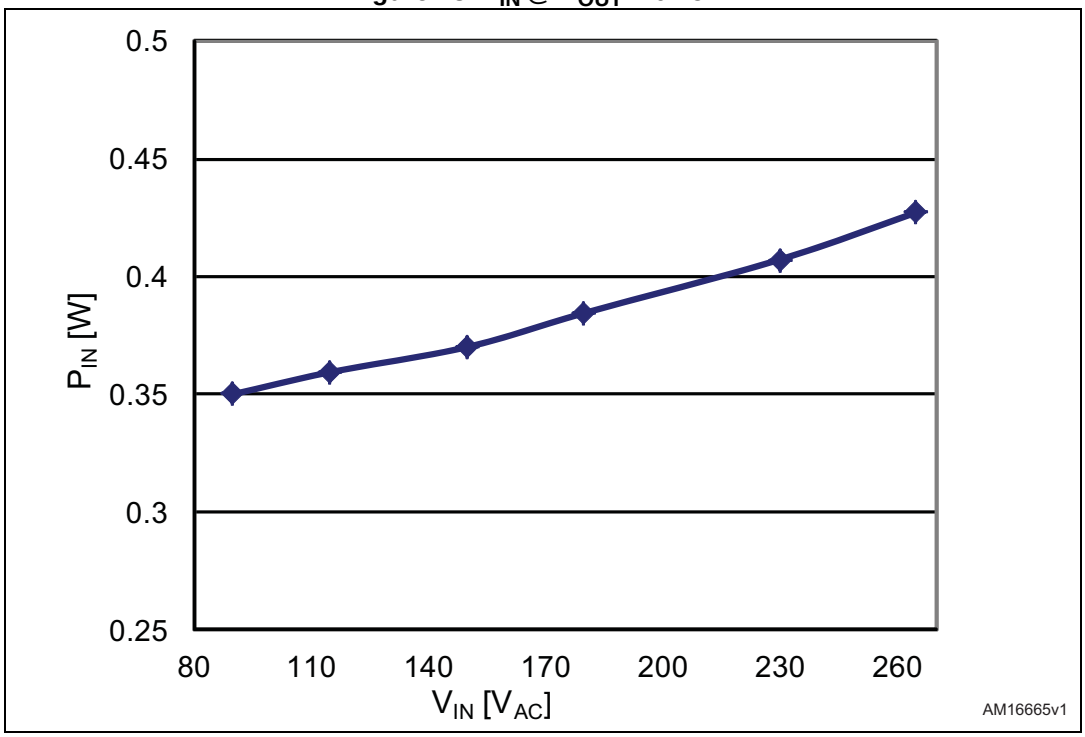
Several criteria can be adopted to measure the performance of a converter. One criterion is to measure the output power (or the efficiency) when the input power is equal to 1 Watt. This measurement is shown in *Figure 17* for different input voltage values.

Figure 17. Efficiency @ P_{IN} = 1 W



Another requirement for light load performance (EuP lot 6) is that the input power should be less than 500 mW when the converter is loaded 250 mW. The evaluation board satisfies this requirement, as shown in *Figure 18*.

Figure 18. P_{IN} @ P_{OUT} = 0.25 W



6 Functional check

6.1 Startup

The start-up phase at maximum load is shown in *Figure 19* and *Figure 21* at both nominal input voltages (115 V_{AC} and 230 V_{AC}).

Figure 19. Startup at V_{IN} = 115 V_{AC}, full load

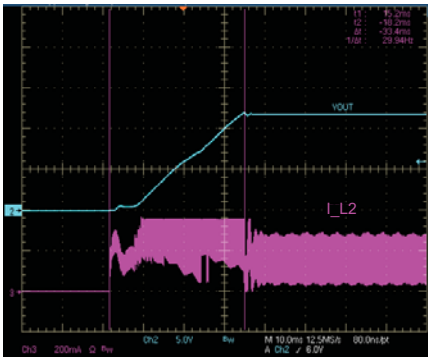


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Figure 20. Startup at V_{IN} = 115 V_{AC}, full load, zoom

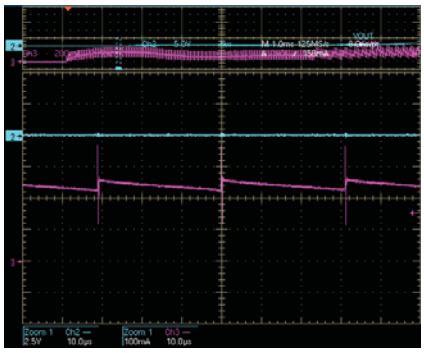

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Figure 21. Startup at V_{IN} = 230 V_{AC}, full load

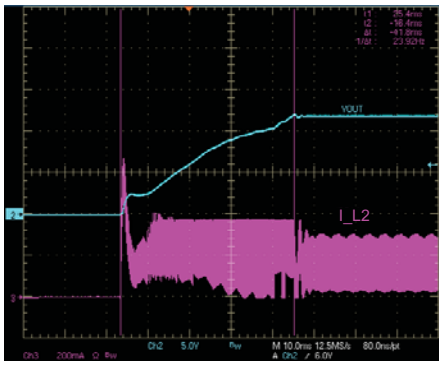

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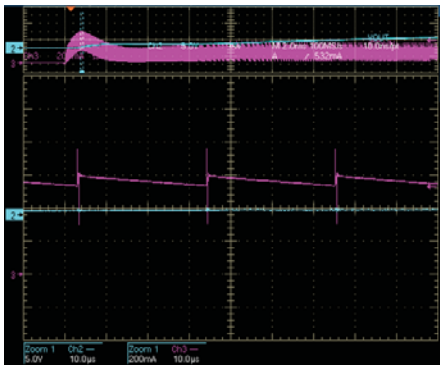
Figure 22. Startup at V_{IN} = 230 V_{AC}, full load, zoom



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6.2 Overload protection

In case of overload or short-circuit (see *Figure 23*), the drain current reaches the I_{DLIM} value (or the one set by the user through the RLIM resistor). In every cycle where this condition is met, a counter is incremented; if it is maintained continuously for the time t_{OVL} (50 msec typical, internally set) the overload protection is tripped, the power section is turned off and the converter is disabled for a $t_{RESTART}$ time (1 sec typical). After this time has elapsed, the IC resumes switching and, if the short is still present, the protection occurs indefinitely in the same way (*Figure 24*). This ensures restart attempts of the converter with low repetition rate, so that it works safely with extremely low power throughput and avoids the IC overheating in case of repeated overload events.

After the short removal, IC resumes working normally. If the short is removed during t_{SS} or t_{OVL}, before the protection tripping, the counter is decremented on a cycle-by-cycle basis down to zero and the protection is not tripped.

If the short-circuit is removed during $t_{RESTART}$, IC must wait for the $t_{RESTART}$ period to elapse before switching is resumed *Figure 26*.

Figure 23. Output short-circuit applied: OLP tripping

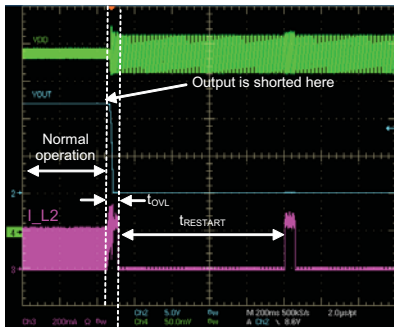

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Figure 24. Output short-circuit maintained: OLP steady-state

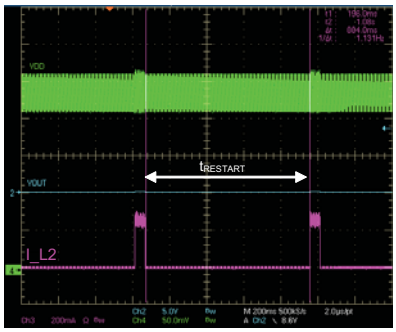

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Figure 25. Output short-circuit maintained: OLP steady-state (zoom)

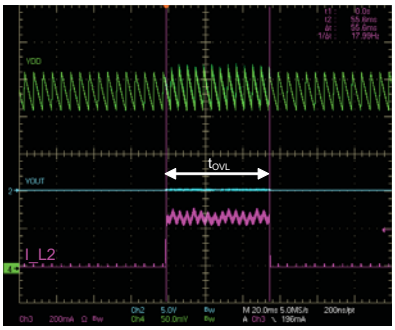

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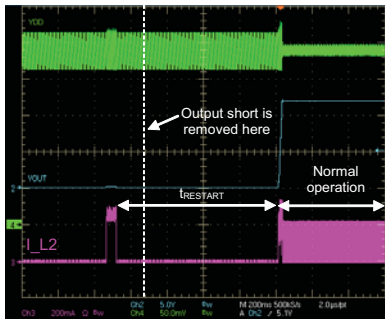
Figure 26. Output short-circuit removal and converter restart



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6.3 Feedback loop failure protection

This protection is available any time IC is externally biased. As the loop is broken (R4 shorted or R5 open), the output voltage V_{OUT} increases and the VIPER06XS runs at its maximum current limitation. VDD pin voltage increases as well, because it is linked to the V_{OUT} voltage through the Daux diode.

If the V_{DD} voltage reaches the V_{DD} clamp threshold (23.5 V min.) in less than 50 msec the IC is shut down by open loop failure protection (see *Figure 27* and *Figure 28*), otherwise by OLP, as described in the previous section. The breaking of the loop has been simulated by shorting the low-side resistor of the output voltage divider, R4 = R4a1+R4b. The same behavior can be induced opening the high-side resistor, R5 = R5a+R5b.

The protection acts in auto-restart mode with $t_{RESTART}$ = 1 sec (*Figure 28*). As the fault is removed, normal operation is restored after the last $t_{RESTART}$ interval has been completed (*Figure 30*).

Figure 27. Feedback loop failure protection: tripping

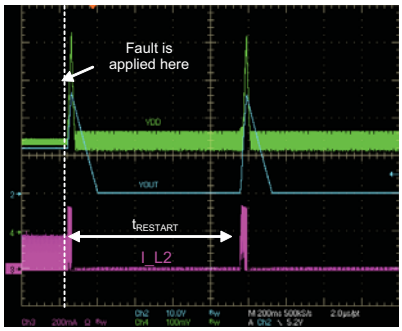

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Figure 28. Feedback loop failure protection: steady-state

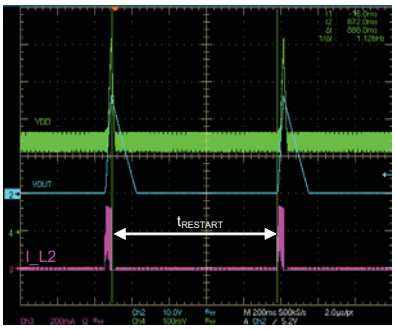

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Figure 29. Feedback loop failure protection: steady-state zoom

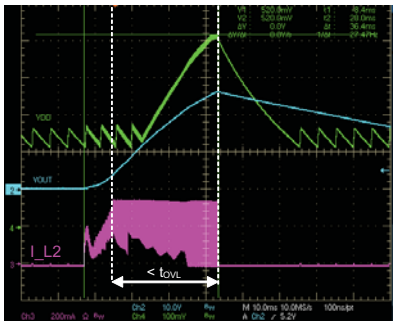

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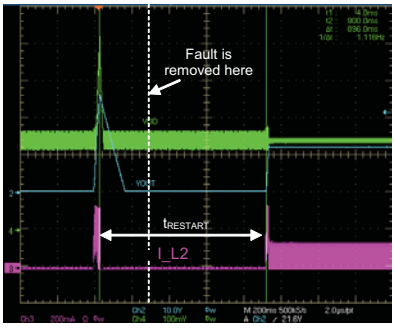
Figure 30. Feedback loop failure protection: converter restart



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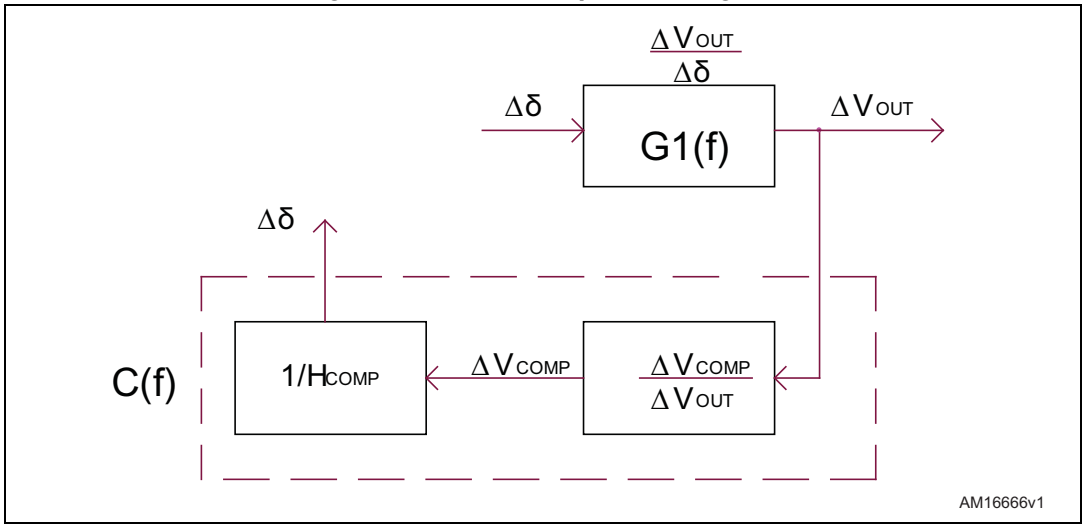
7 Feedback loop calculation guidelines

7.1 Transfer function

The set PWM modulator + power stage is indicated with G1(f), while C(f) is the "controller", the network in charge to assure the stability of the system.

Figure 31. Control loop block diagram



The mathematical expression of the power plant G1(f) in DCM is the following:

Equation 2

$$G1(f) = \frac{\Delta V_{OUT}}{\Delta \partial} = G10 \cdot \frac{1 + \frac{j \cdot f}{fz}}{1 + \frac{j \cdot f}{fp}}$$

where fz is the zero due to the ESR of the output capacitor:

Equation 3

$$fz = \frac{1}{2 \cdot \pi \cdot C_{OUT} \cdot ESR}$$

and fp is the pole due to the output load

Equation 4

$$fp = \frac{1 + \beta \cdot R_{OUT}}{2 \cdot \pi \cdot C_{OUT} \cdot (ESR + R_{OUT} + ESR \cdot \beta \cdot R_{OUT})}$$

with:

Equation 5

$$\alpha = \frac{V_{IN} + V\gamma}{(V_{OUT} + V\gamma)} \cdot \frac{Ipk}{2}$$

Equation 6

$$\beta = \frac{V_{IN} + V\gamma}{(V_{OUT} + V\gamma)^2} \cdot \frac{Ipk}{2} \cdot \partial$$

Equation 7

$$G10 = \frac{\alpha \cdot R_{OUT}}{1 + \beta \cdot R_{OUT}} = \frac{(V_{OUT} + V\gamma) \cdot (V_{IN} + V\gamma) \cdot \frac{Ipk}{2} \cdot R_{OUT}}{(V_{OUT} + V\gamma)^2 \cdot (V_{IN} + V\gamma) \cdot \frac{Ipk}{2}\partial \cdot R_{OUT}}$$

In the above formulas, C_{OUT} and ESR are the capacitance and the equivalent series resistance of the output capacitor respectively, Vy is the forward drop of the free-wheeling diode, $R_{OUT} = V_{OUT}/I_{OUT}$ is the output load, Ipk is the drain peak current at full load and ∂ = Ton*fsw is the duty cycle.

If just an RC series between COMP and GND is chosen as a compensation network, as shown in *Figure 2* (in fact Cc and CFB are not mounted), the mathematical expression of the compensator C(f) is:

Equation 8

$$C(s) = \frac{C_0}{H_{COMP}} \cdot \frac{\left(1 + \frac{j \cdot f}{fzc}\right)}{j \cdot 2 \cdot \pi \cdot f}$$

where:

Equation 9

$$C_0 = \frac{L \cdot fsw}{V_{IN} - V_{OUT}} \cdot \left(\frac{|-Gm|}{C7}\right) \cdot \frac{R4}{R4 + R5}$$

and:

Equation 10

$$fzc = \frac{1}{2 \cdot \pi \cdot R3 \cdot C7}$$

they are chosen in order to ensure the stability of the overall system.

The values of $H_{COMP} = \delta V_{COMP}/\delta I_{COMP}$ and of Gm (error amplifier transconductance) are specified in the VIPER06 datasheet.

7.2 Compensation procedure for a DCM buck

The first step is to choose the pole and zero of the compensator and the crossing frequency.

In this case C(f) has only a zero (fzc) and a pole at the origin, thus a possible setting is:

- fzc = k*fp
- fcross = fcross_sel_≤ fsw /10

where k is chosen arbitrarily. A starting point could be k = 5

After selecting fcross_sel, G1(fcross_sel) can be calculated from *Equation 2* and, since by definition it is $|C(fcross\_sel)*G1(fcross\_sel)| = 1$, C_0 can be calculated as follows:

Equation 11

$$C_0 = \frac{|j \cdot 2 \cdot \pi \cdot fcross\_sel|}{\left|1 + \frac{j \cdot fcross\_sel}{fzc}\right|} \cdot \frac{H_{COMP}}{|G1(fcross\_sel)|}$$

At this point the Bode diagram of G1(f)*C(f) can be plotted, in order to check the phase margin for the stability.

If the margin is not high enough, another choice should be made for k and fcross_sel, and the procedure is repeated.

When the stability is ensured, the next step is to find the values of the schematic components, which can be calculated as follows:

from *Equation 9*

Equation 12

$$C7 = \frac{L \cdot fsw}{V_{IN} - V_{OUT}} \cdot \left(\frac{|-Gm|}{C_0}\right) \cdot \frac{R4}{R4 + R5}$$

and from *Equation 10*

Equation 13

$$R3 = \frac{1}{2 \cdot \pi \cdot fzc \cdot C7}$$

Quantities found in *Equation 12* and *Equation 13* are suggested values. Commercial values are chosen, let us call them C7_act, R7_act, resulting into fzc_act.

Equation 14

$$fzc\_act = \frac{1}{2 \cdot \pi \cdot R3\_act \cdot C7\_act}$$

C_0 value is also recalculated from *Equation 9*

Equation 15

$$C_0\_act = \frac{L \cdot fsw}{V_{IN} - V_{OUT}} \cdot \left(\frac{|-Gm|}{C7\_act}\right) \cdot \frac{R4\_act}{R4\_act + R5(4)\_act}$$

and the compensator becomes:

Equation 16

$$C\_act(f) = \frac{C_{0\_act}}{H_{COMP}} \cdot \frac{\left(1 + \frac{f}{fzc\_act}\right)}{j \cdot 2 \cdot \pi \cdot f}$$

At this point the Bode diagram of G1(f)*C_act(f) should be plotted, and check if the phase margin for the stability is maintained.

8 Thermal measurements

A thermal analysis of the evaluation board in full load condition at T_{AMB} = 25 °C has been performed using an IR camera. The results are shown in the following figures.

Figure 32. Thermal measurement @ V_{IN} = 80 V_{AC}, full load (130 mA) Rbl = 8.2 kohm

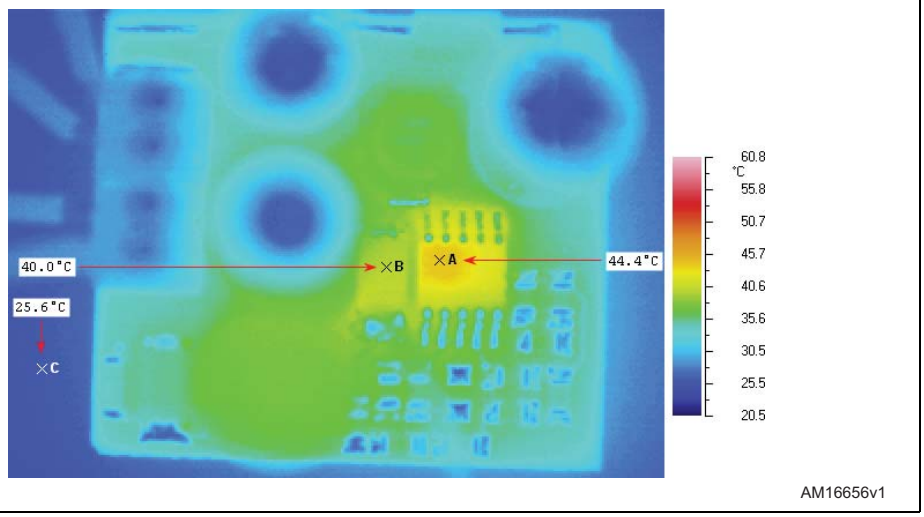


Figure 33. Thermal measurement @ V_{IN} = 115 V_{AC}, full load (130 mA) Rbl = 8.2 kohm

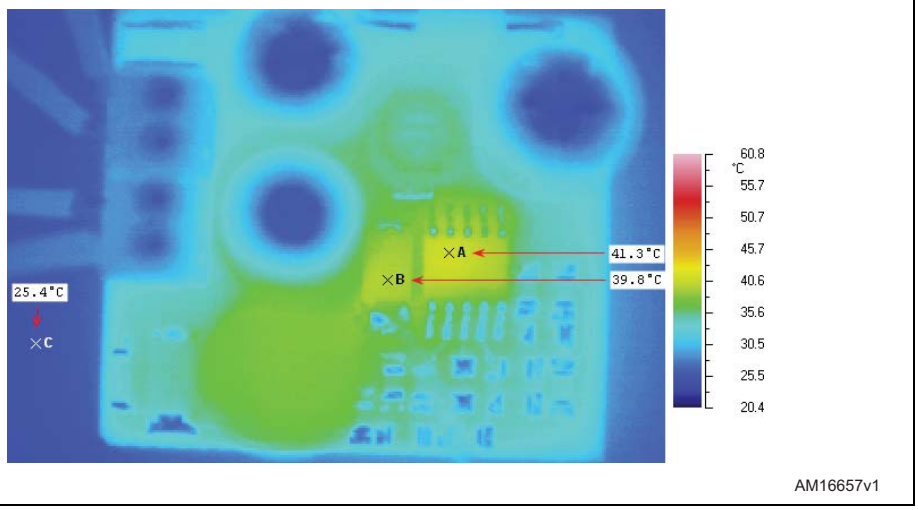


Figure 34. Thermal measurement @ V_{IN} = 230 V_{AC}, full load (130 mA) Rbl = 8.2 kohm

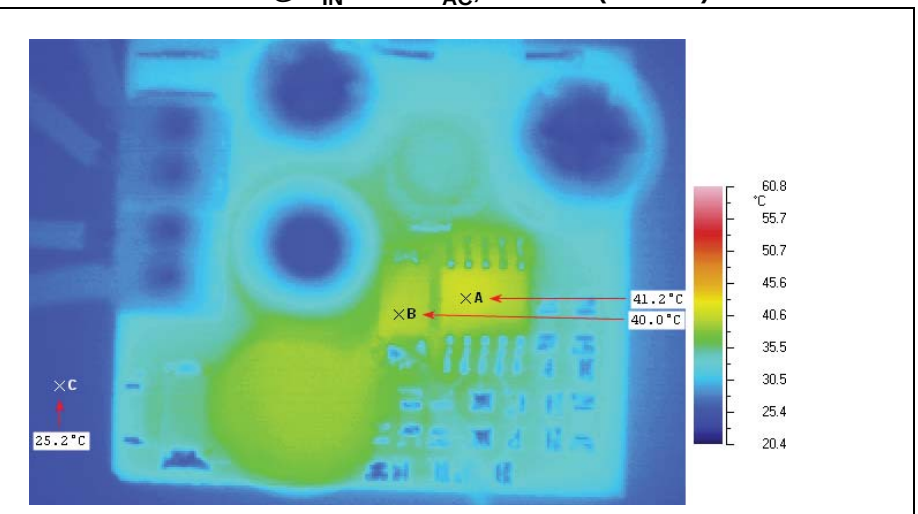
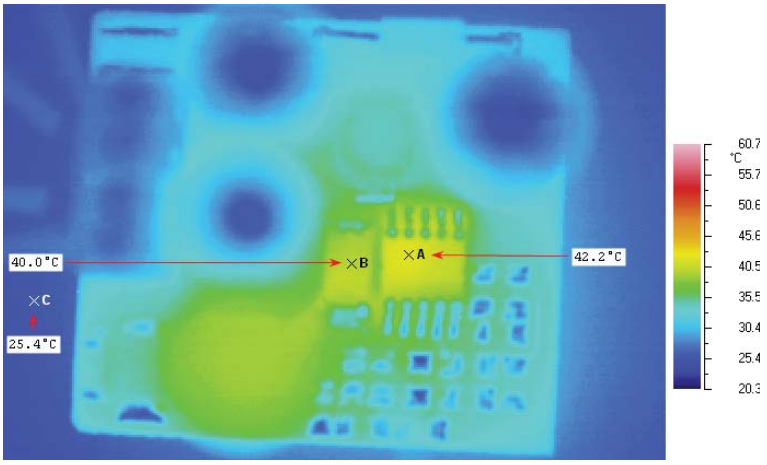


Figure 35. Thermal measurement @ V_{IN} = 265 V_{AC}, full load (130 mA) Rbl = 8.2 kohm



9 EMI measurements

A pre-compliant test of the EN55022 (Class B) European normative has been performed using an EMC analyzer and an LISN. The average EMC measurements at 115 V_{AC}/full load and 230 V_{AC}/full load have been performed and the results are shown in *Figure 36* and *Figure 37*.

Figure 36. Average measurement at full load, 115 V_{AC}

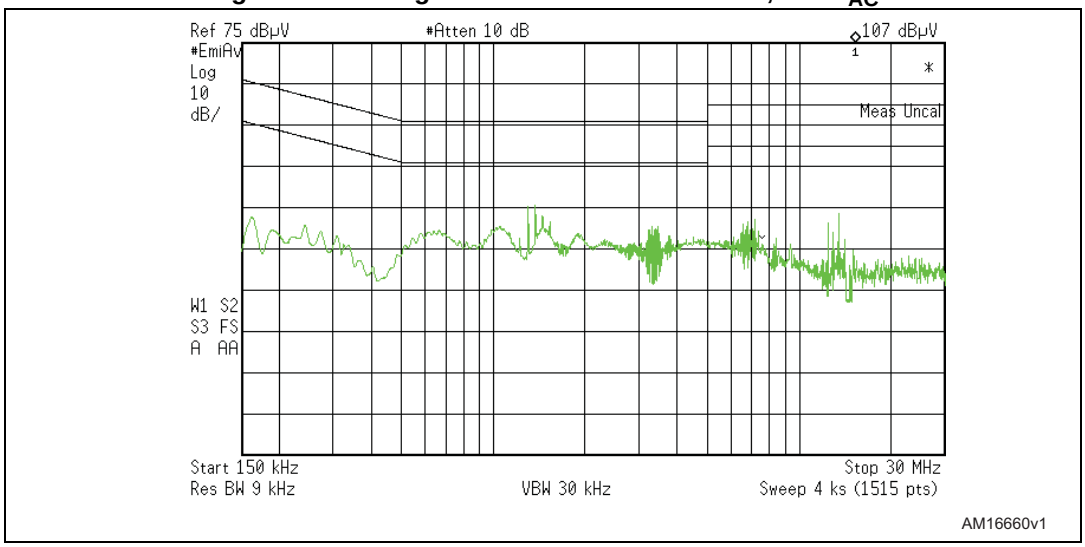
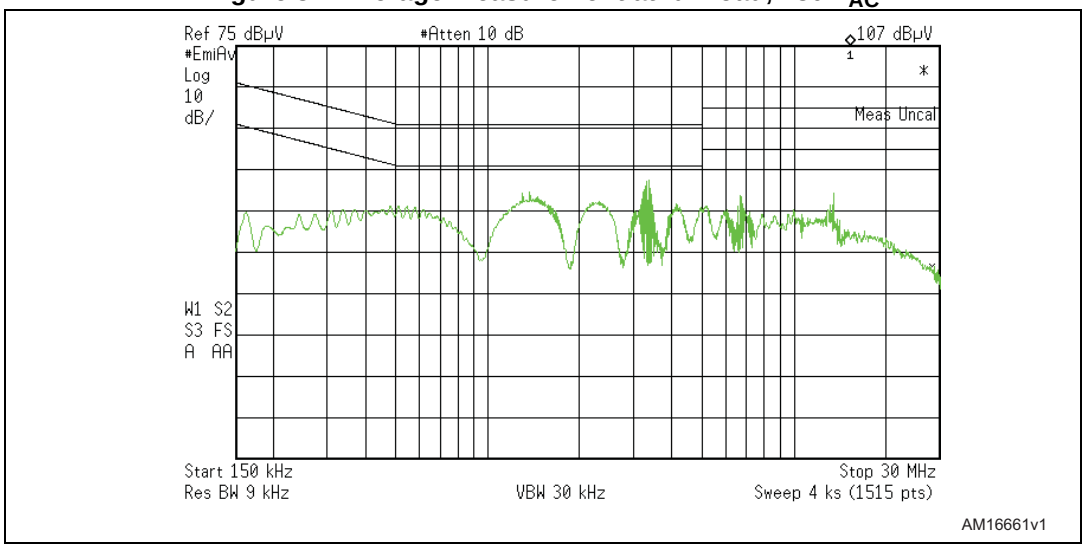


Figure 37. Average measurement at full load, 230 V_{AC}

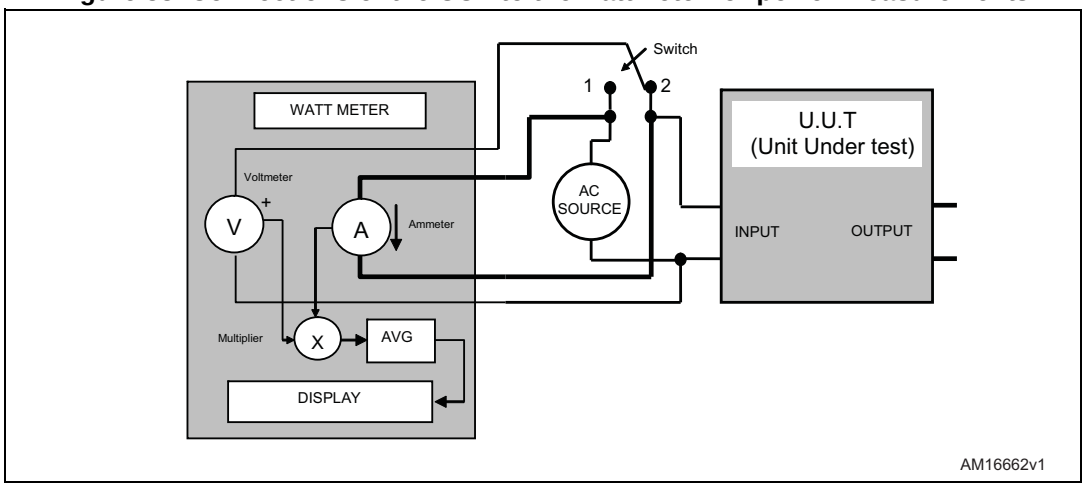


Appendix A Test equipment and measurement of efficiency and light load performance

The converter input power has been measured using a wattmeter. The wattmeter measures simultaneously the converter input current (using its internal ammeter) and voltage (using its internal voltmeter). The wattmeter is a digital instrument so it samples the current and voltage and converts them to digital forms. The digital samples are then multiplied giving the instantaneous measured power. The sampling frequency is in the range of 20 kHz (or higher depending on the instrument used). The display provides the average measured power, averaging the instantaneous measured power in a short period of time (1 sec typ.).

Figure 38 shows how the wattmeter is connected to the UUT (unit under test) and to the AC source and the wattmeter internal block diagram.

Figure 38. Connections of the UUT to the wattmeter for power measurements



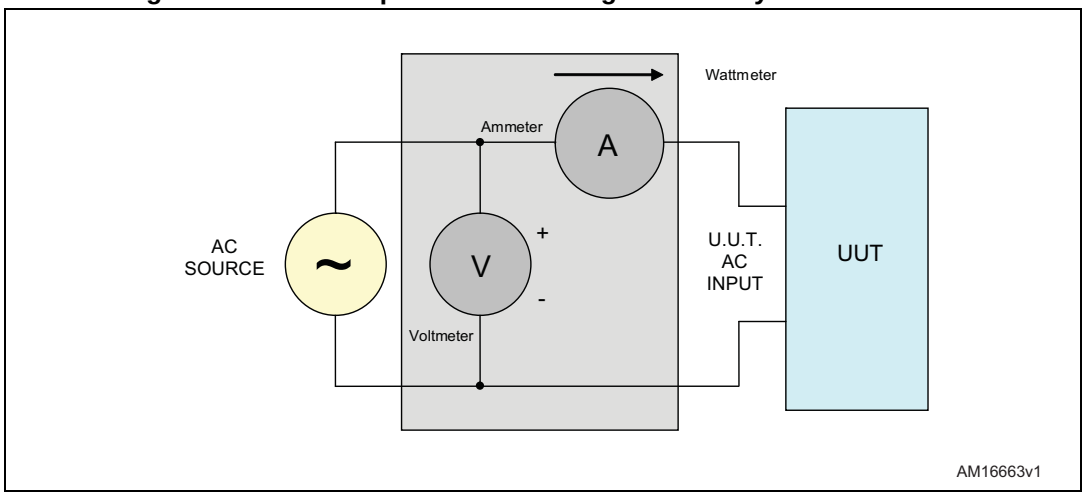
An electronic load has been connected to the output of the power converter (UUT), allowing the converter load current to be set and measured, while the output voltage has been measured by a voltmeter. The output power is the product between load current and output voltage. The ratio between the output power, calculated as previously stated, and the input power, measured by the wattmeter, is the efficiency of converter, which has been measured in different input/output conditions.

A.1 Measuring input power

With reference to *Figure 38*, the UUT input current causes a voltage drop across the internal shunt resistance of ammeter (the ammeter is not ideal so it has an internal resistance higher than zero) and across the cables connecting the wattmeter to the UUT.

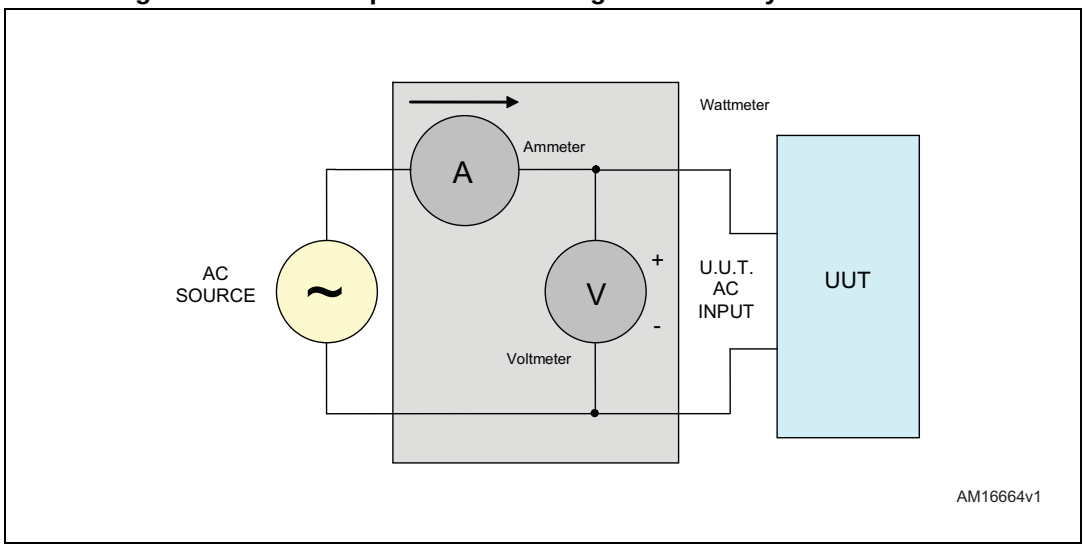
If the switch of *Figure 38* is in position 1 (see also the simplified scheme of *Figure 39*), this voltage drop causes an input measured voltage higher than the input voltage at the UUT input that, of course, affects the measured power. The voltage drop is generally negligible if the UUT input current is low (for example when we are measuring the input power of UUT in light load condition).

Figure 39. Switch in position 1 - setting for standby measurements



In case of high UUT input current (i.e. for measurements in heavy load conditions), the voltage drop can be relevant compared to the UUT real input voltage. If this is the case, the switch in *Figure 38* can be changed to position 2 (see simplified scheme of *Figure 40*) where the UUT input voltage is measured directly at the UUT input terminal and the input current does not affect the measured input voltage.

Figure 40. Switch in position 2 - setting for efficiency measurements



On the other hand, the position of *Figure 40* may introduce a relevant error during light load measurements, when the UUT input current is low and the leakage current inside the voltmeter itself (which is not an ideal instrument and doesn't have infinite input resistance) is not negligible. This is the reason why it is recommended the setting of *Figure 39* to be used for light load measurements and *Figure 40* for heavy load measurements.

If it is not clear which measurement scheme has the lesser effect on the result, try with both and register the lower input power value.

As noted in IEC 62301, instantaneous measurements are appropriate when power readings are stable. The UUT is operated at 100% of nameplate output current for at least 30 minutes (warm-up period) immediately prior to conducting efficiency measurements.

After this warm-up period, the AC input power is monitored for a period of 5 minutes to assess the stability of the UUT. If the power level does not drift by more than 5% from the maximum value observed, the UUT can be considered stable and measurements can be recorded at the end of the 5-minute period. If AC input power is not stable over a 5-minute period, the average power or accumulated energy is measured overtime for both AC input and DC output.

Some wattmeter models allow the integration of the measured input power in a time range and then measure the energy absorbed by the UUT during the integration time. The average input power is calculated dividing by the integration time itself.

10 References

[1] Code of Conduct on energy efficiency of external power supplies, version 4.
[2] VIPER06 datasheet.

Revision history

Table 5. Document revision history

Date	Revision	Changes
30-May-2013	1	Initial release.
25-Jul-2013	2	Updated: *Figure 5*, *Figure 6*, *Figure 7*, *Figure 8*, *Figure 19*, *Figure 21*, *Figure 23*, *Figure 24*, *Figure 25*, *Figure 26*, *Figure 27*, *Figure 28*, *Figure 29* and *Figure 30*.
23-May-2014	3	Changed the title in cover page. Updated *Table 2*.
15-Dec-2014	4	Updated *Equation 8*, *Equation 11* and *Equation 16*.