How to use PWM shutdown for motor control and digital power conversion on STM32 MCUs

Introduction

The purpose of this application note is to describe the STM32 device timer break feature. It details its use with other STM32 internal resources for an overcurrent and overvoltage protection. Namely, in applications related to the motor control and the digital power conversion such as lighting, SMPS, and induction heating.

This application note:

- provides an overview of the timer break feature.
- details how the timer break input is connected to different break sources.
- enumerates the different break event sources.
- provides some scenarios of the PWM output signal response to break events coming from an internal source, an external source, or a combination of both internal and external break signals.
- shows how to implement overcurrent and overvoltage protections using the timer break feature and other embedded peripherals such as comparators and DAC.

This document applies to the products listed in Table 1.

Table 1. Applicable products

Type	Product series
Microcontrollers	• STM32C0 series, STM32C5 series • STM32F0 series, STM32F1 series, STM32F2 series, STM32F3 series, STM32F4 series, STM32F7 series • STM32G0 series, STM32G4 series, STM32G5 series • STM32H5 series, STM32H7 series • STM32L4 series, STM32L5 series • STM32U0 series, STM32U3 series, STM32U5 series • STM32WB series, STM32WL series

1 General information

This document applies to Arm®-based devices.

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Reference documents

[1] Application note *STM32 cross-series timer overview* (AN4013)

2 Break function overview

The break function is available in TIM1, TIM8, TIM20, TIM15, TIM16, and TIM17 timers. These timers are able to generate complementary PWM signals with a dead time insertion for driving power switches in a half-bridge topology.

The purpose of the break function is to protect power switches driven by PWM signals generated with these timers. When triggered by a fault, the break circuitry shuts down the PWM outputs and forces them to a predefined safe state.

Table 2 summarizes the break inputs availability.

Table 2. Timers and break input availability in STM32 devices

-	TIM1	TIM8	TIM20	TIM15	TIM16	TIM17
STM32F0	BRK	-	-	-	-	-
	BRK_ACTH					
STM32F1	BRK	-	-	BRK	BRK	BRK
	BRK_ACTH			BRK_ACTH	BRK_ACTH	BRK_ACTH
STM32F2 **STM32F4**	BRK	BRK	-	-	-	-
	BRK_ACTH	BRK_ACTH				
STM32F3	BRK	BRK	BRK	BRK	BRK	BRK
	BRK2	BRK2	BRK2	BRK_ACTH	BRK_ACTH	BRK_ACTH
	BRK_ACTH	BRK_ACTH	BRK_ACTH	-	-	-
STM32F7	BRK	BRK	-	-	-	-
	BRK2	BRK2				
	BRK_ACTH	BRK_ACTH				
STM32L4 **STM32L5** **STM32U5, STM32C5** **STM32H7**(1) **STM32H5**(2)	BRK	BRK	-	BRK	BRK	BRK
	BRK2	BRK2		System break	System break	System break
	System break	System break		-	-	-
STM32C0 **STM32WB** **STM32WL** **STM32H7Rx/7Sx**	BRK	-	-	-	BRK	BRK
	BRK2				System break	System break
	System break				-	-
STM32G0, STM32U3	BRK	-	-	BRK	BRK	BRK
	BRK2			System break	System break	System break
	System break			-	-	-
STM32G4, STM32G5, **STM32H7P**	BRK	BRK	BRK	BRK	BRK	BRK
	BRK2	BRK2	BRK2	System break	System break	System break
	System break	System break	System break	-	-	-
STM32H503 **STM32U0**	BRK	-	-	-	-	-
	BRK2					
	System break					
STM32L0	BRK	-	-	-	-	-
	-					
	-					

1. *Excluding STM32H7Rx/7Sx and H7P.*
2. *Excluding STM32H503.*

The BRK input can either disable the PWM outputs (inactive state) or force them to a predefined safe state, either active or inactive, after a dead time insertion. This prevents any shoot-through in the half bridge. The BRK2 only disables the PWM outputs (inactive state).

BRK has a higher priority than BRK2. When both protections are triggered, the predefined safe state related to the BRK circuitry overrides the inactive state related to the BRK2 input.

Typically, a permanent magnet 3-phase brushless motor drive uses the protections as follows:

- The BRK2 input as an overcurrent protection, opening the six switches from the power stage.
- The BRK input as an overvoltage protection, overriding the overcurrent and closing the three low-side switches to avoid current regeneration to build up the bus voltage and exceed the capacitor-rated voltage.

As an example in STM32F303xB/C/D/E devices, for a dual motor drive, the comparators 1, 2, and 3 can be dedicated to overcurrent monitoring of the three phases of motor 1 (BRK2 input of TIM1). The comparators 4, 5, and 6 can be dedicated to overcurrent monitoring of the three phases of motor 2 (BRK2 input of TIM8), while the comparator 7 is used for overvoltage monitoring (driving BRK inputs of TIM1 and TIM8).

BRK_ACTH input is connected only to internal signals such as CSS and PVD output. On newer devices like STM32U5 or STM32U3, it is marked as tim_sys_brk (system break interconnect) or as *internal source* but this serves the same purpose. For more details, refer to Section 3: Break implementation.

The availability of break inputs and the break sources depends on the selected STM32 series.

This is summarized in Table 3 and in document [1] which details the available timers.

Table 3. Comparator peripherals availability per STM32 device

Comparator availability may be limited by the package pin count.

-	STM32F0 STM32C5, STM32L0(1), STM32L1(2), STM32U0, STM32U3(5)	STM32F3											STM32L0(1), STM32L1(2)	STM32L4		STM32U5	STM32WB, STM32WL	STM32G0(3)			STM32G4		STM32H5	STM32H7(4), STM32L5	STM32H7P	STM32G5
		STM32F303xB/C	STM32F358xC	STM32F303x6/8	STM32F328x8	STM32F303xD/E	STM32F398xE	STM32F302xB/C/D/E	STM32F302x6/8	STM32F301x6/8	STM32F318x8	STM32F334x4/6/8	STM32F37xxx		STM32L4	STM32L4+			STM32G051/61	STM32G071/81	STM32G0B1/C	STM32G4x1	STM32G4x3	STM32H503			
Filter	-	-	-	-	-	-	-	-	-	-	-	-	-	DFSDM	MDF(5)	-	-	-	-	-	-	-	-	DFSDM	HSP	-
COMP 1	X	X	-	X	X	-	-	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
COMP 2	X	X	X	X	X	X	X	X	X	X(6)	X	X	X	X	X	X	X	X	X	-	X	X	X	X	X	X
COMP 3	-	X	-	X	-	-	-	-	-	-	-	-	-	-	-	-	X	X	X	-	-	X	X	X	X	X
COMP 4	-	X	X	X	X	X	X	-	-	-	-	-	-	-	-	-	-	X	X	-	-	X	X	X	X	X
COMP 5	-	X	-	X	-	-	-	-	-	-	-	-	-	-	-	-	-	-	X	-	-	X	X	X	X	X
COMP 6	-	X	X	X	X	X	X	-	-	-	-	-	-	-	-	-	-	-	X	-	-	X	X	X	X	X
COMP 7	-	X	-	X	-	-	-	-	-	-	-	-	-	-	-	-	-	-	X	-	-	X	X	X	X	X
COMP8	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	X	X

1. *These devices feature comparators, but no advanced timers with break inputs. STM32L010 value line has no comparators either.*
2. *These devices feature comparators, but no advanced timers with break inputs.*
3. *STM32G0x0, STM32G031, and STM32G041 have no comparators.*
4. *Excluding the STM32H7Rx/Sx and H7P line.*
5. *ADF does not feature a break output.*
6. *STM32L412/L422 does not have COMP2.*

3 Break implementation

3.1 TIM1/8/20 break implementation

The source for break BRK channel is an external source connected to one of the BKIN pins (as per selection done in the AFIO controller), with polarity selection and optional digital filtering.

The source of break2 BRK2 channel is an external source connected to one of the BKIN2 pins (as per selection done in the AFIO controller), with polarity selection and optional digital filtering.

The source for BRK_ACTH (or system break interconnect) is an internal signal coming from:

- The comparator output (on STM32Fx)
- The clock security system
- The lockup of Cortex-M family CPUs
- The PVD output
- The SRAM ECC/parity error signal
- The flash ECC error

BRK

- In all series, the input signal on BRK is connected to the BKIN pin.
- Where there are multiple break sources, the resulting signal is a logical OR between the inputs. These include the filters and comparators listed in Table 3 and external sources. In case of power oriented series like for example STM32L4, STM32G4, STM32G5 and STM32H7P the input polarity may be configured individually.
- In the STM32H7P line the break inputs are customizable using a configurable multiplexer, described in detail in the RM.

The polarity feature is available for the BRK input. The filter feature is available as well but not on STM32F1/F2/F4 devices.

BRK_ACTH (or system break)

- In the STM32F1/F2/F4/F7 series, this input only gathers the system level fault signals.
- In the STM32F0 series, BRK_ACTH is connected to the system level fault signals and the comparators outputs (1 and 2).
- In the STM32F3 series, BRK_ACTH is connected to the system level fault signals and the comparators (1, 2, 3, 5, and 6).
- For any non-Fx series, the system break request is connected to the system level fault signals.

When this input is used, the polarity selection and filter features are not available. It is always active high.

BRK_ACTH is enabled using the same bit as BRK (BKE in TIMx_BDTR, x= 1, 8, 20).

If there are several system break input sources, the resulting input signal is an OR between all the input signals. Except for the CSS fault signal, the inputs can be individually disabled using the system control block registers.

Other break inputs, external, filter, or comparator are also ORed together and then with the system break inputs. In case of comparator and external signals, polarity must be observed for the logical OR to work as intended.

BRK2

- In the STM32F3 series, this input signal is a logical OR between the input signal on the BKIN2 pin and the used comparators outputs (1, 2, 3, 4, 5, 6, and 7). If the BKIN2 alternate function is disabled (input not used), the resulting break signal is solely related to the comparators.
- In the STM32F7 series, the input signal on BRK2 is connected to the BKIN2 pin.
- In the STM32L4 series, the input signal on BRK2 is a logical OR between the input signals on the BKIN2 pin, the used comparator (1 or 2) output and the DFSDM break output if configured.
- In the STM32U5 series, the input signal on BRK2 is a logical OR between comparators (1 or 2) and MDF1.
- In the STM32L4 and STM32L5 series, it is possible to configure the polarity of each break source in addition except the DFSDM break output to the polarity configuration inside the timer peripheral using BKCMP1P, BKCMP2P, BKINP in TIMx_OR2 register and BK2CMP1P, BK2CMP2P, BK2INP in TIMx_OR3 register.
- In the STM32G4/STM32G5 series, the input signal on BRK2 is a logical OR between the input signals on the BKIN2 pin and all the used comparators outputs.
- In the STM32U5 and STM32H7 series, it is possible to configure the polarity of each break source in addition except the MDF1 (DFSDM) break output to the polarity configuration inside the timer peripheral using BKCMP1P, BKCMP2P, BKINP in the TIMx_AF1 register and BK2CMP1P, BK2CMP2P, BK2INP in the TIMx_AF2 register.
- In the STM32G4, STM32G5 and STM32C5 series, it is possible to configure the polarity of COMP1-4 using BKCMPxPbits in TIMx_AF1 register and BK2CMPxP in TIMx_AF2 register. The rest of the internal inputs have individual polarity fixed to active high, though the collective polarity is still configurable (BKP, BK2P).
- On other series, polarity is individually configurable for all their available COMPx and BKIN/BKIN2 inputs.
- In the STM32H7P line this input is also routed through multiplexer, allowing more precise control over break inputs from COMP and HSP.

Figure 1 shows the break feature implementation for TIM1 and TIM8 in STM32F0/F1/F2/F4/F7 series devices.
Figure 2 shows the break feature implementation for TIM1, TIM8, and TIM20 in STM32F3 series devices.
Figure 3 shows the break feature implementation for TIM1 and TIM8 in STM32L4 series devices.
Figure 4 shows the break feature implementation for TIM1 and TIM8 in STM32U5 series devices.

Figure 1. Break feature implementation in advanced timers for STM32F0/F1/F2/F4/F7 series devices

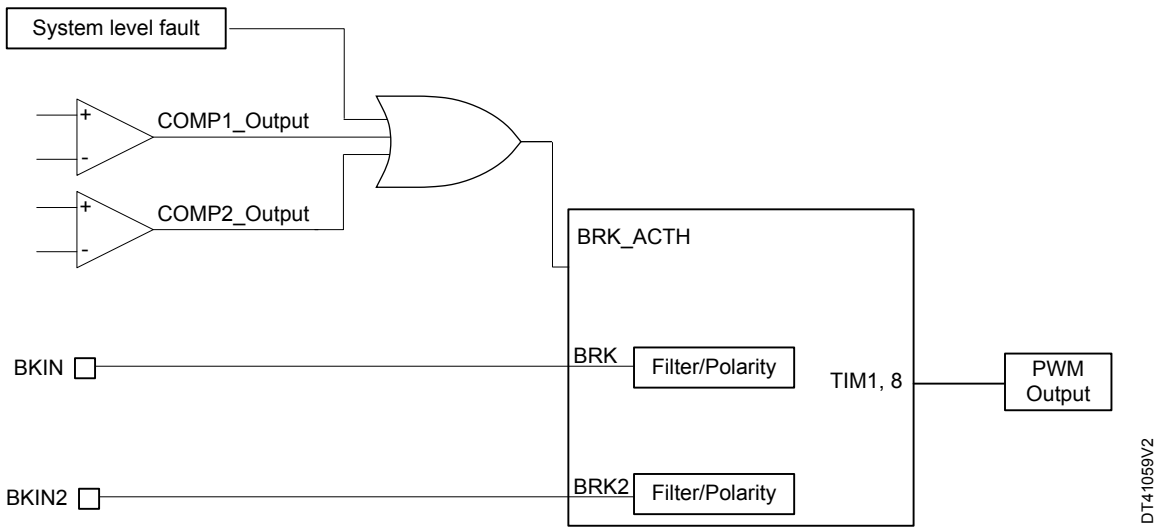


Figure 2. Break feature implementation in advanced timers for STM32F3 series devices

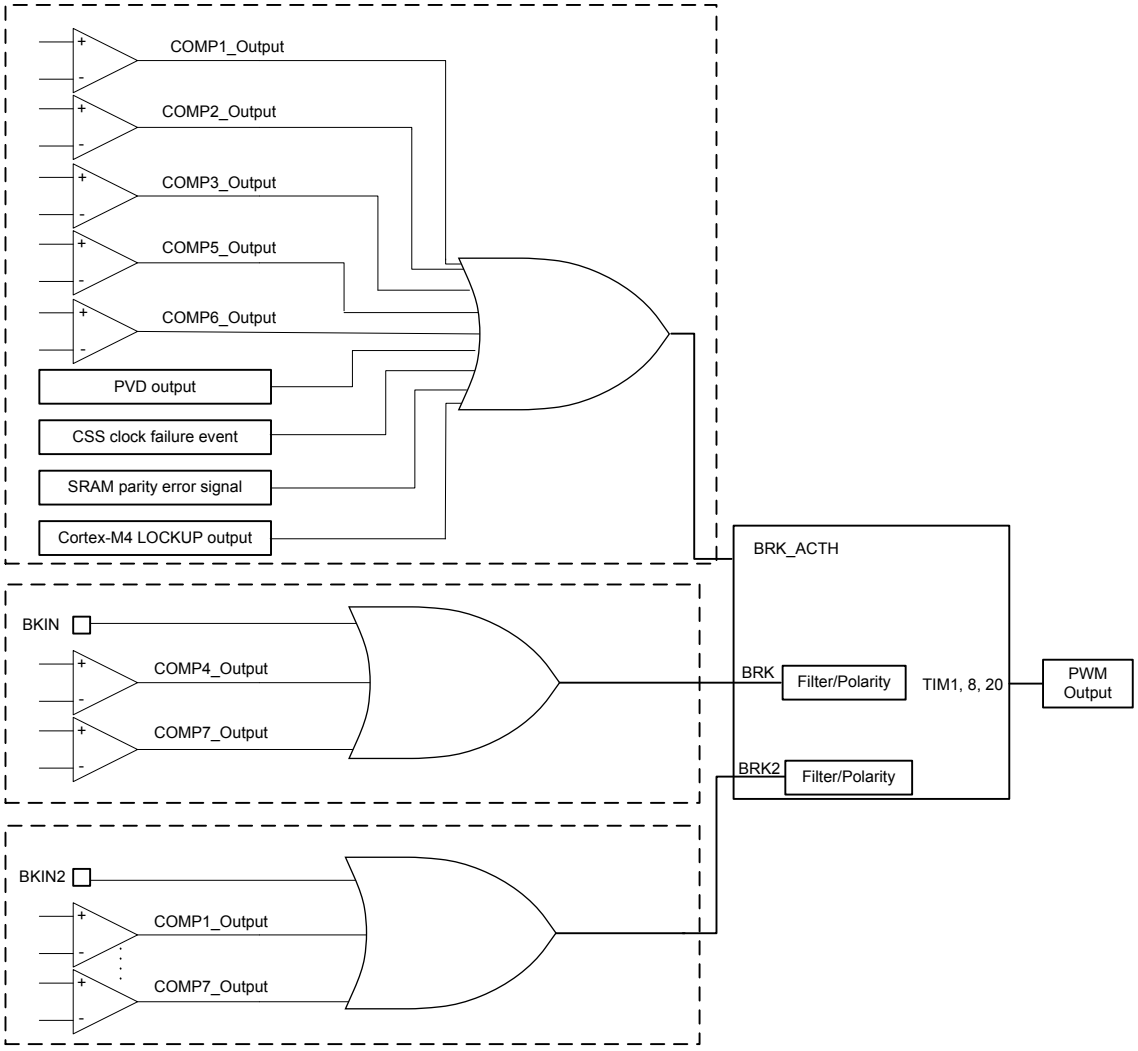


Figure 3. **Break feature implementation in advanced timers for STM32L4 series devices**

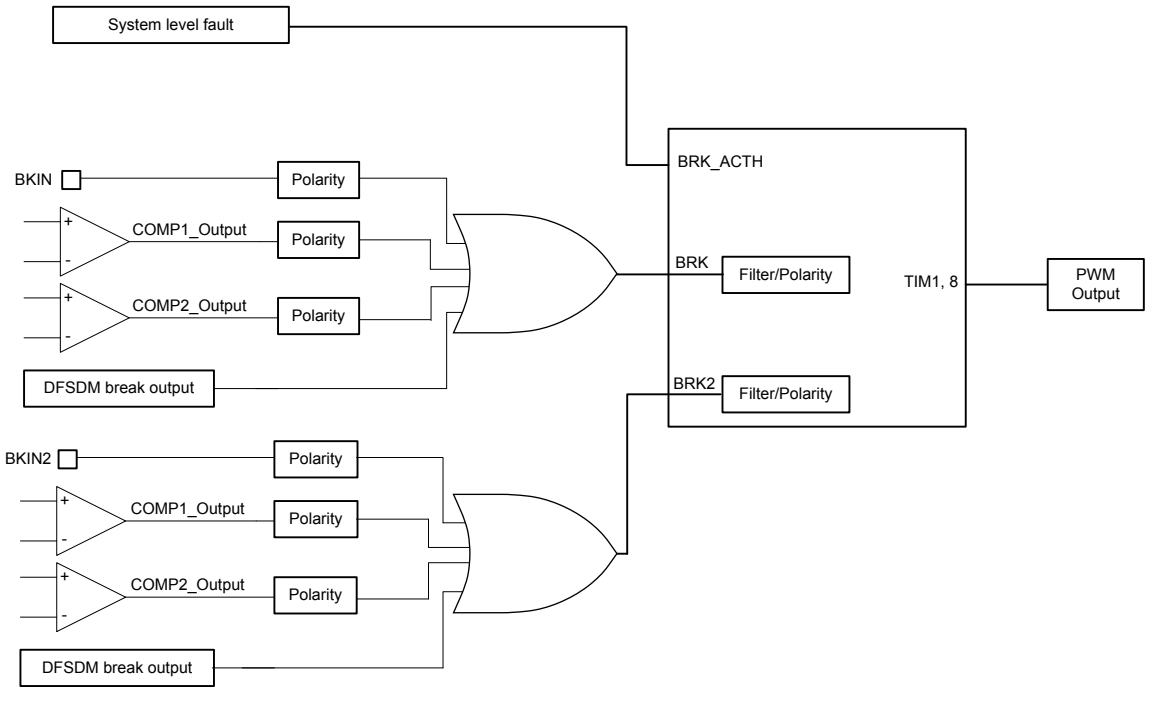
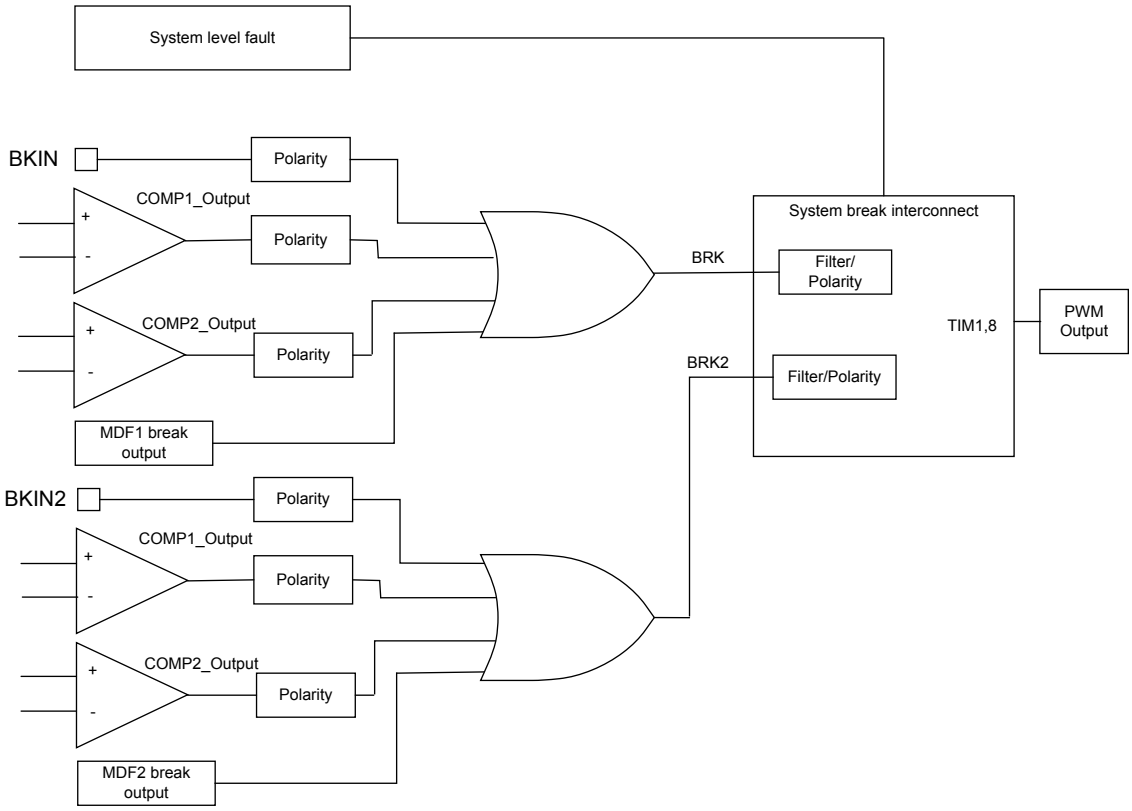


Figure 4. **Break feature implementation in advanced timers for STM32U5 series devices**

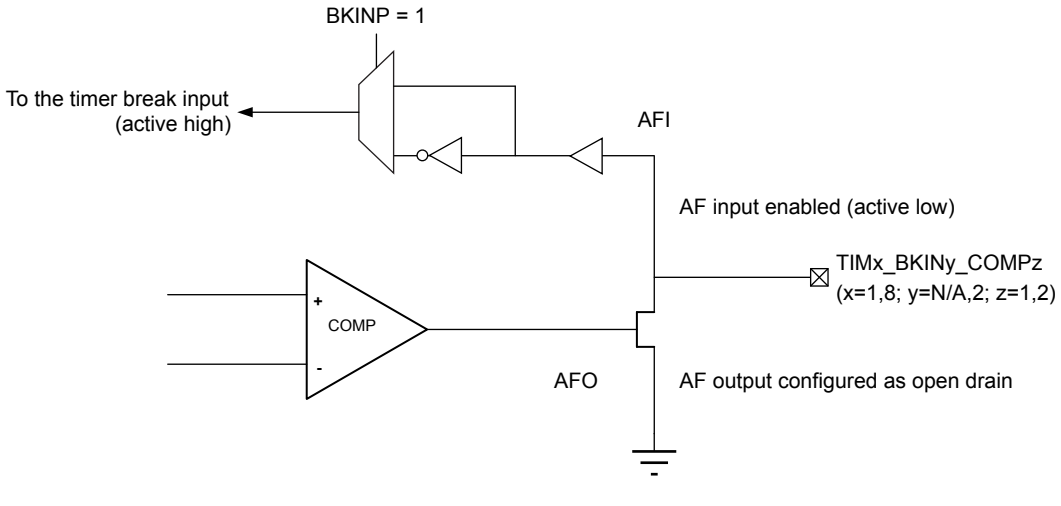


Bidirectional break inputs

For example in the STM32L4/STM32G4/STM32G5 and STM32U5 series, the timer 1 and timer 8 are featuring bidirectional break input/outputs combining the comparator output (to be configured in open drain) and the Timer BKIN input, as represented in Figure 5.

This feature allows information about the global break available for external MCUs with a single-pin.

Figure 5. Output redirection



3.2 TIM15/16/17 break implementation

The source for break BRK channel is an external source connected to one of the BKIN pins (as per selection done in the AFIO controller), with polarity selection and optional digital filtering.

The source for BRK_ACTH is an internal signal coming from:

- The clock security system
- The lockup of Cortex-M family CPUs
- The PVD output
- The SRAM ECC/parity error signal
- The flash ECC error

Inputs from available comparators are ORed with BRK_ACTH signals (on STM32Fx series) or with the external BRK input with polarity selection option.

BRK

- In all series: the input signal on BRK is connected to the BKIN pin.
- In the STM32L4/STM32G4/STM32G5 series: the input signal on BRK is a logical OR between the input signals on the BKIN pin, the used comparator (1 or 2) output and the DFSDM break output if available and configured.
- In STM32U5 series: the input signal on BRK is a logical OR between the BKIN pin, the used comparator (1 or 2) output, and the MDF1 break output.

The polarity selection feature is available for the BRK source.

In STM32L4/STM32G4/STM32G5 series, it is possible to configure the polarity of each break source inside the timer peripheral using BKCMP1P, BKCMP2P, BKINP in the TIMx_OR2 register. This is only not possible for the DFSDM input on the STM32L4.

In STM32U5 series, it is possible to configure the polarity of each break source in addition. Thus, except the MDF1 break output to the polarity configuration inside the timer peripheral. This is done using BKCMP1P, BKCMP2P, BKINP in the TIMx_AF1 register.

Note: On TIM15-17, the filter feature is only available for STM32C5, STM32Gx, STM32Hx, and STM32U5 devices.

BRK_ACTH (or system break)

- In STM32F1/L4 series, this input only gathers the system level fault signals (CSS, PVD output, SRAM parity error, and the Hardfault).
- In STM32F3 series, BRK_ACTH is connected to the system level fault signals and the comparators (1 and 2) for the STM32F37xxx devices and the comparators outputs (3, 5, and 7) for the rest of the STM32F3 series.
- In other series, system break interconnected sources are CSS, flash, and SRAM ECC errors, PVD and core lockup detection.

When this input is used, the polarity selection and filter features are not available. It is always active high.

BRK_ACTH is enabled using the same bit BRK (BKE in TIMx_BDTR, x= 15, 16, 17).

When using BRK_ACTH as break input, the polarity must be configured high. Otherwise, there is no PWM generation independently of the break signal coming from the internal source.

Figure 6 shows the break feature implementation for TIM15, TIM16, and TIM17 in STM32F1 series devices.

Figure 7 shows the break feature implementation for TIM15, TIM16, and TIM17 in STM32F3 series devices.

Figure 8 shows the break feature implementation for TIM15, TIM16, and TIM17 in STM32L4 series devices.

Figure 9 shows the break feature implementation for TIM15, TIM16, and TIM17 in STM32U5 series devices.

Figure 6. Break feature implementation for TIM15, TIM16, and TIM17 for STM32F1 series devices

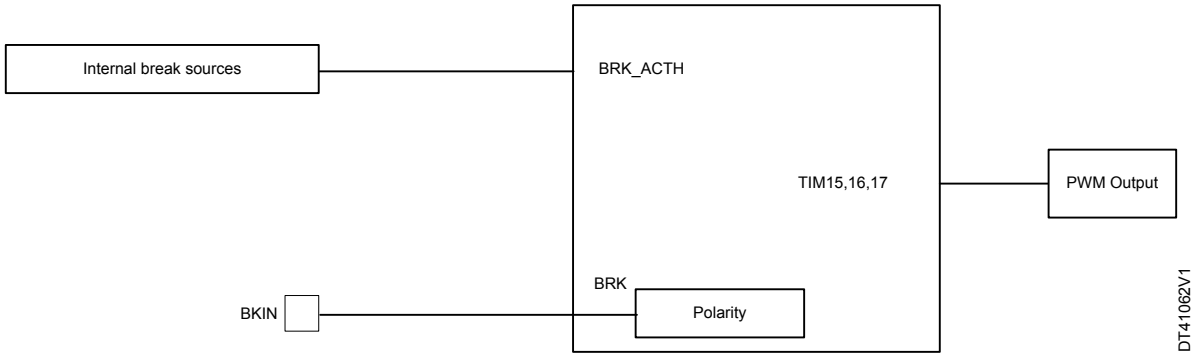


Figure 7. Break feature implementation for TIM15, TIM16, and TIM17 for STM32F3 series devices

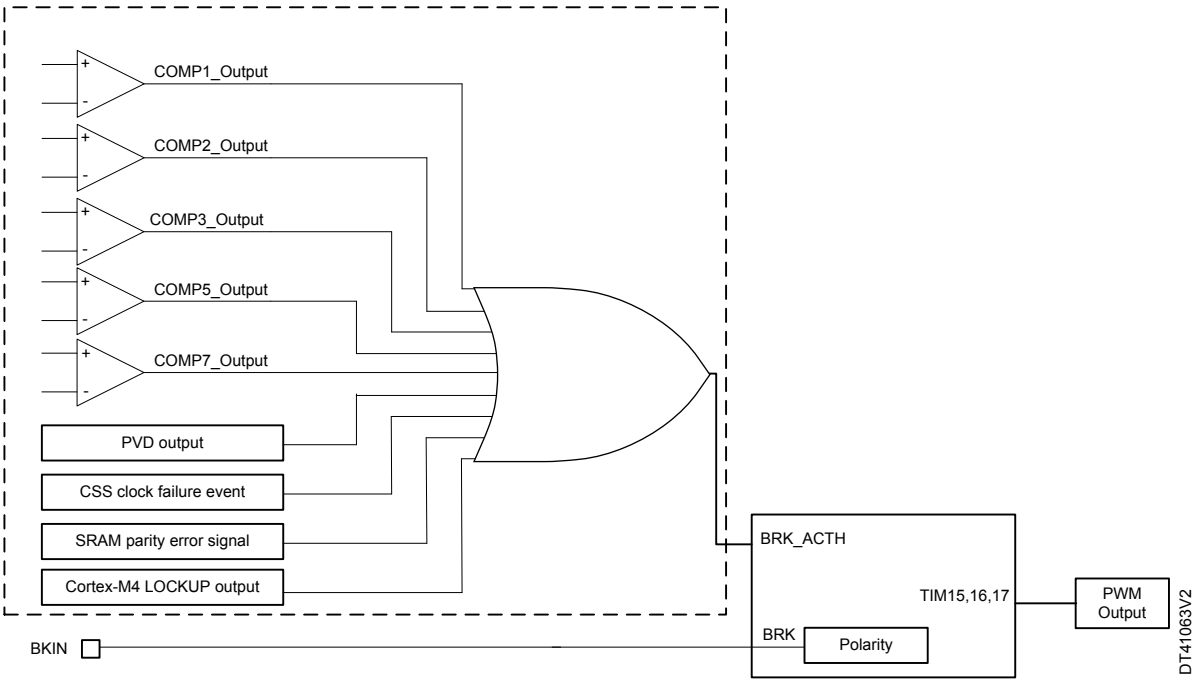
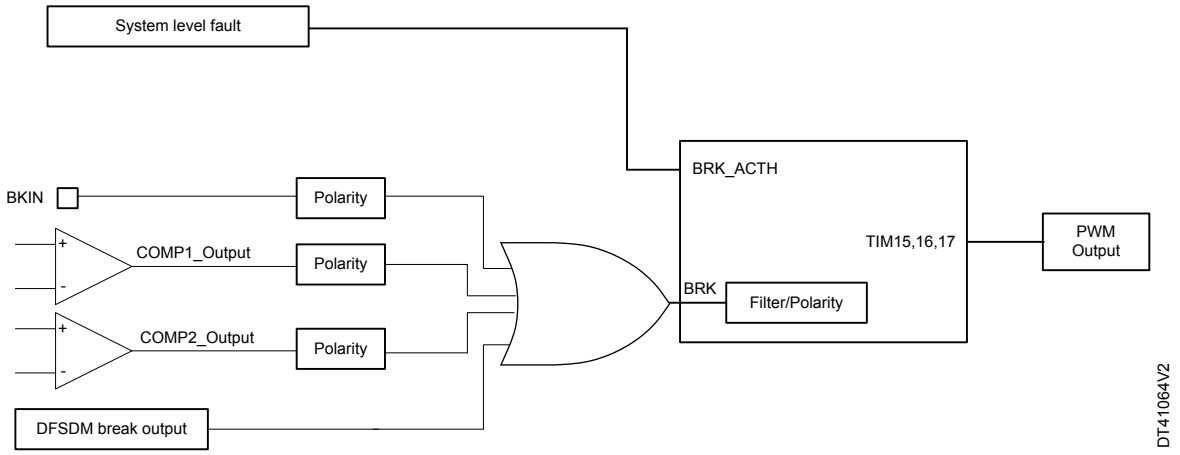
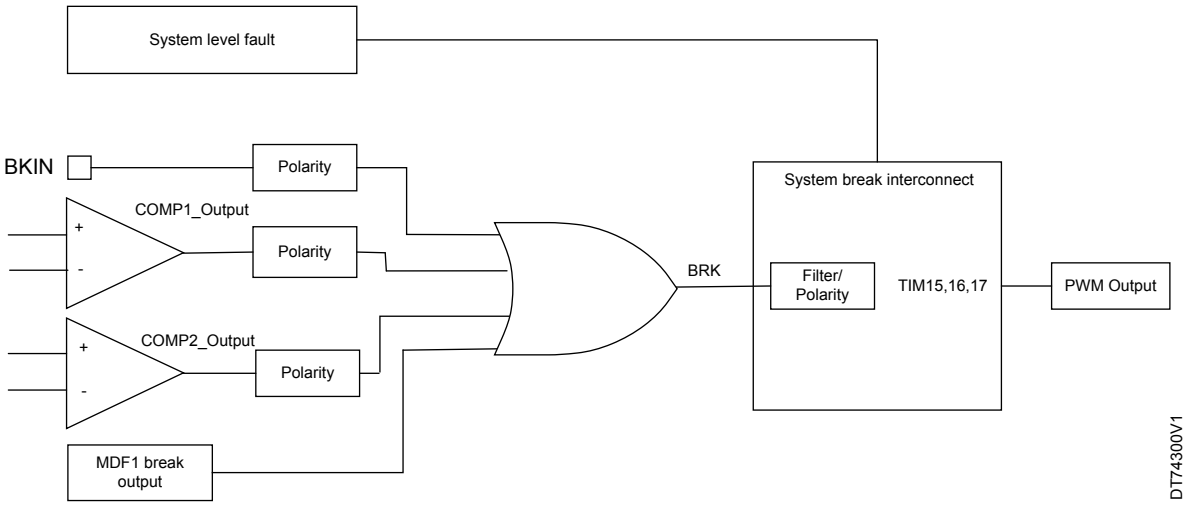


Figure 8. Break feature implementation for TIM15, TIM16, and TIM17 for STM32L4 and STM32H7 series devices



- If only an internal break source is used, the polarity must be configured to high in the software.
- If there are several break input sources, the resulting input signal is an OR between all the input signals.
- If both internal break source and BKIN are used, the resulting break signal is an OR between the signal pin and the internal break signal.
- If the alternate function AF of the BKIN or BKIN2 pin is not activated, the BRK or the BRK2 is connected to the ground. If the state of the BRK or BRK2 polarity is low, in this case if the break function is enabled, the timer output is disabled. Thus, it must configure the break polarity to high. Only in the STM32F1 series it must configure the break polarity to low.

Figure 9. Break feature implementation for TIM15, TIM16, and TIM17 in STM32U5 series devices



Note: STM32G0, STM32H7, STM32WB, and STM32WL are similar to STM32U5, except for MDF.

4 Break sources summary

Table 4 summarizes the available break sources and their connections externally or internally to timers (1, 8, 20, 15, 16, and 17) break inputs.

Table 4. Break input sources

-	BRK	BRK_ACTH (or system break)	BRK2
External connection to pin	BKIN	No corresponding I/O	BKIN2
Internal connection to pin	**In STM32F3:** • Comparators 4 and 7 for TIM1/8/20 • NA for TIM15/16/17 **In STM32G4 and STM32G5:** All comparators, some with polarity control on TIM1/8/20 **In STM32L4 and STM32H7(1):** • Comparators 1 and 2 • DFSDM break output **In STM32U5:** • Comparators 1 and 2 • MDF1 break output	Available signals from: • Clock failure event generated by CSS • PVD output • RAM parity error signal • Cortex-M LOCKUP output (Hardfault) • Comparator outputs (on STM32Fx series) • Flash double ECC error	**In STM32F3:** • Comparators 1, 2, 3, 4, 5, 6, and 7 **In STM32G4 and STM32G5:** All comparators, some with polarity control on TIM1/8/20 **In STM32L4 and STM32H7(1):** • Comparators 1 and 2 • DFSDM break output **In STM32U5:** • Comparators 1 and 2 • MDF1 break output
Polarity feature in case of internal connection	Configurable for most inputs: active high or active low	Always active high	Configurable for some inputs: active high or active low
Polarity feature in case of external break event	Available	NA	Available
Filter feature	Not available in STM32F0, STM32F1, STM32F2, and STM32F4. Only available in STM32F3 advanced timers.	NA	Not available in STM32F0, STM32F1, STM32F2, and STM32F4
Available in	TIM1/8/20/15/16/17	TIM1/8/20/15/16/17	TIM1/8/20 in STM32F3, TIM1/8 in other series
Resulting break signal in case of parallel external or/and internal break sources	It is an OR between the external break signals and the internal ones.		

1. *Excluding the STM32H7Rx/Sx line.*

5 Examples

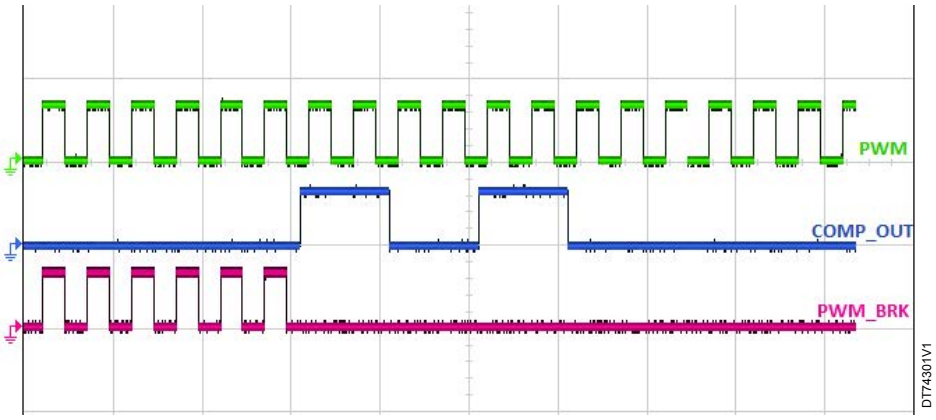
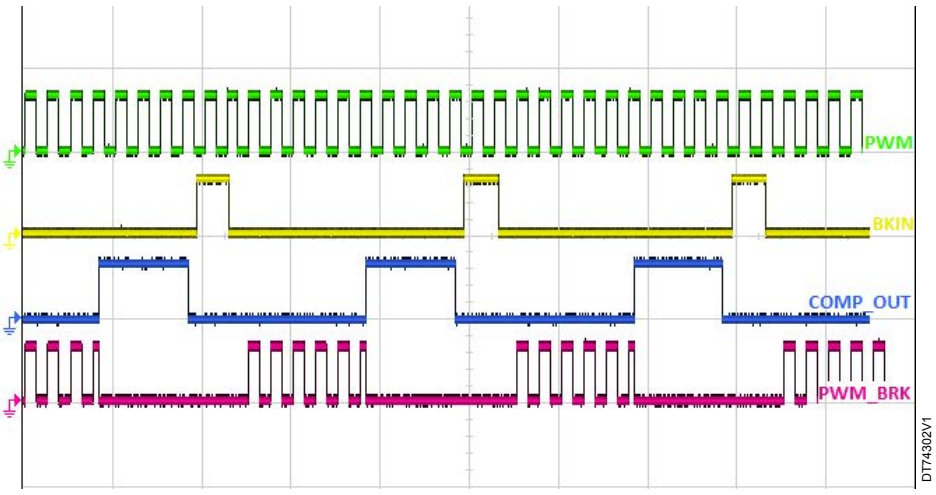
Table 5 shows the PWM output status for TIMx (where x = 1, 8, 20, 15, 16, 17) in response to internal/external break events.

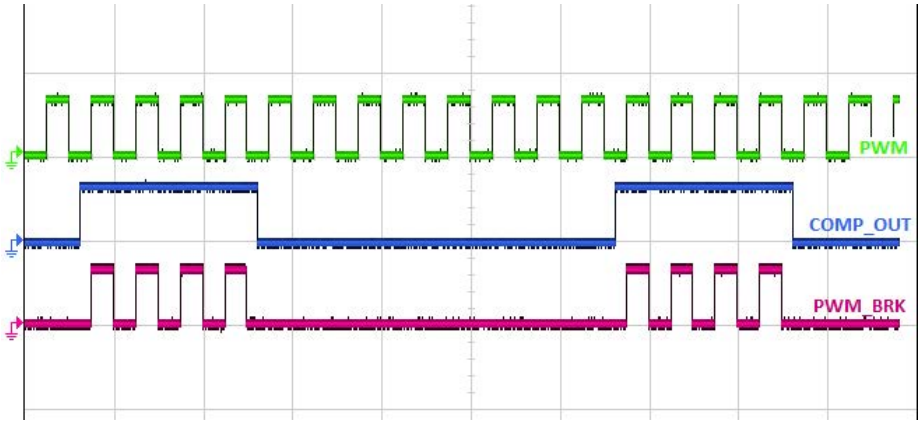
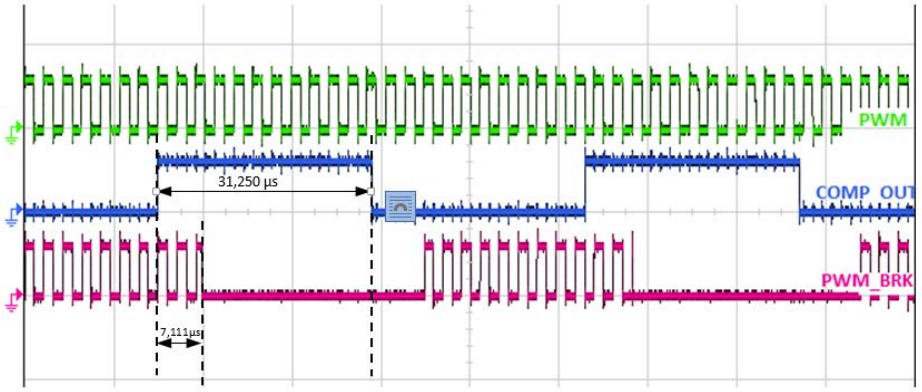
In the following waveforms:

- The PWM signal is the reference waveform (internal signal, before BRK protection).
- The COMP_OUT signal represents the BRK input signal, in our case it is the comparator output.
- The BIN signal is the input signal on BKIN.
- The PWM_BRK signal is the resulting PWM signal on the timer output after break detection.

Table 5. Scenarios of PWM output status in response to internal/external break events

Color legend: green = PWM signal, blue = COMP_OUT signal, yellow = BKIN signal, purple = PWM_BRK signal.

Configuration	Programmed polarity	Result
Comparator 1 output is connected internally to TIM1 BRK_ACTH and TIM1 BKIN alternate function is disabled.	High	The PWM generation is stopped when the comparator output is at the high level, as shown in the following screenshot: 
Comparator 1 output is connected internally to TIM1 BRK_ACTH and TIM1 BKIN alternate function is enabled.	High/Low	The break input signal is an OR between the signal on BKIN and the comparator output. The following screenshot shows an example (polarity = High):  *Note: To show the effect of the two break sources, the bit AOE in the BDTR register is set, allowing to restart the PWM at the next update event.*

Configuration	Programmed polarity	Result
Comparator 4 output is connected internally to TIM1 BRK and the filter is not configured.	Low	The PWM signal is stopped during the break signal low level, as shown in the following screenshot: 
Comparator 4 output is connected internally to TIM1 BRK and the filter is configured.	High	During the window defined by the filter duration, the break event has no impact on the PWM generation even if the break condition is verified. This is the case of the following example (screenshot) where the PWM signal is generated normally when the break signal is at a high level during the window defined by the filter. • The filter duration is 7.111 µs (BKF = 1111b, filter duration is (32*8/fDTS), fDTS = 36 MHz). • The comparator output high level duration is 7.111 µs. 

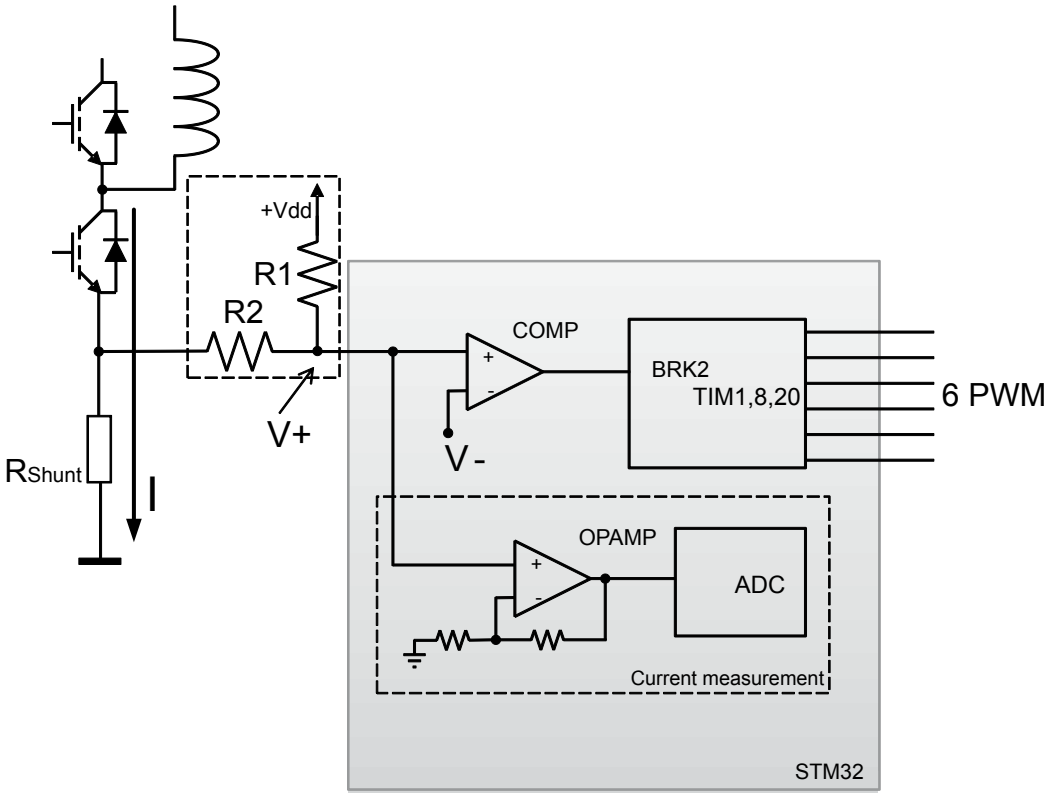
6 Using the break function with other MCU resources

This section focuses on the STM32G4 and STM32F3 series, but some parts may also apply to other STM32 series. In some cases, analogous resources may be used, such as system level fault instead of BRK_ACTH.

6.1 Break function used for overcurrent protection

The STM32F3 and STM32G4 series microcontroller embeds a set of peripherals designed to resolve common motor control issues while reducing the number of required external components. This section describes how to use these peripherals to implement overcurrent protection. Figure 10 shows the overcurrent protection network that can be implemented using the internal resources of the MCU.

Figure 10. Overcurrent protection network implementation block diagram



The principle of this overcurrent protection mechanism can be summarized as follows:

- The phase current of the motor flows in the power transistor of the inverter bridge and passes through the shunt resistor (R_{Shunt}) producing a voltage drop (V+).
- This voltage drop is compared with a threshold (V-) defining the maximum admissible current.
- If the threshold is exceeded, a break signal stops the PWM generation putting the system in a safe state.

All of these actions can be performed using the internal resources of the STM32 and, in particular, the embedded comparators and advanced timer break function (BRK2). In the basic implementation, the only external component required is the shunt resistor that must be sized depending on the current to be monitored and the shunt resistor power rating.

The two dotted line boxes in Figure 10 show the components required to measure current:

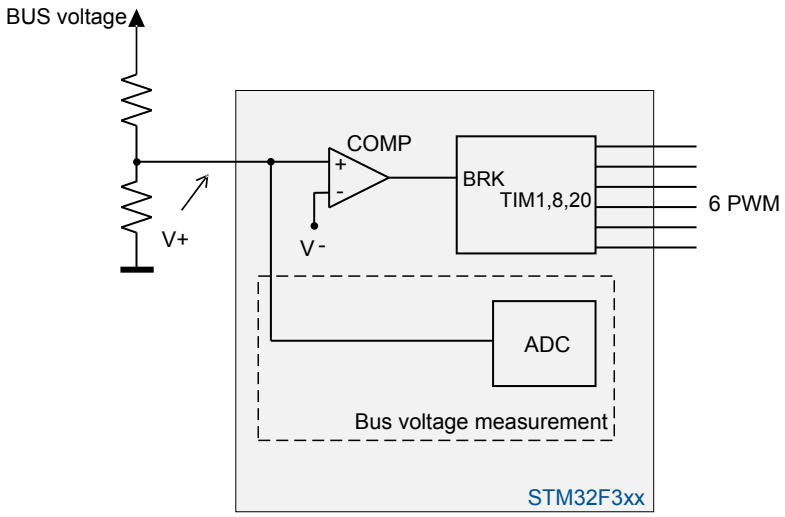
- The R1/R2 resistive network to add an offset necessary to measure AC currents.
- An operational amplifier with a built-in gain setting network.

The amplification network can be implemented externally for specific use cases where the built-in gain settings are not adequate.

6.2 Break function used for overvoltage protection

Figure 11 shows the overvoltage protection network that can be implemented using the internal resources of many STM32 MCUs.

Figure 11. Overvoltage protection network block diagram



In this case, the principle is similar to the one described in Section 6.1 :

- A resistive voltage divider provides a signal proportional to the bus voltage.
- This reading is compared to an overvoltage threshold to generate a fault signal. See also: Appendix A.1: How to use the DAC to define thresholds.
- If the threshold is exceeded, a break signal stops the PWM generation putting the system in a safe state.

As mentioned before, these actions can be performed automatically using the internal comparator. In this case, it is possible to use the second break functionality (BRK) of the advanced timer to differentiate the action to perform on the PWM signals in case of an overcurrent.

In the basic implementation, the only external component required is the voltage divider, which must be sized depending on the bus voltage range requested by the target application, so that it never exceeds the MCU's input maximum admissible voltage level.

The dotted line box in Figure 11 shows the components required for the bus voltage measurement. In this case, amplifying the signal V+ is usually not required (the resistive divider is adjusted for full-range reading), so this signal is fed directly to the analog-to-digital converter.

6.3 Using an external emergency signal together with the internal comparator

Commonly in MC applications, gate driver ICs, such as ST's L639x family or intelligent power modules (IPMs) - such as ST's SLLIMM (small low-loss intelligent molded module) family - have integrated comparators that can protect the inverter (ST's smart shutdown function) while sending an error signal to the microcontroller.

This section shows the possibility to combine these two concepts, as shown in , as to enhance by redundancy the functional safety offered by the "break function".

A first option is when the break function is triggered by internal comparators output only: the error signal coming from ICs or IPMs must not be connected to the microcontroller, thus saving the pin. The configuration to set in this case is summarized in the following table.

Table 6. Comparator output connected internally to break inputs

Description	Register	Bit	Configuration(1)
TIM1/8/20 BRK_ACTH/BRK/ BRK2 polarity	TIMx_BDTR	BKP or BK2P	1 (active high)
Comparator output polarity	COMPx_CSR	COMPxPOL	0 (not inverted), comparators input connected as shown in previous sections
TIM1/8/20 BKIN and BKIN2 AF	GPIOxAFRL or GPIOxAFRH	-	AF is not enabled on BKIN1/2 related pins
TIM1/8/20 BRK and BRK2 enable	TIMX_BDTR	BKE or BK2E	1
COMPx out selection	COMPx_CSR(2)	COMPxOUTSEL	0001: TIM1 BRK or TIM1 BRK_ACTH(3) 0010: TIM1 BRK2 0011: TIM8 BRK or TIM8 BRK_ACTH(4) 0100: TIM8 BRK2 0101: TIM1 BRK2 + TIM8 BRK2 1100: TIM20 BRK or TIM20 BRK_ACTH(5) 1101: TIM20 BRK2 1110: TIM1 BRK2 + TIM8 BRK2 + TIM20 BRK2

1. *Some newer STM32 series, such as STM32U5 abandoned the use of BRK_ACTH identifier using name system level or internal fault instead. The functionality remains analogous.*
2. *In newer products, such as STM32H7P, this register is not present. Selection is made on TIMx side.*
3. *TIM1 BRK in case of COMP4 and COMP7, or TIM1 BRK_ACTH in case of COMPx, x = 1, 2, 3, 5, and 6.*
4. *TIM8 BRK in case of COMP4 and COMP7, or TIM8 BRK_ACTH in case of COMPx, x = 1, 2, 3, 5, and 6.*
5. *TIM20 BRK in case of COMP4 and COMP7, or TIM20 BRK_ACTH in case of COMPx, x= 1, 2, 3, 5, and 6.*

On the contrary, the user may prefer to make use of the external error signal in conjunction with the internal one: the result is an OR between the two. Depending on the external comparator logic, the possible configurations to write are summarized in the following tables.

Table 7. Comparator output connected externally to break inputs, with low break polarity

Description	Register	Bit	Configuration
TIM1/8/20 BRK polarity	TIMx_BDTR	BKP	0 (active low), it means that the external signal goes low during the fault
Comparator output polarity	COMPx_CSR(1)	COMPxPOL	0 (not inverted), comparators input connected as shown in previous sections
TIM1/8/20 BKIN AF	GPIOxAFRL or GPIOxAFRH	-	AF enabled on BKIN pin selected among available
TIM1/8/20 BRK enable	TIMX_BDTR	BKE	1
COMPx out selection	COMPx_CSR(1)	COMPxOUTSEL	0001: TIM1 BRK 0011: TIM8 BRK 1100: TIM20 BRK

1. *In newer products, such as STM32H7P, this register is not present. Selection is made on TIMx side.*

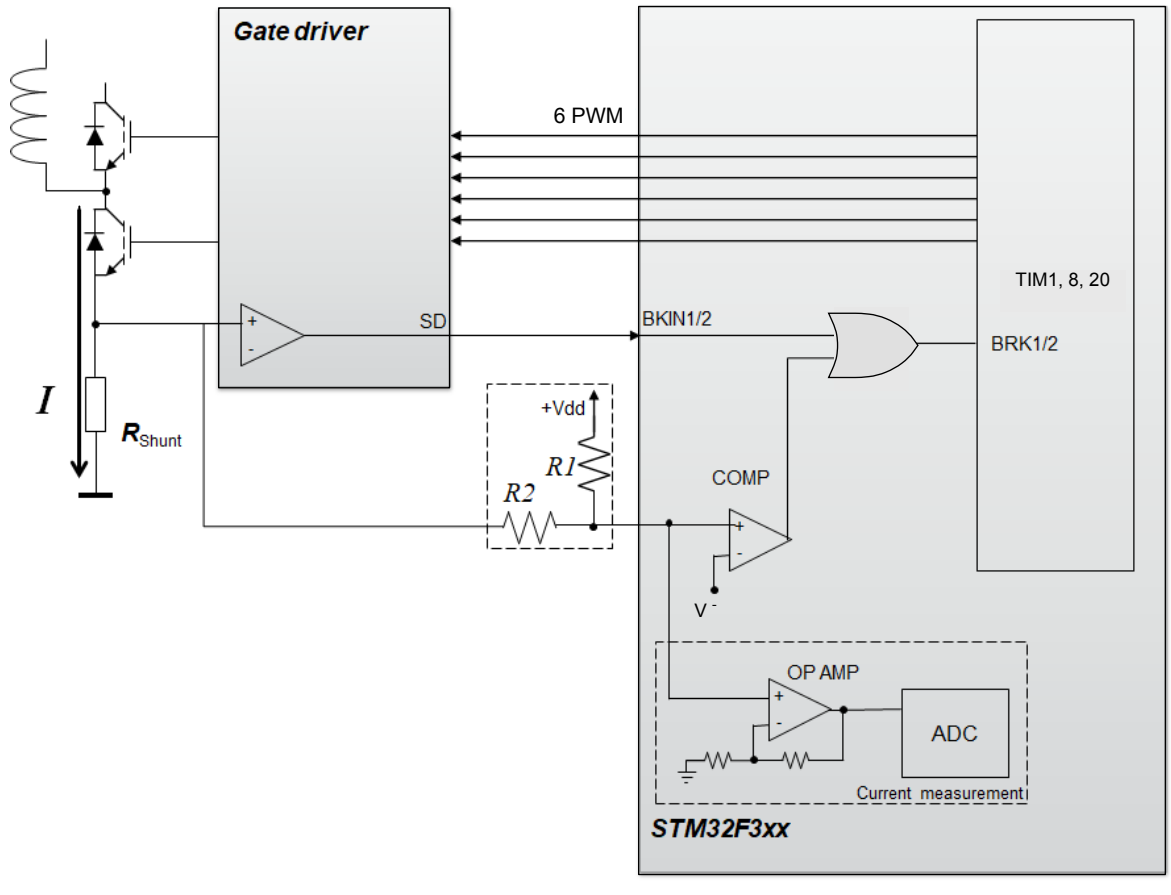
Table 8. Comparator output connected externally to break inputs, with high break polarity

Description	Register	Bit	Configuration
TIM1/8/20 BRK/BRK2 polarity	TIMx_BDTR	BKP or BK2P	1 (active high), it means that the external signal goes high during the fault
Comparator output polarity	COMPx_CSR(1)	COMPxPOL	0 (not inverted), comparators input connected as shown in previous sections
TIM1/8/20 BKIN/BKIN2 AF	GPIOxAFRL or GPIOxAFRH	-	AF enabled on BKIN/BKIN2 pin selected among available
TIM1/8/20 BRK/BRK2 enable	TIMX_BDTR	BKEor BK2E	1
COMPx out selection	COMPx_CSR(1)	COMPxOUTSEL	0001: TIM1 BRK 0010: TIM1 BRK2 0011: TIM8 BRK 0100: TIM8 BRK2 0101: TIM1 BRK2 + TIM8 BRK2 1100: TIM20 BRK 1101: TIM20 BRK2 1110: TIM1 BRK2 + TIM8 BRK2 + TIM20 BRK2

1. *In newer products, such as STM32H7P, this register is not present. Selection is made on TIMx side.*

The comparators output can be optionally enabled as an alternate function on the related GPIO pin, in push-pull or open-drain mode, for signaling to other devices or for debugging purposes.

Figure 12. Combining external and internal protection concept



6.4 Filtering the break input

Programmable filters are available to prevent break functions of advanced timers from being triggered on spurious events (switching noise for instance).

The digital filter feature is available on BRK and BRK2. It is not available on BRK_ACTH. That means that the digital filter is:

- available when the break source is external and comes from the external inputs BKIN/BKIN2.
- available when the break source is internal and connected to BRK or BRK2.
- not available when the break source is internal and connected to BRK_ACTH.

6.5 Locking the selected configuration

Electrical motor drives require a high level of reliability and robustness for the potential damages that may be caused in case of failure.

To increase robustness against software runaways, many STM32 microcontrollers come with a chain of peripherals featuring the lock feature, beginning from the mode of the GPIO pins used for sensing through comparators, operational amplifiers (OPAMP), and advanced timers, down to the GPIO pins used for driving, as shown in Figure 13.

In particular, BRK and BRK2 configurations can be locked using the LOCK bits in the TIMx_BDTR register. At least LOCK level 1 is recommended to freeze DTG/BKE/BKP/AOE/BKF/BK2F/BK2E/BK2P bits in the TIMx_BDTR register and OISx/OISxN bits in the TIMx_CR2 register until the next reset.

Figure 13. Comparator chain configuration locking

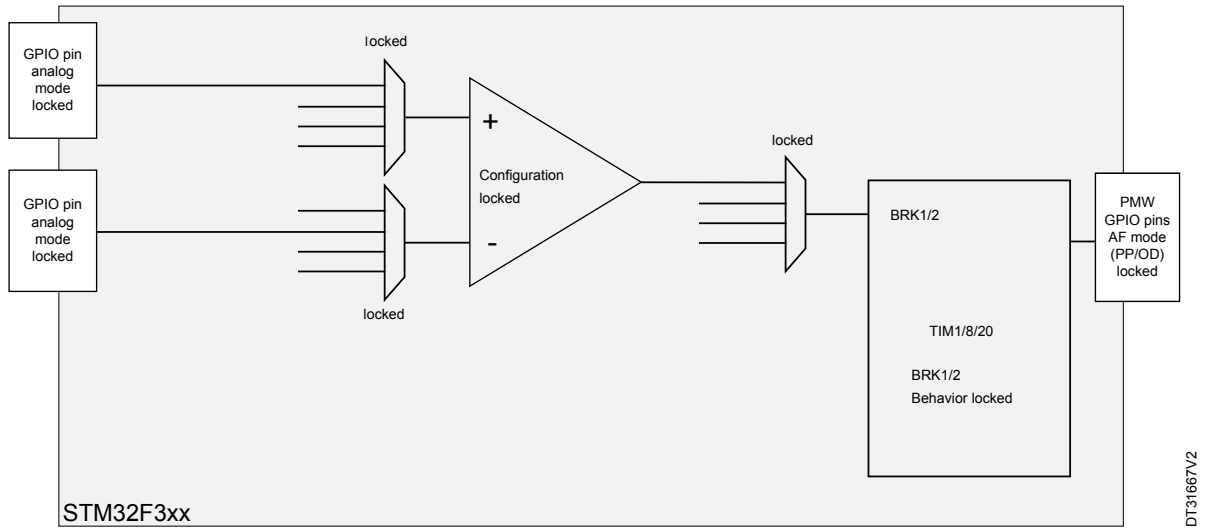


Table 9 summarizes the recommended settings for comparators.

Table 9. Register locking mechanism

Peripheral	Feature	Register	Comment
GPIO port x, pin y	Inverting input, pin mode selection	GPIOx_MODER register, MODERy bit to be configured in analog mode	-
GPIO port x, pin y	Inverting input, pin configuration locking	GPIOx_LCKR register, specific write sequence coded with LCKy bit	MODERy bit (in GPIOx_MODER register) now frozen until next reset
GPIO port w, pin z	Non inverting input, pin mode selection	GPIOw_MODER register, MODERz bit to be configured in analog mode	Not needed if an internal reference is selected
GPIO port w, pin z	Non inverting input, pin configuration locking	GPIOw_LCKR register, specific write sequence coded with LCKz bit	MODERz bit (in the GPIOw_MODER register) now frozen until next reset

Peripheral	Feature	Register	Comment
TIMER 1/8/20	BKIN/BKIN2 configuration locking	TIMx_BDTR register, LOCK bits	LOCK level 1 (at least) recommended: DTG bits in TIMx_BDTR register, OISx, and OISxN bits in TIMx_CR2 register and BKE/BKP/AOE bits in TIMx_BDTR register frozen until next reset

Appendix A

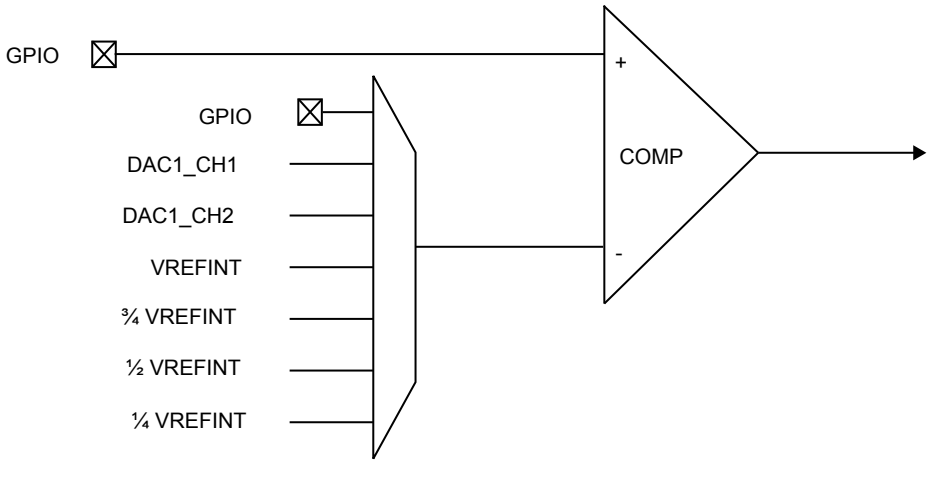
A.1 How to use the DAC to define thresholds

Concerning the network shown in Figure 10 and Figure 11, it is important to properly set the comparator inverting input voltage (V-) to define the threshold levels for overcurrent protection and overvoltage protection.

As shown in Figure 14 below, it is possible to set three different sources as inverting input for the comparator:

- An external reference (GPIO)
- A fixed internal reference (Vref, ¾ Vref, ½ Vref, ¼ Vref)
- A programmable internal reference (DAC)

Figure 14. Inverting input selection



Practical example: overcurrent protection using the offset network

This is the case of Figure 10 when the components inside the dotted line boxes are present. In this case, the formula to compute the overcurrent threshold is the following:

$$I_{th} = \frac{V^{-} - \left(V_{dd} \times \frac{R_2}{R_1 + R_2}\right)}{R_{shunt} \times \left(\frac{R_1}{R_1 + R_2}\right)}$$

Usually the R_1 and R_2 values are used to satisfy the current measurement needs. It is clear that using the internal reference for V- can lead to a threshold value Ith, which is not exactly coincident with the required one.
As explained in this practical example, the internal reference can be used only when there is no need to fine-tune the overcurrent threshold. Otherwise, it is necessary to use the external reference or the variable internal reference. The latter is recommended, because it does not require any external components.

Many STM32 microcontrollers include two 12-bit DAC channels that can be used for this purpose. For three-phase motor drives, it is possible to group three comparators to protect each leg of the inverter bridge versus overcurrent by setting the same DAC channel for all three inverter inputs.

The same can be done in case of dual-motor control with also having the possibility to define two different levels of protection, one for each motor.

Revision history

Table 10. **Document revision history**

Date	Revision	Changes
25-Nov-2013	1	Initial release.
05-Mar-2015	2	Updated cover page with STM32F3 series and adding RM references. Updated the whole document adding TIM20 and replacing STM32F30x/31 x by STM32F3 series. Updated *Section 1: Break function overview* adding *Table 3: Peripherals availability per STM32 devices*. Updated *Figure 1: Break feature implementation for TIM1, TIM8, and TIM20*. Updated *Figure 11: Comparator chain configuration locking*. Updated *Table 9: Register locking mechanism*.
30-Jun-2015	3	Updated *Section 2.2: TIM15/16/17 break implementation* removing the filter feature in BRK and BRK_ACTH paragraphs. Updated *Figure 5: Break feature implementation for TIM15, TIM16, and TIM17 for STM32F1 series devices* replacing filter/polarity by polarity. Updated *Table 4: Break input sources* adding “NA for TIM15/16/17” for 2 lines in BRK column.
03-May-2016	4	Updated cover page title and introduction with the application note applying to STM32 devices. Added *Table 1: Applicable products*. Updated *Section 1: Break function overview*. Added *Table 2: Timers and break input availability in STM32 devices*. Updated *Table 3: Peripherals availability per STM32 devices*. Updated *Section 2: Break implementation*. Updated *Figure 1, Figure 2, Figure 3, Figure 5, Figure 6, and Figure 7*. Updated *Table 4: Break input sources*. Updated *Table 5: Scenarios of PWM output status in response to internal/external break events*. Updated *Section 5: Using the break function with other MCU resources* adding a note. Updated *Section: BRK_ATCH*. Added *Section: Bidirectional break inputs*. Added *Figure 4: Output redirection*.
09-Mar-2022	5	Updated all document with STM32U series in: *Section 1: General information* *Section 4: Break implementation* *Section 5: Break sources summary* *Section 7: Using the break function with other MCU resources* Added: *Figure 4: Break feature implementation in advanced timers for STM32U5 series devices* *Figure 9: Break feature implementation for TIM15, TIM16, and TIM17 in STM32U5 series devices*
05-Jan-2023	6	Updated the whole document to add STM32 series information in: *Section Table 1: Applicable products* *Section Table 3: Timers and break input availability in STM32 devices* *Section Table 4: Comparator peripherals availability per STM32 device* *Section 4.1: TIM1/8/20 break implementation* *Section 4.2: TIM15/16/17 break implementation* *Section 5: Break sources summary*
06-Mar-2024	7	Added STM32U0 series. Updated: • Document title • Table 2. Timers and break input availability in STM32 devices • Table 3. Comparator peripherals availability per STM32 device
20-Feb-2025	8	Added STM32U3 series.

Date	Revision	Changes
		Updated: • Section Introduction • Section 2: Break function overview • Section 3.1: TIM1/8/20 break implementation • Section 4: Break sources summary • Section 6: Using the break function with other MCU resources • Section 6.1: Break function used for overcurrent protection • Section 6.2: Break function used for overvoltage protection • Section 6.5: Locking the selected configuration • Appendix A.1: How to use the DAC to define thresholds
19-Feb-2026	9	Added STM32C5 series. Updated: • Section Introduction • Section 2: Break function overview • Section 3.1: TIM1/8/20 break implementation • Section 3.2: TIM15/16/17 break implementation • Table 2. Timers and break input availability in STM32 devices • Table 3. Comparator peripherals availability per STM32 device
27-Oct-2026	10	Added : STM32G5 series. Updated: • Table 1. Applicable products • Table 2. Timers and break input availability in STM32 devices • Table 3. Comparator peripherals availability per STM32 device • Figure 11. Overvoltage protection network block diagram • Section 3.1: TIM1/8/20 break implementation • Section 3.2: TIM15/16/17 break implementation • Table 4. Break input sources

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