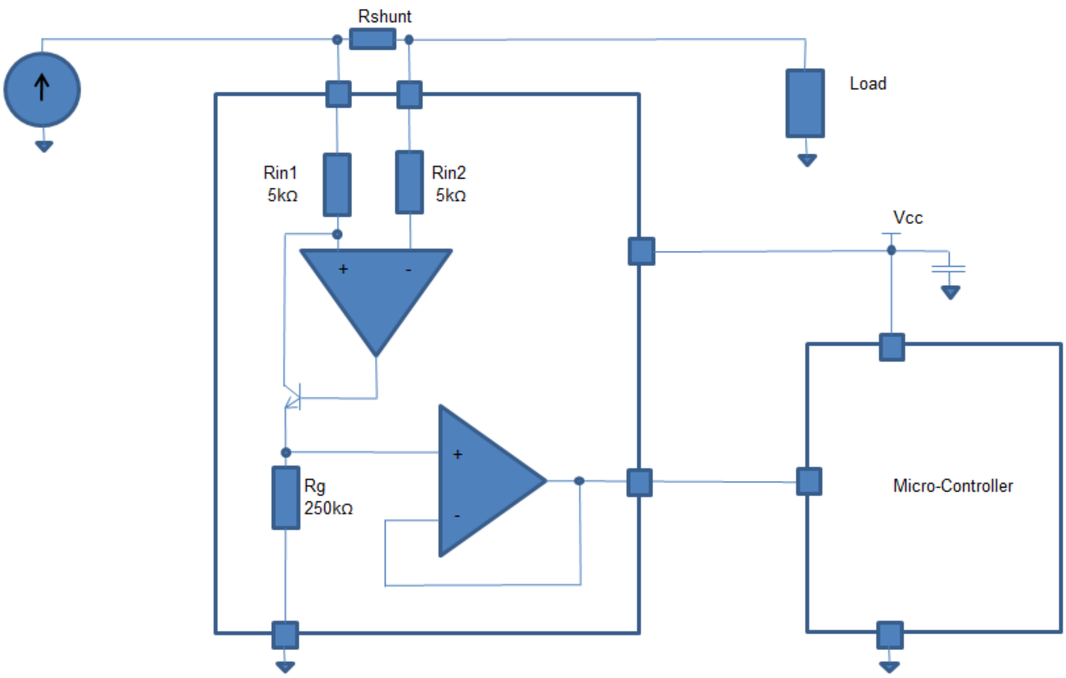
How to filter the input of a high-side current sensing

Introduction

This application note explains how to filter the input signal of a current sensing. The approach is especially useful for applications where the RF constraint is very important.

A high-side current sensing can amplify input differential signals at a common mode voltage well beyond the power supply rail. This common mode voltage in a current-sense amplifier such as the TSC101 can rise to 28 V. In the TSC103, it can go even higher. The device amplifies small voltages across a shunt resistor on the high-voltage rail and feeds it to a low-voltage ADC which is generally embedded into a microcontroller (see figure below). In many applications, the current-sense signal frequently needs to be filtered at the source, ie, across the sense resistor.

Figure 1. **Typical application schematic**



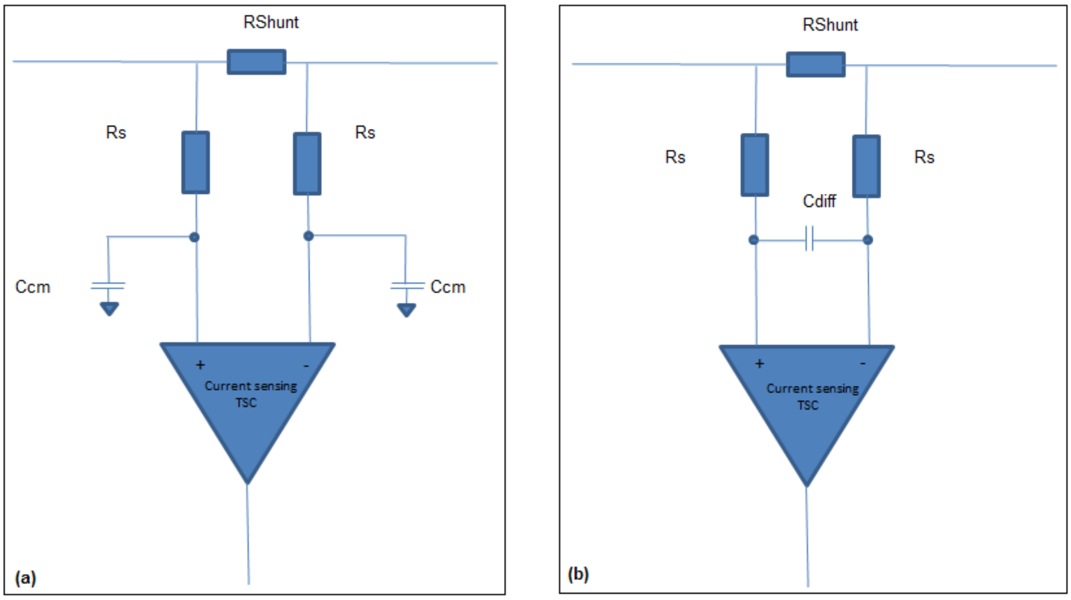
1 Application purpose

In an application such as a power supply or a DC-DC converter, the voltage output is generally noisy. Some spikes load the current. Alternatively, a temporary over voltage might occur creating either common mode or differential noise. Such high frequency signals may be demodulated by the current sensing device, resulting in an error in the current measurement.

Consequently, for power supply and DC-DC converter applications, it is necessary to filter the input path of the current sensing to improve the accuracy of the measurement. Such filters must be successfully implemented by choosing the right component values. If the wrong component values are selected, non-desired offset voltages and gain errors might be introduced, which compromise circuit performance.

Two filtering architectures can be used: a common mode filter and a differential mode filter as shown in figure Figure 2. Common mode (a) and differential mode (b) filters. These two methods of filtering can be combined for more efficient results. The common mode filter increases ESD immunity or filtered temporary overvoltage. The differential mode filter helps to smooth spiky load currents.

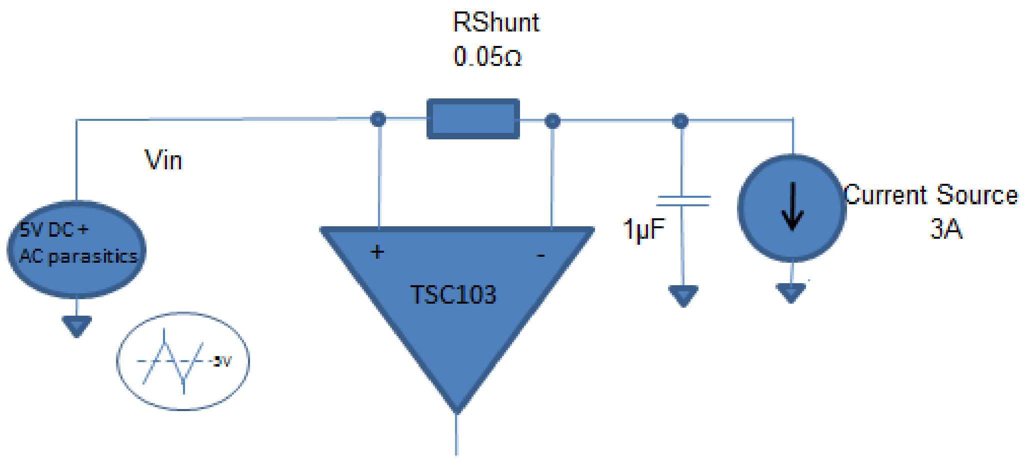
Figure 2. Common mode (a) and differential mode (b) filters



2 Solving the power supply problem

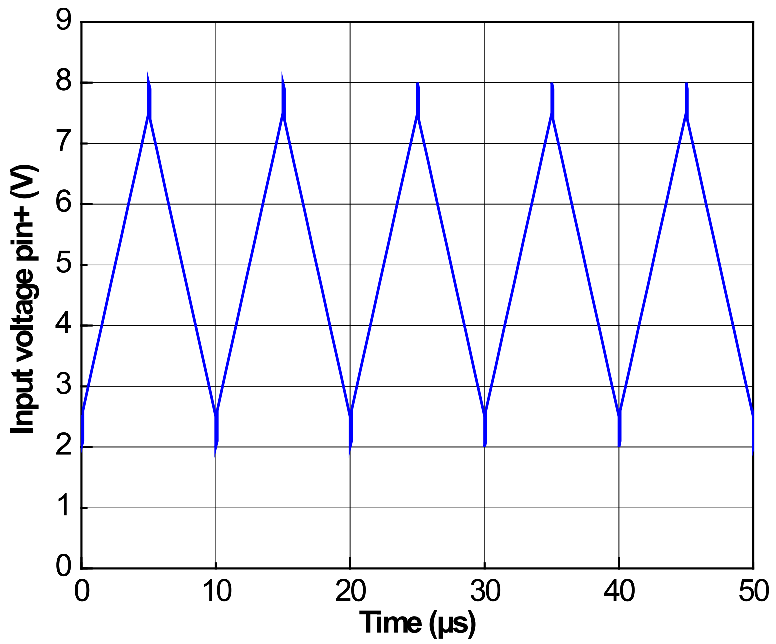
Power supply problems can be solved by considering a power supply that delivers 5 V and 3 A. The current is monitored with a TSC103 current sensing as shown in Figure 3. Application example .

Figure 3. Application example



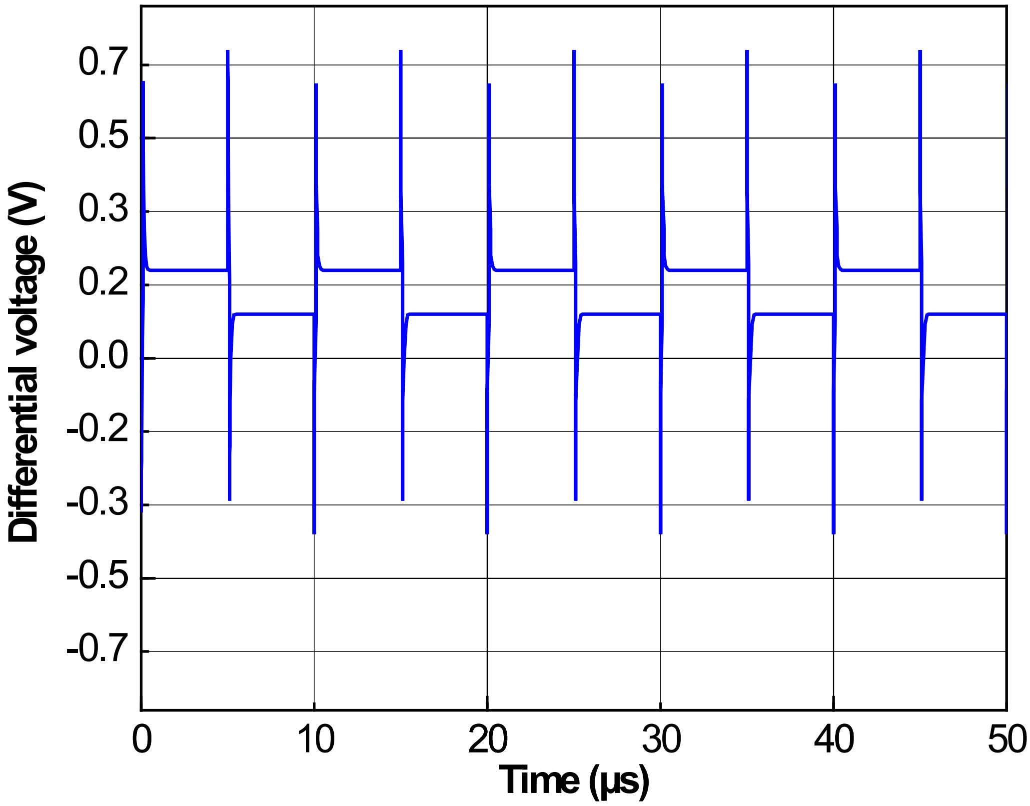
Considering a shunt of 0.05 Ω, the theoretical voltage seen at the input of the TSC103 is 150 mV. Due to the switching mode of the power supply, the provided 5 V has an undesirable high frequency signal as shown in Figure 4. Input pin+ voltage without filtering . This high frequency signal may impact the functioning of the TSC103.

Figure 4. Input pin+ voltage without filtering



The power supply delivers a 5-V DC with a parasitic AC signal at 100 kHz and spikes at high frequency (see Figure 5. Differential voltage without filtering). The question is how to correctly filter the signal before treatment by the TSC103?

Figure 5. Differential voltage without filtering



3 Differential mode filtering

Figure 6 shows a differential mode filter with a cut-off frequency at 8 kHz. Cut-off frequency is given by Equation 1:

$$f = \frac{1}{2 \cdot \pi \cdot 2Rs \cdot Cdiff} \cdot (1) \tag{1}$$

Figure 6. Differential mode filter at 8 kHz

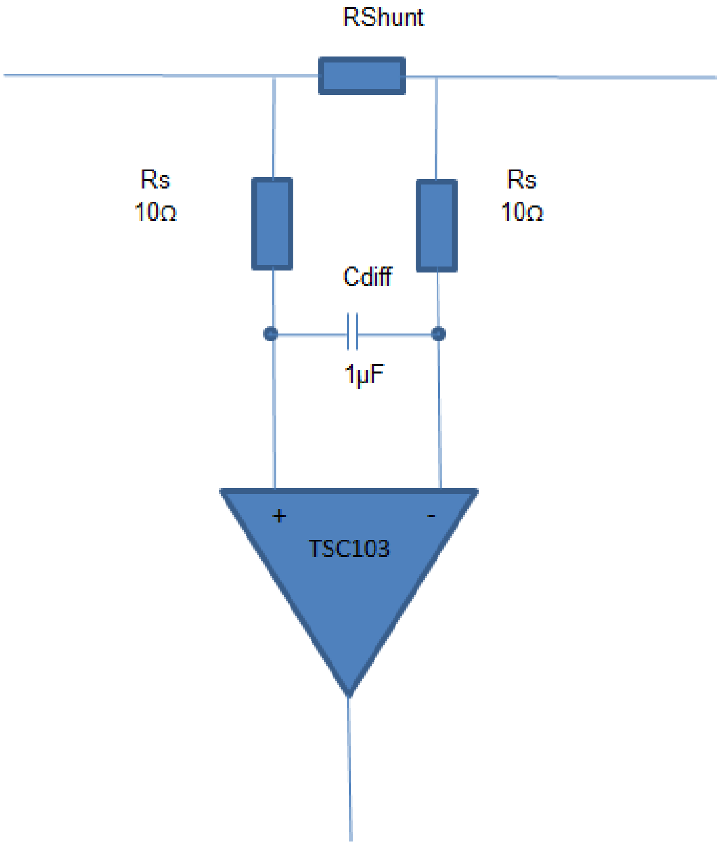
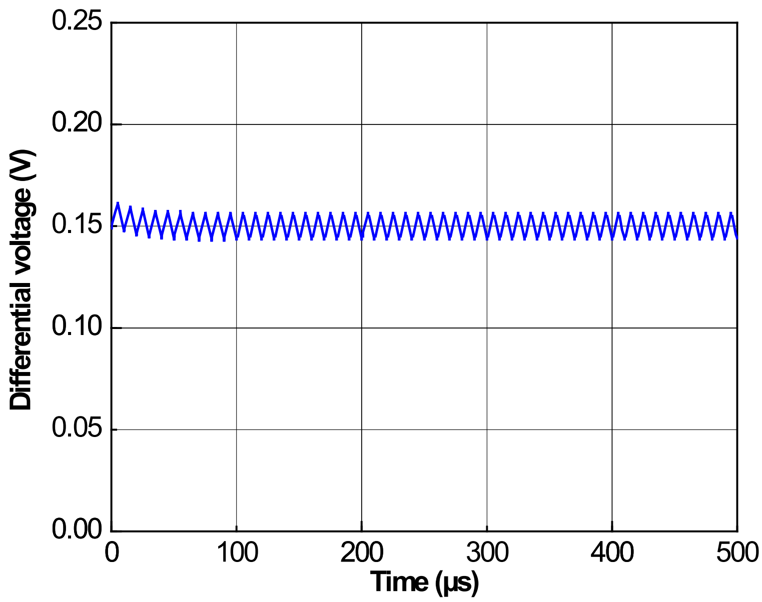


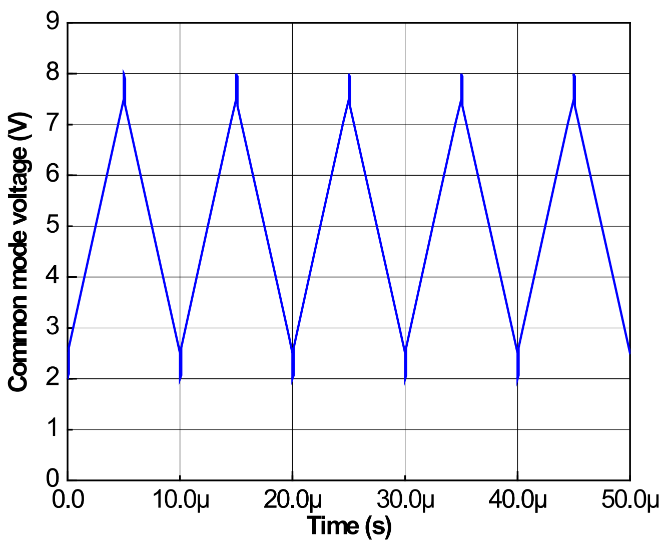
Figure 7. Differential voltage with a differential filter of 8 kHz shows the signal between pin+ and pin- of the TSC103. The high frequency has been correctly filtered.

Figure 7. Differential voltage with a differential filter of 8 kHz



However, the common mode voltage has not been filtered. Even if the TSC103 has an excellent CMRR (see Figure 17. CMRR vs. frequency) of up to 200 kHz, it is important to also remove the high frequency which might cause incorrect behavior (see Figure 8. Input pin+ voltage with a differential filter of 8 kHz).

Figure 8. Input pin+ voltage with a differential filter of 8 kHz



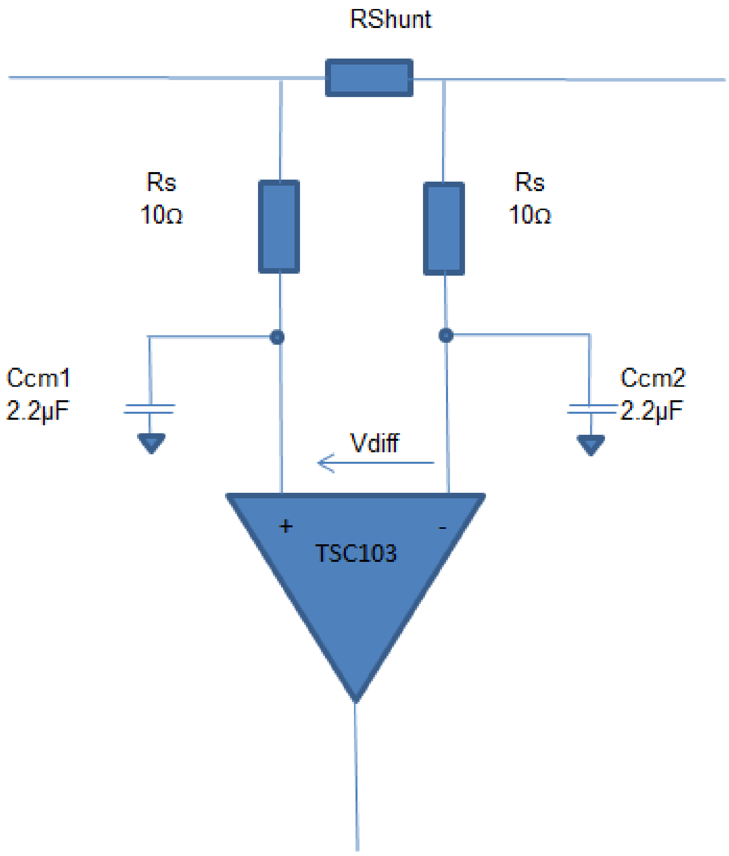
4 Common mode filtering

Figure 9 shows a common mode filter with a cut-off frequency at 7 kHz. The cut-off frequency is given by Equation 2:

$$f = \frac{1}{2 \cdot \pi \cdot Rs \cdot Ccm} (2) \quad (2)$$

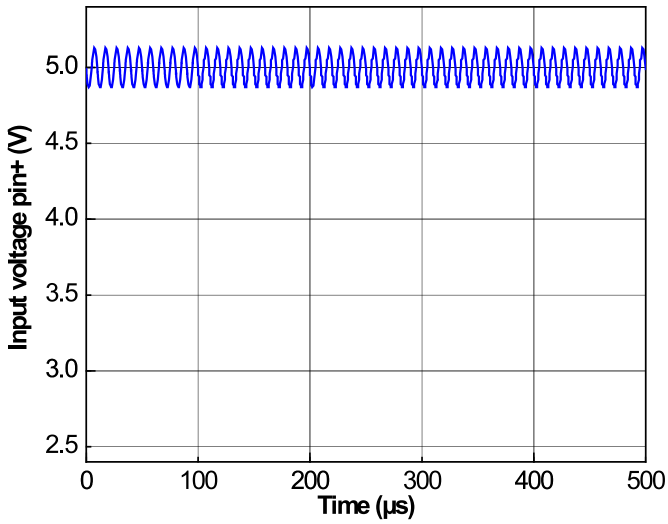
It is recommended to place the same low path filter on each input of the current sensing to equilibrate the two inputs. This avoids adding offset error. Note that particular care must be taken in the choice of the resistances and the capacitances.

Figure 9. Common mode filter at 7 kHz



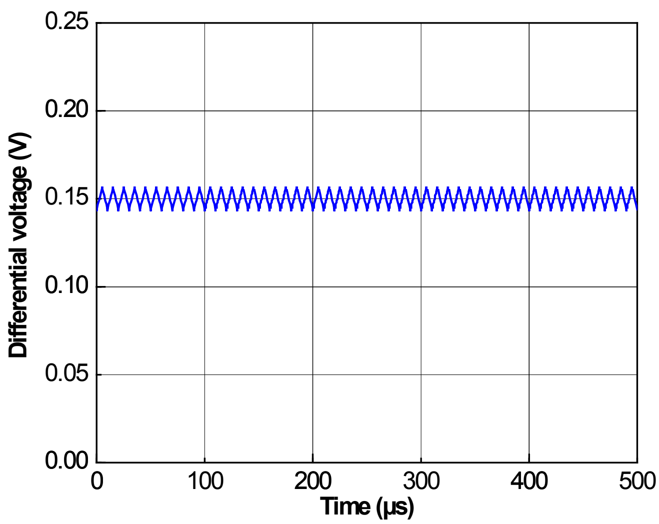
In Figure 10. Input pin+ voltage with Ccm perfectly matched, the high frequency on common mode has been removed with the filter shown.

Figure 10. **Input pin+ voltage with Ccm perfectly matched**



Differential mode can also be filtered as shown in Figure 11. Differential voltage with Ccm perfectly matched. This is the best case scenario where the two filtered capacitances (Ccm1 and Ccm2) are perfectly matched

Figure 11. **Differential voltage with Ccm perfectly matched**



Unfortunately, the capacitances used for filtering are already matched at about 20 %. It is important to take this into consideration because due to the mismatch of the capacitances and resistances, the filter cut-off frequency may be a bit different between the two inputs. In differential mode, this could cause an AC error. An AC error may in turn be amplified by the current sensing and cause additional error.

Equation 3 below expresses the transfer function using a common mode filter. To simplify the calculation, only the mismatch of the capacitance is taken into account (the mismatch of the resistances is generally low at about 1 %). Vin is the voltage source.

$$Vdiff \cong \frac{Vin.Rs.j.\omega(Ccm2 - Ccm1)}{(1+Rs.j.\omega.Ccm1)\times(1+Rs.j.\omega Ccm2)} \quad (3)$$

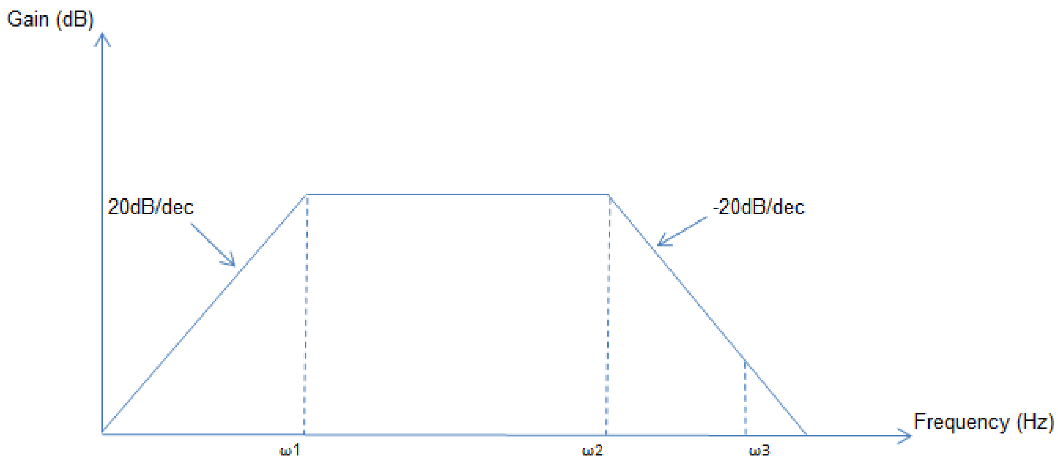
Equation 3 shows that if Ccm1 and Ccm2 are not perfectly matched a differential voltage is created on the input of the current sensing. Equation 3 also shows that two poles appear (see below).

$$\omega 1 = \frac{1}{2.\pi.Rs.Ccm1}$$

$$\omega 2 = \frac{1}{2.\pi.Rs.Ccm2}$$

The transfer function is illustrated in Figure 12. Bode diagram.

Figure 12. Bode diagram



Equation 3 is true for a sinusoidal signal. Normally, the input signal is decomposed in Fourier series (although this depends on the type of input signal) and a first approximate calculation is made taking only the fundamentals into account. From Equation 3 we can extrapolate that at frequencies much higher than ω2, the differential voltage error, due to the mismatch of the Ccm1 and Ccm2 capacitances, is given by Equation 4 below.

$$Vdiff \cong Vin \cdot \frac{Ccm2 - Ccm1}{Ccm2.Ccm1.Rs.\omega 3} \quad (4)$$

5 Estimating differential error

To estimate differential error (Vdiff), the example below considers that the input signal is a triangular one.

Vin = triangular AC at 100 kHz, 5 Vpp

Rs = 10 Ω

Ccm = 2.2 μF with a tolerance of 20 %

Ccm1 = 2.2 μF +20 % = 2.64 μF

Ccm2 = 2.2 μF -20 % = 1.76 μF

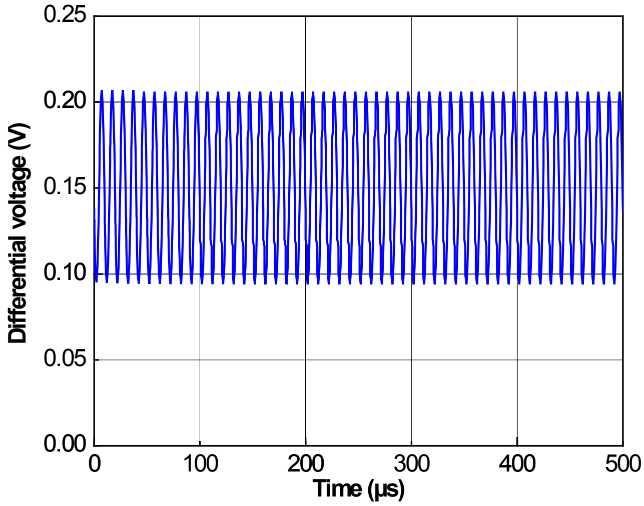
Note that the fundamental amplitude of a triangular signal is lower than the actual signal by a factor of $8/\pi^2$. Bearing this in mind, the estimated differential error can be calculated as follows:

$$Vdiff = 5 \cdot \frac{2.64 \cdot 10^{-6} - 1.76.10^{-6}}{2.64.10^{-6} \times 1.76.10^{-6} \times 10 \times 2 \times \pi \times 100.10^{3}} \times \frac{8}{\pi^2}$$

So, Vdiff = 122 mVpp.

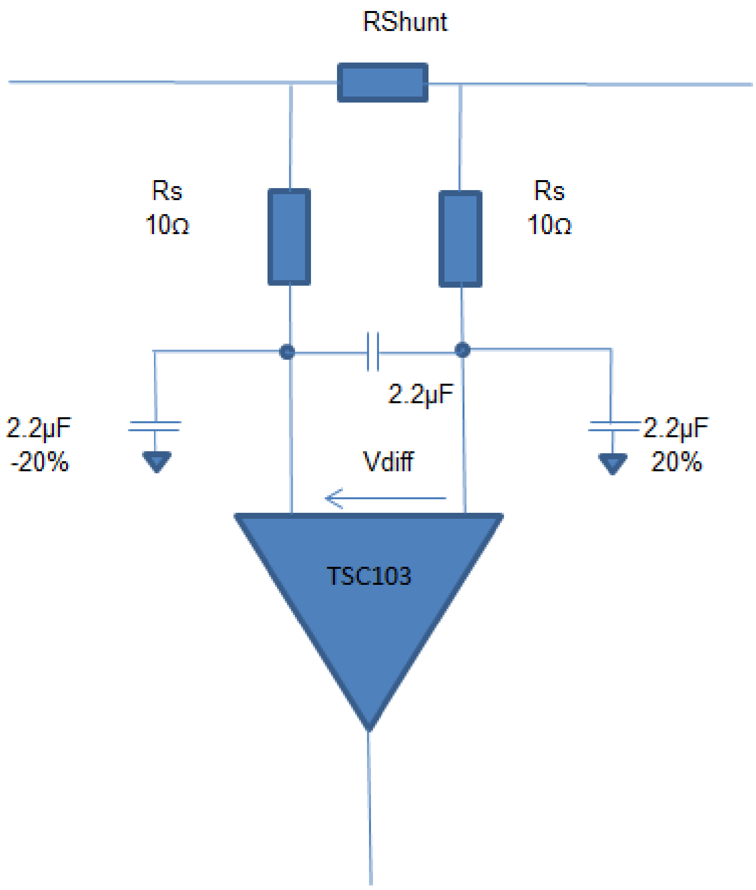
Due to a tolerance of 20% on the filtering capacitance, a theoretical ripple of 122 mVpp appears on the differential input of the current sensing. Going back to the time domain, the Figure 13. Differential voltage with Ccm1 and Ccm2 matched at 20 % shows the impact on the ripple due to the mismatching of the capacitances.

Figure 13. Differential voltage with Ccm1 and Ccm2 matched at 20 %



The ripple is 111 mVpp which means that, in the worst case scenario, Vsense could be equal to 205 mV instead of the expected value of 150 mV. This corresponds to an error of 37 %. To compensate the mismatching of the capacitances it is necessary to add one differential capacitance, as shown in Figure 14. Common and differential mode filter .

Figure 14. Common and differential mode filter



Equation 5 below expresses the transfer function of the common mode and differential mode filtering. To simplify the calculation, only the mismatch of the capacitance is taken into account. Vin is the voltage source.

$$Vdiff \cong \frac{Vin.Rs.j.\omega(Ccm2 - Ccm1)}{(1 + j.\omega.Rs(2.Cdiff + Ccm1)).\left(1 + j.\omega.Rs\left(\frac{2.Cdiff.Ccm1 + Ccm1^2}{2.Cdiff + Ccm1}\right)\right)} \quad (5)$$

A similar bode diagram to Figure 12. Bode diagram is obtained with the following poles:

$$\omega 1 = \frac{1}{2.\pi.Rs.(2.Cdiff + Ccm1)}$$

$$\omega 2 = \frac{2Cdiff + Ccm1}{2.\pi.Rs.(2.Cdiff + Ccm1 + Ccm1^2)}$$

$$\omega 3 = \text{Frequency of the input signal}$$

From Equation 5 we can extrapolate that at frequencies much higher than ω2, the differential voltage error, due to the mismatch of the Ccm1 and Ccm2 capacitances, is given by Equation below:

$$Vdiff \cong Vin \cdot \frac{Ccm2 - Ccm1}{Rs \cdot \omega 3 \cdot \left(2 \cdot Cdiff \cdot Ccm1 + Ccm1^2\right)}$$

We can now re-estimate the differential error (Vdiff) as follows:

$$\text{Vdiff} = 5 \cdot \frac{2.64 \cdot 10^{-6} - 1.76.10^{-6}}{10 \times 2 \times \pi \times 100 \times 10^{3} \times (2 \times 2.2.10^{-6} \times 1.76.10^{-6} + (1.76.10^{-6})^{2})} \times \frac{8}{\pi^{2}}$$

Vin = triangular AC at 100 kHz, 5 Vpp

Rs = 10 Ω

Ccm = 2.2 µF with a tolerance of 20 %

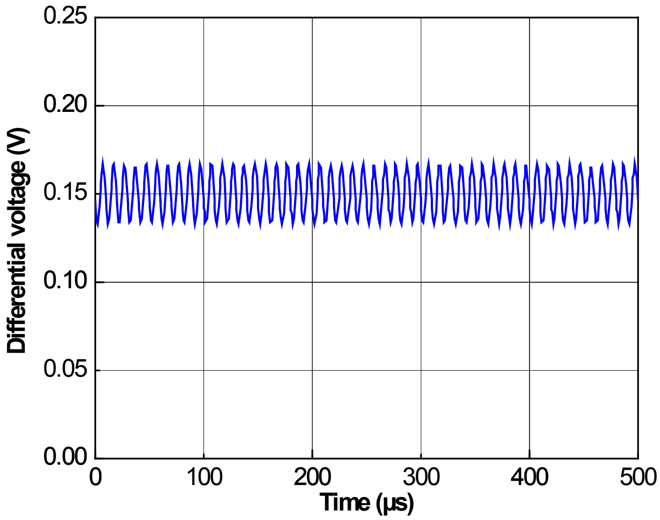
Ccm1 = 2.2 µF +20 % = 2.64 µF

Ccm2 = 2.2 µF -20 % = 1.76 µF

So, Vdiff = 52 mVpp.

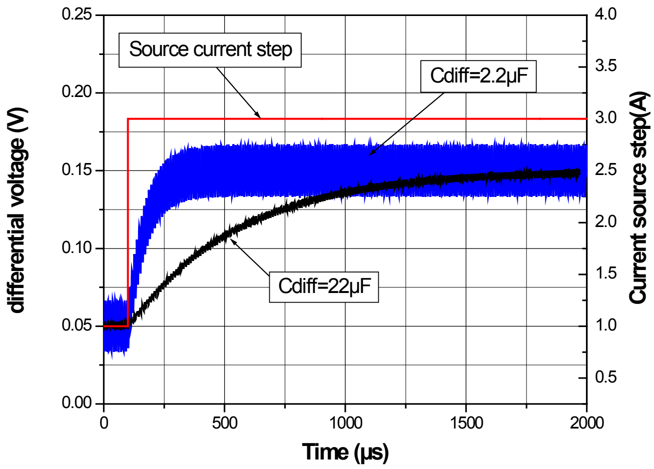
As a result of the differential capacitance, the ripple is 52 mVpp instead of 122 mVpp. Going back to the time domain, Figure 15. Differential voltage with Ccm and Cdiff = 2.2 µF shows the impact of the differential capacitance on the equilibration of the common mode filtering capacitance mismatch. The amplitude of the differential signal present on the input of the current sensing is 34 mV. Consequently, in the worst case scenario, an error of 10 % is obtained.

Figure 15. Differential voltage with Ccm and Cdiff = 2.2 µF



It is still possible to improve the filtering by increasing the differential capacitance. The drawback is that the response time increases. With a Cdiff = 22 µF, the error due to the ripple becomes negligible (1 %) but the response time is much greater. Figure 16. Differential voltage with a different value of Cdiff shows the response time of a 2 A step from the current source with Cdiff = 2.2 µF and 22 µF.

Figure 16. Differential voltage with a different value of Cdiff



In conclusion, the filtering capacitance mismatching impacts negatively on the accuracy of the current measurement. In contrast, the filtering resistance mismatching plays a non-negligible role on current measurement precision.

6 Influence of external serial resistances on accuracy

The TSC current sensing family has some trimmed input resistance. Any external resistance, added in series, produces mismatches leading to both gain and CMR errors. Such errors are typically calculated as follows (where Rin is the specified amplifier input resistance):

$$\text{Gain error (\%)} = 100 - 100 \cdot \frac{Rin}{Rin + Rs}$$

$$\text{CMR (dB)} = 20\log \cdot \frac{Rs.(Rs_{error}\%).2}{Rin}$$

The internal resistance of the TSC103 is 5 kΩ. Assuming that an external resistor of 100 Ω, with a tolerance of 1%, is used for filtering, the common mode rejection ratio due to these external components is 68 dB. There will be a direct impact on the whole CMR as the TSC103 has a minimum CMR of 90 dB.

The fact that Rs is quite big adds to the gain error of 2 %. This really impacts the performance of the device whose typical accuracy provides a maximum total error of 3 %. Therefore, care must be used when introducing input filters.

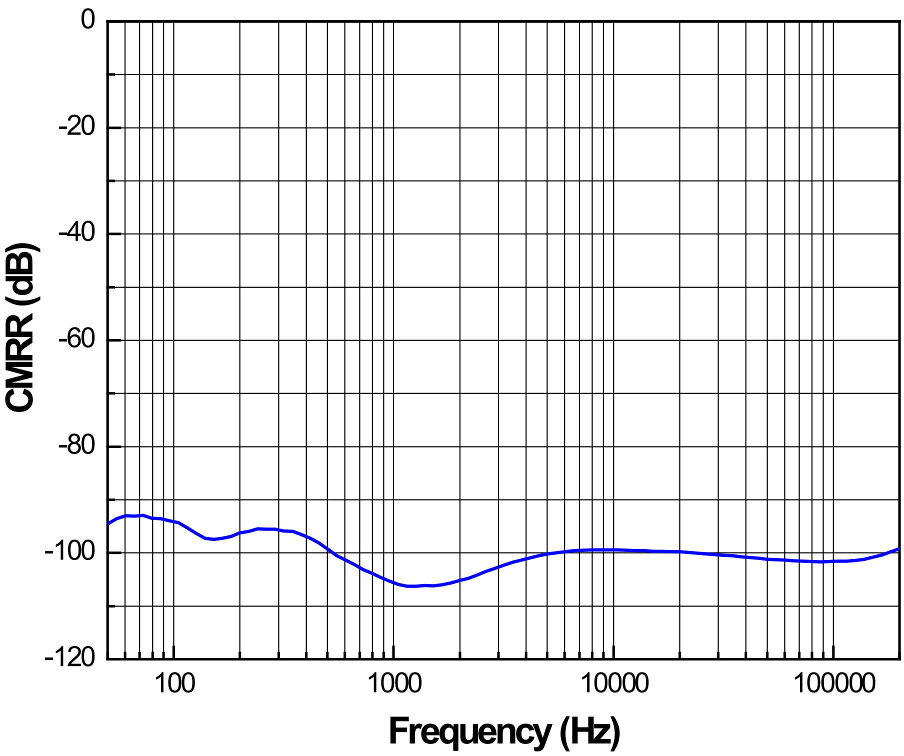
The only way to control this additional gain error is to ensure that the input series resistor, Rs, is small compared to Rin. Using a filter resistor that is less than 10 Ω is strongly recommended. This will ensure that the high original accuracy of the TSC103 is maintained.

Other parameters such as process variation or the temperature coefficient of the resistances must also be taken into consideration as possible error factors of current measurement. The calculation of total error due to external resistances is detailed in the application note AN4369 (Adjustable gain with a current sensing).

7 CMRR vs. frequency

The TSC103 current sensing device offers a very good CMRR vs. frequency (100 dB). The common mode signal up to 200 kHz (see Figure 17. CMRR vs. frequency), is filtered by the current sensing itself. However, to remove the high frequency signal, a common mode filter must be added to the application.

Figure 17. CMRR vs. frequency



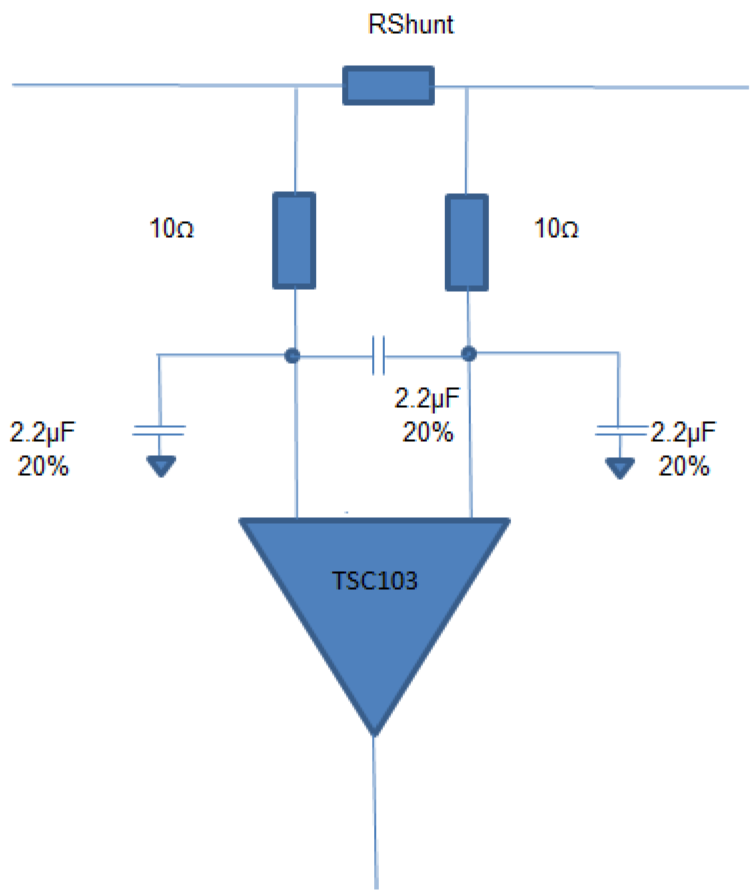
8 Conclusion

When a current sensing works in a high frequency noisy environment, it is mandatory to correctly filter the input of the TSC device, avoiding any parasitic offset due to the high frequency spikes. Both common mode and differential mode paths must be filtered. The best scenario is to match the capacitance between them to avoid adding differential error on the input of the current sensing.

Otherwise, it is important to combine a common mode filter and a differential mode filter to compensate the mismatch of the capacitance (see Figure 18. Configuration to filter a high frequency signal).

It is also important to match the resistances to avoid error on gain and consequently, an error on the precision of the current measurement.

Figure 18. Configuration to filter a high frequency signal



Revision history

Table 1. Document revision history

Date	Revision	Changes
30-Oct-2013	1	Initial release
26-Aug-2020	2	Updated Equation 1 in Section 3 Differential mode filtering

Contents

List of figures