AN4308
Application note

Methods of STCC2540, STCC5011, STCC5021 control

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Introduction

The STCC2540 and STCC5011/STCC5021 (STCCxxxx in text below) devices are combinations of a current limited USB port power switch with the USB 2.0 high-speed data line (D+/D-) switch and the USB charging port identification circuit. Applications include notebook PCs, all-in-one PCs, desktop PCs and other intelligent USB host devices.

The CTL1, CTL2 and CTL3 (CTLx in text below) logic inputs are used to select one of the various operating modes provided by the STCCxxxx. These modes allow the host device to actively select between:

- “Standard Downstream Port” (SDP) (active USB 3.0 data communication with 900 mA support or USB 2.0 data communication with 500 mA support)
- “Charging Downstream Port” (CDP) (active USB data communication with 1.5 A support)
- “Dedicated Charging Port” (DCP) (wall adapter emulation with no data communication and up to 2.5 A support).

The STCCxxxx devices also integrate the autodetect feature that supports both DCP schemes for the “Battery Charging Specification” (BC1.2, a maximum current draw of 1.5 A) enhanced of Korean tablets support and the divider mode (a maximum current draw of 1 A for the STCC5011 or 2 A for the STCC2540 and STCC5021) without the need for an outside user interaction.

The STCC5011/STCC5021 (STCC50x1 in text below) devices support the peripheral attachment detection in the G2/G3 power state and provide charging without the need of waking up the whole host system. The attachment detection is controlled by a combination of the EN and ATTACH_EN pins.

This Application note is focused on selecting the STCCxxxx operating mode by various methods of driving its control inputs (CTLx, EN, ATTACH_EN).

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1 Management of CTLx pins to select operating mode

The selection between the SDP, CDP and DCP operating modes is done through a set of control signals. The STCCxxxx devices have 3 logic inputs, the CTLx to select the suitable operating mode in each platform power state (S0 to S5). The combination of these 3 pins provides the following modes:

Table 1. CTLx truth table (assuming EN = 1, ATTACH_EN = 0)

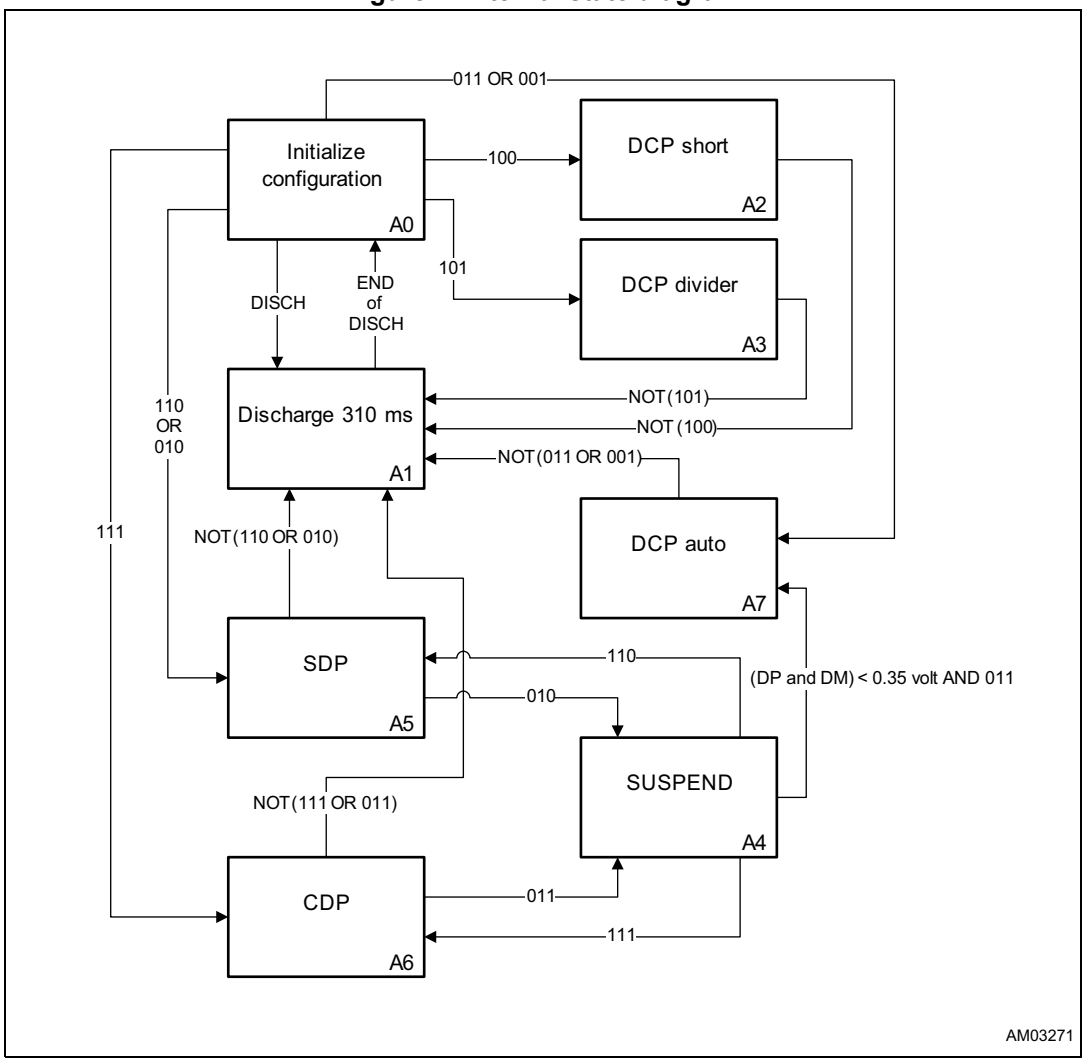
Suitable power state	CTL1	CTL2	CTL3	Mode	Advantages / use case
S0, S3	x	1	0	SDP with full remote wake-up support	If NB is on battery and the battery charge is low, it may be safer not to provide high current for charging PD(1). All PDs attached before transition from S0 to S3 are allowed to wake up the host to S0.
S0	1	1	1	CDP	NB can supply high current to PD
S3	0	1	1	CDP with remote wake-up support for low-speed PDs DCP auto for full-speed and high-speed PDs	Low-speed PDs attached before transition S0 to S3 are allowed to wake up the host to S0. Full-speed and high-speed devices are charged in S3 state.
S4/S5	0	0	1	Autodetect DCP mode	NB can charge PD with high current even if NB is OFF (high power SMPS ON). The most flexible, recommended charging mode.
S4/S5	1	0	0	Forced DCP BC1.2 mode	NB can charge PD with high current even if NB is OFF (high power SMPS ON). Standardized USB charging mode enhanced to support also Korean tablet PDs.
S4/S5	1	0	1	Forced DCP divider mode	NB can charge PD with high current even if NB is OFF (high power SMPS ON). Proprietary charging mode for Apple PDs.
Any, but mostly S4/S5	0	0	0	OFF	If NB battery is low, NB can stop charging process using either this combination or EN pin.

1. PD stands for portable device, NB for notebook. LS stands for low-speed PDs, FS for full-speed PDs and HS for high-speed PDs.

These pins may be controlled in different ways and depending on control types some combinations are useless.

Figure 1 shows the internal state diagram which manages these CTLx combinations.

Figure 1. Internal state diagram



2 Application dependent CTLx controlling options

2.1 CTLx pins controlled by GPIO from embedded controller

In this case, full remote wakeup in the S3 can be achieved by not toggling CTL1 when the NB enters the S3 state. Thus only 2 GPIOs are needed with the CTL1 and CTL2 tied together. The CTL3 pin can be user-configurable (BIOS, etc.) to enable/disable the charging feature.

Table 2. GPIO control truth table

Power state	CTL1 = CTL2	CTL3	Mode
S0/S3	1	0	SDP
S0/S3(1)	1	1	CDP
S4/S5	0	1	DCP auto
Any, typically S4/S5	0	0	OFF

1. No charging of full-speed/high-speed PDs in the S3, but full remote wakeup support

2.2 CTLx pins controlled by $\overline{\text{SLP\_Sx}}$ signals from Intel® chipset

New Intel chipset such as Chief River, X79 (Padsburg), NM10 (Pinetrail) have sleep signals linked to NB power states, described as the $\overline{\text{SLP\_Sx}}$:

Table 3. $\overline{\text{SLP\_Sx}}$ truth table

Power state	$\overline{\text{SLP\_S3}}$	$\overline{\text{SLP\_S4}}$	$\overline{\text{SLP\_S5}}$
S0	1	1	1
S3	0	1	1
S4	0	0	1
S5	0	0	0

The 2 signals $\overline{SLP\_S3}$ and $\overline{SLP\_S4}$ can be used to control CTLx pins: the CTL1 tied to the $\overline{SLP\_S3}$ and the CTL2 tied to the $\overline{SLP\_S4}$. Thus using only 1 GPIO from embedded controller (again the CTL3 pin can be user-configurable (BIOS, etc.) to enable/disable the charging feature), we can control the following modes:

Table 4. $\overline{SLP\_Sx}$ control truth table

Power state	$\overline{CTL1}$ = $\overline{SLP\_S3}$	$\overline{CTL2}$ = $\overline{SLP\_S4}$	CTL3 = GPIO EC	Mode
S0	1	1	0	SDP
S0	1	1	1	CDP
S3	0	1	0	Full remote wakeup
S3	0	1	1	LS devices: remote wakeup. FS, HS devices: DCP auto.
S4/S5	0	0	1	DCP auto
S4/S5	0	0	0	OFF

If CTL3 control is not necessary, the CTL3 can be driven to logic 1[(a)]:

Table 5. Simplified $\overline{SLP\_Sx}$ control truth table

Power state	$\overline{CTL1}$ = $\overline{SLP\_S3}$	$\overline{CTL2}$ = $\overline{SLP\_S4}$	CTL3 pull-up	Mode
S0	1	1	1	CDP
S3	0	1	1	LS devices: remote wakeup. FS, HS devices: DCP auto.
S4/S5	0	0	1	DCP auto

The device can be powered on/off using the EN pin.

a. Internal pull-up on the CTL3 is a metal option, not implemented in current versions of STCCxxxx devices.

2.3 CTLx pins controlled by signals SUSPEND and AC_ADAPTER

In this case, the charging modes are enabled only when the system is powered from AC adapter.

Table 6. SUSPEND and AC_ADAPTER control truth table

Power state	CTL1 = CTL2 = SUSPEND	CTL3 = AC_ADAPTER	Mode
S0	1	0	SDP
S0	1	1	CDP
S3/S4/S5	0	1	DCP auto
S3/S4/S5	0	0	OFF

The drawback of this solution is that it doesn't support remote wakeup in the S3.

Another way may be to use a GPIO from EC to control the CTL2.

Table 7. SUSPEND, AC_ADAPTER and GPIO control truth table

Power state	CTL1 = SUSPEND	CTL2 = GPIO	CTL3 = AC_ADAPTER	Mode
S0	1	1	0	SDP
S0	1	1	1	CDP
S3	0	1	0	SDP
S3	0	1	1	LS devices: remote wakeup. FS, HS devices: DCP auto.
S4/S5	0	0	1	DCP auto
S4/S5	0	0	0	OFF

Or to use 1 GPIO only and the CTL3 pulled-up[b]:

Table 8. SUSPEND and GPIO control truth table

Power state	CTL1 = SUSPEND	CTL2 = GPIO	CTL3 pull-up	Mode
S0	1	1	1	CDP
S3	0	1	1	LS devices: remote wakeup. FS, HS devices: DCP auto.
S4/S5	0	0	1	DCP auto

The device can be powered on/off using the EN pin.

b. Internal pull-up on the CTL3 is a metal option, not implemented in current versions of STCCxxxx devices.

3 Management of the EN pin to control the power consumption

The STCC2540 (and also the STCC50x1) device offers two states where all functionalities are turned off:

- EN = 0, CTLx ignored (for the STCC50x1 also ATTACH_EN = 0 condition applies)
- EN = 1, CTLx = 000

Although from functional point of view these states are almost equivalent, they differ in consumption. In the first case (EN = 0) the consumption of the STCCxxxx is the lowest possible (up to 1 μA) but there is one GPIO needed to control the EN pin, in the second case (CTLx = 000) the consumption is 65 μA but no more GPIO is necessary in most cases.

3.1 EN tied to V_{IN}

This is the simplest case. No more GPIO is necessary. To turn off the device, it is enough to set the CTLx = 000. The drawback is the consumption in the OFF state which is 65 μA.

The EN can also be connected to the POWER GOOD signal of the 5 V SMPS powering the V_{IN} to increase the robustness of the platform (the STCCxxxx device is powered on after the SMPS provides valid output voltage).

3.2 EN driven by GPIO

This case provides more flexibility (the device can be disabled in any case, e.g. if it reports a fault condition) and lowest power consumption in the OFF state. However it needs one more GPIO which complicates the implementation in many platforms.

4 Management of the STCC50x1 attach detector

The attach detector is controlled by the combination of EN and ATTACH_EN inputs according to *Table 9*:

Table 9. Attach detector truth table

EN	ATTACH_EN	Attach detector
0	0	Disabled
0	1	**Enabled**
1	0	Disabled
1	1	Disabled

The goal of the attach detector is to allow the host to turn off the 5 V SMPS (high power supply) for V_{IN} when it is not necessary. This decreases the power consumption to the lowest possible level. In the attach detect mode, the consumption of the STCC50x1 is 12 µA only. After the PD attach is detected, the STCC50x1 asserts the $\overline{\text{CHARGING}}/\overline{\text{ATTACH}}$ output which allows enabling the 5 V SMPS.

Typically the attach detector is useful in S4/S5 states only. In the S0 to S3, the 5 V SMPS is typically always turned on.

The truth table for the 5 V SMPS supply typically looks as *Table 10*:

Table 10. Truth table for 5 V SMPS

Power state	EN	ATTACH_EN	5 V SMPS for V_{IN}
S0	1	0 (X)	Always enabled
S3	1	0 (X)	Always enabled
S4/S5	1	0 (X)	Always enabled, attach detector disabled
S4/S5	0	1	Enabled after attach detect ($\overline{\text{CHARGING}}/\overline{\text{ATTACH}} = 0$) otherwise disabled
S4/S5	0	0	Always disabled

To achieve this truth table, the enable input of the 5 V SMPS for V_{IN} should be controlled by combination of the STCC50x1 $\overline{\text{CHARGING}}/\overline{\text{ATTACH}}$ output and a GPIO or a chipset signal. For Intel chipset, a good candidate is the $\overline{\text{SLP\_S4}}$ signal described in *Section 2.2 on page 5*.

The truth table for this case is following:

Table 11. 5 V SMPS truth table for $\overline{\text{SLP\_S4}}$ and $\overline{\text{CHARGING}}/\overline{\text{ATTACH}}$ control

Power state	$\overline{\text{SLP\_S4}}$	$\overline{\text{CHARGING}}/\overline{\text{ATTACH}}$	5V_SMPS_EN
S0	1	X	ON
S3	1	X	ON
S4/S5	0	1 (attach not detected)	OFF
S4/S5	0	0 (attach detected)	ON

It results to simple logical function: 5V_SMPS_EN = $\overline{\text{SLP\_S4}}$ + $\overline{\text{CHARGING}}/\overline{\text{ATTACH}}$.

This function can be realized either using single gates or simply using discrete MOSFETs and pull-ups to V_{DD}.

4.1 EN and ATTACH_EN controlled by GPIOs

This is the most flexible case consuming most GPIOs, thus not applicable in many applications. The functionality can be programmed exactly as demanded by the application.

4.2 ATTACH_EN = CTL3, CTLx pins controlled by $\overline{\text{SLP\_Sx}}$ signals from Intel chipset

The 2 signals $\overline{\text{SLP\_S3}}$ and $\overline{\text{SLP\_S4}}$ can be used to control CTLx pins: the CTL1 tied to the $\overline{\text{SLP\_S3}}$ and the CTL2 tied to the $\overline{\text{SLP\_S4}}$. Thus using only 1 GPIO from embedded controller (again the CTL3 pin can be user-configurable (BIOS, etc.) to enable/disable the charging feature) and implementing *Table 10: Truth table for 5 V SMPS* described above, we can control the following modes:

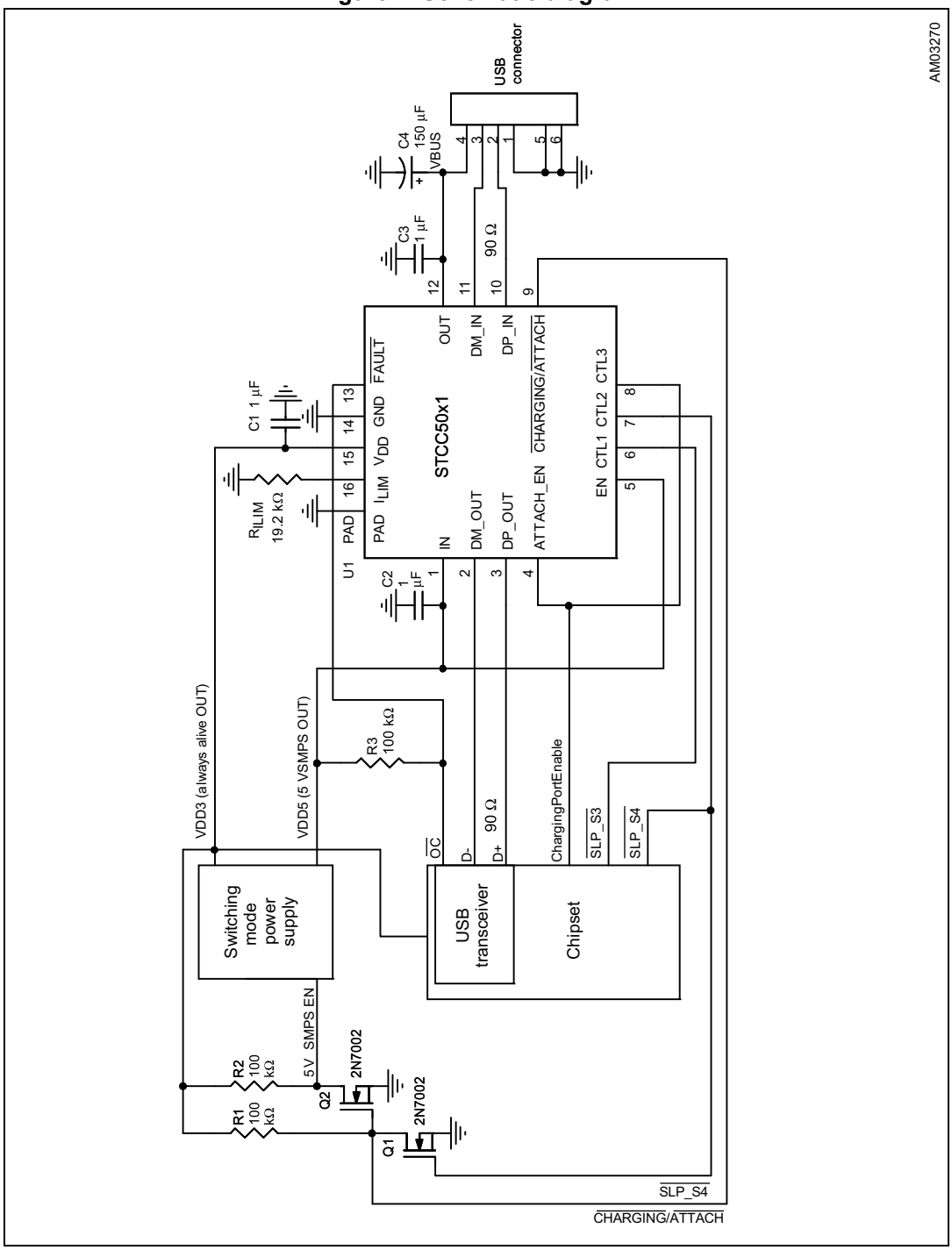
Table 12. STCC50x1 truth table for $\overline{\text{SLP\_Sx}}$ and GPIO control

Power state	$\overline{\text{CTL1}}$ = $\overline{\text{SLP\_S3}}$	$\overline{\text{CTL2}}$ = $\overline{\text{SLP\_S4}}$	ATTACH_EN = CTL3 = GPIO from EC	Mode
S0	1	1	0	SDP
S0	1	1	1	CDP
S3	0	1	0	SDP full remote wakeup
S3	0	1	1	CDP LS remote wakeup / FS, HS DCP auto.
S4/S5	0	0	1	EN = 0: Attach detection. EN = 1: DCP auto.
S4/S5	0	0	0	OFF

5 STCC50x1 application example

The easiest implementation using Intel chipset signals, one GPIO allowing the user to enable/disable the charging mode and discrete realization of 5 V SMPS control is shown in *Figure 2*.

Figure 2. Schematic diagram



The ChargingPortEnable is the GPIO allowing the user to enable/disable the charging mode support in the BIOS. For fully automatic operation without needing any GPIO, the CTL3 and ATTACH_EN can be permanently connected to V_{DD}.

The operating modes are following:

Table 13. Operating modes

Power state	ChargingPortEnable = 0	ChargingPortEnable = 1
S0	SDP	CDP
S3	SDP with remote wakeup for all devices	CDP with remote wakeup for low-speed devices DCP auto in other cases
S4/S5	OFF	OFF until attach detected DCP auto after attach detected

Note: ***Important:*** *The ChargingPortEnable GPIO must be latched in the S0 state when the operating system is running. Toggling it under running operating system causes V_{BUS} discharge pulse and may lead to data transfer interruption!*

6 Revision history

Table 14. Document revision history

Date	Revision	Changes
17-Jun-2013	1	Initial release.