AN4350
Application note

High power factor LED driver with constant voltage regulation based on HVLED815PF

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Introduction

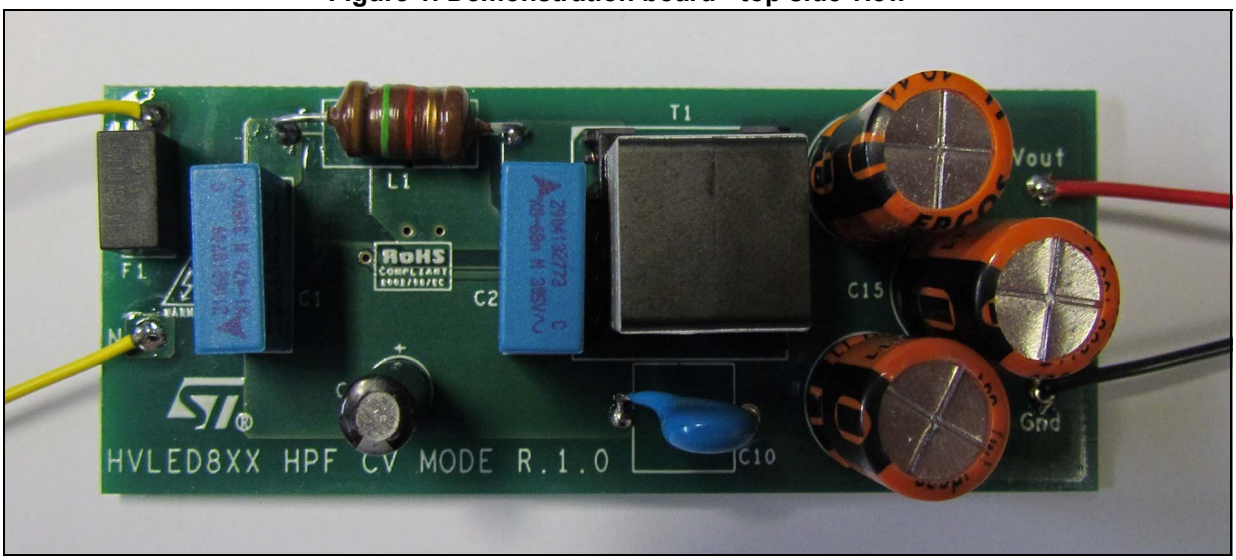
The EVLHVLED815W8CV demonstration board shows how to implement a high power factor LED driver with a constant voltage regulation, using the single-stage primary side HVLED815PF controller.

The HVLED815PF device is an integrated power controller with primary side control to achieve the LED current regulation within ± 5%.

It also has a primary side voltage regulation and this AN shows how to reach the high power factor with the constant voltage (CV) regulation.

The device incorporates an 800 V avalanche rated FET and fits in a standard SO-16 package. An internal start-up circuit eliminates the need for an external start circuitry reducing the component counts/space and increases system efficiency.

Figure 1. Demonstration board - top side view



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1 Features and specification

The main features of the demonstration board are:

- Output constant voltage (CV regulation)
- High power factor - PF > 0.98
- High efficiency - up to 88%
- Primary side regulation - no optocoupler
- Fully isolated output (flyback topology)
- Tight output voltage regulation < ± 3%
- Low total harmonic distortion - THD < 30%
- Automatic self-supply (internal high voltage startup)
- Minimum component count (internal Power MOSFET)

The main electrical specification requirements of the driver are summarized in the list:

- Input voltage (V_{IN}) 230 Vrms (200 - 265 Vac)
- Output voltage (V_{OUT}) 25 V
- Output voltage ripple (ΔV_{OUT}^{pk-pk}) < 3%
- Maximum output current (I_{OUT}^{MAX}) 310 mA
- Overcurrent protection (I_{OUT}^{CC}) 375 mA
- Maximum output power (P_{OUT}^{MAX}) 7.8 W
- LED driver efficiency (η) > 0.85%
- Minimum switching frequency (F_{sw}^{MIN}) 100 kHz
- Reflected voltage (V_R) 100 V

2 Circuit description and design guidelines

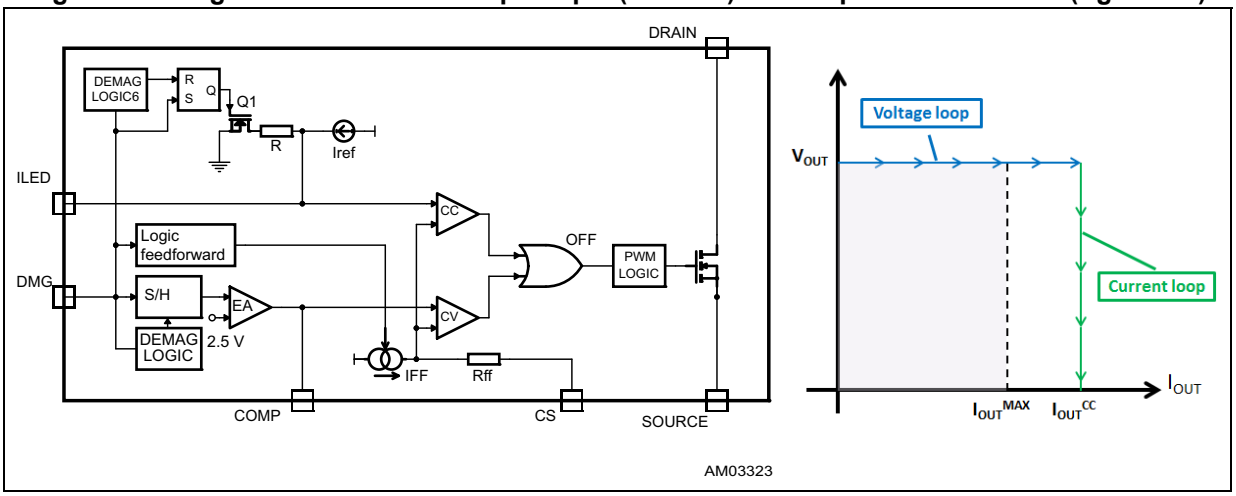
2.1 Preliminary consideration

The HVLED815PF controller is specifically designed to work as a constant current (CC) LED driver with a primary side regulation (PSR) and a high power factor (HPF) capability.

As shown on the left side of *Figure 2*, the HVLED815PF device incorporates two control loops: the current control loop (constant current - CC) trough the ILED pin regulates the LED output current (ILED = I_{OUT}^{CC}) and the voltage control loop (constant voltage - CV) trough the COMP pin regulates the output voltage during the open-LED fault condition.

The voltage control loops can then be used to regulate the output voltage when the output current is lower than the maximum deliverable current (I_{OUT}^{CC}) resulting in an output characteristic showed on the right side of *Figure 2*.

Figure 2. Voltage and current control principle (left side) and output characteristic (right side)



Starting from the standard application schematic (see Figure 1: “Application circuit for high power factor LED driver - single range input” in the HVLED815PF datasheet for the details) the constant current LED driver can be easily “converted” into
a constant voltage LED driver (CV) still keeping the high power factor and low total harmonic distortion (THD).

The high power factor is implemented adding through the R_{PF} resistor a contribution proportional to the V_{IN} input voltage on the CS pin: as a consequence the input current is proportional to the input voltage during the line period, implementing the high power factor correction.

In the CC LED driver the R_{OS} resistor has been mainly used to add on the CS pin a positive contribution proportional to the average value of the input voltage (V_{IN}) in order to keep a good line regulation. The second advantage of the contribution trough the R_{OS} resistor is to keep a good total harmonic distortion (THD) over the line range, because adding a small offset on the CS pin the input current can go to zero when the input voltage is close to zero.

When implementing a CV LED driver the voltage control loop works to keep the output voltage constant and independent from the input voltage, so the contribution proportional to the average value of the input voltage is no more needed.

A small offset on the CS is still useful to keep a good THD and so it can be added using a resistor from the VCC pin instead of a partitioning from the input voltage resulting in a reduction of the dissipated power and the component count/size.

The V_{OUT} output voltage is regulated through the CV loops and it has to be designed in order to have system bandwidth much lower than current loop bandwidth (voltage loop BW << 100 Hz - 120 Hz); the current loop is instead used to set the maximum deliverable current $I_{OUT}{}^{CC}$.

The design can be set defining an equivalent current sense resistor according to the standard HVLED815PF equation for the output current setting:

Equation 1

$$R_{SENSE\_EQ} = \frac{n}{2} \bullet \frac{V_{CLED}}{I_{OUT}{}^{CC}}$$

where *n* is the transformer ratio between the primary (N_P) and secondary side (N_S), V_{CLED} is the internal equivalent reference voltage (V_{CLED} = 0.2 V). See the HVLED815PF datasheet for more details.

2.2 Transformer selection

The main parameters of the flyback transformer (L_P, N_P, N_S, N_{AUX}, L_{LK}) have to be designed in order to sustain the desiderated output voltage (V_{OUT}), the maximum output power (P_{OUT}), the device supply (V_{CC}) and the desiderated reflected voltage on the primary side (V_R).

The transformer magnetization inductance (L_P) is selected as a trade-off between the maximum switching frequency (internally limited up to 166 kHz) and the maximum output power, ~~in~~ according to *Equation 2*:

Equation 2

$$L_{P\_MAX} = \frac{Vin_{MIN}}{\left(1 + \frac{Vin_{MIN}}{V_R}\right)} \bullet \frac{1}{Fsw_{MIN}} \bullet \frac{1}{I_P \bullet \sqrt{2}}$$

where I_P is the primary peak current and it can be estimated using *Equation 3*:

Equation 3

$$I_P(Vin, Iout) = I_{out_{MAX}} \bullet \left(2 \bullet \frac{N_P}{N_S}\right) \bullet \left(1 + \frac{V_R}{\eta \bullet VIN_{MIN}}\right)$$

The ratio between the primary (N_P) and secondary (N_S) winding can be selected to reach the desiderated reflected voltage (V_R), using *Equation 4*:

Equation 4

$$\frac{N_P}{N_S} = \frac{V_R}{V_{OUT} + V_D} \cong \frac{V_R}{V_{OUT}}$$

where V_R is the desiderated reflected voltage, V_D the forward voltage of the output diode.

The V_R reflected voltage is selected as a trade-off between efficiency (higher V_R means lower switching losses on the flyback Power MOSFET) and the absolute voltage on the primary side switching node (higher V_R means higher spike voltage on the Power MOSFET's drain). Typical range of this parameter is between 70 V and 140 V.

Assuming a desiderated reflected voltage of 100 V the ratio becomes:

Equation 5

$$\frac{N_P}{N_S} = \frac{V_R}{V_{OUT} + V_D} = \frac{100V}{25V + 0.8V} = 3.87$$

The ratio between the auxiliary (N_{AUX}) and primary (N_P) winding has to be selected to guarantee the supply voltage for the IC when the output voltage is regulated (during the startup the IC supply voltage is generated by the internal high voltage startup).

Equation 6

$$\frac{N_S}{N_{AUX}} = \frac{V_{OUT} + V_D}{V_{CC(IC)}}$$

where typically the IC voltage is designed in the range of 17 V - 18 V (typ.).

In this design the IC voltage has been selected 15 V resulting in a higher secondary-auxiliary transformer turns ratio:

Equation 7

$$\frac{N_S}{N_{AUX}} = \frac{25V + 0.8V}{15V} = 1.72$$

Assuming a transformer with N_P = 125 T, the secondary and auxiliary winding turn results N_S = 33 T, N_{AUX} = 19 T.

Putting the value of *Equation 7* into *Equation 3* and resolving the *Equation 2*, the maximum transformer magnetization inductance can be estimated:

Equation 8

$$L_{PMAX} = \frac{200V}{\left(1 + \frac{200V}{100V}\right)} \bullet \frac{1}{100kHz} \bullet \frac{1}{310mA \bullet (2 \bullet 3.87) \bullet \left(1 + \frac{100V}{0.85 \bullet 200V}\right) \bullet \sqrt{2}} = 1.73mH$$

The selected magnetization inductance is L_P = 1.4 mH.

The leakage inductor of the transformer should be minimized to reduce the voltage spike on the drain node when the MOSFET is turned OFF - the maximum leakage inductor value is typically selected < 3% of the primary magnetizing value (L_{LK} < 3% • L_P).

2.3 Output voltage control - primary side regulation

The IC is specifically designed to work in a primary side regulation (PSR) and the output voltage is sensed through a voltage partition of the auxiliary winding, as shown in *Figure 3*.

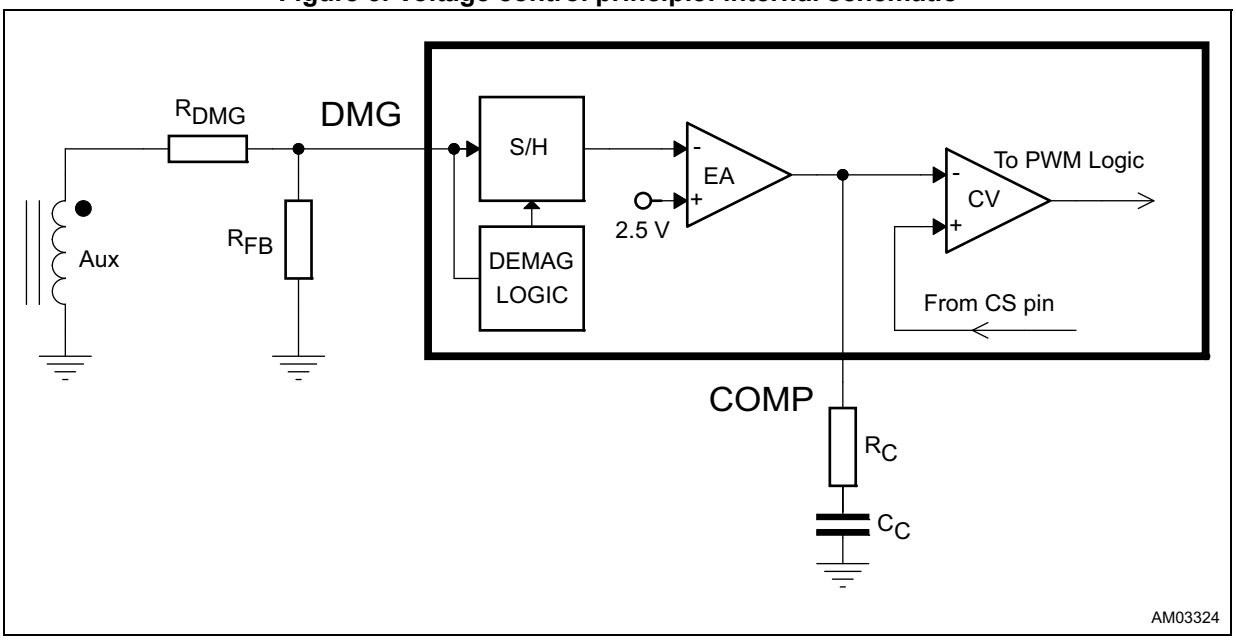
The signal on the DMG pin is sampled-and-held at the end of transformer demagnetization to get an accurate image of the output voltage (V_{OUT}) and it is compared with the internal error amplifier reference voltage V_{REF} (2.51 V typ.).

During the MOSFET's OFF-time the leakage inductance resonates with the drain capacitance and a damped oscillation is superimposed on the reflected voltage. The internal S/H logic is able to discriminate such oscillations from the real transformer demagnetization.

When the DMG logic detects the transformer demagnetization, the sampling process stops, the information is frozen and compared with the error amplifier internal reference.

The internal error amplifier is a transconductance type and delivers on the COMP pin a current proportional to the voltage unbalance of the two inputs: the COMP pin generates the control voltage that is compared with the voltage across the sense resistor, thus modulating the cycle-by-cycle peak drain current to regulate the desiderated output voltage.

Figure 3. Voltage control principle: internal schematic



The COMP pin is used for the frequency compensation: typically an R_C - C_C network, which stabilizes the overall voltage control loop, is connected between this pin and ground.

When implementing the high power factor (HPF - see *Section 2.4: High power factor implementation*), the output voltage control loop must have frequency bandwidth much lower than the “control current loop” (100/120 Hz, that is the double of line input frequency). As a consequence the output voltage control loop has to be designed in order to have bandwidth much lower than 100/120 Hz (i.e. BW_{CV} < 5 - 10 Hz).

Referring to the HVLED815PF datasheet, the average output voltage can be easily programmed trough the R_{FB} resistor, using *Equation 9*:

Equation 9

$$R_{FB} = R_{DMG} \bullet \left[\frac{V_{REF}}{\left(\frac{N_{AUX}}{N_{SEC}} \bullet V_{OUT} \right) - V_{REF}} \right]$$

where N_{AUX} and N_{SEC} are the auxiliary and secondary turn numbers respectively and V_{REF} is the internal reference voltage (2.51 V typ.).

The R_{DMG} resistor is designed to keep the line feed-forward and it can still be calculated as shown in the HVLED815PF datasheet, considering the equivalent R_{SENSE_EQ} resistor defined in *Equation 1*:

Equation 10

$$R_{DMG} = \frac{N_{AUX}}{N_P} \bullet \frac{L_P \bullet R_{FF}}{T_D \bullet R_{SENSE_{EQ}}} = \frac{19T}{125T} \bullet \frac{1.4mH \bullet 45\Omega}{100ns \bullet 1.08\Omega} = 82k\Omega$$

where R_{FF} and T_D - the internal feed-forward resistor and the MOSFET turns OFF delay time respectively. For more details see section 4.7: “Voltage feed-forward block” in the HVLED815PF datasheet.

Using the calculated R_{DMG} resistor, the R_{FB} resistor can be calculated using *Equation 9*.

Equation 11

$$R_{FB} = 82k\Omega \bullet \left[\frac{2.51V}{\left(\frac{19T}{33T} \bullet 25V \right) - 2.51V} \right] = 17.3k\Omega$$

2.4 High power factor implementation

Referring to *Figure 4*, the R_{PF} resistor (R6 on the application schematic) gives a contribution proportional to the input voltage on the CS pin: as a consequence the input current is proportional to the input voltage during the line period, implementing a high power factor correction.

In particular, the contribution proportional to the input voltage is generated using the auxiliary winding - diode in series to the R_{PF} resistor is needed to avoid any injection on the CS pin when the auxiliary winding is positive.

As mentioned in *Section 2.3*, through the R_{OS} resistor (the R14 resistor on the schematic between the CS pin and VCC pin) a positive offset on the CS pin is added, in order to keep a good THD. This offset can be designed using *Equation 12*:

Equation 12

$$V_{OS} = V_{CC} \bullet \frac{[(R_{CS} + R_{SENSE}) \,//\, R_{PF}]}{[(R_{CS} + R_{SENSE}) \,//\, R_{PF}] + R_{OS}} = K \bullet V_{CS}^{CV}$$

where V_{CS}^{CV} is the voltage on the CS pin that is imposed by the voltage control loop and K is a constant that by experience is selected in the range of 2/3 - 3/4.

The voltage on the CS pin depends on the ratio between the delivered output current (I_{OUT}) and the maximum deliverable current (I_{OUT-CC}) and so it can be estimated using *Equation 13*:

Equation 13

$$V_{CS}^{CV}(I_{OUT}) = \left[V_{CLED} \bullet \left(1 + \frac{V_R}{\eta \bullet V_{inRMS}}\right)\right] \bullet \frac{I_{OUT}}{I_{OUT-CC}}$$

where V_R is the reflect voltage ($V_R = V_{OUT} \bullet N_P/N_S$), V_{inRMS} is the RMS value of the input voltage, η is system efficiency and I_{OUT-CC} is the maximum delivered current that can be programmed trough the current control loop.

Assuming then $R_{PF} << R_{CS}$ and $R_{SENSE} << R_{CS}$, *Equation 13* can be simplified and the R_{OS} resistor results:

Equation 14

$$R_{OS} = \frac{V_{CC} - [K \bullet V_{CS}^{CV}]}{[K \bullet V_{CS}^{CV}]} \bullet R_{CS}$$

where V_{CC} is the IC supply voltage and it has been designed according to the secondary-to-auxiliary winding ratio (see *Equation 7*).

The R_{CS} resistor (R1 on the schematic in *Figure 7*) between the CS pin and SOURCE pin is needed to add on the CS pin also the contribution proportional the output current trough the R_{SENSE} resistor.

The R1 resistor is typically selected in the range of 0.5 - 1.0 kΩ in order to minimize the internal feed-forward effect and to minimize the power dissipation on the R_{PF} resistor.

Using the previous formulas the R_{OS} resistor can be estimated:

Equation 15

$$R_{OS} = \frac{V_{CC} - [K \bullet V_{CS}^{CV}]}{[K \bullet V_{CS}^{CV}]} \bullet R_{CS} = \frac{15V - \left[\frac{3}{4} \bullet \left([\ 0.2V \bullet \left(1 + \frac{100V}{0.85 \bullet 200V}\right)\right] \bullet \frac{310mA}{375mA}\right)\right]}{\left[\frac{3}{4} \bullet \left([\ 0.2V \bullet \left(1 + \frac{100V}{0.85 \bullet 200V}\right)\right] \bullet \frac{310mA}{375mA}\right)\right]} \bullet$$

$$\bullet\ 1k\Omega = 76.8k\Omega$$

The capacitor between the CS pin and ground could be useful when the transformer leakage inductor cannot be minimized (voltage spike on the drain pin could be coupled from the CS net).

The R_{PF} resistor gives a contribution proportional to the input voltage and it can be estimated using *Equation 16*, considering the maximum input voltage:

Equation 16

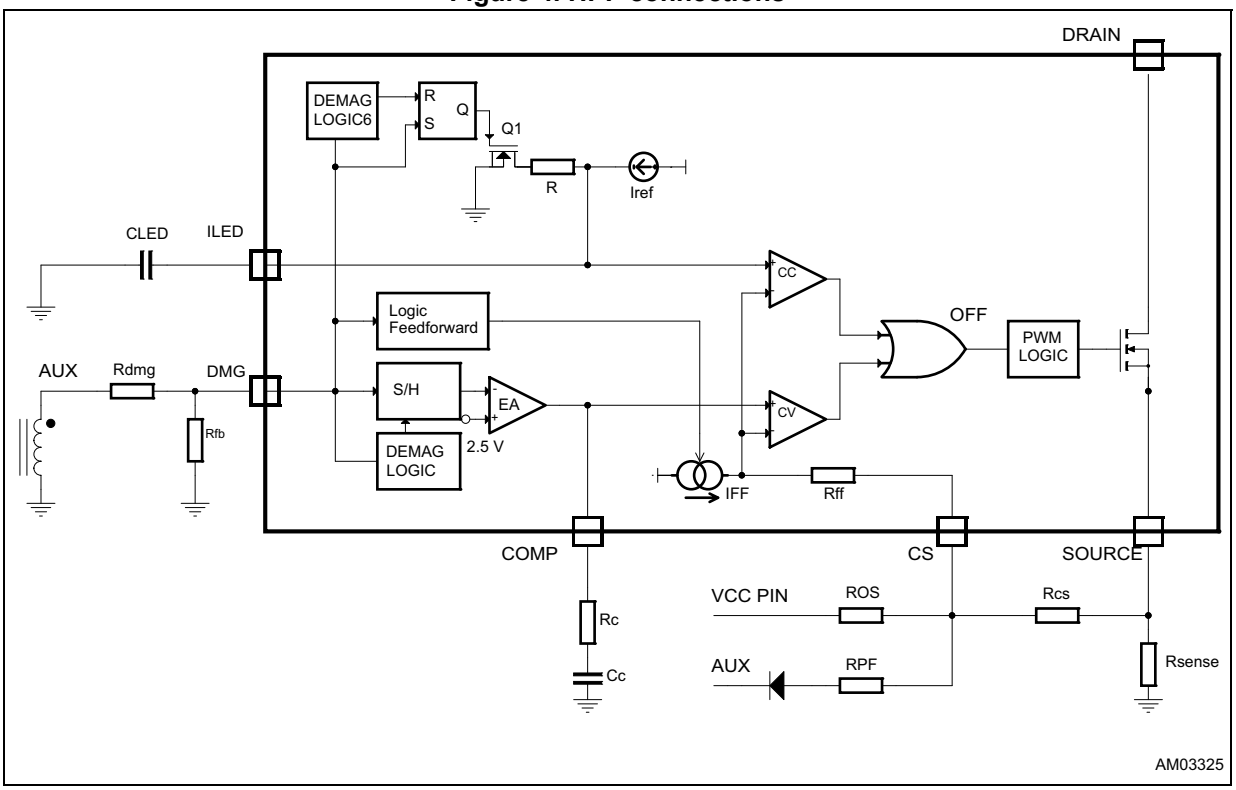
$$R_{PF} = R_{CS} \bullet \left[\frac{(V_{inMAX} \bullet \sqrt{2} \bullet R_{OS} \bullet N_{AUX}) - (V_{CC} \bullet R_{CS} \bullet N_P) - (0.75 \bullet R_{OS} \bullet N_P)}{N_P \bullet [0.75 \bullet R_{OS} + V_{CC} \bullet R_{CS}]}\right]$$

Using the calculated value of N_{AUX}, N_P, R_{OS} and R_{CS} the R_{PF} resistor results:

Equation 17

$$R_{PF} = 1k\Omega \bullet \left[\frac{(265V \bullet \sqrt{2} \bullet 76.8k\Omega \bullet 19T) - (15 \bullet 1k\Omega \bullet 125T) - (0.75 \bullet 76.8k\Omega \bullet 125T)}{125T \bullet [0.75 \bullet 76.8k\Omega + 15V \bullet 1k\Omega]}\right] = 59k\Omega$$

Figure 4. HPF connections



The voltage loop changes the voltage on the CS pin to keep the output voltage regulated. Respect to the standard circuit (no high power factor implementation trough R_{PF} and R_{OS}), the contributions proportional to V_{IN} trough the R_{PF} resistor and the offset trough the R_{OS} resistor give of course a modification of the voltage across the R_{SENSE} resistor generating a different gain between the R_{SENSE} and CS pin.

The V_{OS} offset voltage is basically selected to have no input current when the input voltage is close to zero at the minimum line condition: as a consequence the voltage across the R_{SENSE} resistor is basically equal to the voltage generated by the R_{PF} resistor.

The R_{SENSE} can be estimated imposing the equality between the two ratios, in the worst-case condition (minimum line and maximum deliverable current $I_{OUT}{}^{CC}$):

Equation 18

$$\frac{V_{CS}{}^{CV}}{R_{SENSE\_EQ}} = \left[\frac{R_{CS} \bullet \left(\frac{V_{AUX}}{R_{PF}} \bullet \frac{1}{\sqrt{2}}\right)}{R_{SENSE}}\right]$$

where V_{AUX} is the voltage present at the auxiliary winding when the MOSFET is ON:

Equation 19

$$V_{AUX} = V_{IN} \bullet \frac{N_{AUX}}{N_P}$$

Replacing *Equation 1*, *Equation 13*, and *Equation 18* in *Equation 17*, the R_{SENSE} resistor results:

Equation 20

$$R_{SENSE} = \frac{1}{2} \bullet \frac{N_{AUX}}{N_S} \bullet \frac{R_{CS}}{R_{PF}} \bullet \frac{1}{I_{OUT\_CC}} \frac{V_{inRMS\_MIN}}{\left(1 + \frac{V_R}{\eta \bullet V_{inRMS\_MIN}}\right)}$$

The resistors R_{SENSE}, R_{FB}, R_{DMG}, R_{OS}, R_{CS}, R_{PF} determine the output voltage and the maximum deliverable current setting - suggested accuracy of these parameters is 1%.

2.5 Output filter

The output filter has to be designed to respect the output voltage ripple specification ($\Delta V_{OUT}^{pk\text{-}pk}$). In this kind of application, the single-stage high power factor, the high frequency ripple at the switching frequency can be neglected respect to the low frequency ripple at double line frequency (100/120 Hz).

The output capacitor value can then be estimated using *Equation 21*:

Equation 21

$$C_{outMIN} \cong \frac{0.4}{\pi} \bullet \frac{I_{OUT}^{MAX}}{fline \bullet \Delta V_{OUT}^{PK-PK}} = \frac{0.4}{\pi} \bullet \frac{310mA}{50Hz \bullet 0.75V} = 1005\mu F$$

For this design, three output capacitors of 330 µF/64 mΩ/35 V have been selected.

2.6 Voltage control loop compensation

As mentioned in *Section 2.3* the voltage control loop must have frequency bandwidth much lower than the “control current loop” to avoid any interaction between the two loops. The current loop “works” at the double of line input frequency (100 - 120 Hz), resulting in suggested voltage loop bandwidth in the range of 5 - 10 Hz (BW_{CV} < 1/10 of current loop bandwidth).

The small signal system voltage loop gain can be estimated considering the equivalent schematic in *Figure 5.*

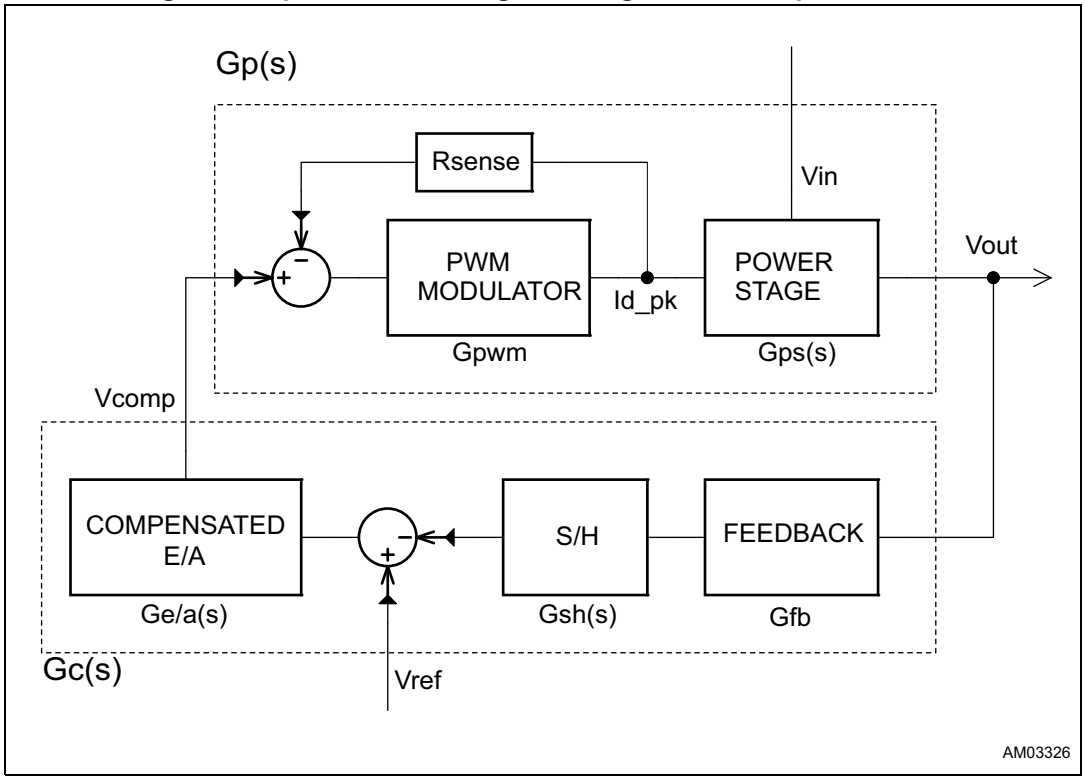
Equation 22

$$Gloop\_CV(s) = Gp(s) \bullet Gc(s) = [Gpwm \bullet Gps(s)] \bullet [Gea(s) \bullet Gsh(s) \bullet Gfb]$$

where the previous transfer functions are:

- Gpwm is the internal PWM modulator gain (Gpwm = 0.5)
- Gps(s) is the power stage transfer function (transformer and output filter)
- Gfp is the feedback gain between the V_{OUT} and DMG pin
- Gsh(s) is the internal sample and hold transfer function
- Gea(s) is the error amplifier transfer function (COMP pin network)

Figure 5. Equivalent small signal voltage control loop schematic



The power stage transfer function is calculated considering the transfer function of a standard flyback converter:

Equation 23

$$Gps(s) = Go\_ps \bullet \frac{\left(1 + \frac{s}{\omega z1\_ps}\right) \bullet \left(1 - \frac{s}{\omega z2\_ps}\right)}{\left(1 + \frac{s}{\omega p\_ps}\right)}$$

Equation 24

$$Go\_ps = \frac{1}{2} \bullet \frac{N_P}{N_S} \bullet \frac{R_{OUT}}{R_{SENSE}} \bullet \frac{1 - d_P}{1 + d_P}$$

Equation 25

$$\omega z1\_ps = \frac{1}{ESR \bullet C_{OUT}}$$

Equation 26

$$\omega z2\_ps = \frac{\left(\frac{N_P}{N_S}\right)^2 \bullet R_{OUT} \bullet (1 - d_P)^2}{L_P \bullet d_P}$$

Equation 27

$$\omega p\_ps = \frac{1 + d_P}{R_{OUT} \bullet C_{OUT}}$$

where *ESR* is the equivalent output capacitor resistance and d_p is the primary duty-cycle that depends on the input and output voltage and it can be estimated with *Equation 28*:

Equation 28

$$d_P = \frac{V_R}{V_R + \eta \bullet V_{inRMS}}$$

The power stage presents one pole at low frequency (this pole is basically related to the output filter time constant), and two zeros. Note that one zero is positive, resulting in a negative contribution on the phase margin.

Replacing the component value on *Equation 25*, *Equation 26*, *Equation 27* and considering the V_{inRMS_typ} and I_{OUT}^{MAX}, the frequency singularities of the power stage result:

fp_ps = 2.6 Hz fz1_ps = 2.5 kHz fz2_ps = 183 kHz.

The feedback gain transfer function is the ration between the output voltage and the DMG pin, and it is calculated using *Equation 29*:

Equation 29

$$Gfb = \frac{N_{AUX}}{N_S} \bullet \frac{R_{FB}}{R_{FB} + R_{DMG}}$$

The sample and hold transfer function can be neglected because system voltage loop bandwidth is much lower than the system switching frequency (the pole of the sample and hold circuitry is at higher frequency than system bandwidth $BW_{CV} << Fp_{S\&H}$):

Equation 30

$$Gsh(s) \cong 1$$

Typically an R_C - C_C series network is connected between the COMP pin and ground to compensate the system loops, resulting in the following error amplifier transfer function:

Equation 31

$$Gea(s) = Gea0 \bullet \frac{\left(1 + \frac{s}{\omega z\_ea}\right)}{s}$$

Equation 32

$$Gea0 = \frac{gm}{C_C}$$

Equation 33

$$\omega z\_ea = \frac{1}{R_C \bullet C_C}$$

where *gm* is the transconductance gain of the internal operational transconductance amplifier (gm = 2.2 mS typ). For more details, see the HVLED815PF datasheet - Table 5: “Electrical characteristics”.

Inserting the *Equation 22* to *Equation 33* in *Equation 21*, the small signal system control loop transfer function results:

Equation 34

$$Gloop\_CV(s) = Gloop0 \bullet \frac{\left(1 + \frac{s}{\omega z1\_ps}\right) \bullet \left(1 - \frac{s}{\omega z2\_ps}\right)}{\left(1 + \frac{s}{\omega p\_ps}\right)} \bullet \frac{\left(1 + \frac{s}{\omega z\_ea}\right)}{s}$$

Equation 35

$$Gloop0 = \frac{1}{2} \bullet \left(\frac{1}{2} \bullet \frac{N_P}{N_S} \bullet \frac{R_{OUT}}{R_{SENSE}} \bullet \frac{1 - d_P}{1 + d_P}\right) \bullet \left(\frac{N_{AUX}}{N_S} \bullet \frac{R_{FB}}{R_{FB} + R_{DMG}}\right) \bullet \left(\frac{gm}{C_C}\right)$$

As mentioned in *Section 2.3* control voltage loop bandwidth (BW_{CV}) has to be designed at very low frequency (i.e. 5 - 10 Hz) to avoid the interaction with the “current loop”: as a consequence the zeros of the power stage can be typically “neglected” because they are at much higher frequency than system bandwidth resulting in a simplified loop gain calculation:

Equation 36

$$Gloop\_CV(s) \cong Gloop0 \bullet \frac{1}{s} \bullet \frac{\left(1 + \frac{s}{\omega z\_ea}\right)}{\left(1 + \frac{s}{\omega p\_ps}\right)}$$

Equation 35 shows the simplified voltage control loop gain formula having two pole and one zero in the frequencies range of interest.

The external compensation network (R_C, C_C) introduces a pole in the origin and one zero that can be selected to both stabilize the system voltage control loop and to obtain desiderated system bandwidth BW_{CV}.

Considering the control loop gain estimated in *Equation 36*, the R_C resistor and the C_C capacitor can be programmed using the following relationships:

Equation 37

$$R_C \cong BW_{CV} \bullet \left(\frac{4 \bullet \pi \bullet C_{OUT} \bullet R_{SENSE}}{gm} \bullet \frac{N_S^2}{N_{AUX} \bullet N_P} \bullet \frac{R_{FB} + R_{DMG}}{R_{FB}} \bullet \left(1 + \frac{V_R}{\eta \bullet V_{inRMS}}\right)\right) =$$

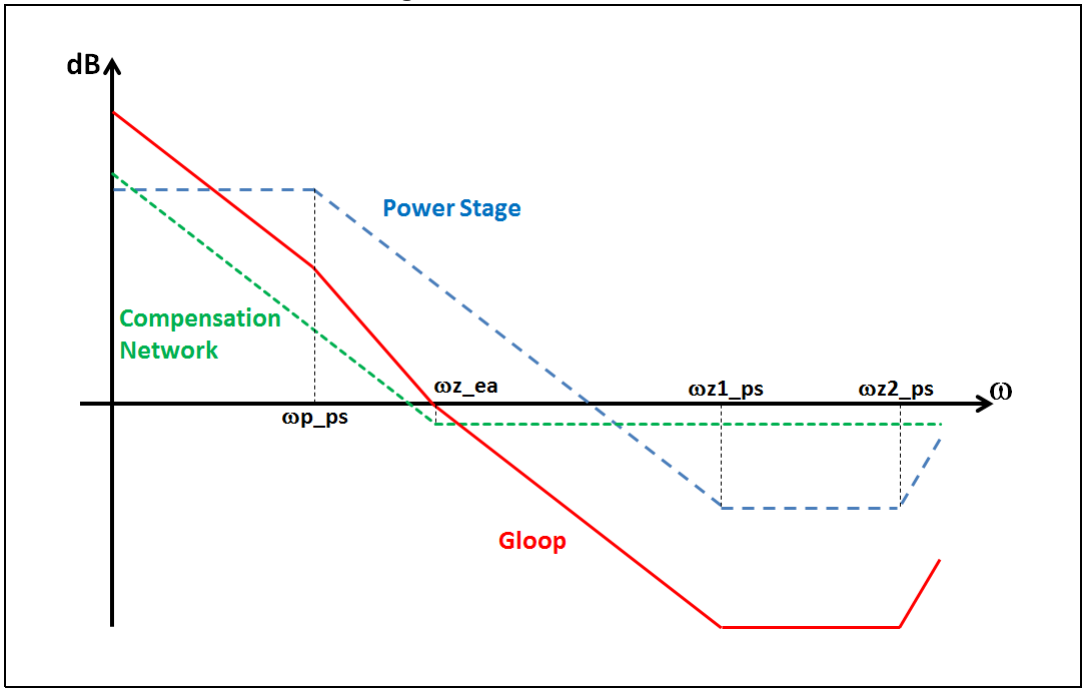
$$= 5 \bullet \left(\frac{4 \bullet \pi \bullet 3 \bullet 330\mu F \bullet 1.875\Omega}{2.2mS} \bullet \frac{33T^2}{19T \bullet 125T} \bullet \frac{17.3k\Omega + 82k\Omega}{17.3k\Omega} \bullet \left(1 + \frac{100V}{0.85 \bullet 230V}\right)\right) = 215\Omega$$

Equation 38

$$C_C \cong \frac{1}{R_C \bullet (4 \bullet \pi \bullet BW_{CV})} = \frac{1}{220\Omega \bullet (4 \bullet \pi \bullet 5Hz)} = 74\mu F$$

A capacitor between the COMP pin and ground can be also added to remove the high frequency voltage ripple without impacting on the transfer function (i.e. adding a small capacitor in the range of few nF).

Figure 6. Transfer function



2.7 System design tips

Starting from the estimated value using *Equation 11*, *Equation 15*, *Equation 17*, *Equation 20*, *Equation 37* and *Equation 38*, further fine tuning on the real LED driver board could be necessary and it can be easily done considering that:

- Decreasing the R_{PF} resistor value, the power factor effect increases
- Decreasing the R_{OS} resistor value, the input current close to zero decreases
- Decreasing the R_{SENSE} resistor value, the maximum deliverable output current increases
- Increasing the C_C compensation capacitor, the system phase margin increases and voltage loop bandwidth decreases.
- Decreasing the R_C compensation resistor, the voltage loop gain/bandwidth decreases and also the ripples on the COMP pin.

3 Schematic and bill of materials

Figure 7. Demonstration board schematic

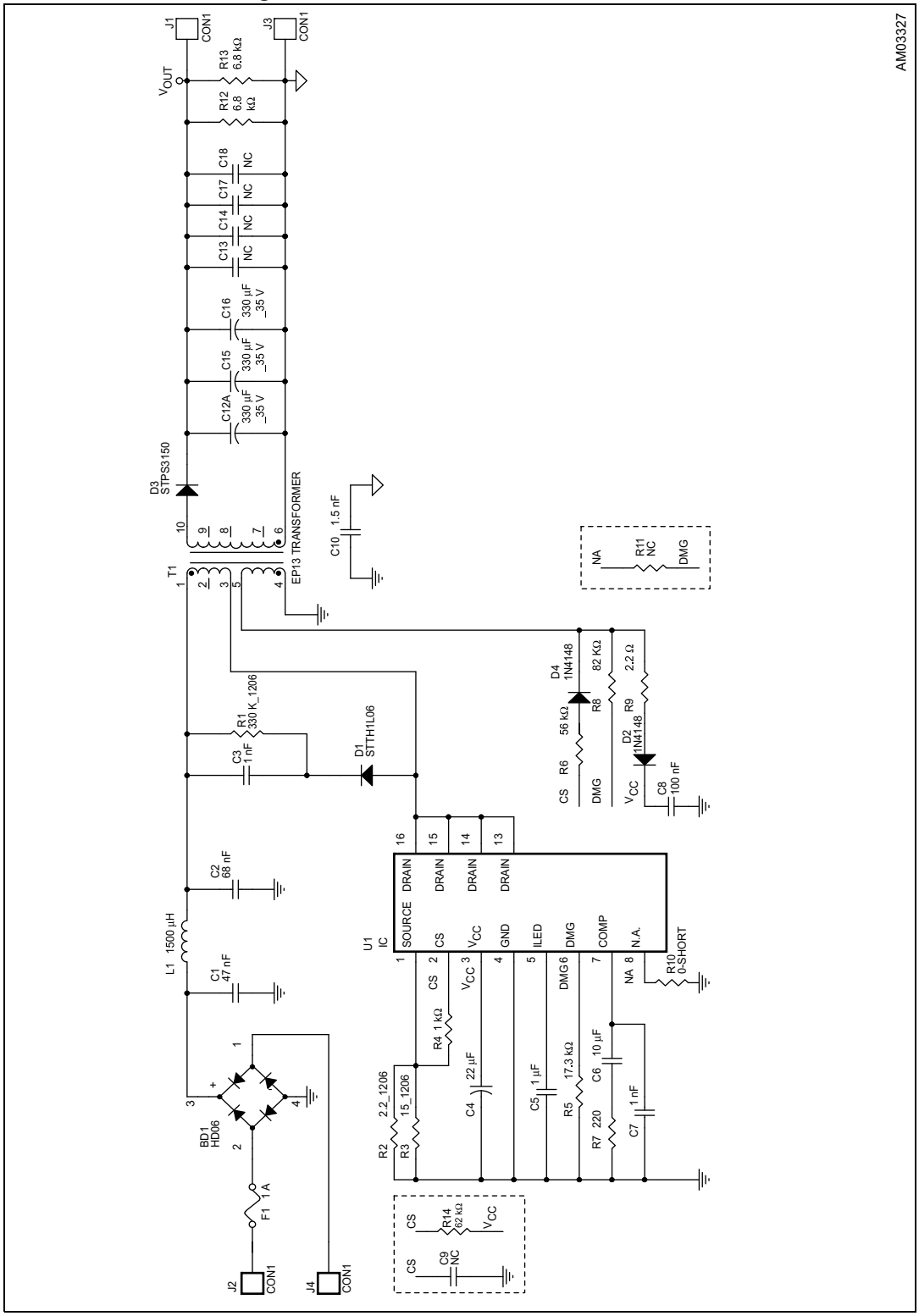


Table 1. Bill of materials (BOM)

Ref.	Value	Part number	Vendor	Package	Description
BD1	600 V-0.8 A	HD06-T	DIODES ® INC.	Mini DIP	Bridge rectifier
C1	47 nF	B32921C3473	EPCOS	DIP 5 x 11 x 13	Input filter capacitor
C2	68 nF	B32921C3683	EPCOS	DIP 5 x 11 x 13	Input filter capacitor
C3	1 nF	C3216X7R2J102K	TDK	SMD 1206	Snubber capacitor
C4	22 µF/50 V	EEUFR1H220	Panasonic	RADIAL 5 x 11.5	V_{CC} filter capacitor
C5	1 µF	C2012X5R1E105K	TDK	SMD 0805	ILED pin filtering
C6	10 µF	C2012X5R0J106M	TDK	SMD 0805	C_C - compensation network
C7	1 nF			SMD 0805	C_P - compensation network
C8	100 nF/25 V			SMD 0805	V_{CC} filter capacitor
C9	NC			SMD 0805	CS pin filtering
C10	1500 pF	DE1E3KX152MN5A	Murata		Y2 capacitor
C12A	330 µF/35 V	B41888C7337M	EPCOS	RADIAL 10 x 16	Output capacitor
C13	NC			SMD 1206	Output MLCC capacitor
C14	NC			SMD 1206	Output MLCC capacitor
C15	330 µF/35 V	B41888C7337M	EPCOS	RADIAL 10 x 16	Output capacitor
C16	330 µF/35 V	B41888C7337M	EPCOS	RADIAL 10 x 16	Output capacitor
C17	NC			SMD 1206	Output MLCC capacitor
C18	NC			SMD 1206	Output MLCC capacitor
D1	1 A/600 V	STTH1L06	STMicroelectronics®	SMB FLAT	Snubber diode
D2		1N4148		SOD-123	Self-supply diode
D3	3 A/150 V	STPS3150UF	STMicroelectronics	SMB FLAT	Output filter diode
D4		1N4148		SOD-123	PF network diode
F1	1 A -250 V	MCMSF 1 A 250 V	MULTICOMP	DIP 4 x 8	Input fuse
L1	1.5 mH	B82145A1155J000	EPCOS	DIP 6.5 x 12	Input inductor
R1	330 kΩ			SMD 1206	Snubber resistor
R2	2.2 Ω - 1%			SMD 1206	R_{SENSE} resistor
R3	15 Ω - 1%			SMD 1206	R_{SENSE} resistor
R4	1 kΩ - 1 %			SMD 0805	R_{CS} resistor
R5	17.3 kΩ - 1%			SMD 0805	R_{FB} resistor
R6	56 kΩ - 1%			SMD 0805	R_{PF} resistor
R7	220 Ω			SMD 0805	R_C compensation network
R8	82 kΩ - 1%			SMD 0805	R_{DMG} resistor
R9	2.2 Ω			SMD 0805	V_{CC} filtering
R10	0 Ω			SMD 0603	Optional
R11	NC			SMD 0603	Optional

Table 1. Bill of materials (BOM) (continued)

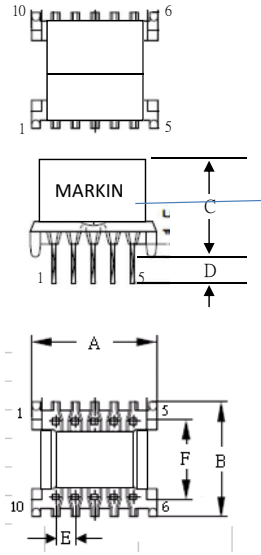
Ref.	Value	Part number	Vendor	Package	Description
R12	6.8 kΩ			SMD 0805	Minimum load
R13	6.8 kΩ			SMD 0805	Minimum load
R14	62 kΩ - 1%			SMD 0805	R_{OS} resistor
T1		SRW13EP-XxxH003	TDK	TROUGH HOLE 10-pin	Flyback transformer
U1		HVLED815PF	STMicroelectronics	SO-16	IC with integrated MOS

4 Transformer specifications

Figure 8. Transformer specifications

担当:SATO	RoHS対応品	用途:Lighting	

[1] 外観及び寸法 APPEARANCE & DIMENSIONS (UNIT:mm)



X11725-6
TDK X YMDDHH

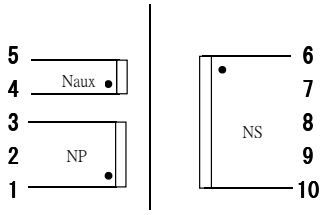
A: 17.5 mm MAX
B: 17.0 mm MAX
C: 15.5 mm MAX
D: 3.3±0.5 mm
E: 3.0±0.5 mm
F: 11.0±0.5 mm
d: 0.6±0.1 mm

All products are fixed with the adhesive.

安全規格 SAFETY STANDARDS

沿面空間距離 Over Surface & Air Spacings
1次PRI.-2次SEC. ----mm MINIMUM
2次SEC.-CORE ----mm MINIMUM

[2] 巻線仕様 WINDING SPECIFICATION



Bottom View

PIN 2,7,8,9 should be pulled off

AL-Value=90nH/N^2(Z+G) (GAP : R20)

No.	コイル COIL	端子 TERMINAL	巻数 TURNS	ワイヤ WIRE	巻法	25Ux8.0
1	N P1	1 - 3	125	1UEW 0.14	FIT+SPACE	1.2TS
2	N S	6 - 10	33	1UEW 0.30	FIT+SPACE	1.2TS
3	N aux	4 - 5	19	1UEW 0.14	SPACE	2.2TS

Lp 1--3 = (1.4mH★Ref.)±10% at10kHz/1V, Le 5--3 = ---uH MAX (Sec shorted) at10kHz/1V
耐圧 P-S :AC0.6KVrms 1s 2mA
P-CORE:AC0.60kVrms 1s 2mA
S-CORE:AC0.6kVrms 1s 2mA
IR :P-S,PS-CORE 100 MΩ MIN. at DC 500V

APPROVED	CHECKED	DESIGNED	CUSTOMER	ST 御中
		周小波	MODEL	SRW13EP-XxxH003
		2013/6/4	DWG. No.	X11725 ISSUE 6

5 PCB layout

Figure 9. PCB layout - top side

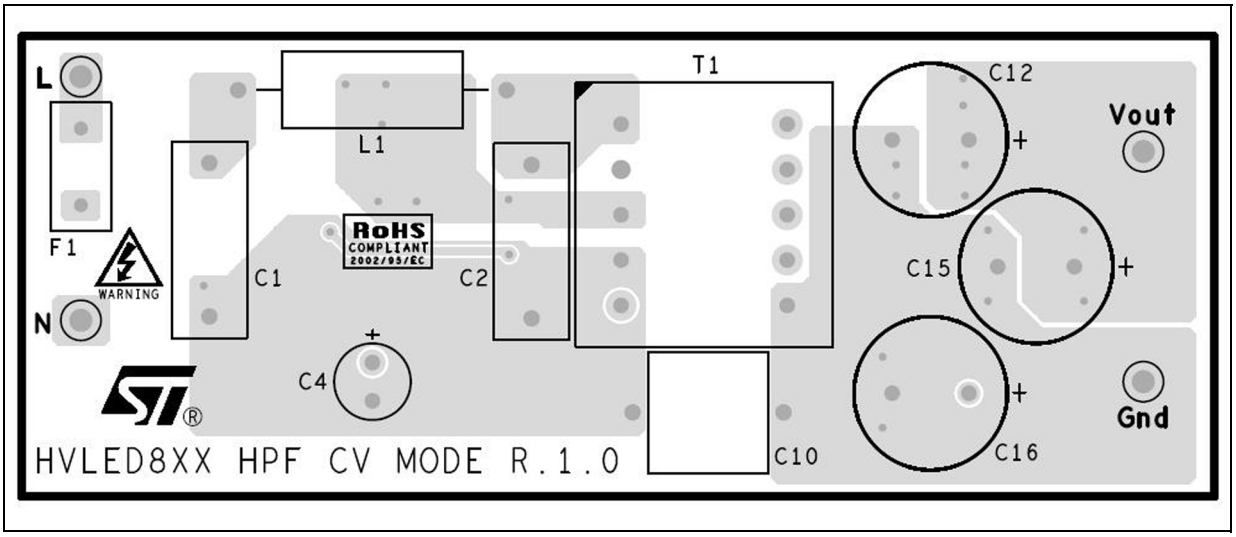
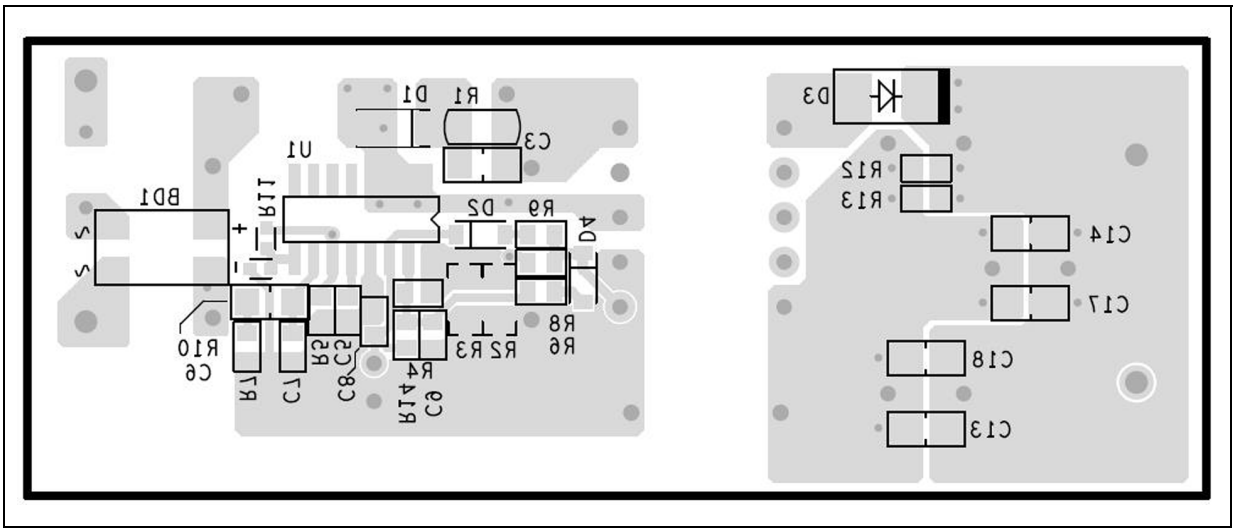


Figure 10. PCB layout - bottom side



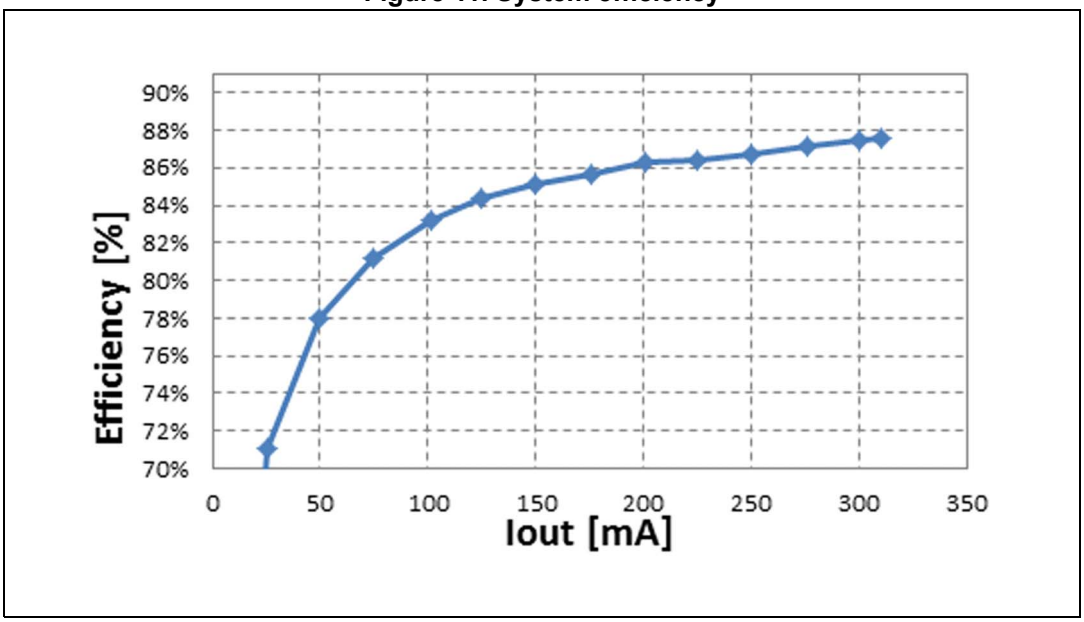
6 Test results

From *Figure 11* to *Figure 18* are shown the main results of the demonstration boards at nominal line input voltage (230 Vac).

6.1 Efficiency

System efficiency is higher than 80% starting from 20% of the rated maximum load (about 70 mA) and it increases up to 88% at the maximum load.

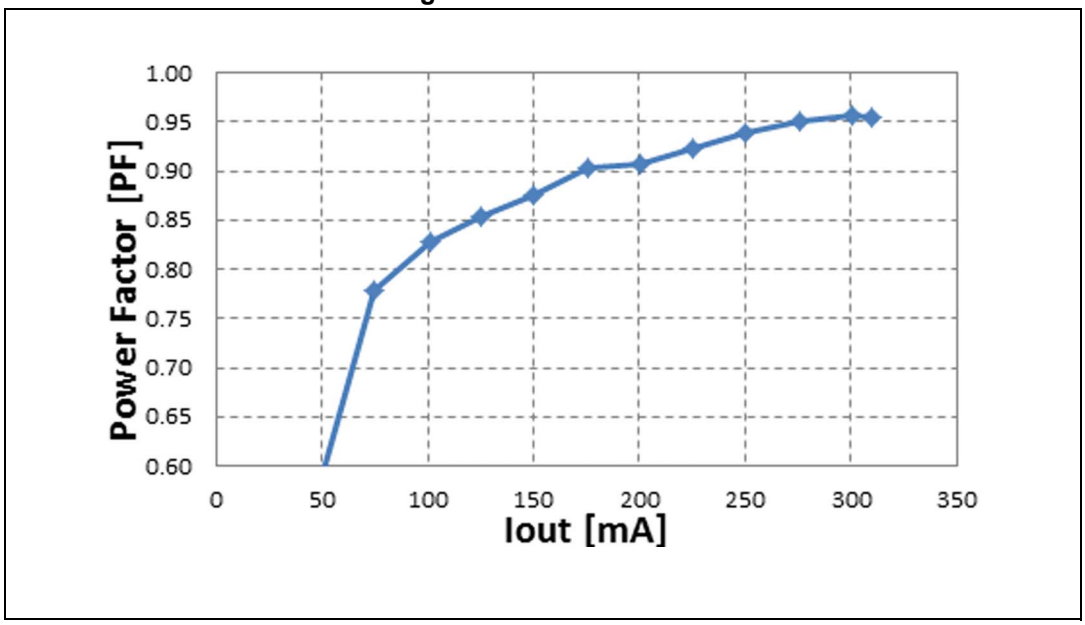
Figure 11. System efficiency



6.2 Power factor

The power factor is higher than 0.75 starting from 20% of the rated maximum load (about 70 mA) and increases up to 0.95 at maximum load.

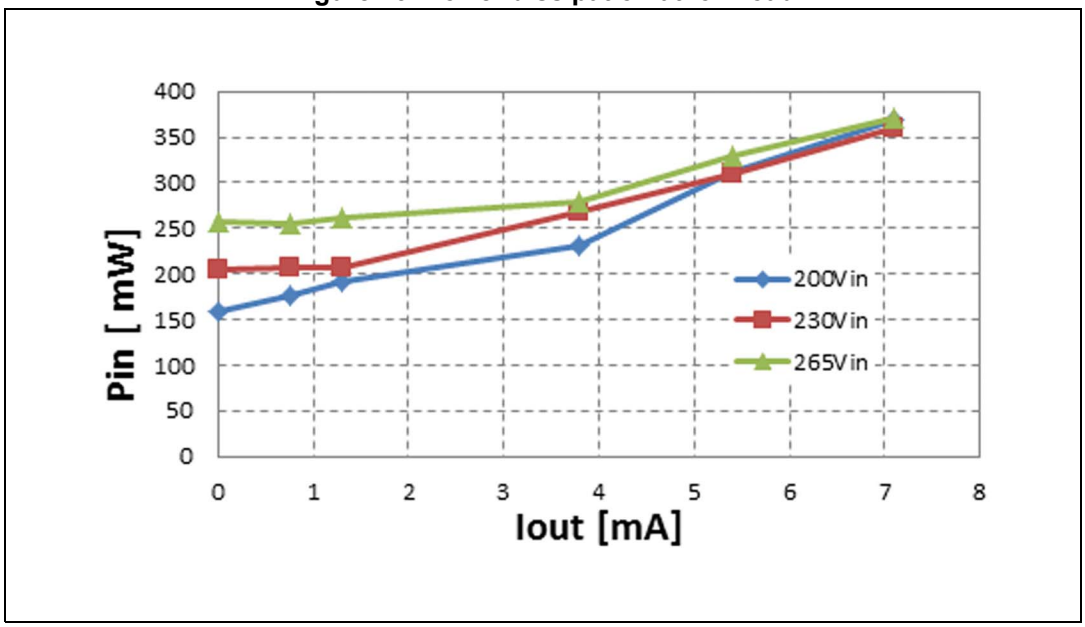
Figure 12. Power factor



6.3 Standby power dissipation

The power consumption of the demonstration board in standby condition (no load) is below 300 mW.

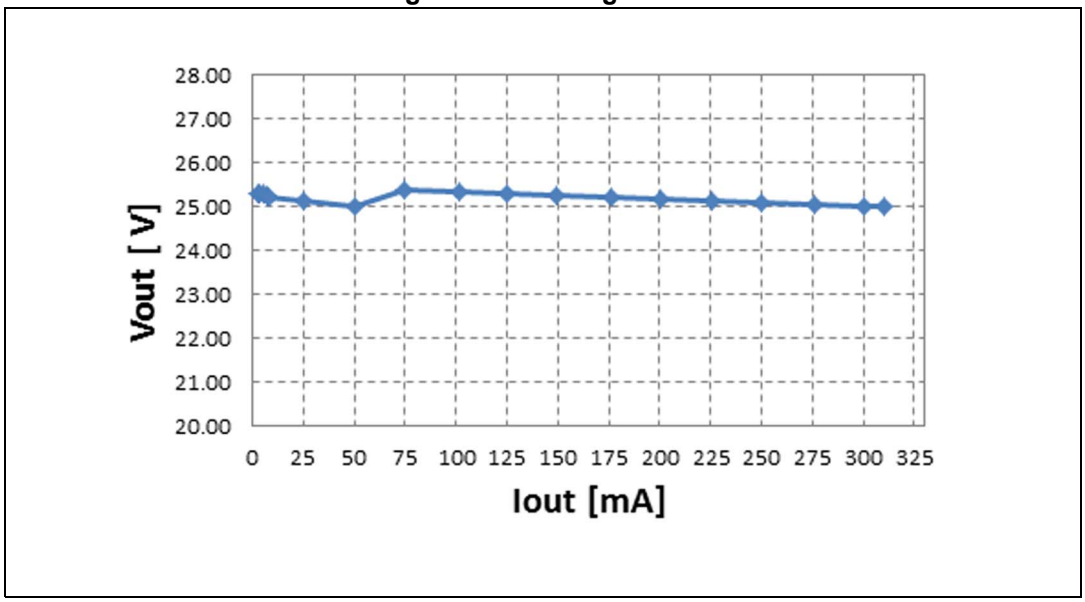
Figure 13. Power dissipation at low load



6.4 Line regulation

The average output voltage is regulated within ± 0.8% from no load to full load.

Figure 14. Line regulation



6.5 Harmonic distortion

The demonstration board respects the EC61000-3-2 Class D specification.

Figure 15. Harmonic distortion at 310 mA

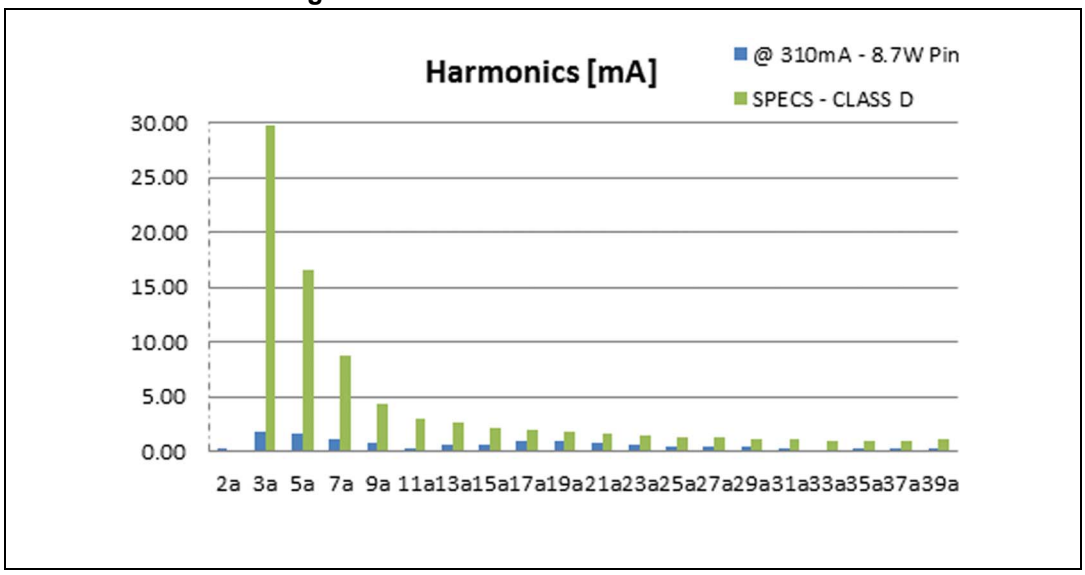


Figure 16. Harmonic distortion at 275 mA

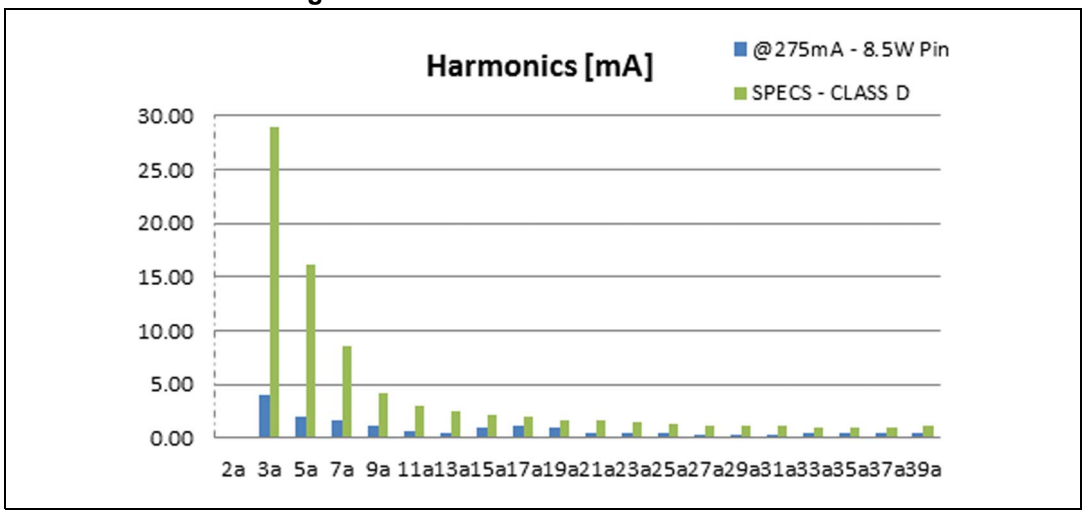


Figure 17. Harmonic distortion at 200 mA

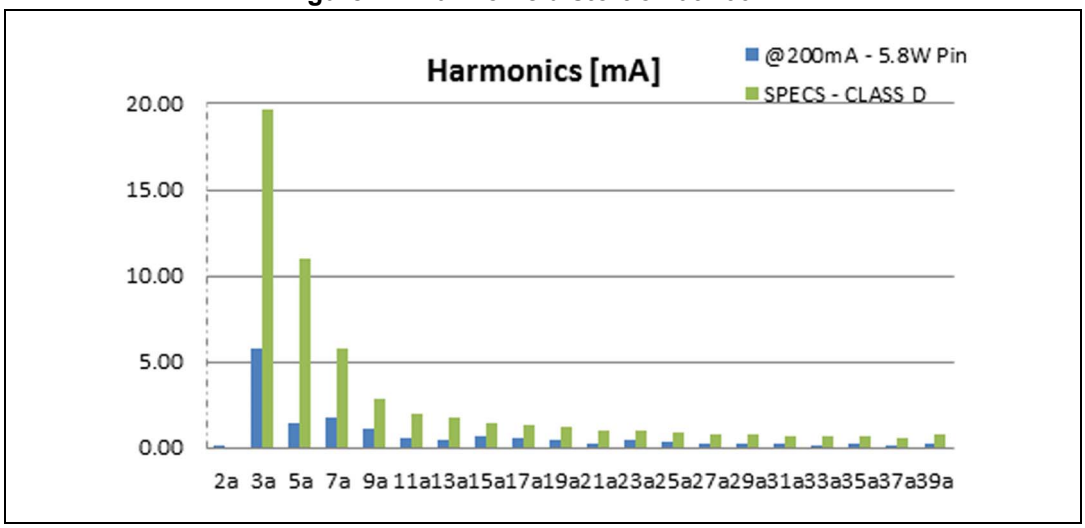
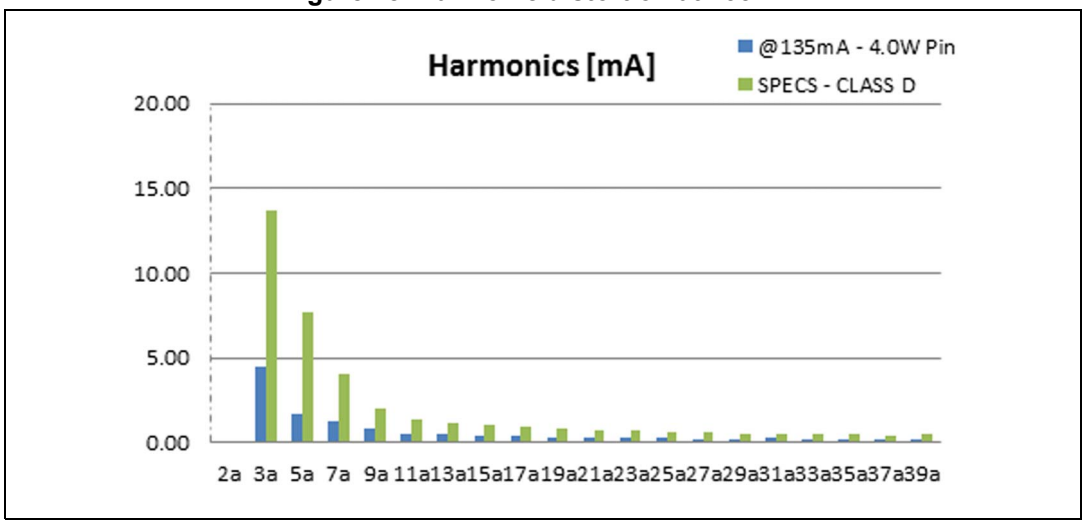


Figure 18. Harmonic distortion at 135 mA



6.6 Thermal measurement

All component temperatures are below 50 °C - a thermal test has been performed at ambient temperature (25 °C).

Figure 19. Thermal test - top side

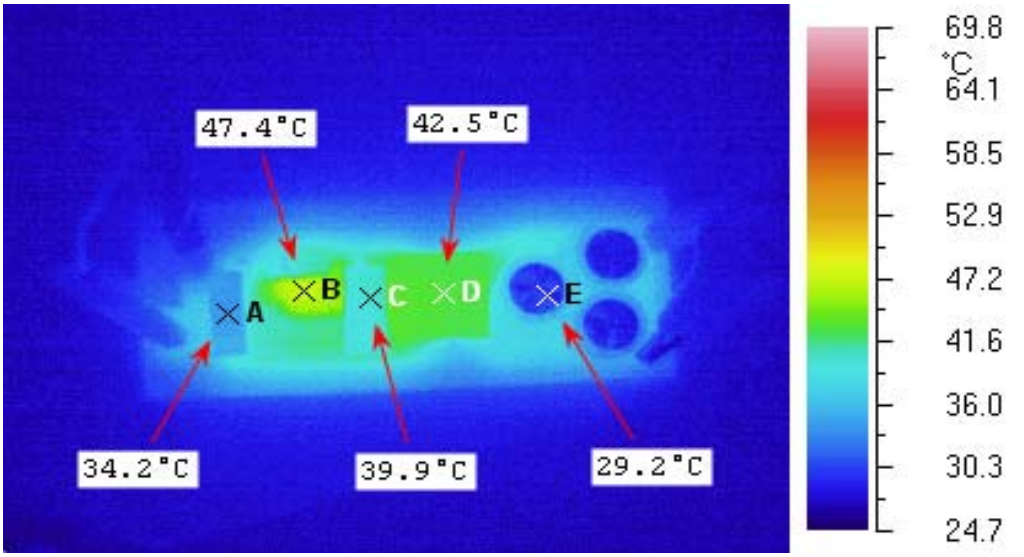


Table 2. Thermal test - top side

Label	Component
A	Input capacitor (C1)
B	Input inductor
C	Input capacitor (C2)
D	Transformer
E	Output capacitor

Figure 20. Thermal test - bottom side

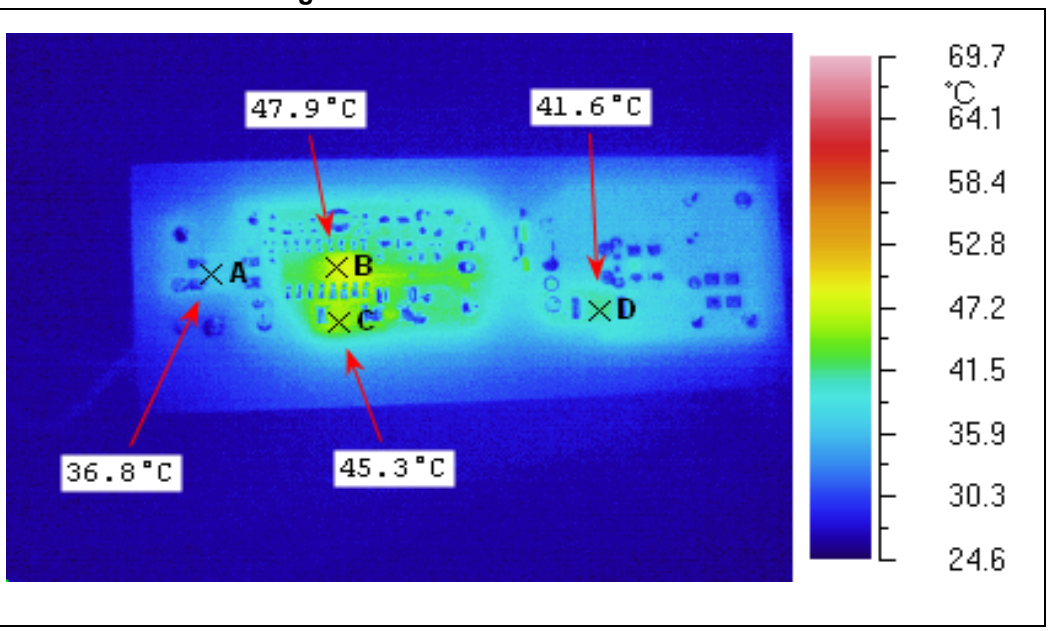
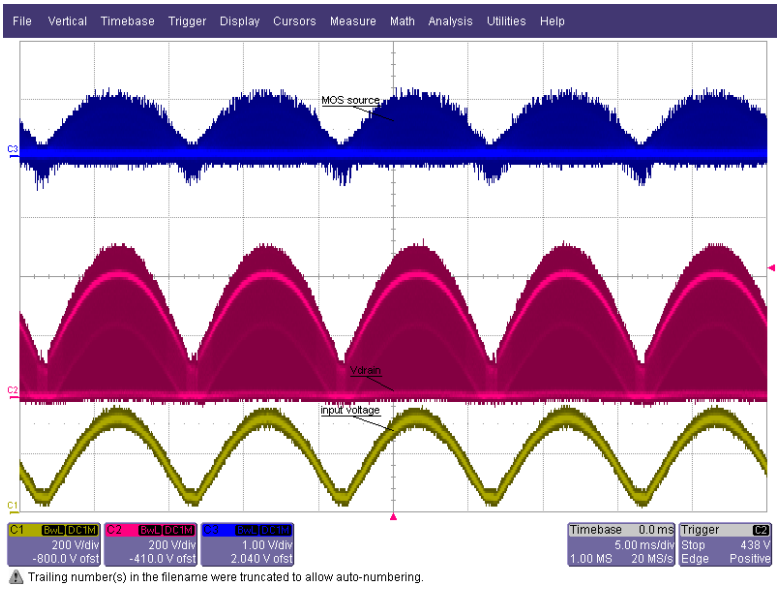


Table 3. Thermal test - bottom side

Label	Component
A	Bridge diode
B	IC (HVLED815PF)
C	Snubber
D	Output diode

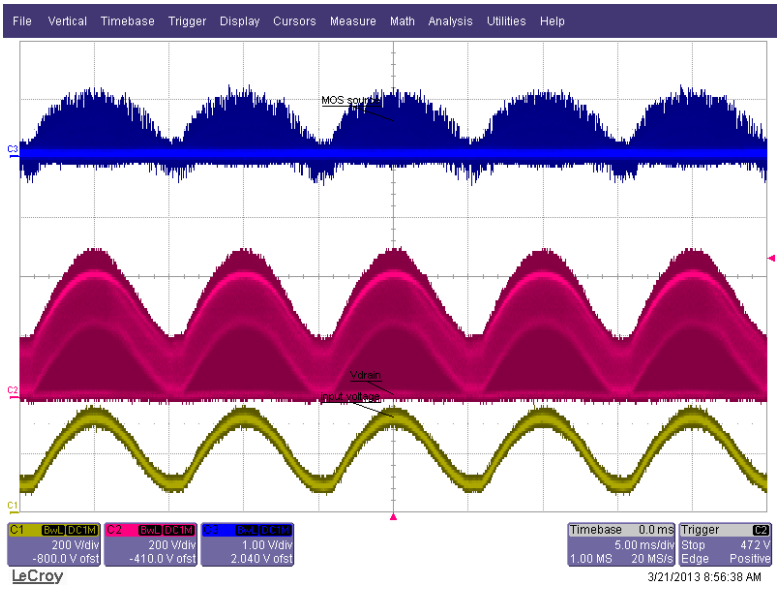
6.7 Waveforms

Figure 21. MOSFET current at I_{OUT}^{max}



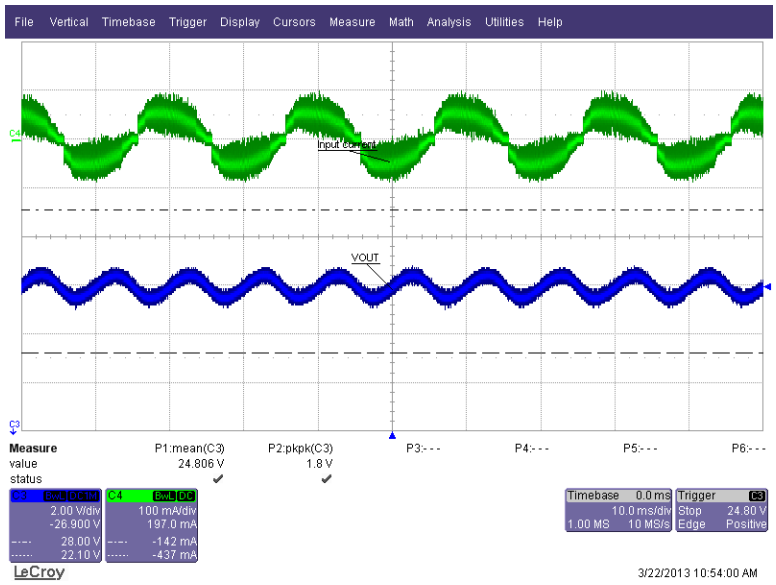
CH1 (brown): rectified input voltage
CH2 (purple): MOSFET drain
CH3 (blue): MOSFET source

Figure 22. MOSFET current at $I_{OUT}^{max}/2$



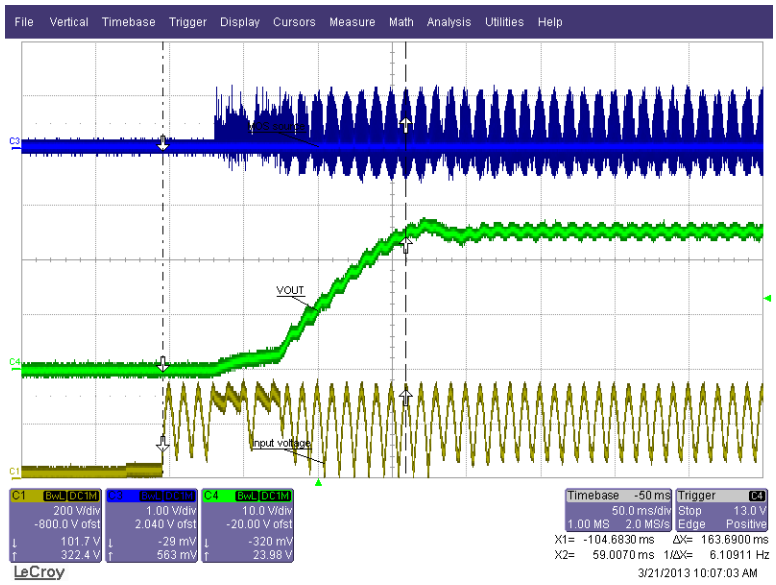
CH1 (brown): rectified input voltage
CH2 (purple): MOSFET drain
CH3 (blue): MOSFET source

Figure 23. Steady-state condition



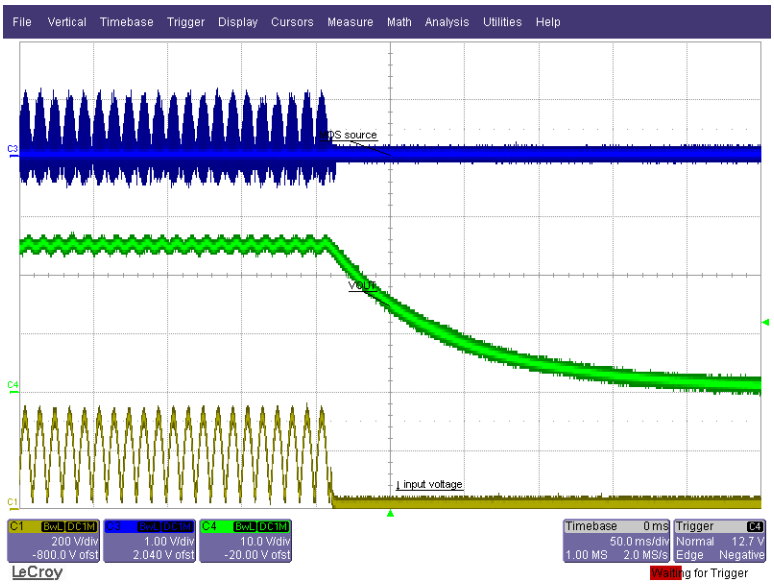
CH3 (blue): output voltage
CH4 (green): input current

Figure 24. Startup at I_{OUT}^{max}



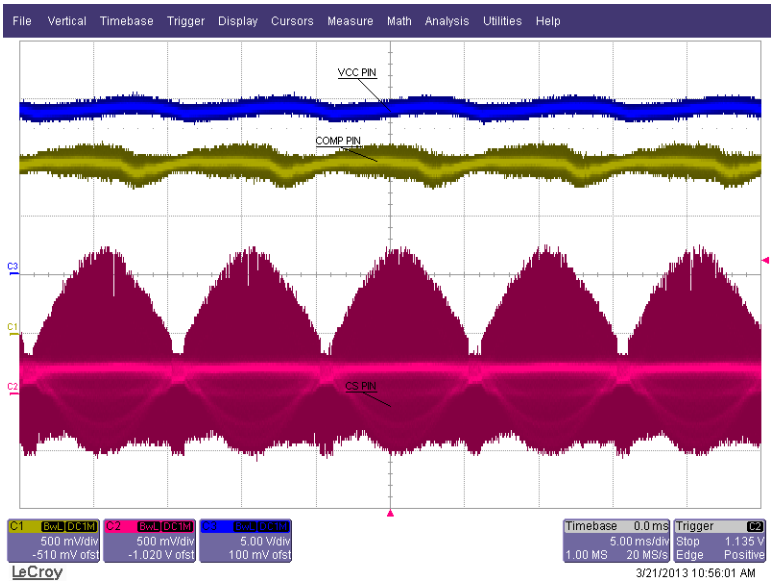
CH1 (brown): rectified input voltage
CH3 (blue): MOSFET source
CH4 (green): output voltage

Figure 25. Shutdown at I_{OUT}^{max}



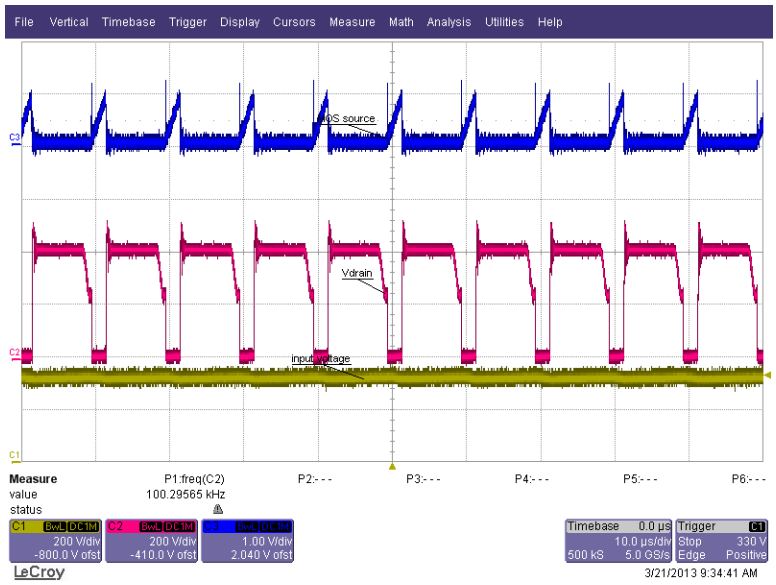
CH1 (brown): rectified input voltage
CH3 (blue): MOSFET source
CH4 (green): output voltage

Figure 26. COMP pin at I_{OUT}^{max}



CH1 (brown): COMP pin
CH2 (purple): CS pin
CH3 (blue): VCC pin

Figure 27. Switching frequency at I_{OUT}^{max}

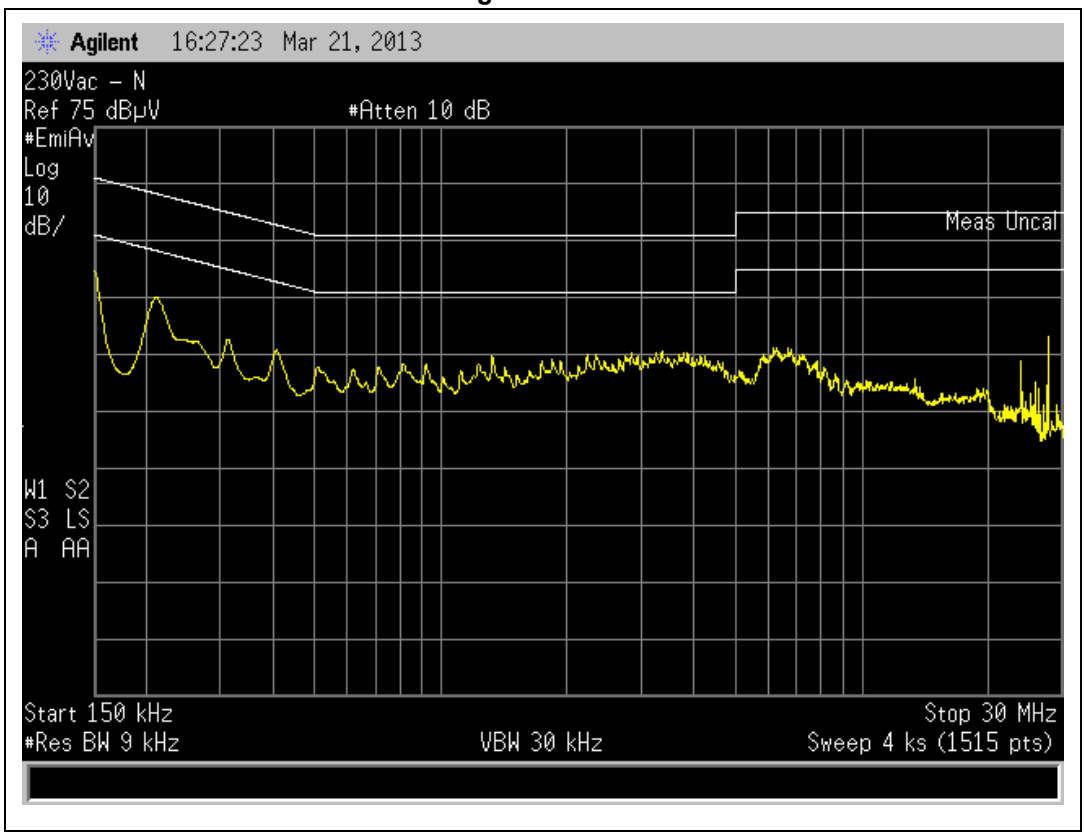


CH1 (brown): rectified input voltage (on the peak)
CH2 (purple: MOSFET source
CH3 (blue): MOSFET drain

7 Electromagnetic compatibility

The demonstration board meets the EN55015 - average limits.

Figure 28. EMI



8 Supporting material

Documentation

- ST HVLED815PF datasheet, “Offline LED driver with primary-sensing and high power factor up to 15 W”
- ST AN1059, ”Design equations of high-power-factor flyback converters based on the L6561”
- ST AN1262, “Offline flyback converters design methodology with the L6590 family”.

9 Revision history

Table 4. Document revision history

Date	Revision	Changes
10-Feb-2014	1	Initial release.