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**L99ASC03G PMSBLDC sensorless 3-phase motor driver**

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**Introduction**

The L99ASC03G is a 3-phase BLDC driver IC. The device can drive six external MOSFETs in BLDC drive systems and detect back EMF zero-crossing events, thus allowing sensorless rotor position detection.

This application note is intended to provide guidance to users on specific application-related topics.

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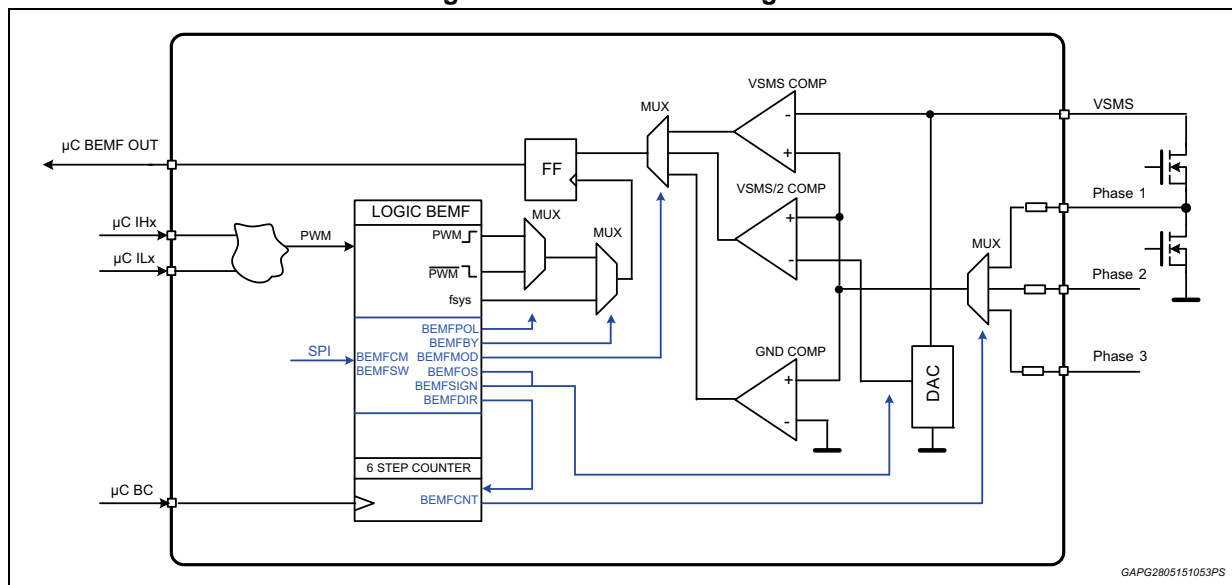
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# 1 BEMF Zero crossing detection internal peripheral

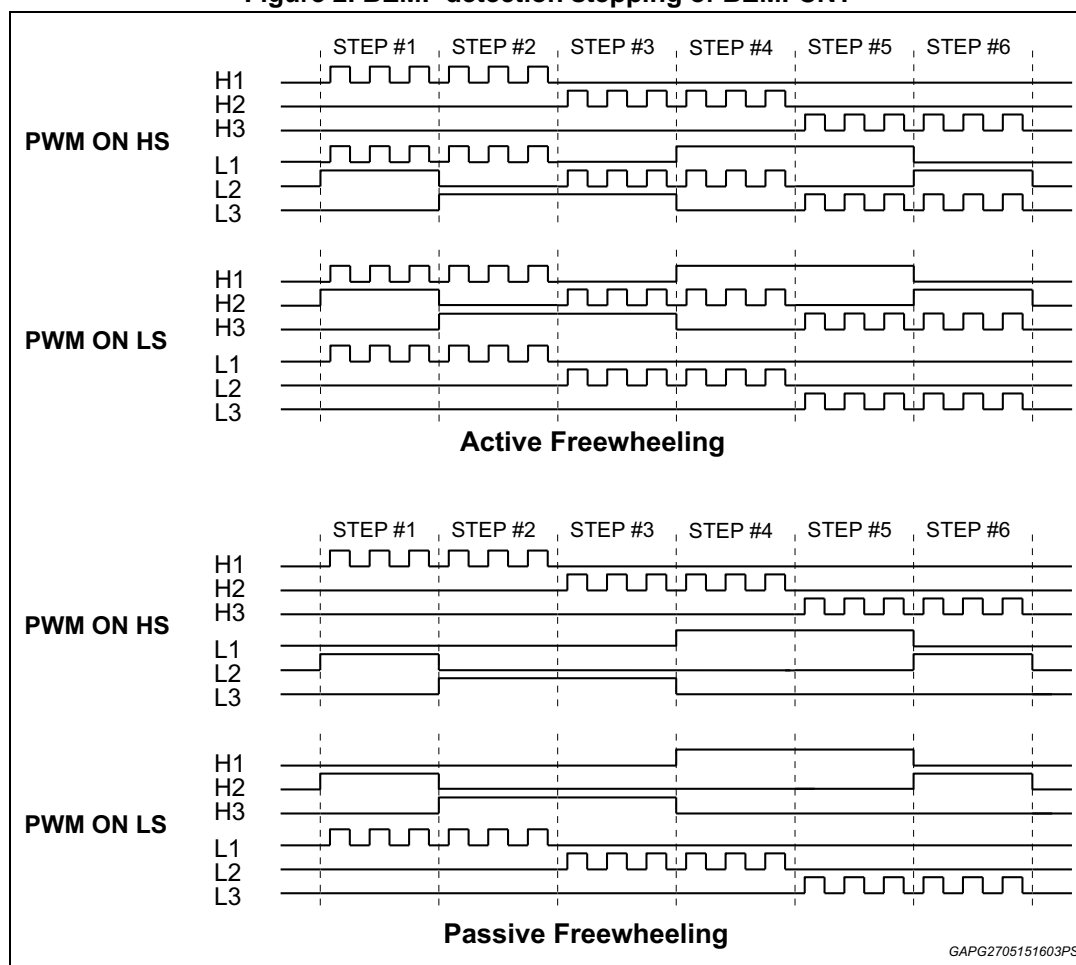
Designed to achieve the six step driving mode, the BEMFIP is based on a 6 step counter (BEMFCNT bits) which selects, according to [Figure 2](#), the floating phase sent to the input of three comparators in order to detect its BEMF Z crossing event. Of course we will select just one of the 3 comparator outputs through the BEMFMOD bit and sample it. The PWM sampling signal will be the one of the input channel (either ILx or IHx) chosen by the combinations of the following bits: BEMFCNT, BEMFSW, BEMFMOD & BEMFPOL (the sampling signal could be the driving PMW at the HSides, or the driving PWM at the LSides, or the active freewheeling PWM at the LSides, or the active freewheeling PWM at the HSides), whereas the PMW sampling edge will depend upon the combinations of the BEMFMOD & BEMFPOL bits. Even though everything seems a bit tricky, almost everything is done automatically by the BEMF IP state machine itself.

**Figure 1. BEMFIP block diagram**



For instance, according to [Figure 2](#), for BEMFCNT = 1 the floating phase sent to the comparators will always be phase #3, namely the motor terminal connected to SH3 pin, and the PWM sampling signal will be either IH1 or IL1. With the PWM on the HS MOSFETs (BEMFSW = 0) and BEMFMOD = 1, selecting the BUS/2 comparator output, the PWM input signal used to sample the output of the BUS/2 comparator will be IH1, whereas with the PWM on the LS MOSFETs (BEMFSW = 1) and BEMFMOD = 1, the PWM input signal used to sample the output of the BUS/2 comparator (BEMFMOD = 1) will be, this time, IL1.

Figure 2. BEMF detection stepping of BEMFCNT

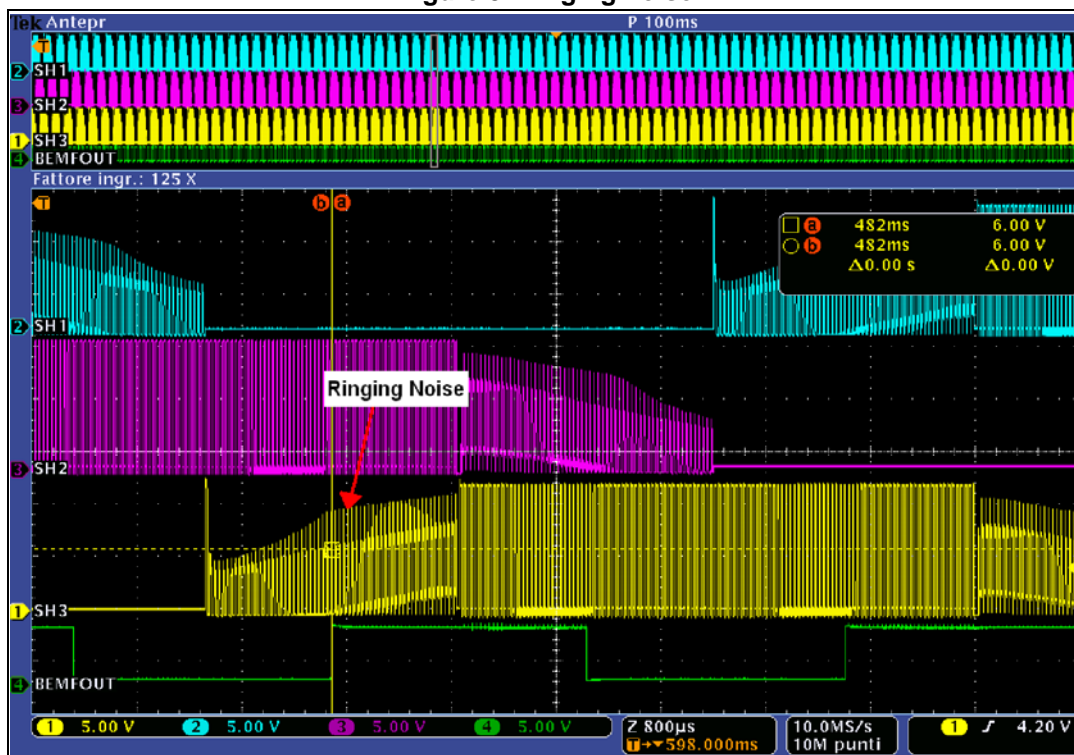


To avoid detecting a false Z crossing event due to the PWM switching noise (ringing: see [Figure 3](#)), we recommend reading the floating phase as far as possible from the switching edges, this is why the output of the selected comparator can be sampled by the appropriate edge of the appropriate PWM signal (Driving PWM signal or Active Freewheeling PWM signal). Therefore, for LOW DUTY CYCLES we recommend using the GND comparator for PWM on the HS MOSFETs and the VSMS comparator for PWM on the LS MOSFETs to detect free of noise Z crossing event, in this case, in fact, the floating phase will be sampled usually at the end of the active freewheeling PWM TON (this means close to the end of the driving PWM TOFF). Whereas for HIGH DUTY CYCLES we recommend using the  $V_{SMS/2}$  comparator to detect free of noise Z crossing events. In this case, in fact, the sampling will be performed always at the end of the driving PWM TON. While in the latter case the output of the  $V_{SMS/2}$  comparator is always sampled at the turning OFF command edge of the driving PWM signal. In the previous case the output of the GND/BUS comparator can be either sampled at the turning OFF command edge of the active freewheeling PWM signal for BEMFPOL = 1 or at the turning ON command edge of the driving PWM signal (this option is mandatory when there is no active freewheeling). The BEMFBY bit allows switching from the PWM sampling source to the internal 10MHz sampling source, mandatory selection for a PWM with a 100% Duty Cycle. [Table 1](#) provides the PWM sampling edge according to the bits configuration.

Table 1. PWM edge used for filtering the selected BEMF Z crossing comparator output

BEMFMOD	BEMFSW	BEMF comparator selected	BEMFPOL	BEMF sampling	Comment
0	0 (PWM on HS)	GND comparator	0	HS turn-on	To be used for passive freewheeling. We recommend selecting the GND comparator output for low PWM duty cycles.
0	0 (PWM on HS)	GND comparator	1	LS turn-off	To be used for active freewheeling. We recommend selecting the GND comparator output for low PWM duty cycles.
0	1 (PWM on LS)	V <sub>SMS</sub> comparator	0	LS turn-on	To be used for passive freewheeling. We recommend selecting the V <sub>SMS</sub> comparator output for low PWM duty cycles.
0	1 (PWM on LS)	V <sub>SMS</sub> comparator	1	HS turn-off	To be used for active freewheeling. We recommend selecting the V <sub>SMS</sub> comparator output for low PWM duty cycles.
1	0 (PWM on HS)	V <sub>SMS/2</sub> comparator	X	HS turn-off	We recommend selecting the V <sub>SMS/2</sub> comparator output for high PWM duty cycles.
1	1 (PWM on LS)	V <sub>SMS/2</sub> comparator	X	LS turn-off	We recommend selecting the V <sub>SMS/2</sub> comparator output for high PWM duty cycles.

Figure 3. Ringing noise



The BEMFCNT can be updated via SPI by writing its new value on it, or through a positive pulse (the width of the pulse must be greater than 1µs) at the BC input pin. The update mode, set by the BEMFCM bit is exclusive, this means that in SPI mode, a pulse over the BC pin will not update the counter value. This implies that the first value of the counter must be written before selecting the BC mode. Besides, in BC mode, the BEMF counter will automatically increase or decrease its value at the reception of a positive pulse according to the BEMFDIR bit value. Definitely the BC mode is useful for motors with a very high step switching frequency that would be for sure limited by the SPI communication itself.

A programmable offset can be added to the  $V_{S_{MS/2}}$  comparator threshold for Pre-Commutation. The offset sign is automatically updated in BC mode by the positive pulses, while it has to be overridden in SPI mode at each BEMFCNT update event. Be aware that demagnetization pulses could appear at the BEMFOUT pin, to filter them the BEMFCNT will have to be updated after a certain delay from a commutation event taking into account the demagnetization time. To understand better the demag pulses filtering at the BEMFOUT pin by delaying the BEMFCNT update events respect to the commutation events, we will consider [Figure 4](#) concerning a 100% duty cycle PWM. The concept is the same with a duty cycle different than 100%, in fact the only difference would be the sampling frequency. In case of a 100% duty cycle the sampling of the selected comparator output, the  $V_{S_{MS/2}}$  comparator, will be done at 10MHz. Let's focus on the red vertical line of [Figure 4](#). The line shows where, after the commutation, we updated the BEMFCNT, thus changing the signal to be sampled, in order to detect the next crossing event, from SH1 to SH3. As it can be seen from the picture, if we had continued sampling SH1 until the end of the demag pulse, we would have completely filtered the SH3 demag pulse at the BEMFOUT pin. This could have been made possible, merely by delaying the BEMFCNT update event respect to the related commutation event until the end of the demag pulse itself. In the example shown by [Figure 4](#) the BEMFCNT was updated right during the demag pulse, that is why the pulse is partially but not totally filtered at the BEMFOUT pin.



Figure 4. BEMFCNT update event



Customers not interested in detecting the rotor position through the *BEMF Detection* IP, could use it to read the motor speed. In this latter case two consecutive zero crossing events, corresponding to signal transitions (one rising edge and one falling edge, excluding of course demagnetization pulses) at the BEMFOUT pin, will provide the step time.

## 2 Flashing an external microcontroller

The watchdog inside the L99ASC03G acts on both the NRES pin and the VDD pin.

In case these pins are connected to an external microcontroller, then either the watchdog has to be disabled or the connections have to be removed before flashing the microcontroller.

To flash the microcontroller, one of the following techniques could be chosen:

1. Put the L99ASC03G in VDD Standby Mode with ICMP = 1 and then download the microcontroller firmware. Care must be taken in order not to wake up the device from VDD Standby Mode (via SPI frame or INH high).  
Since the watchdog is disabled in VDD Standby Mode when ICMP = 1, the device will not act on the NRES pin and on the VDD pin while the firmware code is downloaded into the microcontroller.
2. Put the L99ASC03G in Flash Mode and then download the firmware.  
Regardless of its operating mode, the device can be put in Flash Mode by applying a voltage greater than  $V_{BC,rising}$  (see L99ASC03G datasheet) at the BC pin.  
We recommended connecting the BC input pin to GND if not used or to a microcontroller GPIO if used, to update the BEMFCNT in block commutation mode.
3. Remove the NRES connection between the microcontroller and the device, power the microcontroller through an external 5V source and then download the firmware.  
During the download process the device will most likely enter in VBAT STDBY mode due to missing WDG trigger, hence the device will have to be woken up from VBAT STDY mode after the programming phase. Once programmed, the NRES and VDD connections will have to be restored and the system rebooted.

### 3 Quick motor startup

Assuming no ongoing failure condition that would hinder the gate drivers to work (in fact there are several errors that disable the gate drivers), the following steps are the minimum ones required for a quick startup of the motor:

- Pull the DISABLE pin low
- Send a **Clear all status register command** to the driver
- Program the PCSO/PCSI bits with any value different from zero
- Configure the BEMFIP properly (not needed if the BEMFIP is not used)
- Start triggering the Watchdog
- Drive the IHx and the ILx inputs properly to drive the MOSFETs and make the motor spin

If any failing condition that disables the gate drivers will still be ongoing, before running any of the foresaid steps the failing conditions affecting the gate drivers should be all removed. For instance, in case of a power supply slow ramp, the application, with the device exiting from a POR, could face a temporary (the time span within this condition will depend on the ramp up slope) VDD\_UV condition, which will disable the gate drivers. To overcome this situation the microcontroller should continuously send clear all status registers commands until VDD\_UV failures will no longer be detected.

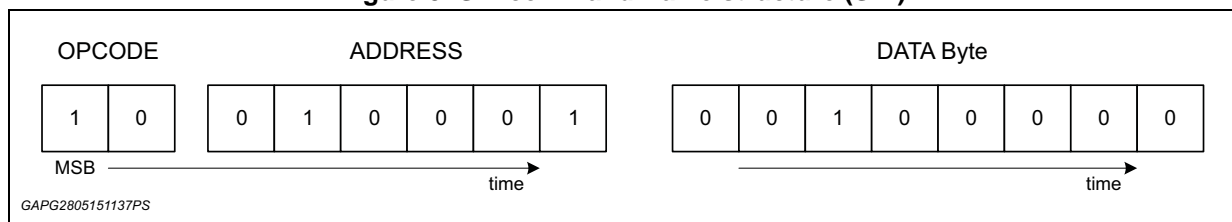
## 4 Diagnostic

Diagnostic information is classified in different categories: Functional Errors (FE), Device Errors (DE), Fail Safe errors (FS) and Global Warnings (GW).

Once entered in FS condition due to a detected FS event, all the control registers are *write* protected, except the following bits: WDG trigger & GOSTBY/STBYSEL, which allow sending the device in one of the two possible STDBY modes, even though the device is in FS condition. In Fail Safe condition the following features will be disabled and all the control registers, except Control Register 1 and DSFT\_DIS bit, will be reset to default values. These are the blocks disabled in Fail Safe condition: CP, BEMFIP, CSA & GATE DRIVERS (actively discharged before disabling them). Some events detected by default as faults could be programmed just to trigger warnings instead. This latter option can be controlled/modified by SPI. An error flag, except NRDY (automatically cleared), can be cleared only if the related fault condition ended before the reception of the related R&C command; otherwise the flag will not be cleared. Since the NRDY flag will automatically be cleared as soon as the VCP, right after a POR, rises above the VCPLow threshold, it could happen that a reading command of the content of SR1, that includes the NRDY flag, received while the NRDY flag is being automatically cancelled, returns the following wrong temporary reading of the status register (SR1):0800h for CPLOWM = 1 or 0200h for CPLOWM = 0 (of course assuming the NRDY flag the only one responsible for a GSB value different than 80h. In fact the expected value returned by a reading command should be 0840h or 0240h respectively). After this temporary wrong value read any further reading command of SR1 will return to its correct value, which is 8000h.

It is important to know that the device supports bitwise Read and Clear operations for each status register. This means that a R&C operation can be addressed to specific status flags. For instance to clear just the DISABLE status flag (BIT5) of Status Register 1, the microcontroller should send the following binary code to achieve the desired effect without clearing any other flag of the same register:

**Figure 5. SPI command frame structure (SDI)**



## 5 Watchdog

In Active Mode, as soon as the NRES pin is released, the watchdog starts with a Long Open Window (LOW). To end the LOW and start the window watchdog, a 1 has to be written to the WDTRIG bit in CR1 before the LOW expires (typ. 65ms). If this does not occur, a watchdog fault event is generated; after 15 consecutive watchdog faults, the device enters VBAT Standby Mode. Writing 0 to the WDTRIG bit during the LOW has no effect.

Once in window mode, the WDTRIG bit has to be toggled within the open window. Writing the previous value to this bit has no effect. A watchdog trigger command is accepted only at the CSN rising edge of the corresponding SPI frame.

When the ICMP bit is set to 1, the watchdog is disabled during VDD Standby Mode and restarts with a LOW after a wake-up event.

Conversely, when the ICMP bit is set to 0, the watchdog state in VDD Standby Mode depends on the current drawn from the VDD regulator (IDD). If this current is greater than the ICMP threshold, then the watchdog remains active, otherwise it is disabled and restarts with a LOW after a wake-up event. Moreover, if IDD becomes greater than the ICMP threshold in VDD Standby Mode when ICMP=0, then the watchdog is automatically re-enabled.

Watchdog failures are generated when toggling the WDTRIG bit during the closed window or when the watchdog period or the LOW have expired.

After 8 consecutive watchdog failure events, the VDD regulator is turned off for 200ms and then re-enabled. In case of 7 additional and consecutive watchdog failures, the device enters VBAT Standby Mode.

When a watchdog failure occurs, the WDF bits are incremented. They are cleared as soon as a valid watchdog trigger is received. After a watchdog failure, a reset pulse is generated at the NRES pin, the watchdog restarts with a LOW, the FSWD flag is latched and the device enters a fail-safe state until the FSWD flag is read and cleared via SPI.

The watchdog is always disabled in Flash Mode. To disable it in Active Mode, the WDDIS bit has to be set to 1 in Flash Mode before entering Active Mode.

## 6 Unused pins

[Table 2](#) shows the recommended connections for the unused pins of the device.

**Table 2. Unused pins connection**

Block/feature not used	Pins	Connection
CSA	CSI+/CSI-	Tied together and connected to GND
	CSO	OPEN
Disable	DIS	GND
Analog MUX	AOUT	OPEN
BEMF detection IP	BEMFOUT	OPEN
	BC <sup>(1)</sup>	GND <sup>(2)</sup>
Digital output	DOUT	OPEN
Interrupt to microcontroller	NINT	OPEN
NC	PIN 28	OPEN or VDD
	PIN 25	OPEN or 1 K $\Omega$ to VS
5 V voltage regulator	VDD	Ceramic capacitor $\geq$ 660 nF tied to GND and at least 6 mA dummy load
	NRES	Open or to a microcontroller GPIO to monitor microcontroller reset attempts triggered by the device
INH wake-up source from Standby Modes	INH	OPEN or GND

1. BEMF detection IP not used or BEMFCNT SPI update mode selected.
2. In Active Mode, the BC pin can be connected to GND. However it can be pulled high to enter Flash Mode and program the external microcontroller.

## 7 PRE-DRIVE tests

Before driving the MOSFETs, it is possible to detect whether any of the motor phases is disconnected or short-circuited either to GND or to the supply voltage. This diagnosis can be performed thanks to three switches that can be closed or opened through the following control bits of Control Register 7:

ISTEST(x): control bit for the sink current of leg x:

- 0: sink current disabled
- 1: sink current enabled

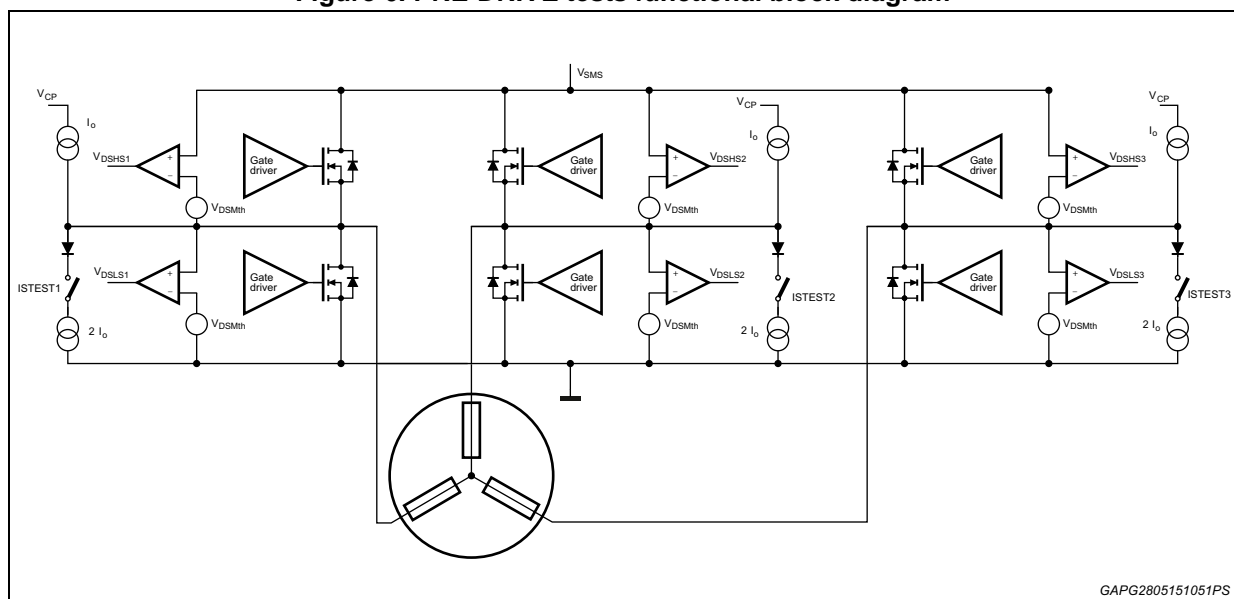
ISTEST(x) = 0 means that the corresponding x switch is open.

The tests shown in [Table 3](#) allow the detection of disconnected motor terminals and short circuits of at least one motor terminal either to GND or to supply voltage, without turning on any external MOSFET.

During the PRE-DRIVE tests, the DS Monitoring threshold (DSMTH[1,0]) has to be set to 2 V and the gate driver sink current bits (PCSI[3:0]) have to be set to the max value (1111b).

When changing the ISTEST bits, a certain time has to elapse before reading the result of each test from Status Register 7 (SR7) in order to allow the diagnostic currents to settle in the motor phases and yield a steady-state voltage drop over the external MOSFETs. In order to perform the PRE-DRIVE tests, the ISTEST\_EN bit has to be set to 1. This is to allow the SR7 bits to change their state without turning on the external MOSFETs.

Figure 6. PRE-DRIVE tests functional block diagram



In this case, no flag is reported in the Global Status Byte (GSB) due to the SR7 bits.

When the PRE\_DRIVE tests are complete, the SR7 bits have to be cleared right after setting the ISTEST\_EN to 0. Otherwise, the status of the SR7 bits would be reflected in the GSB. It is also recommended to set the ISTEST(x) bits back to 0 at the end of the PRE-DRIVE tests.

Table 3. PRE-DRIVE tests summary table

ISTEST_EN	ISTEST(1)	ISTEST(2)	ISTEST(3)	DSHS(1)	DSLS(1)	DSHS(2)	DSLS(2)	DSHS(3)	DSLS(3)	Comment
1	0	0	0	0	1	0	1	0	1	No short to ground
1	0	1	1	1	0	X <sup>(1)</sup>	X	X	X	No open load at phase 1
1	1	0	1	X	X	1	0	X	X	No open load at phase 2
1	1	1	0	X	X	X	X	1	0	No open load at phase 3
1	1	1	1	1	0	1	0	1	0	No short to battery

1. X= do not care.

**Example 1**

To test the connection of Phase1, the ISTEST\_EN bit and the ISTESTx bits have to be set as follows: ISTEST\_EN = 1, ISTEST[1] = 0, ISTEST[2] = ISTEST[3] = 1. The result of this test is given by the DSHS1 and DSLS1 bits in Status Register 7. If the result is DSHS1 = 1 and DSLS1 = 0 this means that Phase1 is connected, otherwise for DSHS1 = 1 and DSLS1 = 1 Phase1 is disconnected.

In fact, considering the SH1 pin for ISTEST1 = 0 and ISTEST2 = ISTEST3 = 1, if Phase1 is disconnected, then I<sub>o</sub> pulls up SH1 (no pull-down current is present, as ISTEST1 is open), thus yielding DSHS1 = 0 and DSLS1 = 1 (see Figure 7). Conversely, in case all motor phases are connected, we have a pull-up current of 3I<sub>o</sub> and a pull-down current of 4I<sub>o</sub>, which yields DSHS1 = 1 and DSLS1 = 0 (see Figure 8).

Figure 7. PRE-DRIVE test example: Phase 1 disconnected

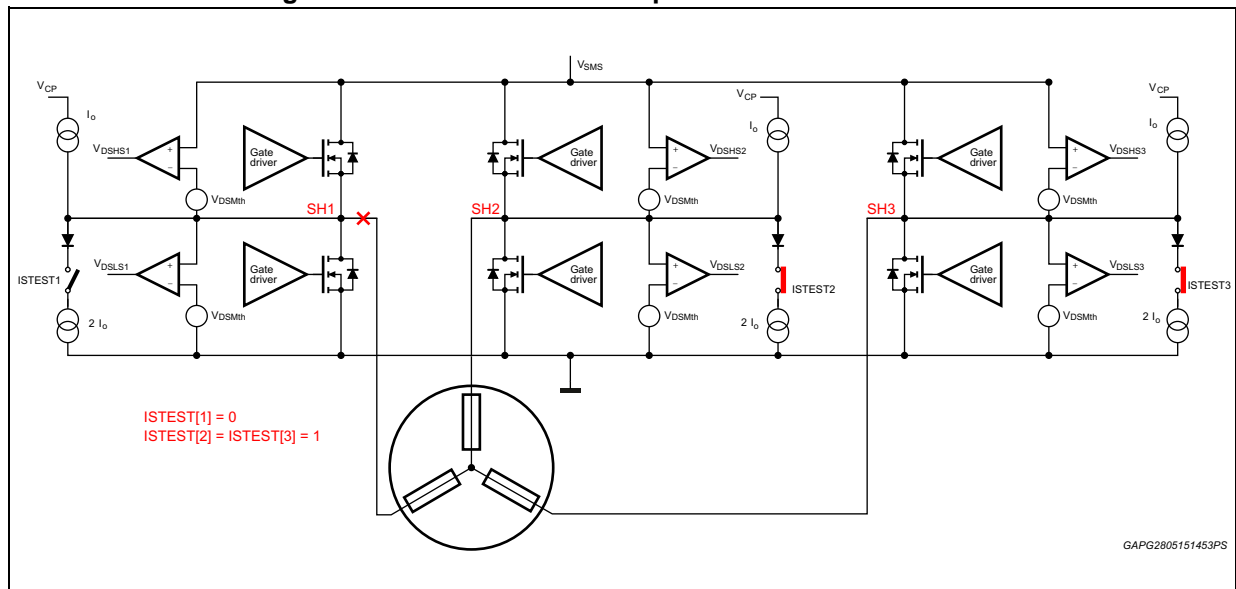
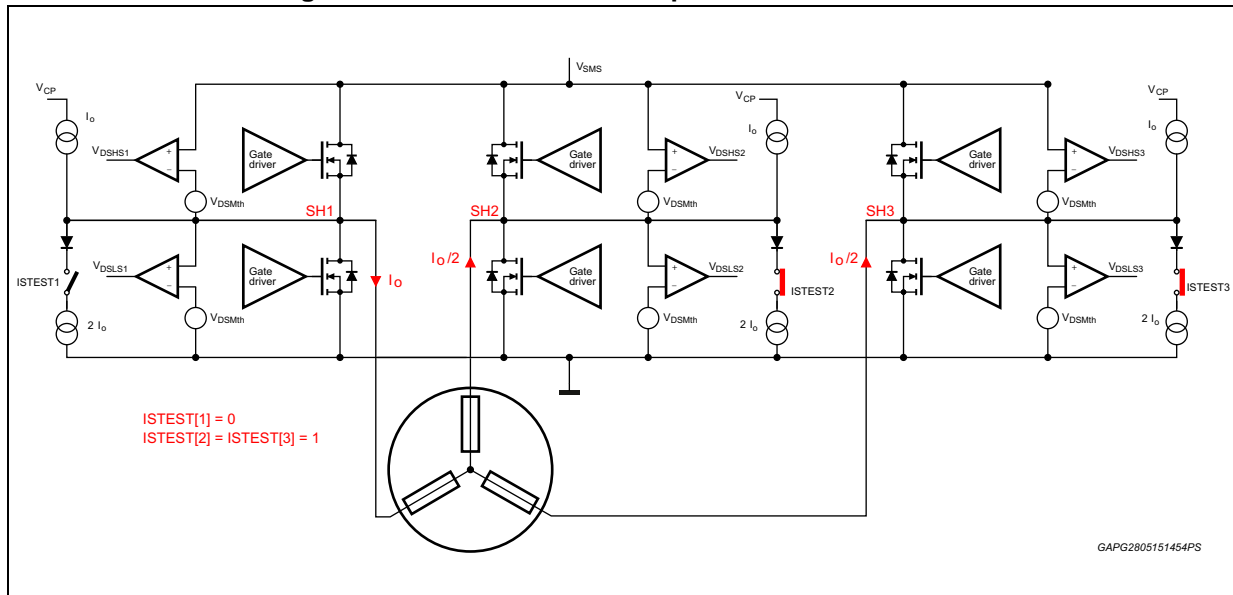




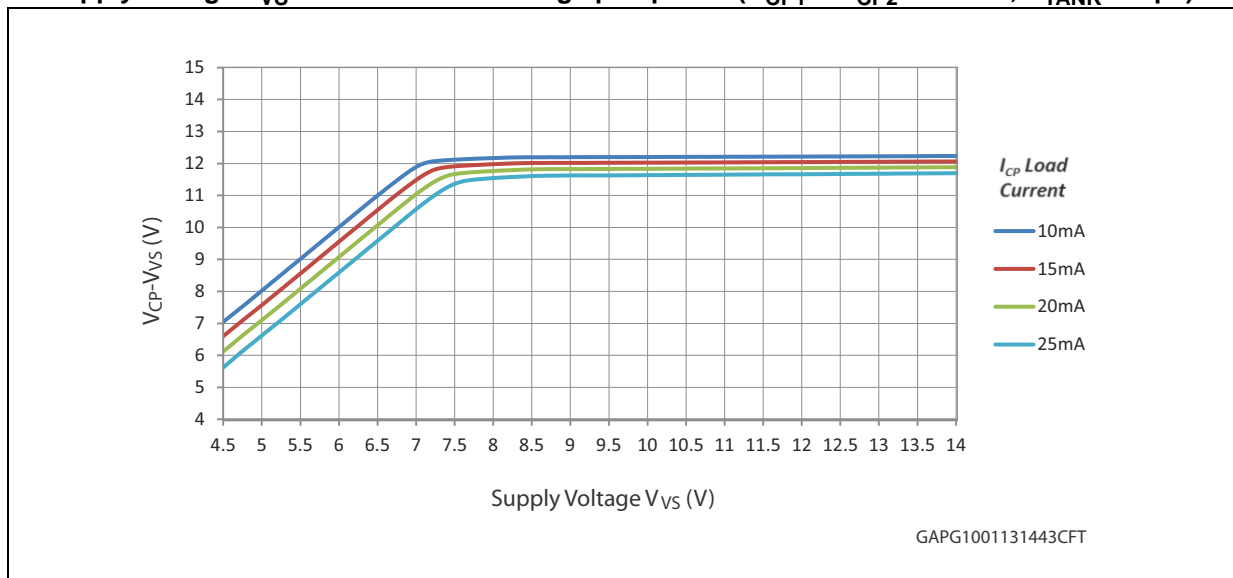
Figure 8. PRE-DRIVE test example: Phase 1 connected



### Charge pump output voltage

The integrated two-stage charge pump is supplied from the VS pin. The curves in [Figure 9](#) have been measured on one L99ASC03G unit at room temperature. [Figure 9](#) can be used in conjunction with the  $V_{CPLOW}$  parameter in the datasheet to assess if the charge pump can provide enough voltage to drive the external MOSFETs and if the L99ASC03G will set the CPLOW flag (bit 7 in Status Register 1).

Figure 9. Difference between charge pump output voltage and input supply voltage vs. input supply voltage  $V_{VS}$  as a function of charge pump load ( $C_{CP1} = C_{CP2} = 220 \text{ nF}$ ,  $C_{TANK} = 1 \text{ }\mu\text{F}$ )



## 8 Estimating power dissipation

The power dissipation  $P_D$  of the L99ASC03G depends on use conditions and external components. Considering the main contributions, we can write:

$$P_D = P_{VDD} + P_{REG} + P_{CP} + P_{DRV}$$

where

$P_{VDD}$ : power dissipation of the VDD voltage regulator

$P_{REG}$ : power dissipation of the internal voltage regulator

$P_{CP}$ : power dissipation of the charge pump

$P_{DRV}$ : power dissipation of the gate drivers

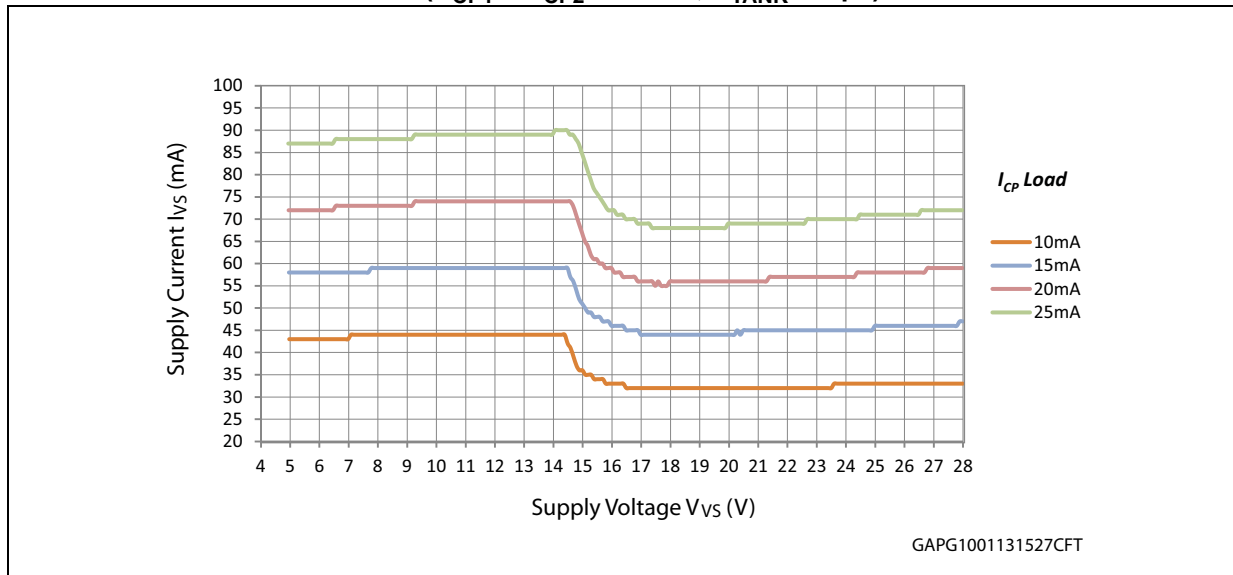
$$P_{VDD} = (V_{VSREG} - V_{VDD}) \times I_{VDD}, \text{ with } V_{VDD} = 5V$$

$$P_{REG} = V_{VSREG} \times I_{VSREG}, \text{ with } I_{VSREG} = 25mA \text{ max}$$

As to  $P_{CP}$  and  $P_{DRV}$ , no formula can be used to calculate their contribution. Application-related parameters have a direct influence on these terms, such as the total gate charge of the external MOSFETs ( $Q_G$ ), the PWM frequency used to drive the motor ( $f_{PWM}$ ) and the number of MOSFETs switched in a PWM period ( $N$ ). Using external gate resistors will reduce the power dissipation in the L99ASC03G.

As a worst-case scenario,  $P_{CP}$  and  $P_{DRV}$  can be estimated by using [Figure 10](#). The curves in [Figure 10](#) have been measured on one L99ASC03G unit at room temperature.

**Figure 10. Supply current at VS pin vs. input supply voltage  $V_{VS}$  as a function of charge pump load ( $C_{CP1} = C_{CP2} = 220 \text{ nF}$ ,  $C_{TANK} = 1 \text{ }\mu\text{F}$ )**



## 9 Calculation example

Let's assume the following use conditions:

$$V_{VSREG} = V_{VS} = 12V$$

$$I_{VDD} = 20mA$$

$$Q_G = 60nC$$

$$f_{PWM} = 25kHz$$

$$N = 6$$

From the above mentioned formulas for  $P_{VDD}$  and  $P_{REG}$  we get

$$P_{VDD} = (V_{VSREG} - V_{VDD}) \times I_{VDD} = (12V - 5V) \times 20mA = 140mW$$

$$P_{REG} = V_{VSREG} \times I_{VSREG} = 12V \times 25mA = 300mW$$

The load at the charge pump output due to the external MOSFETs is

$$I_{CP} = N \times f_{PWM} \times Q_G = 9mA$$

By looking at [Figure 10](#), for a charge pump load of 10mA ( $\approx 9mA$ ) at  $V_{VS} = 12V$ , the input current  $I_{VS}$  is 44mA. The power consumption from the VS pin can be estimated as

$$P_{VS} = V_{VS} \times I_{VS} = 12V \times 44mA = 528mW$$

The worst-case total power dissipation  $P_D$  can thus be estimated as

$$P_D = P_{VDD} + P_{REG} + P_{VS} = 140mW + 300mW + 528mW = 968mW$$

## 10 CSA and OC comparator

Besides Overcurrent (OC) monitoring, the combination of CSA and OC comparator can be used for the sensor less initial Rotor Position Detection. The sensor less initial RPD is performed by energizing the motor coils in a specific way and sequence in order to measure the phase-to-phase inductance variation, which depends on the relative position between rotor and stator. Based on the known relationship  $V = Ldi/dt$ , this can be achieved by measuring the time needed to reach a given overcurrent level in the energized phases that is low enough to keep the rotor still. The microcontroller can program the desired overcurrent level and measure the required time. Before starting the sensor-less initial RPD process, the OCFT\_DIS bit has to be set to 1 to disable the OC filtering time. This also prevents the CSAOC flag from being set in case an OC event is detected. Moreover, the DMUX bit has to be set to 1 to have the output of the OC comparator connected to the DOUT pin.

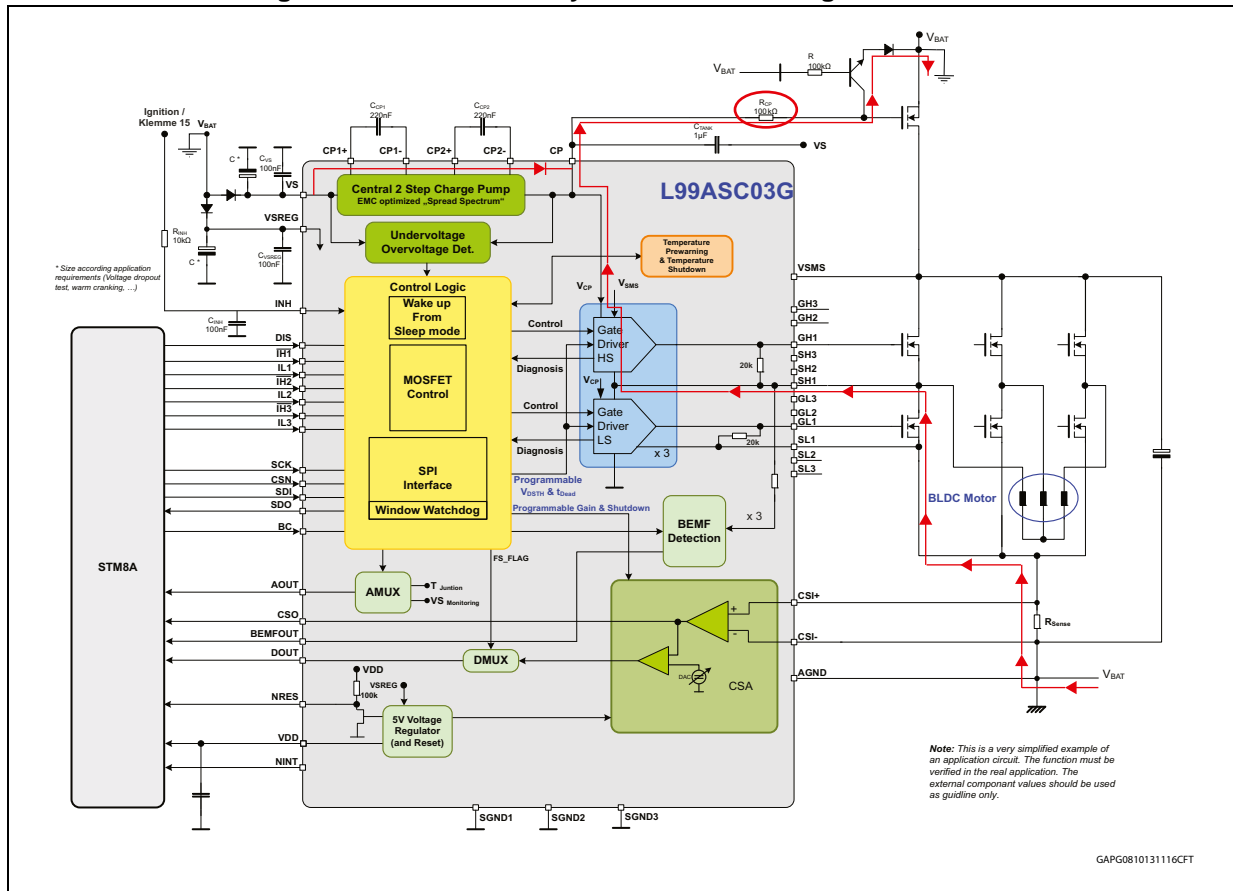
## 11 External components

Since the source and sink currents of the L99ASC03G gate drivers are adjustable via SPI, there is no need to have gate resistors to control the MOSFETs slew rate. However, gate resistors may be used to dampen the ringing that could slow down the MOSFET turn-on. External resistors between gate and source of each MOSFET could be used as an additional safety measure against accidental disconnection of the MOSFET gate pins from the driver. In fact, an internal resistor is present between each gate pin and the related source pin of the device to prevent the gate from floating.

There is no need for an external VGS clamp either, since there is an internal circuit that will keep the VGS between the following values:  $V_{SLx} + 9 / V_{SHx} + 9$  and  $V_{SLx} + 13 / V_{SHx} + 13$ . The capacitor between VSMS and GND has to be sized according to the application. Due to the Drain Source Monitoring we recommend connecting each SLx and SHx pin directly to the source of the corresponding MOSFET, in order to have separate paths. The direct drive inputs have internal pull-ups and pull-downs in order to avoid an accidental turn-on of the MOSFETs due to noise. Be careful that the BC input pin absolute max rating is 20 V. VDD must have at least 660 nF (ESR < 50 mΩ) connected between VDD and GND, close to VDD, with a minimum load of 6 mA. The capacitance between CPx+ and CPx- should be 220nF, while the capacitance between CP and VS should be 1 μF. As shown in [Figure 11](#), it is recommended to insert a 100 kΩ resistor between the CP pin and the gate of the reverse battery protection MOSFET to minimize the current flowing in case of reverse battery.

VS and VSREG should have a 100 nF ceramic capacitor placed close to each pin and GND and also an electrolytic capacitor to be sized depending on application. We recommend placing a 10K series resistor followed by a 100 nF cap at the INH pin to protect it against ESD up to ±6 KV coming from the module connector.

Figure 11. Reverse battery current flow through the device



## 12 Trick and tips

When exiting VBAT Stand-by mode, all of the three high-side MOSFETs turn-on for few hundreds microseconds. During this time, the MOSFETs are protected against a short of the outputs to GND through Vds monitoring protection, any how - in order to avoid this turn-on to happen - it's sufficient to reset PCSO[3:0] bits before entering VBAT stand-by mode.

## 13 Revision history

Table 4. Document revision history

Date	Revision	Changes
19-Mar-2014	1	Initial release.
29-May-2015	2	Updated <i>Figure 2: BEMF detection stepping of BEMFCNT on page 6</i> .
10-Jun-2016	3	Updated <i>Section 1: BEMF Zero crossing detection internal peripheral</i> ; title in <i>Section 3: Quick motor startup</i> . Added <i>Section 12: Trick and tips</i> .
16-May-2018	4	Changed Rpn L99ASC03 in L99ASC03G.



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