AN4372
Application note

STEVAL-ISA134V1: 12 V / 4 W, 115 kHz isolated flyback

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Introduction

This document describes a 12 V - 4 W power supply in isolated flyback topology with VIPer06HN, a new off-line high voltage converter by STMicroelectronics.

The main features of the device are: 800 V avalanche rugged power section, PWM operation at 115 kHz with frequency jittering for lower EMI, cycle-by-cycle current limit with adjustable set point, on-board soft-start and safe auto-restart after a fault condition.

The available protections are: thermal shutdown with hysteresis, delayed overload protection, open loop failure protection (the last one is available only if auxiliary winding is used).

The present flyback converter is suitable for different applications. It can be used as an external adapter or as an auxiliary power supply in consumer equipment.

Figure 1. Evaluation board image: power supply board. Top layer

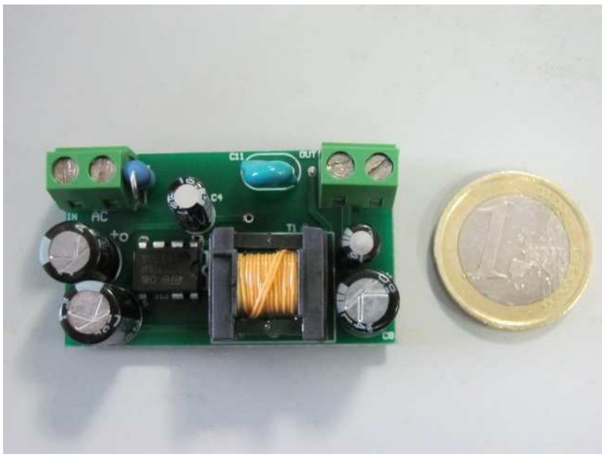
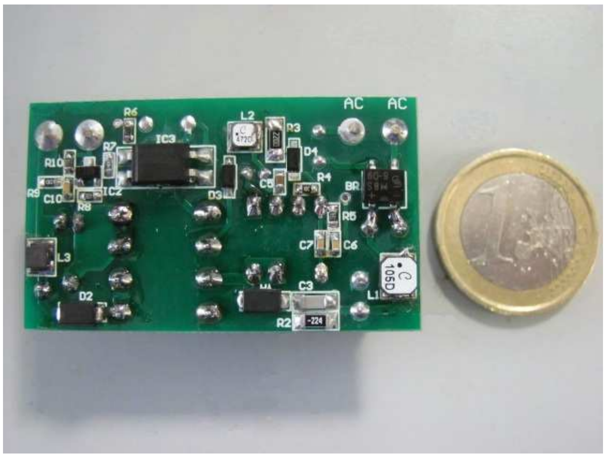


Figure 2. Evaluation board image: power supply board. Bottom layer



Contents

1 Test board: design and evaluation

The electrical specifications of the evaluation board are listed in *Table 1*.

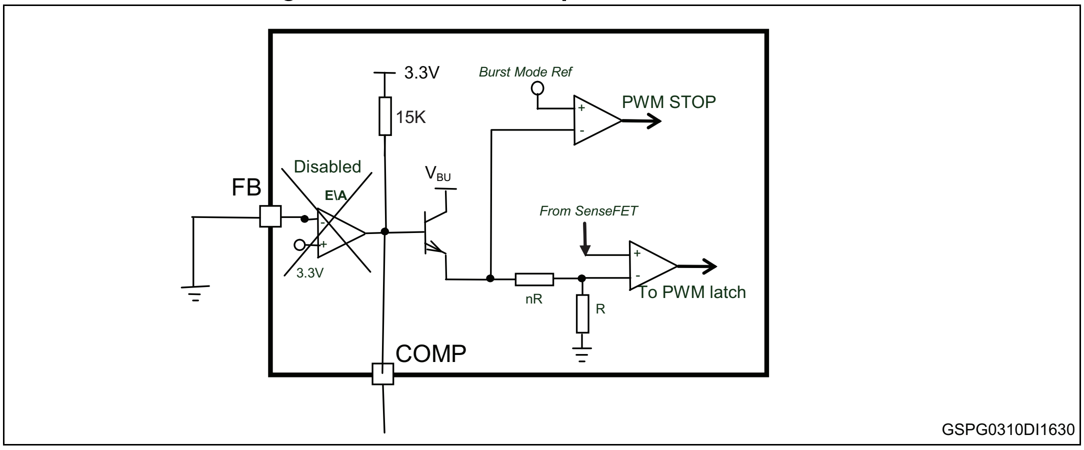
Table 1. Electrical specifications

Parameter	Symbol	Value
AC main input voltage	V_{IN}	[85 V_{AC}; 265 V_{AC}]
Main frequency	f_L	[50 Hz; 60 Hz]
Output voltage	V_{OUT}	12 V
Max output current	I_{OUT}	333 mA
Precision of output regulation	Δ_{VOUT_LF}	±5%
High frequency output voltage ripple	Δ_{VOUT_HF}	50mV
Min active mode efficiency	η_{AV}	71%
Max ambient operating temperature	T_{AMB}	60 ºC

The power supply is set in isolated flyback topology. The schematic is given in *Figure 4*, the bill of materials (BOM) in *Table 2*. Input section includes a resistor R1 for inrush current limiting, a diode bridge (BR) and a Π filter for EMC suppression (C1, L1, C2). The transformer core is a standard E13. A clamp network (D1, R2, C3) is used for leakage inductance demagnetization.

Being an isolated topology, FB pin must be connected to ground in order to disable the internal error amplifier. In this case, the feedback signal is transferred to the primary side through an opto-isolator, connected in parallel with the compensation network (R5, C6, C7) to the COMP pin.

Figure 3. FB and COMP pin internal structure



The resistor connected between LIM pin and ground, lowers the default current limitation of the device (according to the I_{DLIM} vs R_{LIM} graphic reported in the datasheet) to the value which is needed for the desired power throughput, thus avoiding unnecessary overstress on the power components. A small LC filter has been added at the output in order to filter the high frequency ripple.

At power-up the DRAIN pin supplies the internal HV start-up current generator which charges the C4 capacitor up to V_{DDon}. At this point the power MOSFET starts switching, the generator is turned off and the IC is powered by the energy stored in C4.

The IC is supplied by the auxiliary winding and the voltage delivered has to stay always above the V_{DDcs_on} threshold (11,5V max), in order to avoid that the HV start-up is activated. Auxiliary winding is connected to the V_{DD} pin through D3 and L2, where the inductor component is used to filter voltage spike on V_{DD} pin, during power MOSFET turn-OFF.

This solution is preferred because, using a resistor, the continuous voltage on V_{DD} pin would be reduced and the voltage could fall below the V_{DDcs_on} threshold.

An external clamp on V_{DD} pin (Zener diode and resistor) is used to protect the pin when overvoltage, due to an increase of output voltage, occurs on itself.

Figure 4. Electrical schematic

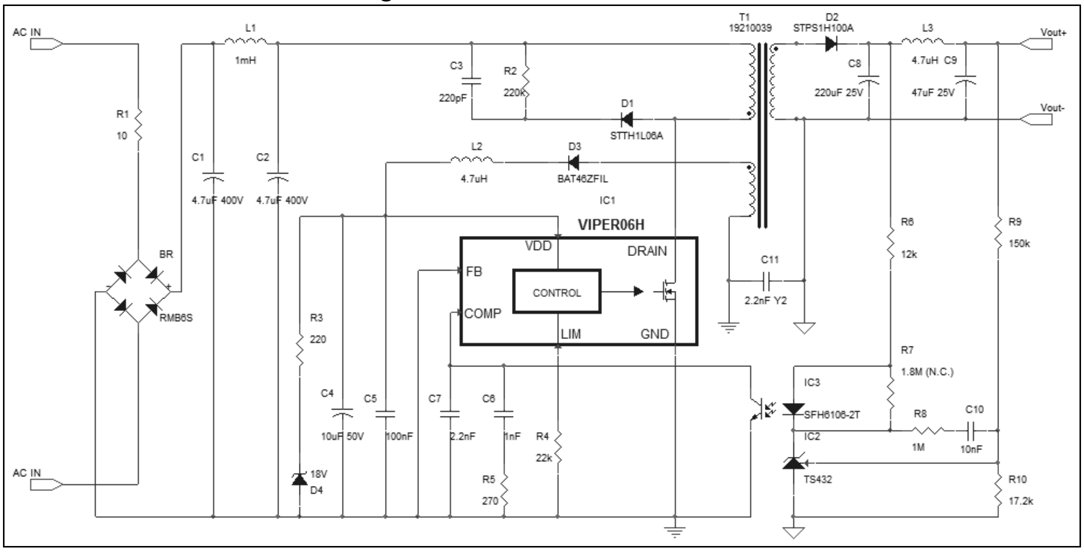


Table 2. Bill of materials (BOM)

Reference	Part	Description	Note
BR	RMB6S	0.5 A - 600 V bridge	Taiwan Semiconductor
R1		10 Ω - 1 W resistor	5% tolerance
R2		220 kΩ - 1/3 W resistor	5% tolerance
R3		220 Ω - 1/3 W resistor	5% tolerance
R4		22 kΩ - 1/10 W resistor	1% tolerance
R5		270 Ω - 1/10 W resistor	5% tolerance
R6		12 kΩ - 1/10 W resistor	5% tolerance
R7		1.8 MΩ - 1/10 W resistor (N.C.)	5% tolerance
R8		1 MΩ - 1/10W resistor	5% tolerance
R9		150 kΩ - 1/10 W resistor	1% tolerance
R10		17.2 kΩ - 1/10 W resistor	1% tolerance
C1,C2		4.7 µF - Electrolytic capacitor 400 V	Rubycon
C3		220 pF - Capacitor 630 V	
C4		10 µF - Electrolytic capacitor 50 V	Rubycon
C5		100 nF - Capacitor 50 V	
C6		1nF - Capacitor 50 V	
C7		2.2 nF - Capacitor 50 V	
C8	ZL series	220 µF - Electrolytic capacitor 25 V	Rubycon
C9	ZL series	47 µF - Electrolytic capacitor 25 V	Rubycon
C10		10 nF - Capacitor 50 V	
C11		2.2 nF - Capacitor Y2	
D1	STTH1L06A	Ultrafast diode 1A – 600 V	ST
D2	STPS1H100A	Power Schottky 1 A – 100 V	ST
D3	BAT46ZFIL	Signal Schottky 0.15 A – 100 V	ST
D4	MMSZ5248B-V-GS08	Zener diode 18 V 0.5 W	
T1	1921.0039	Flyback transformer	Magnetica
	7508110341 Rev. 6A		Wurth
IC1	VIPer06HN	Offline primary controller	ST
IC2	TS432ILT	Low voltage adjustable shunt reference	ST
IC3	SFH6106-2T	Optocoupler	Vishay
L1	LPS4414	1 mH - Power inductor	Coilcraft
L2	LPS3008	4.7 µH - Power inductor	Coilcraft
L3	ME3220	4.7 µH - Power inductor	Coilcraft

The transformer characteristics are listed in the table below

Table 3. Transformer characteristics

Parameter	Value	Test conditions
Manufacturer	Magnetica	
Part number	1921.0039	
Primary inductance	1.5mH ± 15%	Measured at 1 kHz, T_{AMB} = 20 °C
Leakage inductance	17µH Nom.	Measured at 10 kHz, T_{AMB} = 20 °C
Primary to secondary turn ratio (3 - 4)/(5, 8)	6.87	Measured at 10 kHz, T_{AMB} = 20 °C
Primary to auxiliary turn ratio (3 - 4)/(2 - 1)	5.5	Measured at 10 kHz, T_{AMB} = 20 °C
Saturation current	0.27 A	Primary, B_{SAT} = 0.3 T, T_{AMB} = 20 °C
Operating current	0.22 A	Primary, P_{OUT} = 3.6 W, T_{AMB}=20 °C

Figure 5. Dimensional drawing and pin placement diagram - bottom view

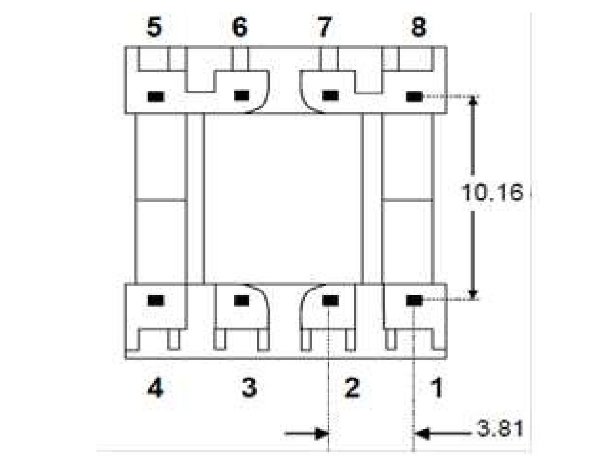


Figure 6. Dimensional drawing and pin placement diagram - electrical diagram

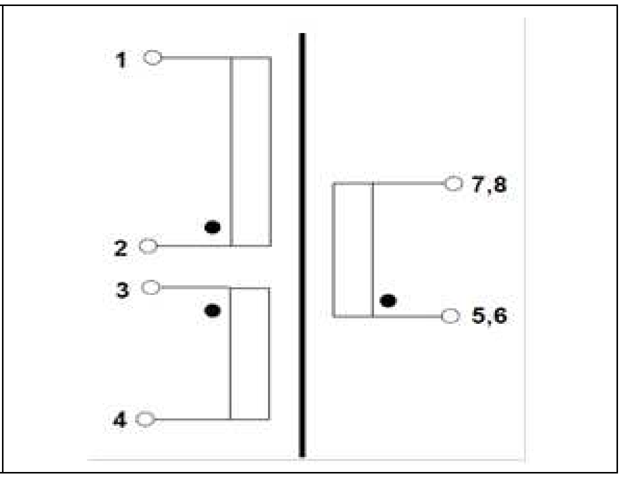


Figure 7. Dimensional drawing and pin placement diagram - side view 1

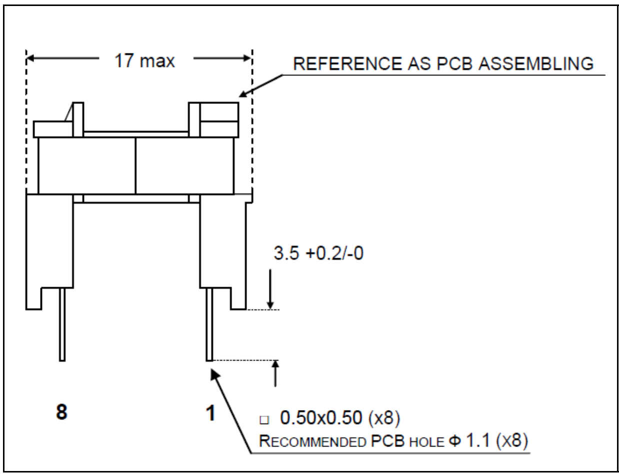
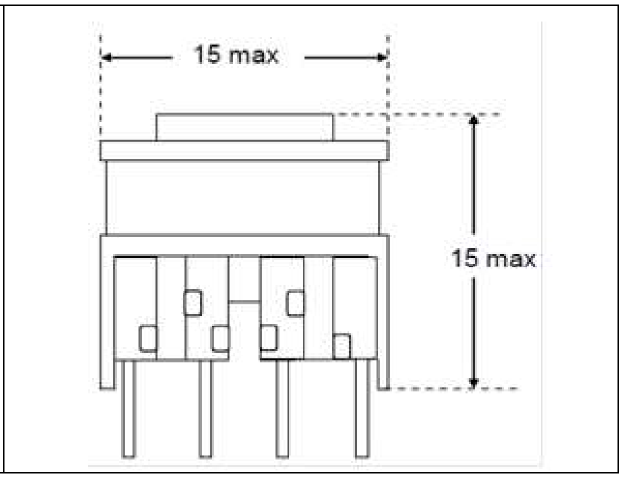


Figure 8. Dimensional drawing and pin placement diagram - side view 2



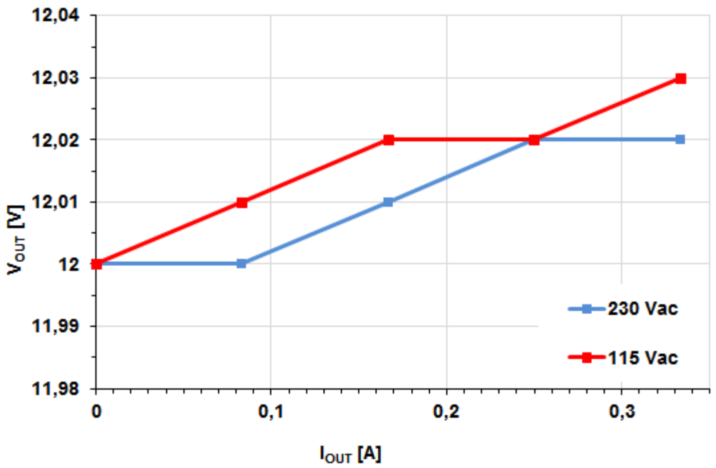
1.1 Output voltage characteristics

Output voltage of the board is measured in different line and load conditions. *Table 4* and *Figure 9* show the results. The output voltage value is affected little by line or load variations.

Table 4. Output voltage line-load regulation

V_{IN} (V_{AC})	V_{OUT} (V)			
	No load	**0.17 A**	**0.25 A**	**0.33 A**
85	12,00	12,02	12,03	12,03
115	12,00	12,02	12,02	12,03
150	12,00	12,01	12,02	12,03
180	12,00	12,01	12,02	12,03
230	12,00	12,01	12,02	12,02
265	12,00	12,00	12,01	12,02

Figure 9. Output voltage load regulation at nominal input voltages ($115\ V_{AC}$ and $230\ V_{AC}$)



1.2 Efficiency measurements

Any external power supply (EPS) must be capable of meeting the international regulation agency limits. The European code of conduct (EC CoC) and US Department of Energy (DoE - US EISA 2007) limits are taken as reference. EPS limits are fixed up to 70.88% when the average efficiency is measured. The efficiency of the converter has been measured in different load and line voltage conditions. The efficiency measurements have been performed loading at 25%, 50%, 75% and 100% of maximum rate at $115\ V_{AC}$ and $230\ V_{AC}$. *Table 5* and *Table 6* show the results.

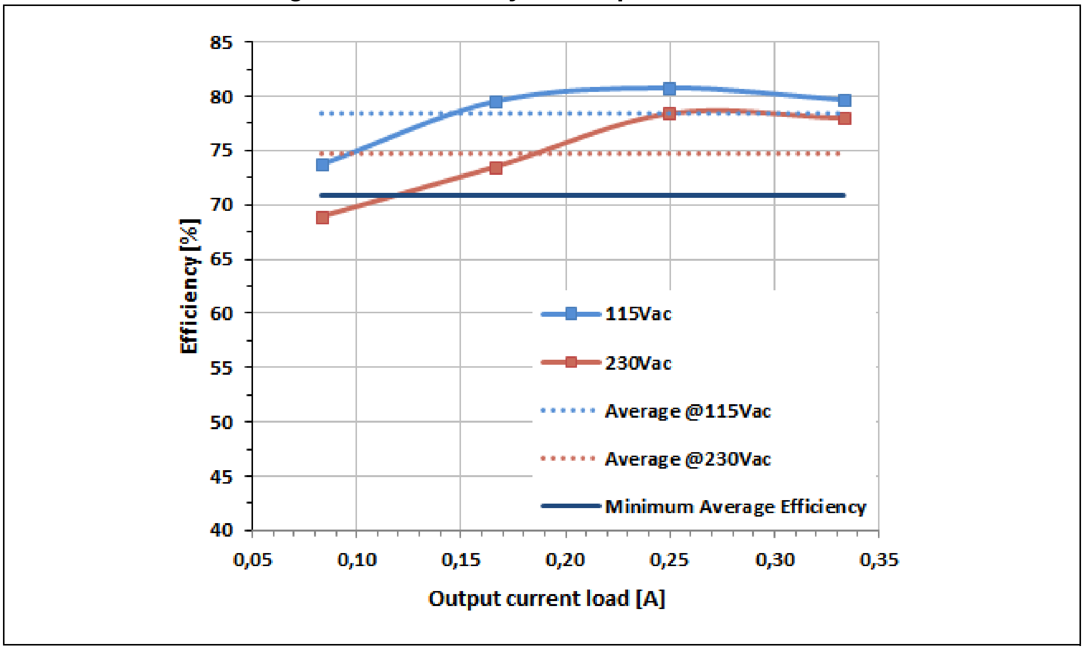
Table 5. Efficiency at $115\ V_{AC}$

%Load	I_{OUT} (A)	V_{OUT} (V)	P_{IN} (W)	P_{OUT} (W)	Efficiency%
25%	0,08	12,01	1,356	1,000	73.73
50%	0,17	12,02	2,516	2,001	79.54
75%	0,25	12,02	3,716	3,002	80.79
100%	0,33	12,03	5,027	4,006	79.69
Average efficiency					78.44

Table 6. Efficiency at $230\ V_{AC}$

%Load	I_{OUT} (A)	V_{OUT} (V)	P_{IN} (W)	P_{OUT} (W)	Efficiency%
25%	0,08	12,00	1,449	0,999	68.94
50%	0,17	12,01	2,720	2,000	73.52
75%	0,25	12,02	3,828	3,002	78.42
100%	0,33	12,02	5,131	4,003	78.01
Average efficiency					74.72

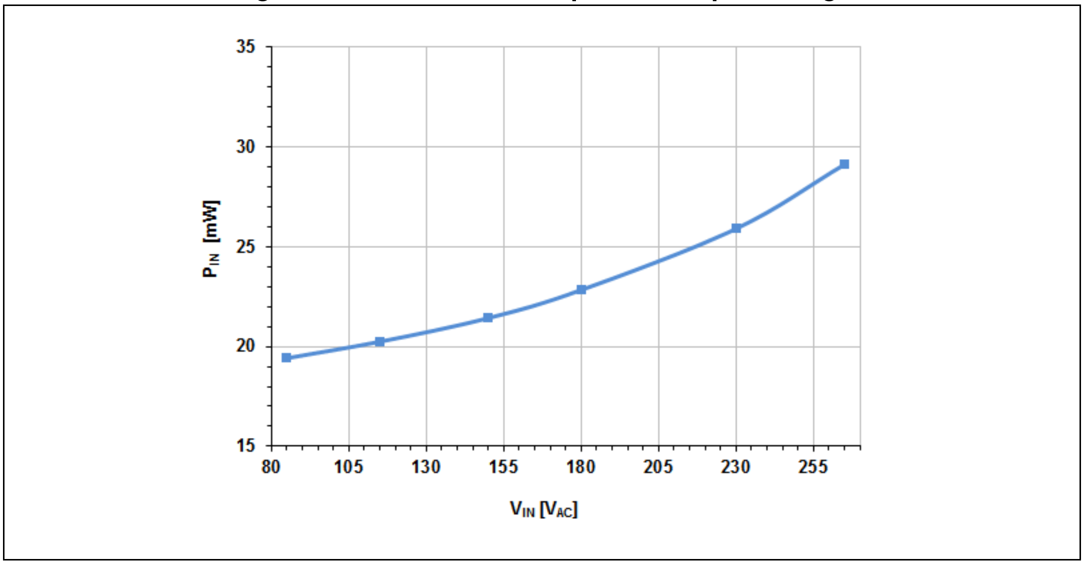
Figure 10. Efficiency vs. output current load



1.3 No load consumption

The input power of the converter has been measured in no load condition, in this situation the converter works in burst mode so that the average switching frequency is reduced.

Figure 11. No load consumption vs. input voltage



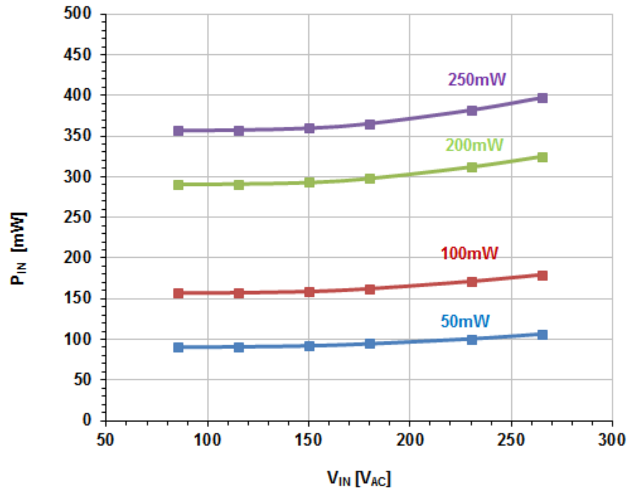
1.4 Light load consumption

Even if the EC CoC and DoE US EISA 2007 do not have other requirements regarding light load performance, in order to give quite complete information we report the input power of the evaluation board in light load conditions.

In particular, in order to be comply with EuP Lot 6, the EPS requires an efficiency higher than 50% when the output load is 250 mW.

The presented evaluation also meets this requirement.

Figure 12. Light load consumption at different output power



2 Typical board waveforms

Drain voltage and current waveforms in full load condition are reported for minimum and maximum input voltage in *Figure 13* and *Figure 14*, and for the two nominal input voltages in *Figure 15* and *Figure 16* respectively.

Figure 13. Drain current and voltage at full load at 85 V_{AC}

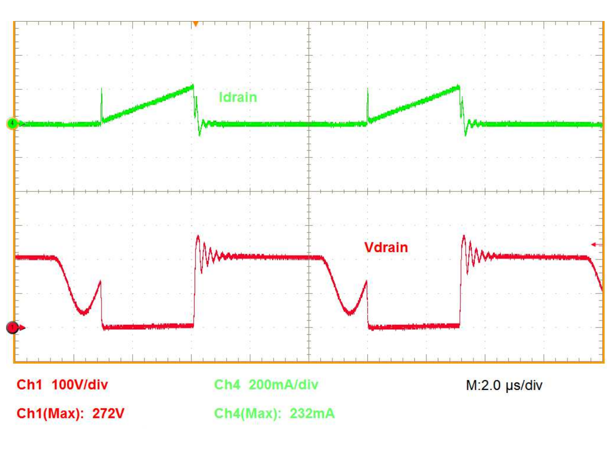


Figure 14. Drain current and voltage at full load at 265 V_{AC}

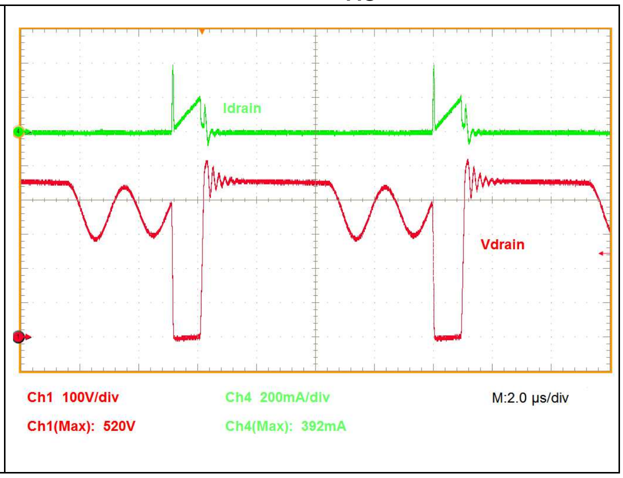


Figure 15. Drain current and voltage at full load at 115 V_{AC}

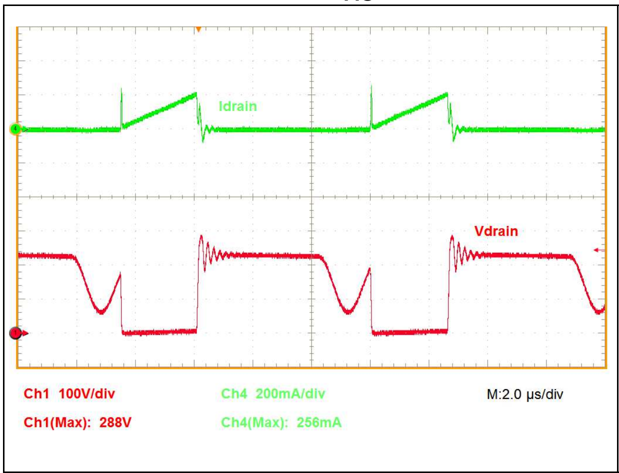
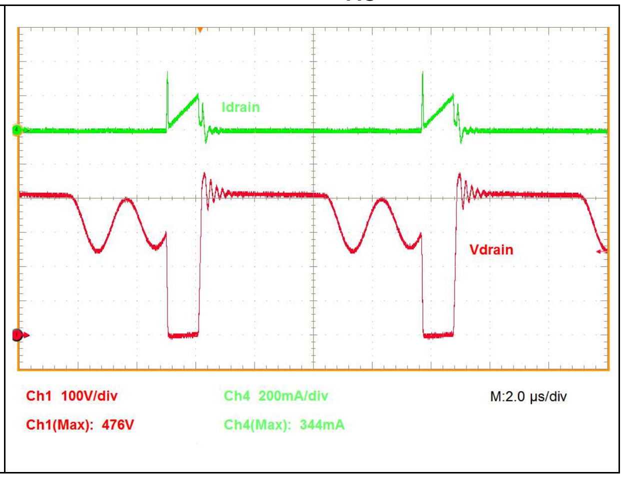


Figure 16. Drain current and voltage at full load at 230 V_{AC}



The output ripple at switching frequency was also measured. The board is provided with LC filter, to further reduce the ripple without reducing the overall output capacitor's ESR.

The voltage ripple across the output connector (V_{OUT}) and before the LC filter (V_{OUT_PRE}) was measured, in order to verify the effectiveness of the LC filter. The following two diagrams show voltage ripple at 115 V_{AC} (*Figure 17*) and at 230V_{AC} (*Figure 18*) at full load condition.

Figure 17. Output voltage ripple at full load at 115 V_{AC}

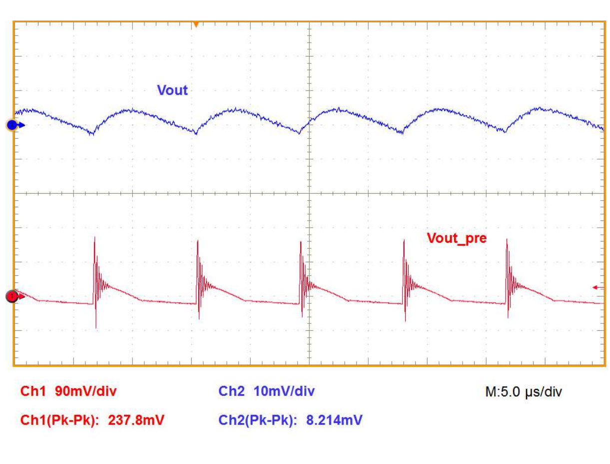
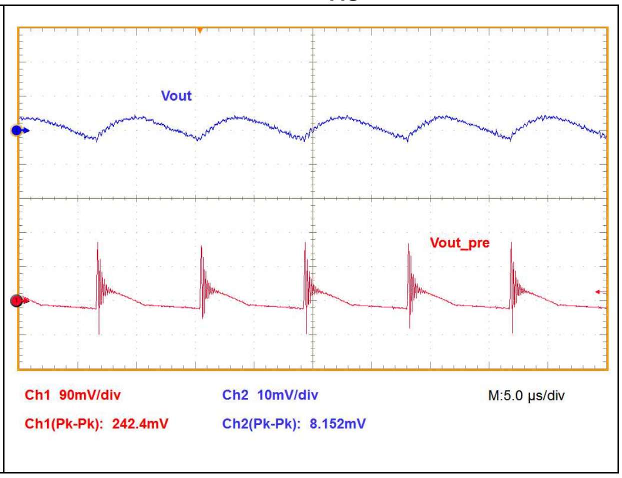


Figure 18. Output voltage ripple at full load at 230 V_{AC}



As the load is so low that the voltage at the COMP pin falls below the V_{COMPL} internal threshold (1.1 V typical), the VIPER06HN is disabled. At this point, the feedback reaction, to the energy delivery stop, will make the COMP pin voltage increase again and when it goes 40mV above the V_{COMPL} threshold the device restarts switching. This results in a controlled on/off operation which is referred to as “burst mode”. This mode of operation keeps low the frequency-related losses when the load is very light or disconnected, making it easier to comply with energy saving regulations.

The figures below show the output voltage ripple when the converter works in burst mode operation and supplied with 115 V_{AC} and with 230 V_{AC} respectively.

Figure 19. Output voltage ripple during burst mode operation at 115 V_{AC}

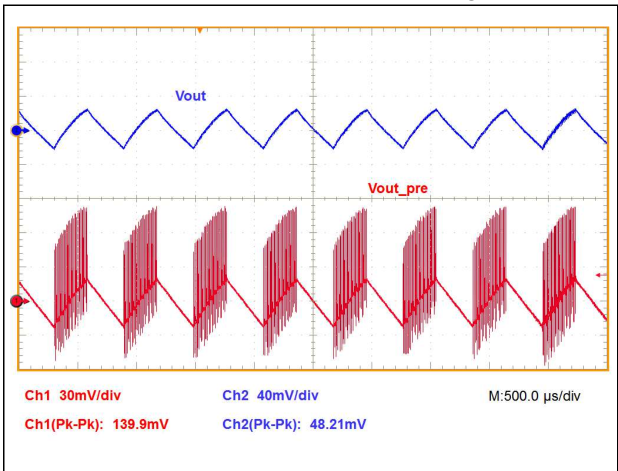
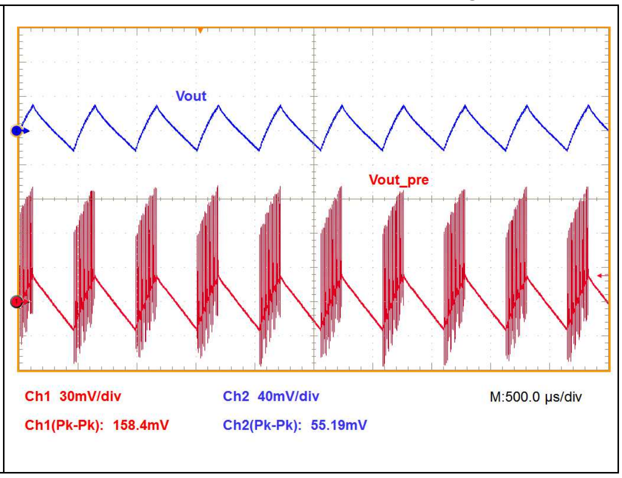


Figure 20. Output voltage ripple during burst mode operation at 230 V_{AC}



2.1 Dynamic step load regulation

In any power supply is important to measure the output voltage when the converter is submitted to dynamic load variations, in order to be sure that good stability is ensured and no overvoltage or undervoltage occurs.

The test has been performed, for both nominal input voltages, varying output load from 0 to 100% of nominal value.

In any tested condition, no abnormal oscillations were noticed on the output and over/under shoot were well within acceptable values.

Figure 21. Dynamic step load (0 to 100% output load) at 115 V_{AC}

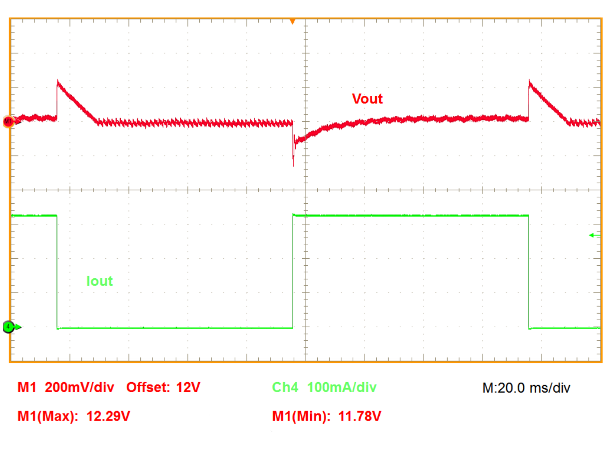
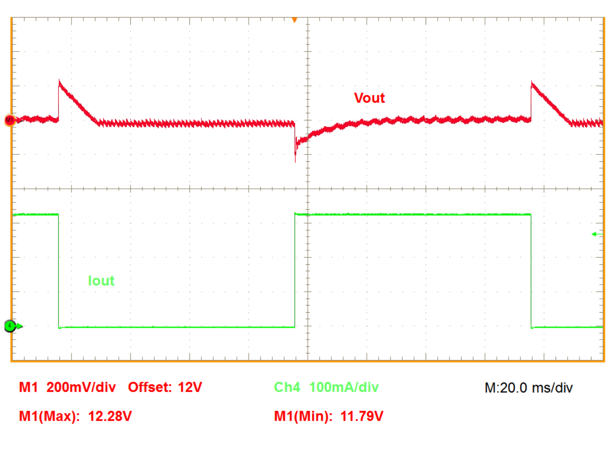


Figure 22. Dynamic step load (0 to 100% output load) at 230 V_{AC}



3 Soft-start

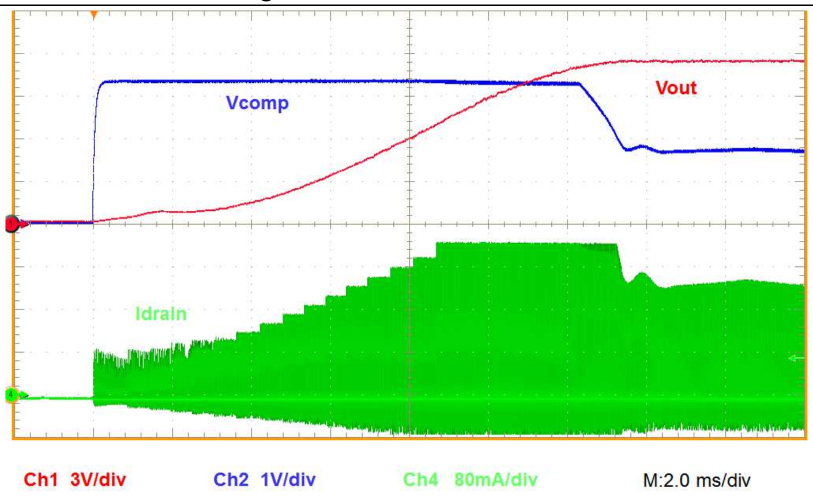
When the converter starts, the output capacitor is discharged and needs some time to reach the steady state condition. During this time, the power demand from the control loop is the maximum, while the reflected voltage is low. These two conditions could lead to a deep continuous operating mode of the converter.

Also, when the power MOSFET is switched on, it cannot be switched off immediately as the minimum on time (T_{ON_MIN}) has to be elapsed. Because of the deep continuous working mode of the converter, during this T_{ON_MIN}, an excess of drain current can over-stress the component of the converter as well as the device itself, the output diode, and the transformer. Transformer saturation is also possible under these conditions.

To avoid all the described negative effects, the VIPer06HN implements an internal soft-start feature. As the device starts to work, no matter the control loop request, the drain current is allowed to increase from zero to the maximum value gradually.

The drain current limit is increased in steps, and the values range from 0 to the fixed drain current limitation value (value that can be adjusted through an external resistor) is divided in 16 steps. Each step length is 64 switching cycles. The total length of the soft-start phase is about 8.5 ms. *Figure 23* shows the soft-start phase of the presented converter when it is operating at minimum line voltage and maximum load

Figure 23. Soft-start feature



4 Protection features

In order to increase end-product safety and reliability, VIPer06HN has some protection features: overload and short-circuit protection and open loop failure protection.

In the following sections these protections are tested and the results are presented.

4.1 Overload and short-circuit protection

In case of overload or output short-circuit (see *Figure 24*), the drain current reaches the I_{DLIM} value (or the one set by the user through the R_{LIM} resistor). Every cycle this condition is met and a counter is incremented; if it is maintained continuously for the time t_{OVL} (50 msec typical, internally fixed), the overload protection is tripped, the power section is turned off and the converter is disabled for a $t_{RESTART}$ time (1 sec typically). After this time has elapsed, the IC will resume switching and, if the short is still present, the protection will occur again (*Figure 25*). This ensures restart attempts of the converter with low repetition rate, so that it works safely with extremely low power throughput and avoiding the IC overheating in case of repeated overload events.

Moreover, every time the protection is tripped, the internal soft start-up function is invoked (*Figure 26*), in order to reduce the stress on the secondary diode.

After the short removal, the IC will resume working normally. If the short is removed during t_{SS} or t_{OVL}, i.e. before the protection tripping, the counter will be decremented on a cycle-by-cycle basis down to zero and the protection will not be tripped.

If the short-circuit is removed during $t_{RESTART}$, the IC will be waiting that $t_{RESTART}$ has elapsed before resume switching (*Figure 27*).

Figure 24. Overload protection: output short-circuit applied

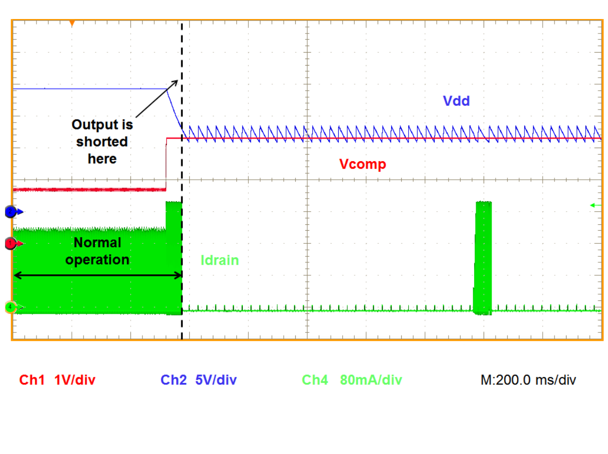


Figure 25. Overload protection: continuous output short-circuit

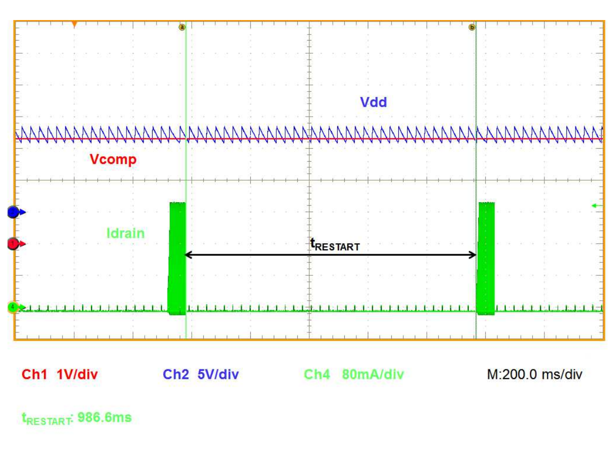


Figure 26. Overload protection: soft start and t_{OVL}

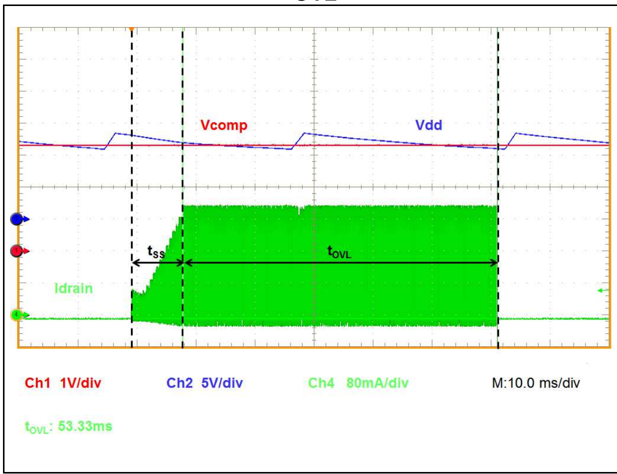
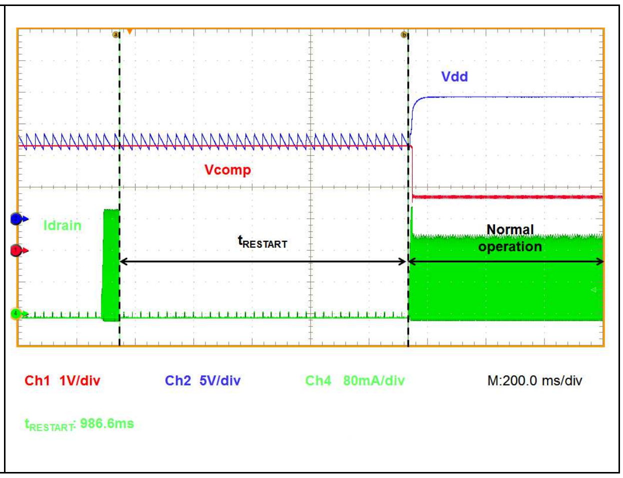


Figure 27. Overload protection: short-circuit removal



4.2 Open-loop failure protection

This kind of protection is useful when the device is supplied by an auxiliary winding and it's activated when feedback loop failure or auxiliary winding disconnection occurs.

If R9 is open or R10 is shorted, the VIPer06HN works at its drain current limitation. The output voltage, V_{OUT}, will increase as the auxiliary voltage V_{AUX} does, which is coupled with the output through the secondary-to-auxiliary turns ratio.

As the auxiliary voltage increases up to the internal V_{DD} active clamp, $V_{DDclamp}$ (23.5 V minimum), and the clamp current injected on the V_{DD} pin exceeds the latch threshold, I_{DDol} (4 mA minimum), a fault signal is internally generated and the device stop switching even if the t_{OVL} isn't elapsed yet (see *Figure 29*).

To verify the effectiveness of this protection the external clamp on V_{DD} pin has been removed.

Figure 28. Open loop failure protection: R9 open, $t_{RESTART}$

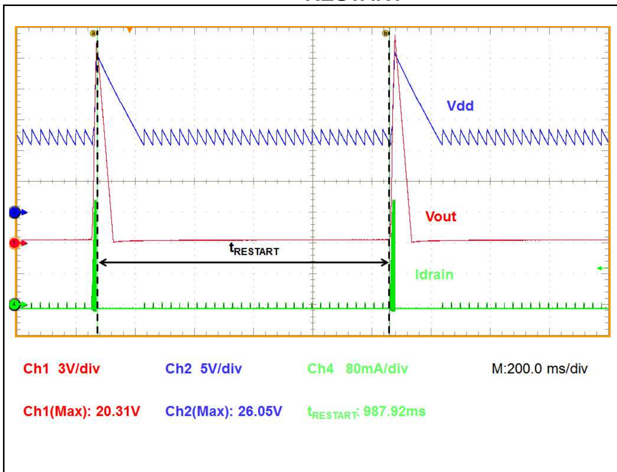
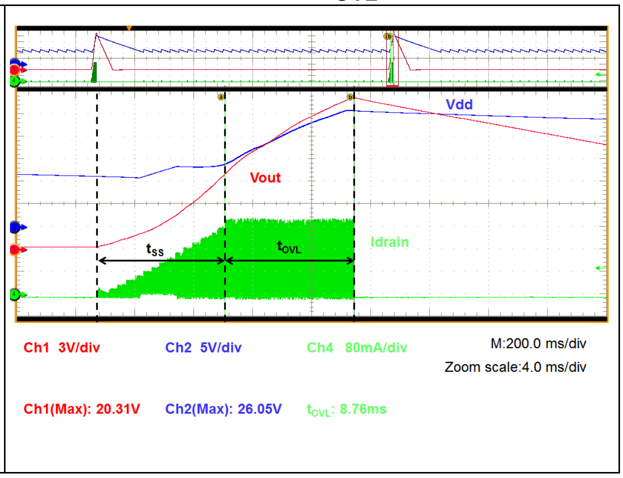


Figure 29. Open loop failure protection: R9 open, t_{OVL}



5 Conducted noise measurements

The VIPer06HN frequency jittering feature allows the spectrum to be spread over frequency bands, rather than being concentrated on single frequency value. Especially when measuring conducted emission with the average detection method, the level reduction can be several dBµV.

A pre-compliance test for the EN55022 (Class B) European normative was performed and peak measurements of the conducted noise emissions at full load and nominal mains voltages are shown in *Figure 30* and *Figure 31*. As seen in the diagrams, in all test conditions there is a good margin for the measurements with respect to the limits.

Figure 30. CE peak measurement at 115 V_{AC} full load

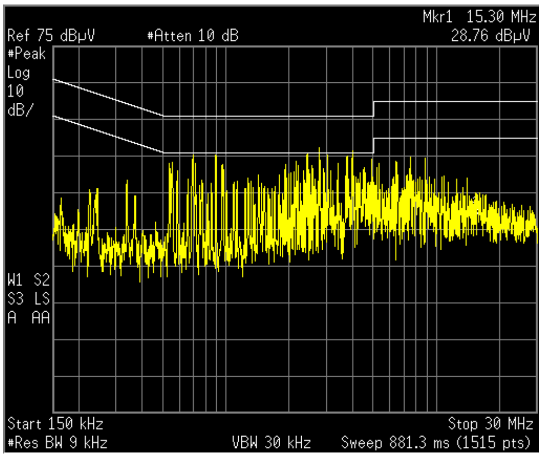
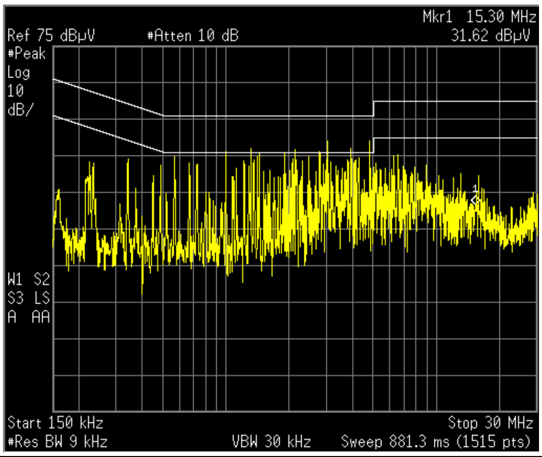


Figure 31. CE peak measurement at 230 V_{AC} full load



6 Thermal measurements

A thermal analysis of the board has been performed using an IR camera for the two nominal input voltages (115 V_{AC} and 230 V_{AC}) in full load condition. The results are shown in *Figure 32* to *Figure 35* and summarized in *Table 7*.

Figure 32. Thermal map at 115 V_{AC} full load. Top layer

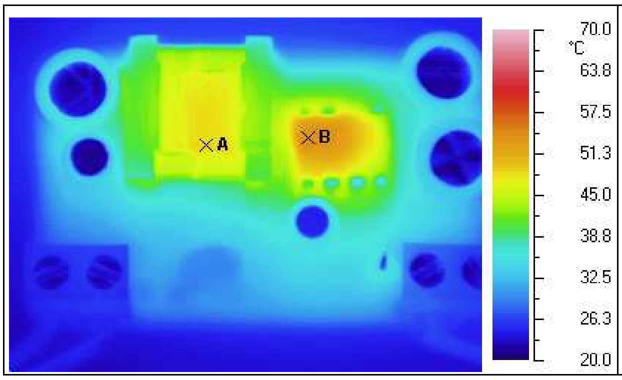


Figure 33. Thermal map at 115 V_{AC} full load. Bottom layer

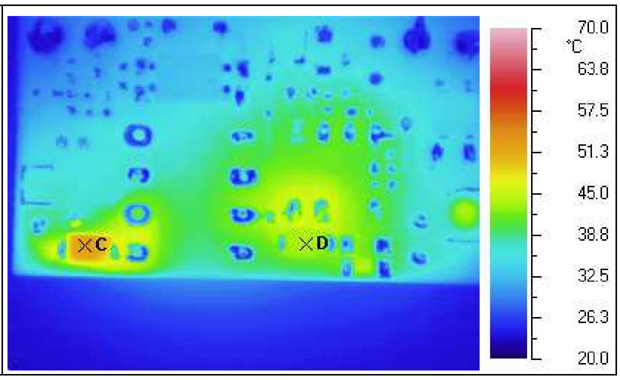


Figure 34. Thermal map at 230 V_{AC} full load. Top layer

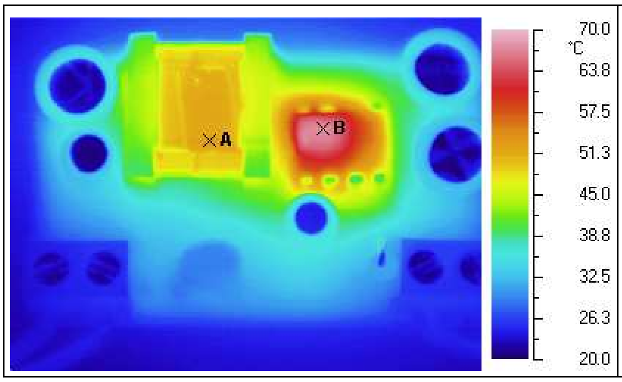


Figure 35. Thermal map at 230 V_{AC} full load. Bottom layer

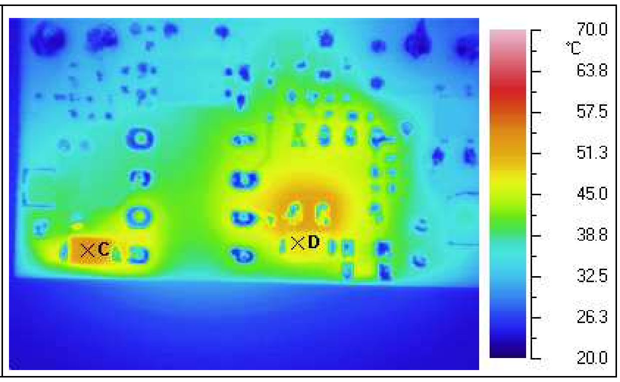


Table 7. Temperature of key components (T_{amb} = 25 °C, emissivity = 0.95 for all points)

Point	Temp (°C)		Reference
	115 V_{AC}	230 V_{AC}	
A	48.9	52.6	Transformer
B	54.0	67.4	VIPer06HN
C	52.6	53.6	Output diode
D	43.9	48.2	Snubber diode

7 Conclusions

In this document a flyback has been described and characterized. Special attention was paid to efficiency and low load performances and the bench results were good with very low input power in light load condition. The efficiency performance have been compared with requirements of the ECoC and DoE regulation programs for external AC/DC adapter with very good results, being the measured active mode efficiency always higher respect the minimum required.

Also the EMI emission are quite low, even if using a low cost input filter.

8 Evaluation tools and documentation

The VIPER06HN evaluation board order code is: STEVAL-ISA134V1.

Further information about this product is available in the VIPER06 datasheet at www.st.com.

9 Revision history

Table 8. Document revision history

Date	Revision	Changes
15-Oct-2013	1	Initial release.
16-May-2016	2	Added: new T1 part 7508110341 Rev 6A in *Table 2*.