AN4381
Application note

Current sharing in parallel diodes

Introduction

The use of diodes in parallel is commonly found in power electronic design. An important consideration for this practice is the current sharing between diodes due to the difference of electrical characteristics. This application note highlights the cause of the behavior of several diodes are connected in parallel. Some recommendations will be given to help the designer to produce a safe design. An electro-thermal model is described which simulates the current and junction temperature of each diode for given application conditions. This tool is illustrated using an example.

Contents

1 Current sharing

1.1 The basics

Consider a simple example of two 5 A, 600 V ultrafast diodes in a TO-220 package (STTH5R06) connected in parallel and mounted on a common heat sink. *Figure 1* shows the forward voltage V_F of two STTH5R06 diodes (D_1 and D_2) versus forward current I_F at different junction temperatures. Diodes D_1 and D_2 have a difference of forward voltage equal to 550 mV at $T_{j1} = T_{j2} = 25$ °C. This reference value will be expressed as:

ΔV_F(5A, 25 °C) = 550 mV.

This system satisfies the equations:

Equation 1

$I_T(t) = I_{F1}(t) + I_{F2}(t)$

Equation 2

$V_{F1}(t,I_{F1},T_{j1}) = V_{F2}(t,I_{F2},T_{j2})$

In this first example $I_T(t)$ = 10 A = cst. For diode D_1, having a lower forward voltage characteristic than D_2, I_{F1} will be higher than I_{F2}. When $T_{j1} = T_{j2} = 25$ °C (for example when the converter starts up) we get:

Equation 3

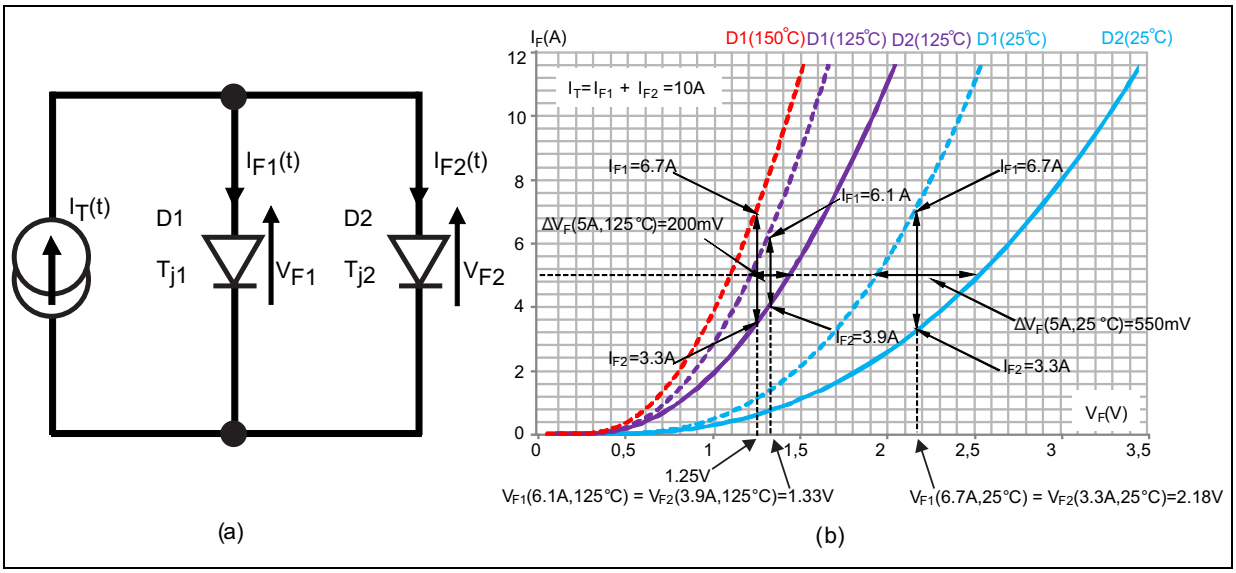
I_{F1} = 6.7 A, I_{F2} = 3.3 A (I_T = 10 A)

and

Equation 4

V_{F1}(6.7 A, 25 °C) = V_{F2}(3.3 A, 25 °C) = 2.18 V

Figure 1. Two 5 A, 600 V ultrafast diodes (STTH5R06) connected in parallel



1.2 Thermal effects

Two thermal effects need to be considered. The first one due to the negative temperature coefficient of V_F is very well known. The second one, due to dependency of α_{VF} on V_F is practically unknown.

1.2.1 Thermal effects due to the negative temperature coefficient of V_F

Assume that in thermal steady state equilibrium the junction temperature of these two diodes is equal to 125 °C. From *Figure 1.b* we can deduce:

Equation 5

I_{F1} = 6.1 A, I_{F2} = 3.9 A (I_T = 10 A)

and

Equation 6

V_{F1}(6.1 A, 125 °C) = V_{F2}(3.9 A, 125 °C) = 1.33 V

For D_1, having higher forward current than D_2, T_{j1} will be higher than T_{j2}. Assuming now T_{j1} = 150 °C and T_{j2} = 125 °C we get:

Equation 7

I_{F1} = 6.7 A, I_{F2} = 3.3 A (I_T = 10 A)

and

Equation 8

V_{F1}(6.7 A, 150 °C) = V_{F2}(3.3 A, 125 °C) = 1.25 V

The negative temperature coefficient of the forward voltage drop ($\alpha_{VF} < 0$) increases the current unbalance between each diode. It is practically true for every technology of diode excepted for silicon carbide diodes for which $\alpha_{VF} > 0$ in the operating area. The negative impact of this well-known thermal effect is in practice limited by the fact that all the diodes are generally mounted on a common heat sink (see *Figure 12*). The case temperature being approximately the same for each diode, the difference of junction temperature Δ_{Tj} can be determined by:

Equation 9

$$\Delta_{Tj} = R_{TH(j\text{-}c)}\Delta_P$$

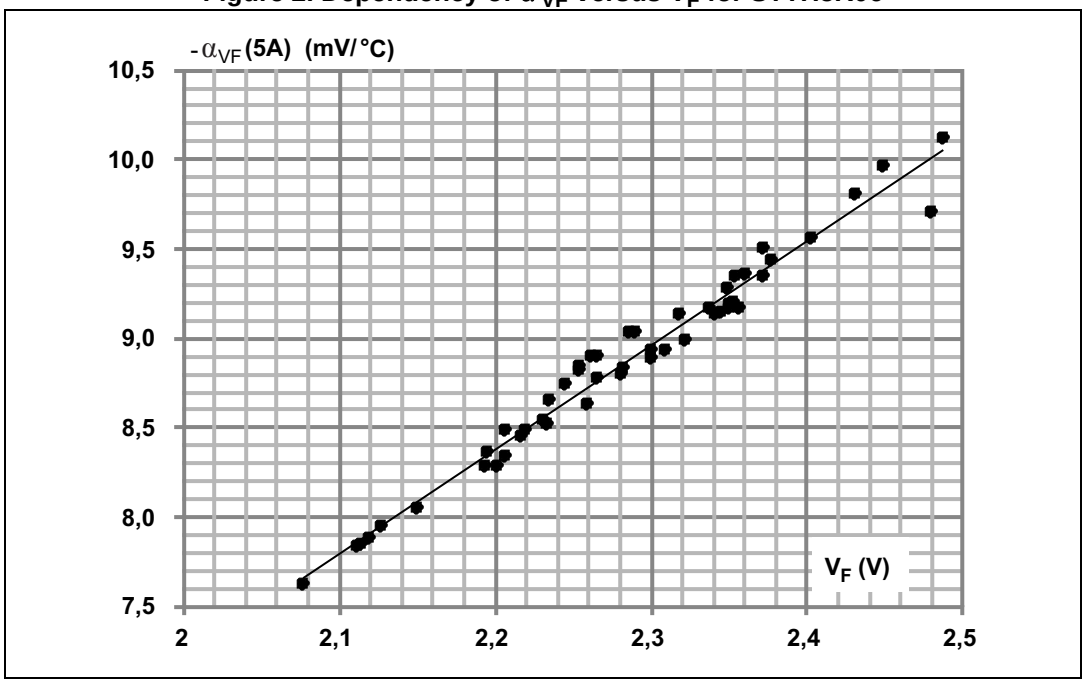
Where $R_{TH(j\text{-}c)}$ is the junction to case thermal resistance and Δ_P the difference of power losses between each diode. Generally Δ_{Tj} is lower than 25 °C, limiting the current unbalance due to the temperature.

1.2.2 Thermal effects due to the dependency of α_{VF} versus V_F

The second thermal effect is linked to the dependency of temperature coefficient α_{VF} versus forward voltage drop V_F. *Figure 1.b* shows that diode D_1, having a lower voltage drop than D_2, has at the same time, a lower absolute value of α_{VF}. This law is confirmed by *Figure 2* giving the relationship between α_{VF} and V_F for different STTH5R06. Each point corresponds to one diode. α_{VF} is measured for a forward current of 5 A.

This second thermal effect is favorable for current equilibrium and partially counteracts the first thermal effect.

Figure 2. Dependency of α_{VF} versus V_F for STTH5R06



1.3 Worst case configuration

To produce a safe design it is important to consider the worst case situation represented in *Figure 3*. D_1 has the lower V_F and diodes D_2 to D_n have the higher V_F. We will define by $\Delta V_{Fmax}(I_0, 25\ °C)$ the maximum forward voltage dispersion of all the diodes at 25 °C and at current rating I_0, for example I_0 = 5 A for an STTH5R06. This configuration is defined by: diode D_1 with $V_{F1}(I_0, 25\ °C)$ and diodes D_2 to D_n with:

Equation 10

$$V_{F2}(I_0, 25\ °C) = V_{Fn}(I_0, 25\ °C) = V_{F1}(I_0, 25\ °C) + \Delta V_{Fmax}(I_0, 25\ °C)$$

At the thermal steady state equilibrium we now get:

$$I_T(t) = I_{F1}(t) + I_{F2}(t) + \ldots + I_{Fn}(t)$$

$$I_{F2}(t) = \ldots = I_{Fn}(t)$$

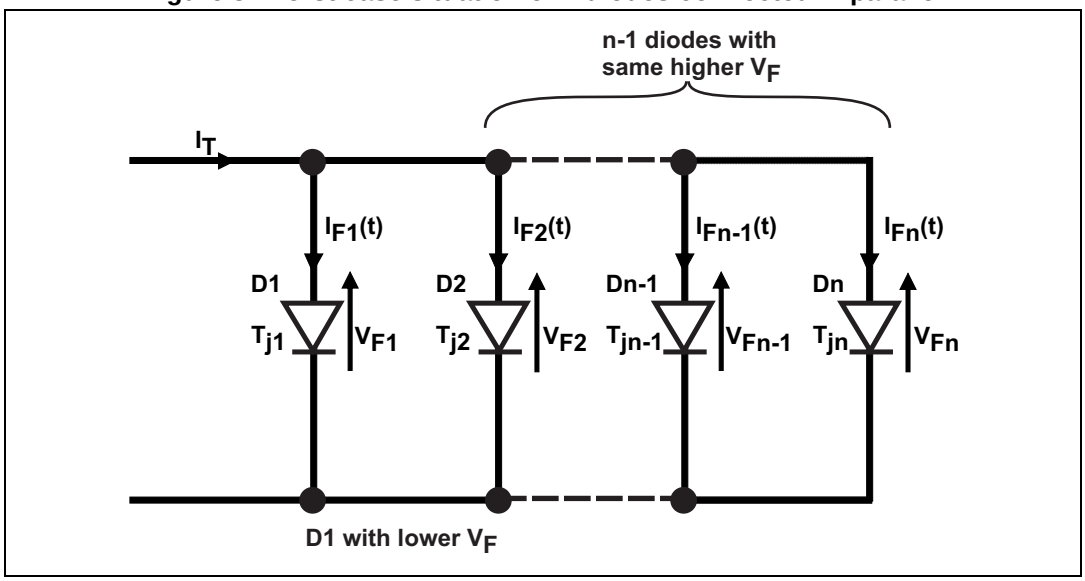
$$T_{j1} > T_{j2} \ldots T_{jn}$$

Equation 11

$V_{F1}(I_{F1},T_{j1}) = V_{F2}(I_{F2},T_{j2}) = \ldots = V_{Fn}(I_{Fn},T_{jn})$

$T_{j2} = \ldots = T_{jn}$

Figure 3. Worst case situation of n diodes connected in parallel



To ensure a safe design, **the more stressed diode (D_1) has to work within its specified limits** in terms of junction temperature, rms current, and transient surge current capability. The goal of the simulation tool presented in *Section 2* is to address this question.

1.4 V_F and Q_{RR} of diodes connected in parallel

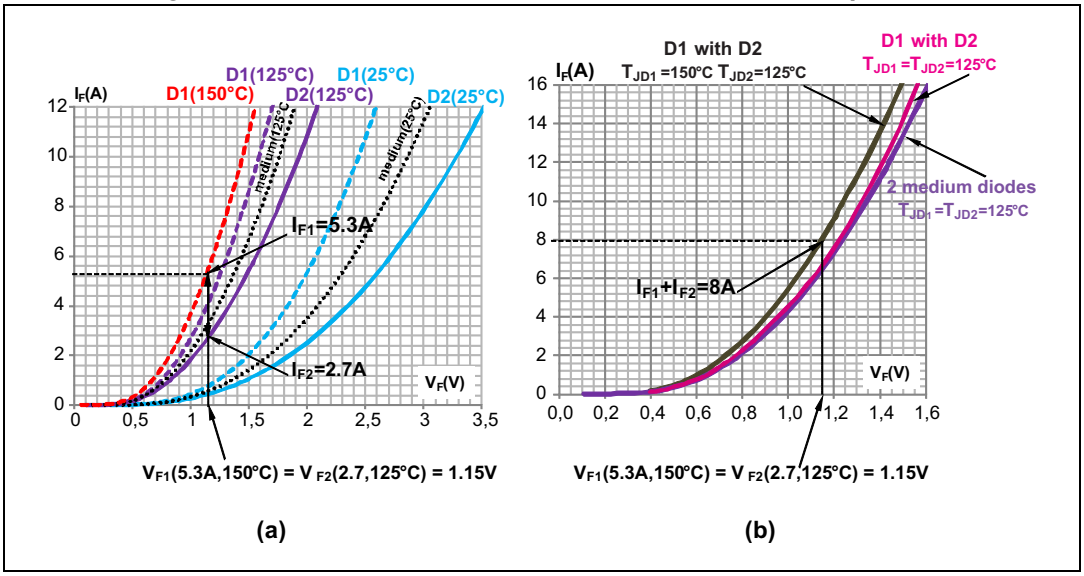
We first compare the forward voltage characteristic of the two diodes D_1 and D_2 connected in parallel with the case of two medium diodes also connected in parallel. *Figure 4.a* shows again the forward characteristic of D_1 and D_2 with the corresponding medium characteristic. *Figure 4.b* shows V_F of D_1 connected with D_2 when $T_{j1} = T_{j2} = 125$ °C and when $T_{j1} = 150$ °C and $T_{j2} = 125$ °C ($\Delta_{Tj} = 25$ °C corresponding to the worst case with a common heat sink) which can be compared with the two medium diodes at $T_{j1} = T_{j2} = 125$ °C. The curves from *Figure 4.b* can be deduced from the curves of *Figure 4.a*. For example, V_F at 8 A of D_1 connected with D_2 when and $T_{j1} = 150$ °C and $T_{j2} = 125$ °C is defined by:

Equation 12

$V_{F1}(5.3\text{ A}, 150\text{ °C}) = V_{F2}(2.7\text{ A}, 125\text{ °C}) = 1.15\text{ V}$

In this particular case, the resulting forward characteristic of the 2 medium diodes is approximately the same as for D1 connected with D2 at $T_{j1} = T_{j2} = 125$ °C but is higher when $T_{j1} = 150$ °C and $T_{j2} = 125$ °C.

Figure 4. Worst case situation of n diodes connected in parallel



We now use, the same approach to compare reverse recovery charges: Q_{RR} at I_T = 10 A and V_R = 400 V, versus dI_F/dt for different configurations. Consider the method employed with an example. In the case of diode D_1 (T_{j1} = 150 °C) in parallel with D_2 (T_{j2} = 125 °C) for I_T = 10 A we get I_{F1} = 6.7 A and I_{F2} = 3.3 A. Since $I_T = I_{F1} + I_{F2}$, we have:

Equation 13

$dI_T/dt = dI_{F1}/dt + dI_{F2}/dt$

If dI_T/dt = 300 A/µs, we get dI_{F1}/dt = 200 A/µs and dI_{F2}/dt = 100 A/µs. *Figure 5*.b shows the switching oscillograms of D_1 at I_{F1} = 6.7 A, dI_{F1}/dt = 200 A/µs, T_{j1} = 150 °C and that of D2 at I_{F2} = 3.3 A, dI_{F2}/dt = 100 A/µs, T_{j2} = 125 °C. In these conditions accurate measurements give:

Equation 14

$Q_{RR(D1)}$(6.7 A, 200 A/µs, 150 °C) = 125 nC, $Q_{RR(D2)}$(3.3 A, 100 A/µs, 125 °C) = 59 nC

So Q_{RR} of D_1 in parallel with D_2 is:

Equation 15

$Q_{RR(D1 + D2)} = Q_{RR(D1)} + Q_{RR(D2)}$ = 184 nC

Assume now two diodes D_1 are connected together. Obviously the current will be well balanced so we have: I_{F1} = 5 A, dI_{F1}/dt = 150 A/µs, T_{j1} = 125 °C. Measurements give:

Equation 16

$Q_{RR(D1)}$(5 A, 150 A/µs, 125 °C) = 80 nC

Equation 17

So $Q_{RR(2\ D1)} = 2 \bullet Q_{RR(D1)}$(5 A, 150 A/µs, 125 °C) = 160 nC

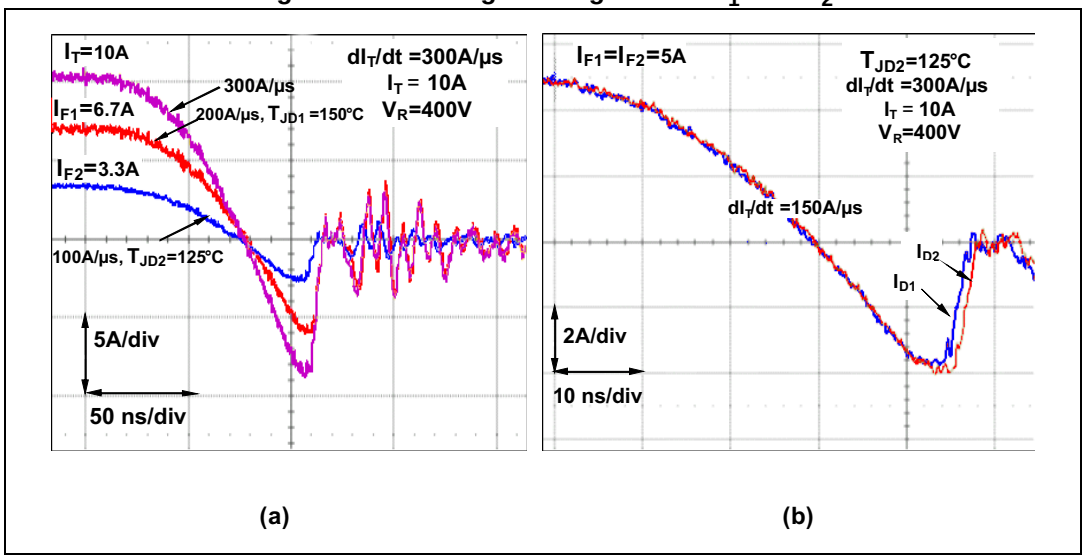
In the same way we obtain:

Equation 18

So $Q_{RR(2\ D2)} = 2 \bullet Q_{RR(D2)}(5\ A, 150\ A/\mu s, 125\ °C) = 150\ nC$

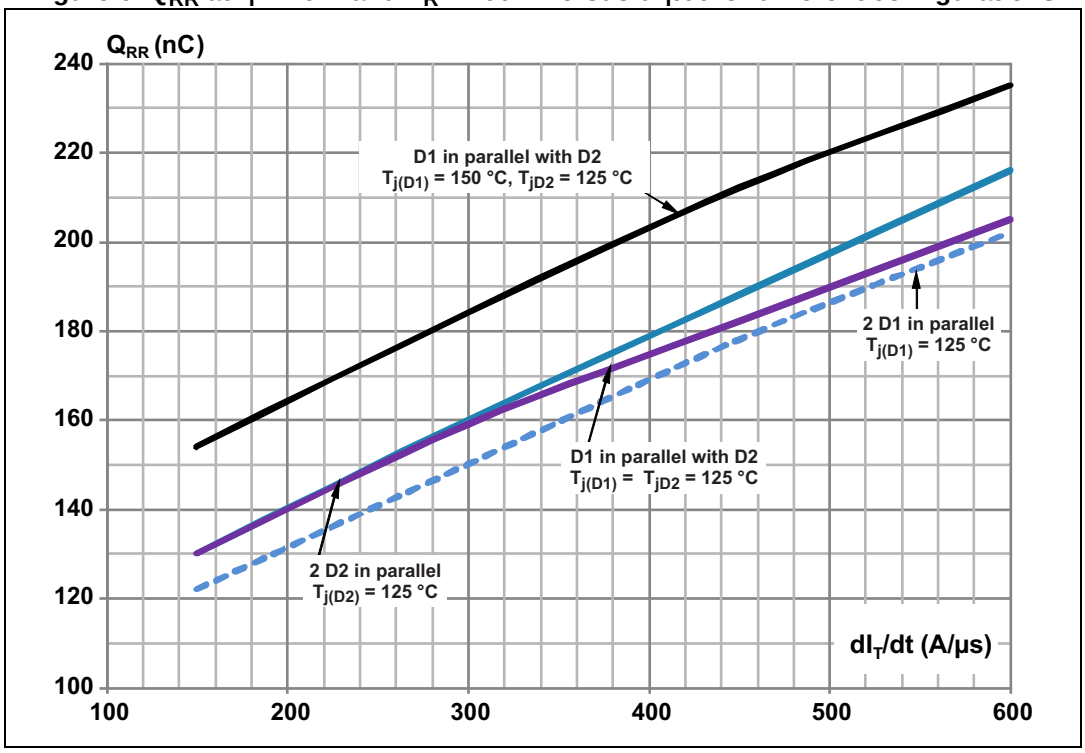
It is interesting to note that while D_1 has a lower forward voltage drop than D_2, the reverse recovery charges are higher for D_1.

Figure 5. Switching oscillograms of D_1 and D_2



Using this method for different dI_T/dt we get the diagrams shown in *Figure 6*.

Figure 6. Q_{RR} at I_T = 10 A and V_R = 400 V versus dI_T/dt for different configurations



To summarize, the V_F and Q_{RR} comparison between two STTH5R06 in parallel having a dispersion of ΔV_F(5A, 25 °C) = 550 mV with the ideal case constituted by medium diodes indicates that these characteristics are close when junction temperatures are identical. When the junction temperature difference between D_1 and D_2 increases, V_F tends to decrease slightly and Q_{RR} tends to increase slightly. We cannot make a general conclusion from a particular case, but this example shows the general trend and illustrates a method which can be employed for others configurations.

1.5 Considerations of maximum dispersion: ΔV_{Fmax} (I_0, 25 °C)

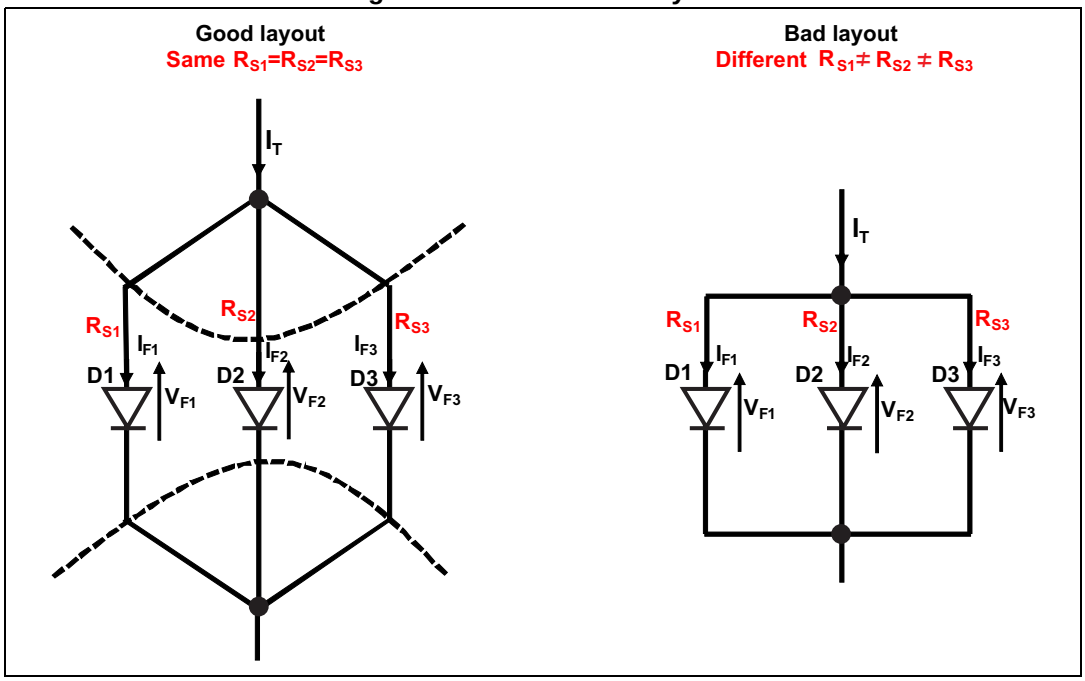
The above considerations show the key impact of the maximum dispersion ΔV_{Fmax}(I_0, 25 °C) on the current imbalance. For a designer it is not always easy to know this value. However, the following information can be given:

- ΔV_{Fmax}(I_0, 25 °C) increases with the voltage rating (V_{RRM}). That means the forward voltage dispersion of 600 V ultrafast diodes will be higher than the dispersion of 200 V ultrafast diodes. The same consideration can be applied between 200 V ultrafast diodes and 100 V Schottky diodes and between 100 V Schottky diodes versus 45 V Schottky diodes.
- For ultrafast diodes having the same V_{RRM} ΔV_{Fmax}(I_0, 25 °C) is higher for faster diode families. For example, If we consider 600 V ST ultrafast diodes, R family (Rapid) has higher dispersion than the L family (Low V_F).
- Practically all ST common cathode diodes in the same package can be connected in parallel without any precaution. Since these diodes are on the same die, ΔV_{Fmax}(I_0, 25 °C) is very low.
- Low voltage Schottky diodes (V_{RRM} < 60 V) can also be connected in parallel without precaution.
- Sometimes, designers fix by establishing a maximum ΔV_{Fmax}(I_0, 25 °C) for all diodes connected in parallel to ensure a safe design. A good value can be: ΔV_{Fmax}(I_0, 25 °C) = 40 mV. With this value, the current will be equitably shared between each diode and the thermal effects will become negligible.

1.6 Layout recommendation

The basic recommendation is to use a symmetrical layout as illustrated in *Figure 7*.

Figure 7. Good and bad layouts



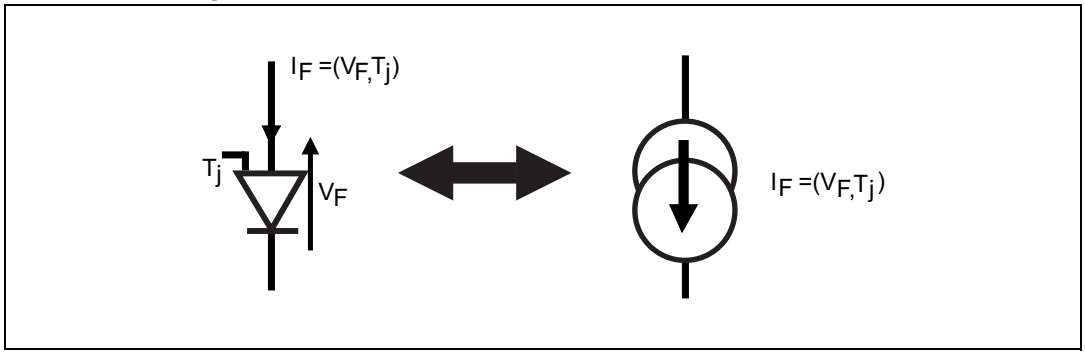
If the layout is not symmetrical, the connection resistors will increase the current imbalance. In contrast, a symmetrical layout will balance the current in each diode. To have a real impact, the values of these resistors have to be of the same order as the resistance of the diodes. Adding the small resistance in series with each diode can be a good way to balance the current. On the other hand this solution will generate more power losses and will decrease the efficiency of the converter. We can observe in *Figure 4*.b that the resistance of the diode R_D increases with lower forward current I_F. So paralleling will be easier for lower current. The dependency of R_D versus I_F can also be considered as a compensation effect

2 Electro-thermal model of diodes in parallel

2.1 DC Forward characteristic model

The first step is to construct a forward characteristic model of the diode (see *Figure 8*).

Figure 8. Model of the forward characteristic of the diode



This is defined by the following current generator I_F depending on T_j and V_F

Equation 19

$$I_F(V_F,T_j) = a_0(T_j) + a_1(T_j)V_F + a_2(T_j)V_F^2 + a_3(T_j)V_F^3 + a_4(T_j)V_F^4 + a_5(T_j)\sqrt{V_F}$$

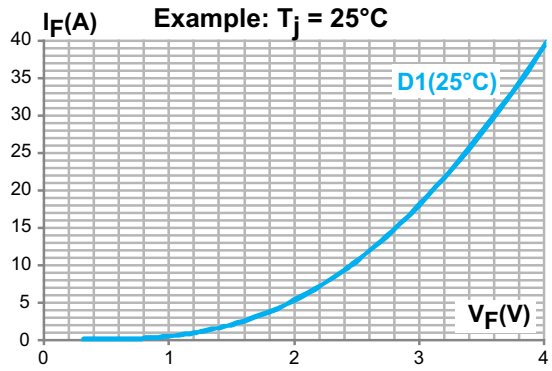
Each coefficient $a_i(T_j)$ is of the form:

Equation 20

$$a_0(T_j) = a_{00} + a_{01}T_j + a_{02}T_j^2 + a_{03}T_j^3$$

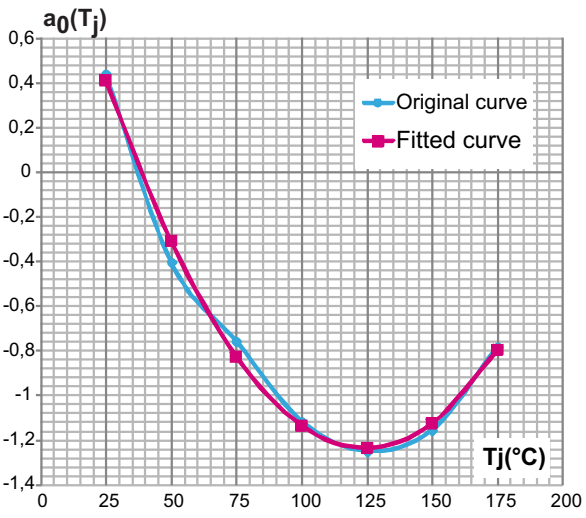
Figure 9 and *Figure 10* give respectively a_i(25 °C) and a_{0j} coefficients for a STTH5R06.

Figure 9. ai(25 °C) coefficients of STTH5R06



a0(25°C)	0.443113633610841
a1(25°C)	1.823450442549035
a2(25°C)	-1.596962213365812
a3(25°C)	1.497001749151565
a4(25°C)	-0.139628758047056
a5(25°C)	-1.59534418112371

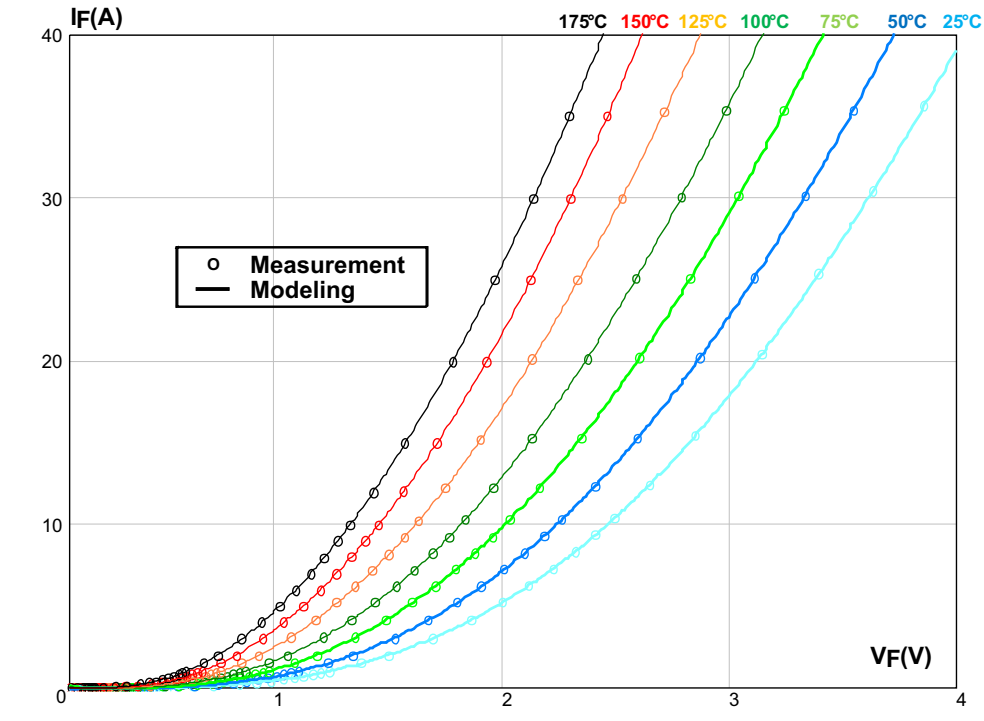
Figure 10. a_{0i} coefficients of STTH5R06



a_{00}	1.330314150823049
a_{01}	-0.040753310751888
a_{02}	0.000157525320538
a_{03}	0.000000033311313

Figure 11 illustrates the precision of this model.

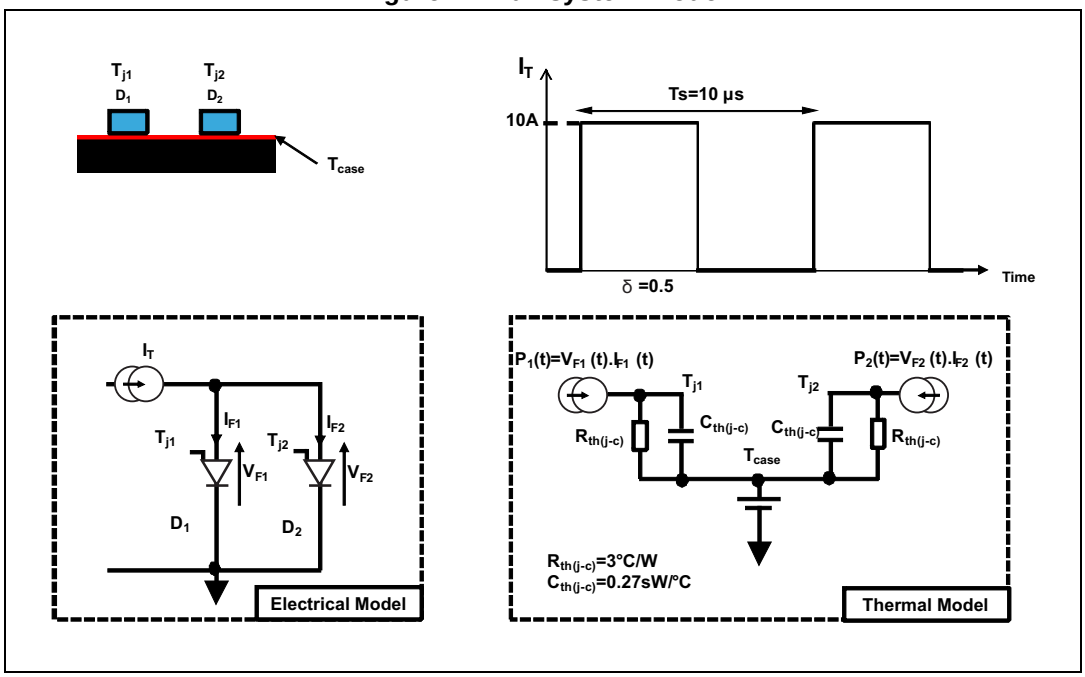
Figure 11. Forward characteristic comparison between model and measurement



2.2 Full system model

Having now obtained a good model of the forward characteristic of the diode, we can construct the model of the total system. Without loss of generality, we consider the simple example represented in *Figure 12*. It consists of two STT5R06 diodes mounted on the same heat sink. The total current $I_T(t)$ is rectangular with a switching period T_S = 10 µs, a duty cycle δ = 0.5 and a peak current I_P = 10 A. The full model of this system is also shown in *Figure 12*. We can distinguish the electrical model defined in the previous paragraph from the thermal model. In this example the case temperature of the heat sink is constant and is equal to T_{case} = 100 °C. It is important to understand that these two models will work together. V_{F1} and V_{F2} depend on T_{j1} and T_{j2} which depend on the power losses in the diodes (P_1 and P_2). Thus T_{j1} and T_{j2} depend upon V_{F1} and V_{F2}

Figure 12. Full system model



In this application note we consider only conduction losses. This hypothesis is justified not only for Schottky and silicon carbide diodes but also for the major applications using ultrafast diodes. Effectively, major switching losses, due to reverse recovery charges, are generally dissipated in the companion switch (MOSFET or IGBT) and do not affect the current imbalance of the diodes. For applications for which switching losses generated in the diodes are not negligible versus conduction losses, it is possible to complete the model. This more complex model is not covered in this application note.

2.3 Simulation results

The simulations were performed with STTH5R06 having different values of ΔV_{Fmax}(5 A, 25 °C). *Figure 13* shows the forward voltage characteristic of seven STTH5R06 diodes at T_j = 25 °C and gives ΔV_{Fmax}(5 A, 25 °C) versus the reference diode D_{ref} having the highest V_F.

Figure 13. STTH5R06 with different ΔV_{Fmax}(5 A, 25 °C)

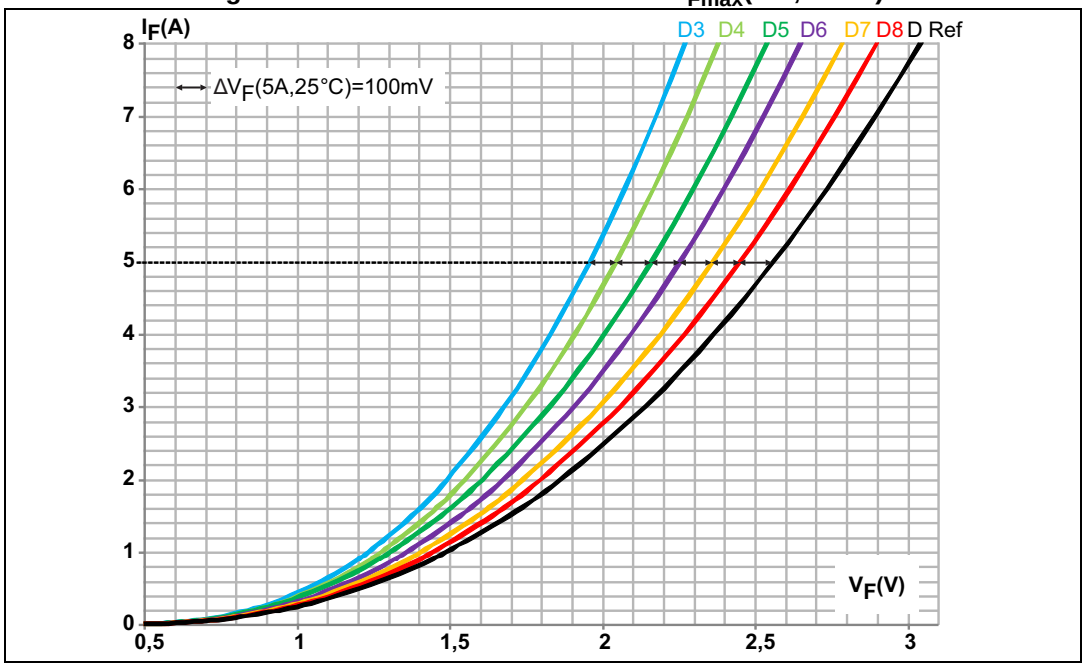
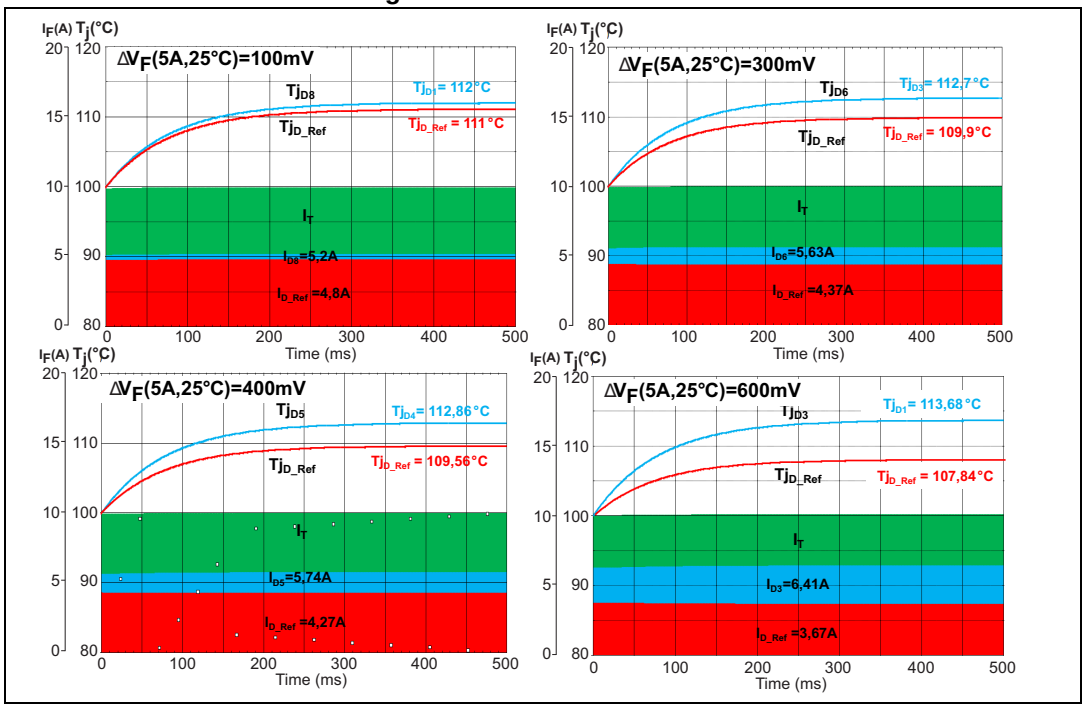


Figure 14 represents the variation current and junction temperature versus time of each diode for respectively ΔV_{Fmax}(5 A, 25 °C) equal to 100 mV, 300 mV, 400 mV and 600 mV. The current imbalance and the difference of junction temperature between D_{ref} and the other diode increase with ΔV_{Fmax}(5 A, 25 °C). Even for ΔV_{Fmax}(5 A, 25 °C) = 600 mV, the difference of junction temperature is low (< 6 °C), in this example the thermal effect of negative $\alpha_{VF} < 0$ is weak. Up to ΔV_{Fmax}(5 A, 25 °C) = 300 mV the current imbalance is low (I_{Dref} = 4.37 A, I_6 = 5.63 A).

Figure 14. Simulation results



2.4 Comments about simulation

This simulation can be easily extrapolated to more complex configurations integrating n diodes, more accurate thermal models (for example Cauer type circuit thermal model) including models of the heat sink, layout resistors, more complex $I_T(t)$ current wave forms. If designers are only interested in knowing steady state current and junction temperature it is possible to reduce the calorific capacity (C_{TH}) to gain simulation time. This tool can be used to analyze both current imbalance and difference of temperature for transient surge currents.

3 Conclusions

This application note shows the impact of forward voltage dispersion is generally more critical than thermal effects for the current imbalance problem. To perform a safe design it is important to be sure the most stressed diode works within its specified limits in the worst case situation. The simulation tool described allows estimation of the junction temperature and current of each diode for transient and steady state phases.

4 Revision history

Table 1. Document revision history

Date	Revision	Changes
30-Jul-2014	1	Initial release.