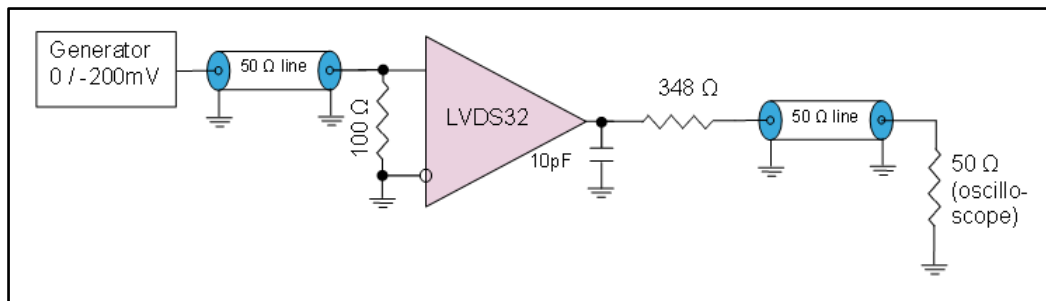


Fail-safe feature of the RHFLVDS32A and RHFLVDSR2D2

Jean-Louis Bernet

The fail-safe feature guarantees a known CMOS output state for each receiver embedded in the RHFLVDS32A and RHFLVDSR2D2 devices (see [Figure 1](#)). This CMOS state is a stable, electrical, high-level output, when differential inputs are shorted (0 V differential) or left opened. Entering and exiting fail-safe mode gives the timing values t_{D1} and t_{D2} respectively. These timing values are typically 1 μ s (see device datasheets).

Figure 1: Fail-safe test implementation



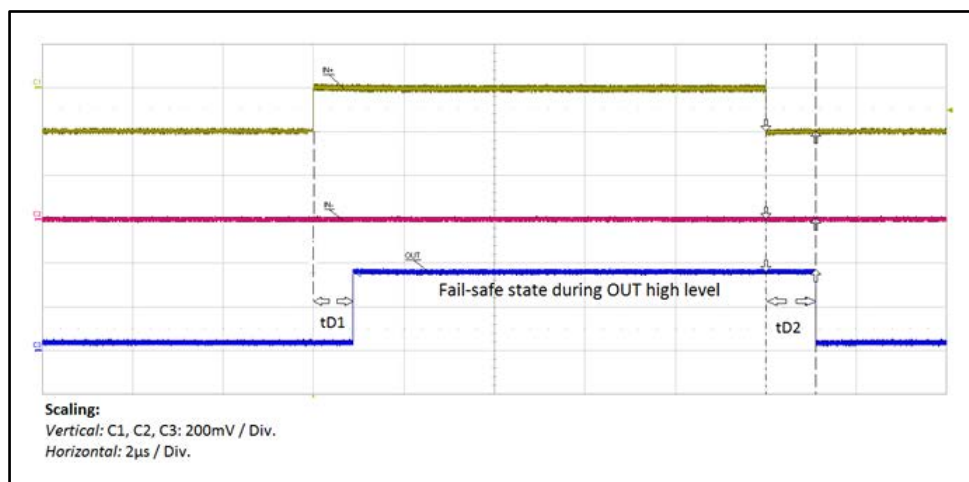
One way to measure t_{D1} and t_{D2} (see [Figure 2](#)) is as follows:

- toggle the input IN+ between -200 mV and 0 V (oscilloscope_channel 1)
- set input IN- to stable 0 V (oscilloscope_channel 2)

The fail-safe state occurs during high state on the output (oscilloscope_channel 3).

Note: the output level is attenuated, due to measurement constraints (~1/8)

Figure 2: Fail-safe delays of t_{D1} and t_{D2}



Revision history

Table 1: Document revision history

Date	Revision	Changes
28-Feb-2014	1	Initial release

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