AN4544
Application note

IGBT datasheet tutorial

Introduction

This application note is intended to provide detailed explanations about parameters and diagrams included in the datasheet of trench-gate field stop IGBTs offered in discrete packages such as: TO-247, TO-220, D^{2}PAK, etc. This document helps the user to better understand the datasheet parameters and characteristics by explaining the interaction with the influence of conditions as temperature or gate voltage.

Thanks to this application note the designer can also use the information included in datasheet according to his needs.

Datasheet values, for dynamic characterization tests, refer to a specific testing setup with its individual characteristics. Therefore, these values can vary according to the user's application.

Most of the included diagrams, tables and explanations are related to the STGW40V60DF datasheet. Concerning the latest version of datasheet for this product, please refer to our website.

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1 General IGBT overview

The insulated-gate bipolar transistors (IGBTs) combine a MOS gate with high-current and low-saturation-voltage capability of bipolar transistors as illustrated in *Figure 1*, and they are the right choice for high-current and high voltage applications.

IGBT and MOSFET operation is very similar. A positive voltage, applied from the emitter to gate terminals, produces a flow of electrons toward the gate terminal in the body region. If the gate to emitter voltage is equal or above the threshold voltage, electrons flow toward the gate to form a conductive channel across the body region, allowing current to flow from the collector-to-emitter. (It allows electrons to flow from the emitter to the collector). This flow of electrons attracts holes, or positive ions, from the p-type substrate to the drift region toward the emitter. The balance in trade-offs among switching speed, conduction loss, and ruggedness is finely tuned and the latest technology, especially for high voltage (> 400 V) devices, improves speed and conduction so that IGBTs are overrun on the high frequency application scenario, which was dominated by Power MOSFET. *Figure 2* shows a series of simplified equivalent circuits for an IGBT.

Figure 1. Cross section of a trench field-stop IGBT

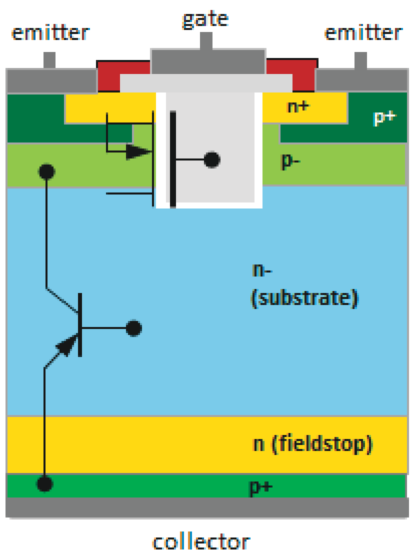
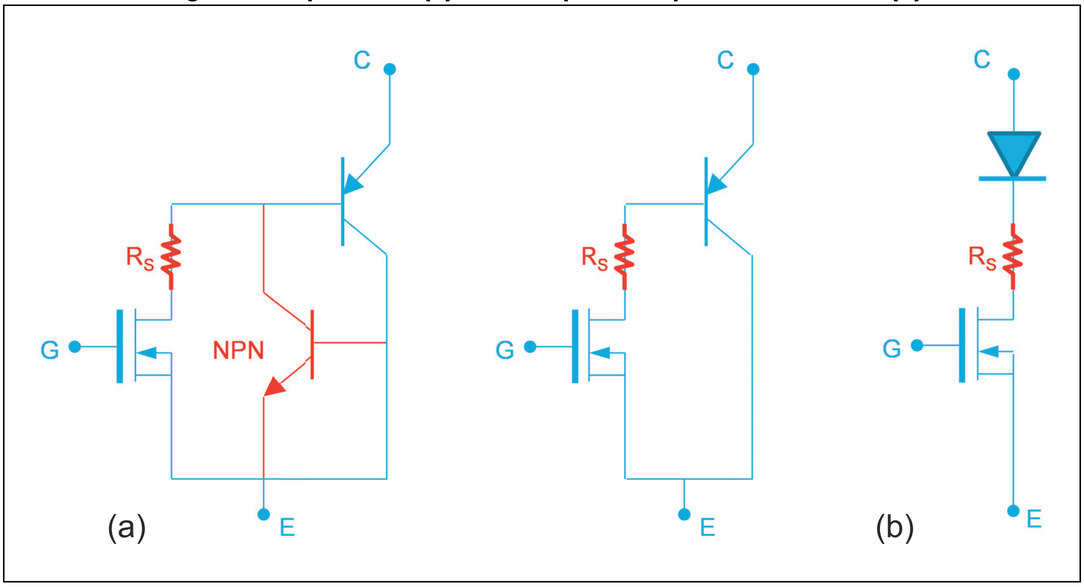


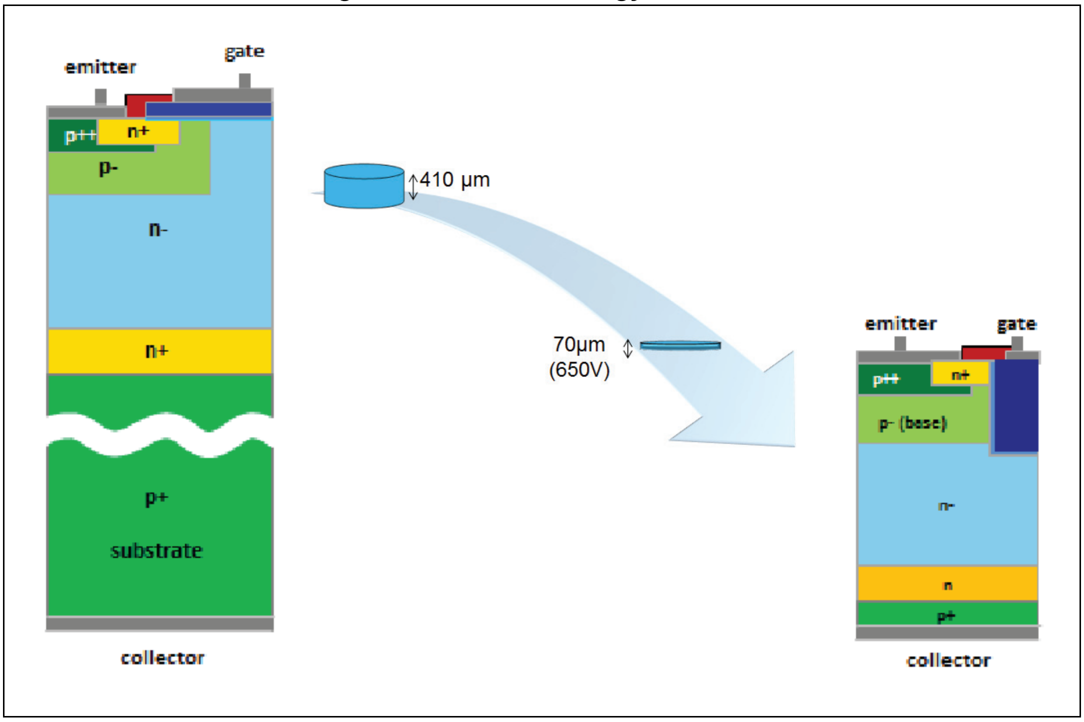
Figure 2. Equivalent (a) and simplified equivalent circuits (b)



1.1 IGBT technology evolution

The trench field-stop technology includes several benefits if compared to the planar PT (punch through). Implanted back-emitter and field-stop for a better control of the dynamic behavior together with the introduction of the trench structure offer an improved performance like lower conduction and switching loss, much higher robustness and a significant R_{TH} reduction due to very thin die.

Figure 3. IGBT technology evolution



2 Datasheet explanation

2.1 Datasheet status

The status of the product development can be:

- Target data
- Preliminary data
- Final data

Target data describes the design goal of a future product to be developed. Values from target datasheet are useful just for the initial calculations and approximations. The information and values of a target datasheet cannot be guaranteed for the final product. The dimensioning of an inverter should be only based on a preliminary or final datasheet.

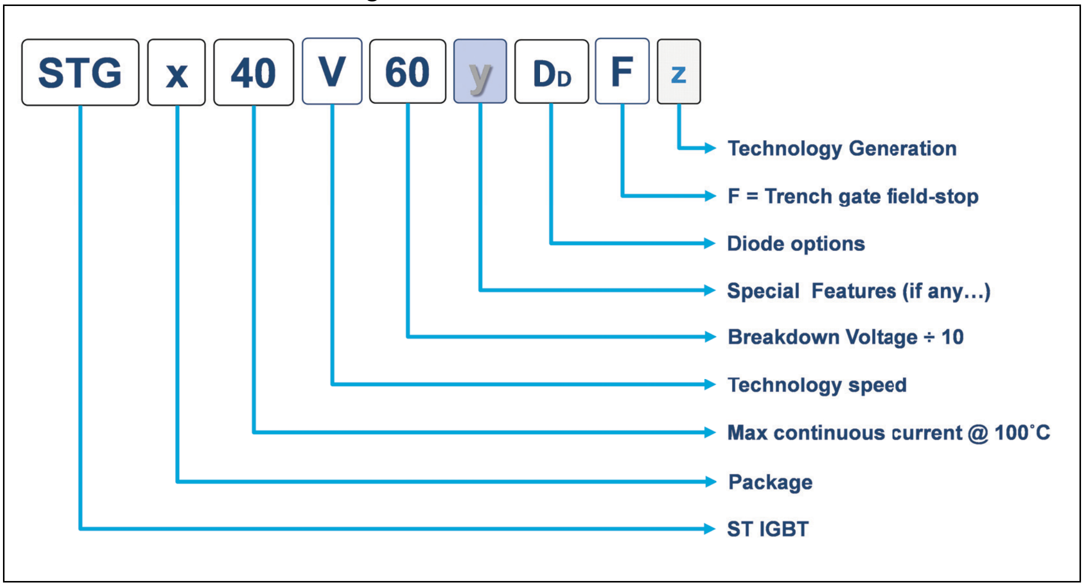
During the development phase, parts are labeled with the suffix "ES" and they are supplied with a special document. This kind of samples can be used for preliminary and functional tests during the early stages of a product development phase. Samples marked as ES are not liable to product change notification (PCN).

Preliminary data is based on components whose manufacture is close to production. The difference between a preliminary and a final datasheet is that certain values are still missing, for example the maximum values. These missing values in the preliminary datasheet are marked TBD to be defined. Reliability and lifetime are partly, but not finally approved.

Final data is based on final components. Making is based on productive tooling for mass production. Reliability and lifetime are approved and released. The final datasheet is completed with values which were missing in the preliminary datasheet. In case of major changes for products in production, a PCN has to be issued.

2.2 IGBT nomenclature meaning

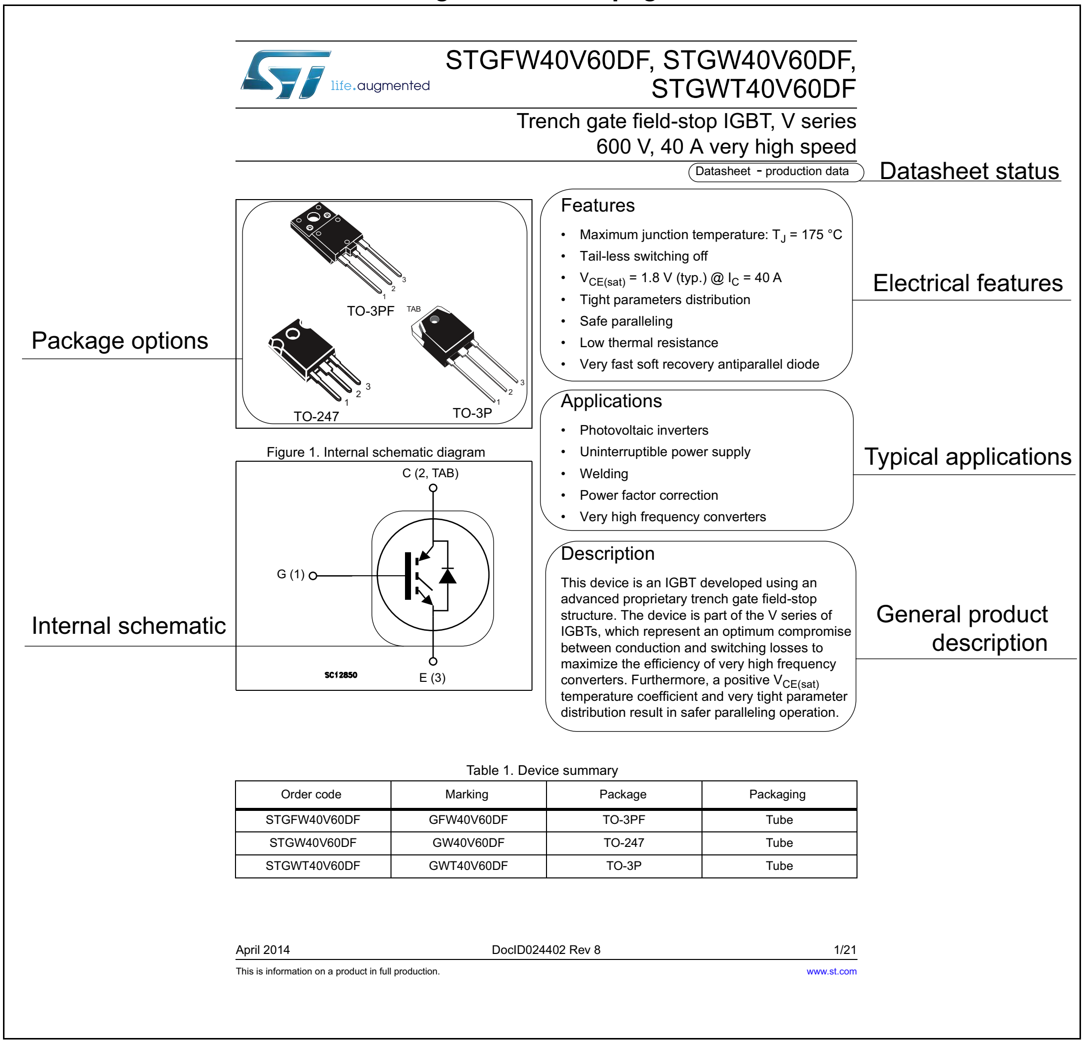
Figure 4. Nomenclature scheme



2.3 First page of datasheet

This section explains the electrical properties of IGBT products. Otherwise specified, values apply to a temperature of 25 °C.

Figure 5. Cover page



life.augmented

STGFW40V60DF, STGW40V60DF, STGWT40V60DF

Trench gate field-stop IGBT, V series 600 V, 40 A very high speed

Datasheet - production data

Datasheet status

Package options

TO-3PF TAB

TO-247

TO-3P

Features

- Maximum junction temperature: T_J = 175 °C
- Tail-less switching off
- $V_{CE(sat)}$ = 1.8 V (typ.) @ I_C = 40 A
- Tight parameters distribution
- Safe paralleling
- Low thermal resistance
- Very fast soft recovery antiparallel diode

Electrical features

Applications

- Photovoltaic inverters
- Uninterruptible power supply
- Welding
- Power factor correction
- Very high frequency converters

Typical applications

Figure 1. Internal schematic diagram

C (2, TAB)

G (1)

E (3)

SC12850

Internal schematic

Description

This device is an IGBT developed using an advanced proprietary trench gate field-stop structure. The device is part of the V series of IGBTs, which represent an optimum compromise between conduction and switching losses to maximize the efficiency of very high frequency converters. Furthermore, a positive $V_{CE(sat)}$ temperature coefficient and very tight parameter distribution result in safer paralleling operation.

General product description

Table 1. Device summary

Order code	Marking	Package	Packaging
STGFW40V60DF	GFW40V60DF	TO-3PF	Tube
STGW40V60DF	GW40V60DF	TO-247	Tube
STGWT40V60DF	GWT40V60DF	TO-3P	Tube

April 2014 DocID024402 Rev 8 1/21

This is information on a product in full production. www.st.com

2.4 Absolute maximum ratings

They are the maximum values of current, voltage, temperature, power dissipation, recommended by manufacturers for their product type. To achieve reliable and long term operation of a device, the device has to operate within these specified ratings.

2.4.1 Collector-to-emitter voltage (V_{CES})

The continuous collector-to-emitter voltage (V_{CES}) is the maximum voltage that the collector-to-emitter junction can support at temperature of 25 °C. Gate and emitter terminals are shorted together.

Table 1. V_{CES} maximum ratings showed in absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CES}	Collector-emitter voltage (V_{GE} = 0)	600	V

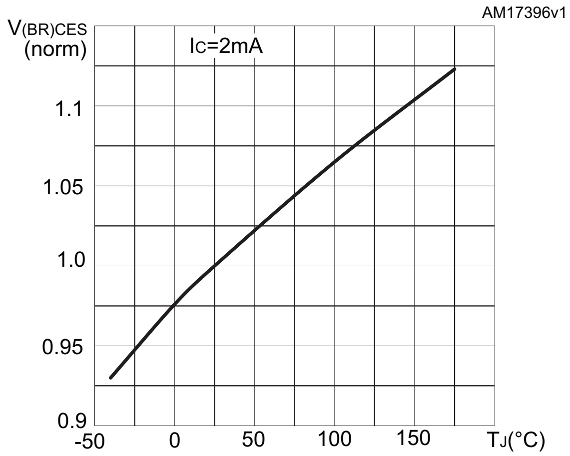
This value, in case of low temperature, decreases by a factor of approximately:

Equation 1

$$BV_{CES} = 0.1\frac{\%}{°C}$$

with a typical trend showed in the following figure.

Figure 6. Normalized $V_{(BR)CES}$ vs. junction (case) temperature



2.4.2 Continuous collector current rating (I_C)

Nominal continuous collector current (I_C) can flow through the device while the case temperature (T_C) is held at the specified level, with the junction temperature rising to its maximum ratings due to the dissipated power of the device.

Table 2. Nominal continuous I_C in absolute maximum ratings

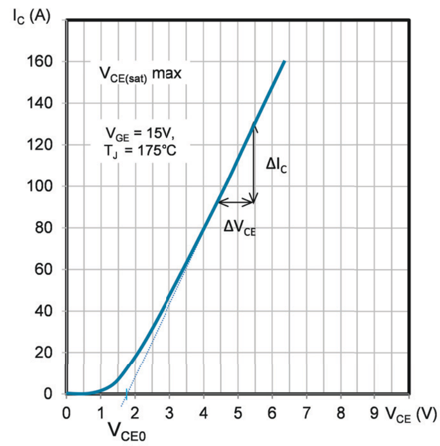
Symbol	Parameter	Value	Unit
I_C	Continuous collector current at T_C = 25 °C	80	A
I_C	Continuous collector current at T_C = 100 °C	40	A

The formula for the calculated collector current (I_C) is the following:

Equation 2

$$P_{TOT} = \frac{T_{Jmax} - T_C}{R_{th(J-C)}} = V_{CE} \cdot I_C$$

Figure 7. How to calculate the continuous collector current using the output characteristic curve



Equation 3

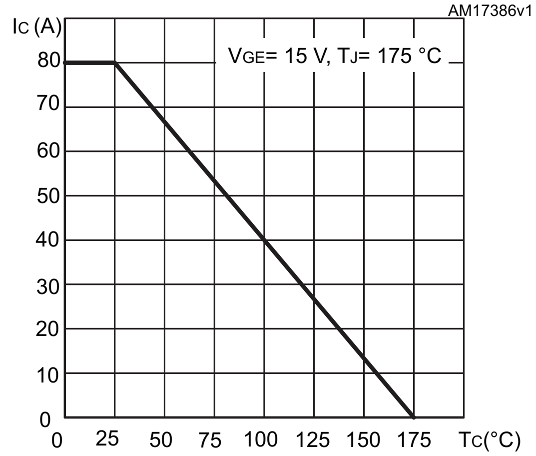
$$R_{CEO} = \frac{\Delta V_{CE}}{\Delta I_C}$$

Equation 4

$$I_C = \frac{-V_{CEO} + \sqrt{V^2{}_{CEO} + 4 \bullet R_{CEO} \bullet \left(\frac{T_{Jmax} - T_C}{R_{TH(JC)}}\right)}}{2 \bullet R_{CEO}}$$

Furthermore, power dissipation and continuous collector current are both reported in the datasheet as function of the case temperature (T_C).

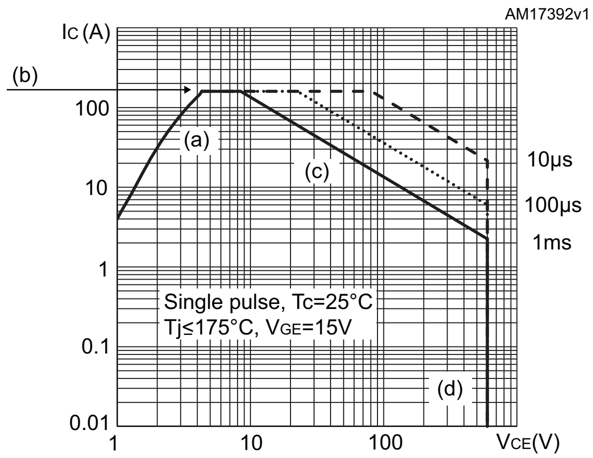
Figure 8. Collector current vs. case temperature



2.4.3 Forward biased safe operating area (FBSOA)

This shows the collector current I_C as a function of the collector-emitter voltage V_{CE} at different pulses.

Figure 9. Forward bias safe operating area



a) This area is limited by the conduction loss $V_{CE(sat)}$ at maximum junction temperature.

b) The top limit is related to the maximum pulsed collector current.

c) This area depends on the pulse length of the applied power pulse, the thermal impedance changes and leads to different maximum power losses. For a given pulse length, the thermal impedance Z_{thJC} has to be determined by looking at the specific diagram.

d) The maximum breakdown voltage $V_{(BR)CES}$ is determined by the technology and limits the diagram on the right-hand side.

2.4.4 Peak of collector current ratings (I_{CP})

These ratings indicate how much pulsed current the device can handle, which is significantly higher than the rated continuous current.

Table 3. Pulsed I_C details in absolute maximum ratings

Symbol	Parameter	Value	Unit
I_{CP}(1)	Pulsed collector current	160	A

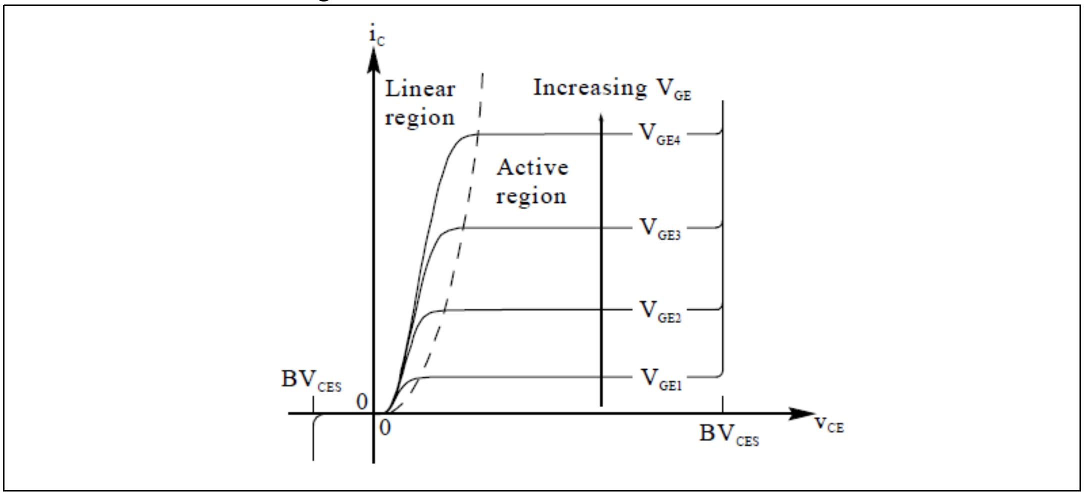
1. Pulse width limited by maximum junction temperature.

The purposes of I_{CP} ratings are:

- Keeping IGBT operating conditions in the “linear” region of its transfer characteristic (see *Figure 10*). There is a maximum collector current for a respective gate-emitter voltage that the IGBT conducts. If the operating point at a given gate-emitter voltage goes above the linear region, the result is a significant collector-emitter voltage rise and consequent rise of conduction loss and possible device destruction.

- Preventing burnout or latchup. Although the pulse width is theoretically too short to overheat the die, exceeding the I_{CP} ratings can cause burnout or latchup.
- Preventing the die overheats. The note *1* implies that I_{CP} is based on a thermal limitation depending on the pulse width. This is always true for two reasons:
  - There is some margin in the I_{CP} ratings
  - Whatever the failure mechanism is, overheating is the observed end result
- Avoid excessive current through the bond wires

Figure 10. IGBT transfer characteristics



Regarding I_{CP} thermal limitation, the temperature rise depends on the pulse width, time among pulses, heat dissipation, and $V_{CE(sat)}$ as well as the shape and magnitude of the current pulse. Remaining within I_{CP} limits does not assure that the maximum junction temperature is not exceeded.

2.4.5 Gate-to-emitter voltage (V_{GE})

Table 4. V_{GE} information showed in maximum ratings

Symbol	Parameter	Value	Unit
V_{GE}	Gate-emitter voltage	±20	V

V_{GE} stands for the allowable range voltage between the gate and emitter terminals. Exceeding V_{GE} range may result in permanent device degradation due to oxide breakdown and dielectric rupture. Remaining within these ratings assures application reliability. This value, with reasonable guard band, is 100% tested and warranted.

2.4.6 Maximum power dissipation (P_{TOT})

Table 5. IGBT total power showed in absolute maximum ratings

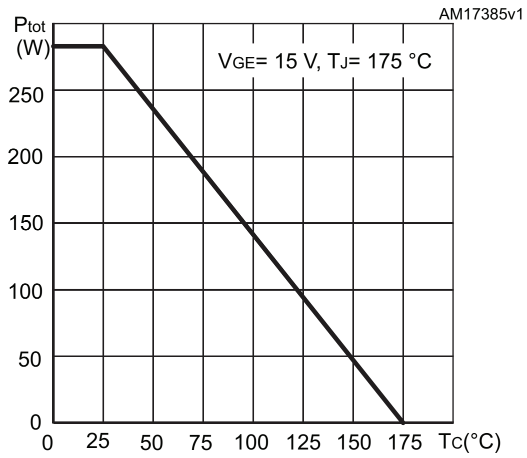
Symbol	Parameter	Value	Unit
P_{TOT}	Total dissipation at T_C = 25 °C	283	W

Equation 5

$$P_{TOT} = \frac{T_{Jmax} - T_C}{R_{th(J-C)}}$$

The maximum power dissipation is related to a given case temperature (T_C), the maximum junction temperature (T_J) and the thermal resistance ($R_{TH(J-C)}$).

Figure 11. Power dissipation vs. case temperature



2.4.7 Operating junction and storage temperature range (T_J) and (T_{STG})

Table 6. Ratings for storage and junction temperature in the table of absolute maximum ratings

Symbol	Parameter	Value	Unit
T_{STG}	Storage temperature range	- 55 to 150	°C
T_J	Operating junction temperature	- 55 to 175	°C

These limits are set to assure an acceptable lifetime of the product. Operating out of the temperature limits could damage the device affecting its lifetime. A reduction of operating junction temperature, every 10 °C doubles the device lifetime.

2.4.8 Thermal resistance (R_{th})

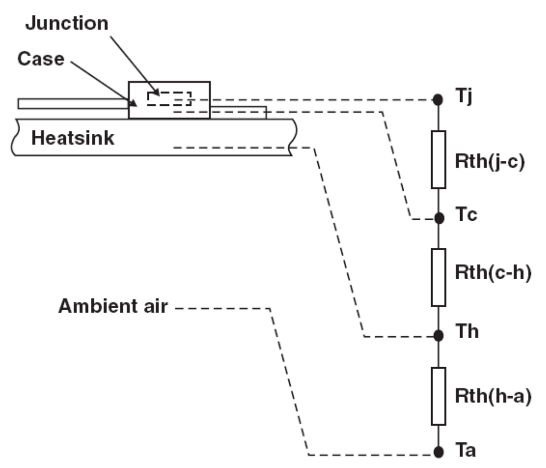
Thermal resistance relates to the heat conduction properties of the device (temperature per unit of power, °C/W). R_{th} can be described as follows:

$R_{th(JC)}$: thermal resistance from the device junction to the device case. It is the thermal resistance when the package is mounted on the infinite heatsink

$R_{th(CH)}$: the contact thermal resistance between the device case and the heatsink

$R_{th(HA)}$: thermal resistance from the heatsink to ambient

Figure 12. Thermal resistance scheme



The thermal resistance stated in datasheet refers to the above mentioned $R_{TH(J-C)}$ and to the overall $R_{TH(J-A)}$.

Table 7. Absolute maximum ratings for J-C and J-A thermal resistances

Symbol	Parameter	Value	Unit
R_{thJC}	Thermal resistance junction-case IGBT	0.53	°C/W
R_{thJC}	Thermal resistance junction-case diode	1.14	°C/W
R_{thJA}	Thermal resistance junction-ambient	50	°C/W

Equation 6

$$R_{th(j-a)} = R_{th(j-c)} + R_{th(c-h)} + R_{th(h-a)}$$

2.4.9 Maximum transient thermal impedance (Z_{thJC})

Transient thermal impedance takes into account the heat capacity of the device to estimate temperatures resulting from power loss on transient base.

Figure 13. Maximum normalized Z_{thJC} function of pulse duty factor (δ) and loading time (t_p)

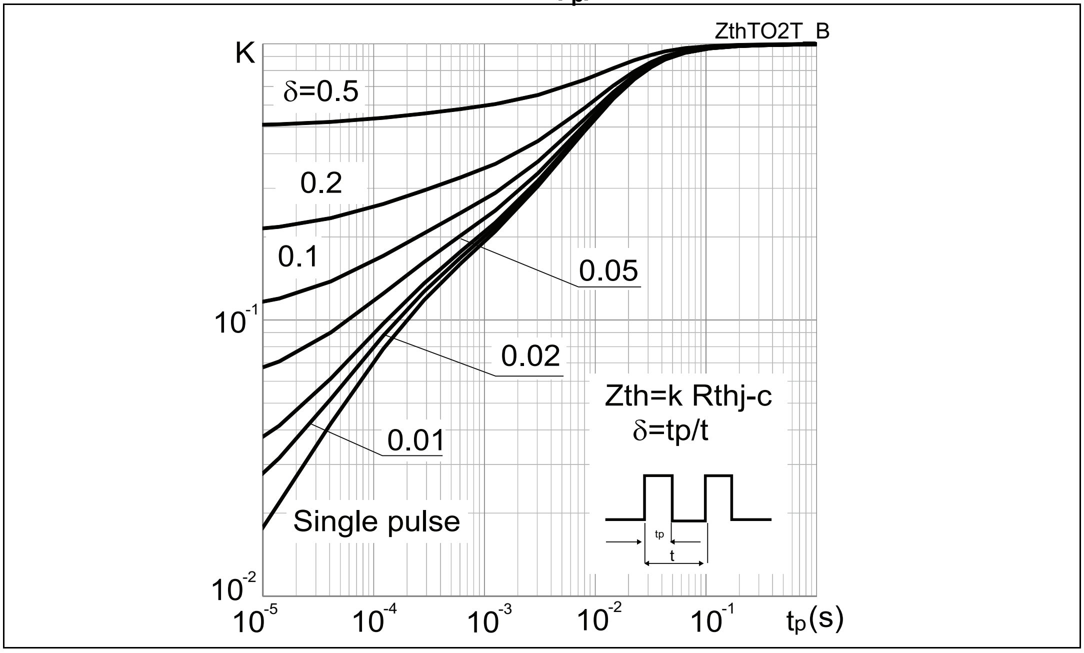


Figure 13 shows the variation of the normalized thermal impedance for the specified pulse duty factor δ=tp/t as a function of the loading time tp (pulse width).

The dissipated heat has to pass through several different layers with their thermal resistances and thermal capacitances. Therefore, according to the pulse length, either the thermal resistance or the thermal capacitance handle with the device's behavior. The increase of the junction temperature can be calculated as follows: $T_{Jstart} = T_C$:

Equation 7

$$T_j = T_{Jstart} + \Delta T_j = T_{Jstart} + Z_{thJc}(t_p,\delta) \times P_{tot} = T_{Jstart} + k(t_p,\delta) \times R_{thJc} \times P_{tot}$$

2.5 Static characteristics

These describe the behavior of the device in steady-state conditions either in the off-state or in conduction.

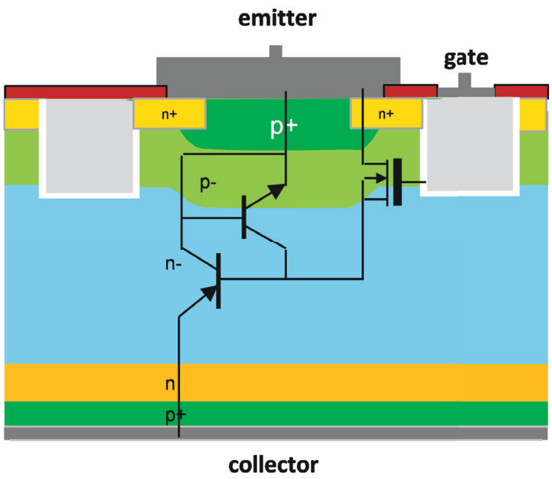
Table 8. Static characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)CES}$	Collector-emitter breakdown voltage (V_{GE} = 0)	I_C = 2 mA	600			V
$V_{CE(sat)}$	Collector-emitter saturation voltage	V_{GE} = 15 V, I_C = 40 A		1.8	2.3	V
		V_{GE} = 15 V, I_C = 40 A T_J = 125 °C		2.15		
		V_{GE} = 15 V, I_C = 40 A T_J = 175 °C		2.35		
V_F	Forward on-voltage	I_F = 40 A		1.7	2.45	V
		I_F = 40 A, T_J = 125 °C		1.4		V
		I_F = 40 A, T_J = 175 °C		1.3		V
$V_{GE(th)}$	Gate threshold voltage	V_{CE} = V_{GE}, I_C = 1 mA	5	6	7	V
I_{CES}	Collector cut-off current (V_{GE} = 0)	V_{CE} = 600 V			25	µA
I_{GES}	Gate-emitter leakage current (V_{CE} = 0)	V_{GE} = ± 20 V			250	nA

2.5.1 Collector-to-emitter saturation voltage - $V_{CE(sat)}$

$V_{CE(sat)}$ is the on-state collector-to-emitter voltage drop and represents the IGBT power dissipation during conduction time. This voltage is a function of collector current (I_C) gate-emitter voltage (V_{GE}) and junction temperature (T_J) and so it is specified at the rated I_C, V_{GE} = 15 V and T_J = 25 °C, 125 °C and 175 °C. The IGBT is used as a switch and the range of V_{CE} is within the saturation region. Increasing V_{GE} rises the channel conductivity and reduces $V_{CE(sat)}$, while increasing the collector current also increases the $V_{CE(sat)}$.

Figure 14. Cross section of a trench field-stop IGBT



From the equivalent circuit, $V_{CE(sat)}$ is given by:

Equation 8

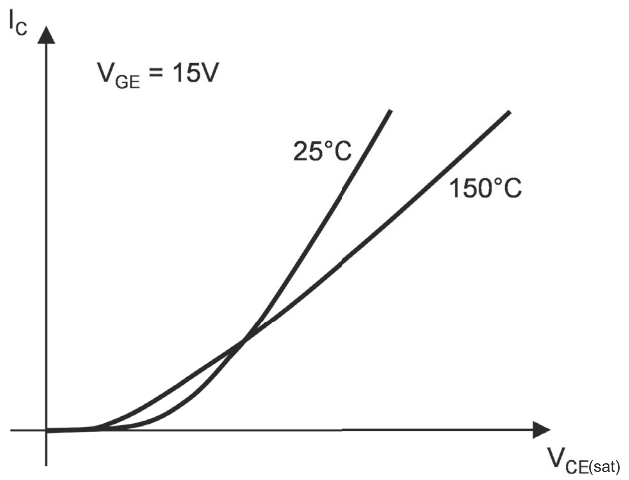
$$V_{CE(sat)} = V_{BE(PNP)} + I_{MOS} \times (R_S + R_{CH})$$

where:

- $V_{BE(PNP)}$ is the base-emitter voltage of PNP transistor (see *Figure 16*)
- I_{MOS} is the drain current of the Power MOSFET
- R_S is the resistance of the conductivity modulated n-region
- R_{CH} is the channel resistance of the Power MOSFET

Furthermore $V_{CE(sat)}$ is temperature sensitive and decreases according to the temperature rise (negative temperature coefficient) until a certain crossover point is reached, after which $V_{CE(sat)}$ begins increasing (positive temperature coefficient).

Figure 15. Output characteristics



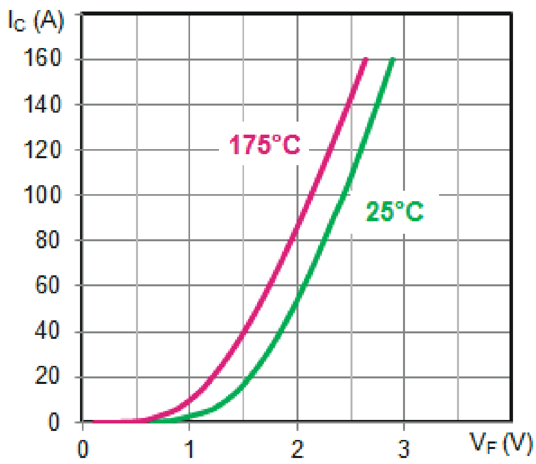
If crossover point is well below I_C operation range (like the STGW40V60DF), the IGBT has a positive temperature coefficient.

This crossover point is a function of device's geometry.

2.5.2 Forward on-voltage (V_F)

Diode forward voltage is specified under the maximum I_F (diode continuous forward current @ T_C=100 °C) and at case temperatures of 25 °C and 100 °C.

Figure 16. Forward on-voltage



2.5.3 Collector cut-off current (I_{CES})

This is the leakage current flowing from collector-to-emitter when the device is off, at a specified collector-to-emitter and gate-emitter voltage. This parameter is a function of V_{CES} and T_J. I_{CES} increases basing on V_{CES} and T_J rise.

2.5.4 Gate-to-emitter leakage current (I_{GES})

This is the gate-emitter leakage current specified at the recommended gate-emitter voltage (V_{GE}) with collector-emitter shorted (V_{CE} = 0) and T_J = 25 °C.

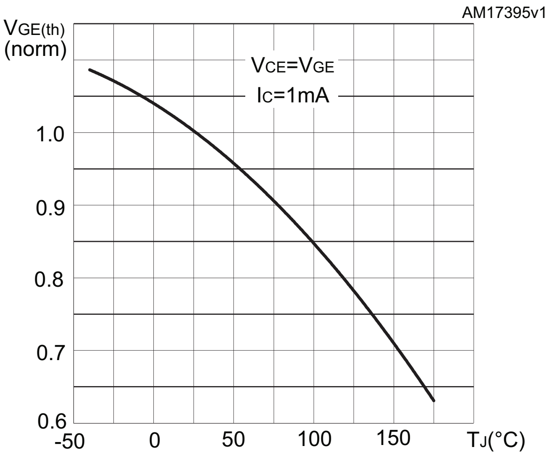
2.5.5 Gate-to-emitter threshold voltage ($V_{GE(th)}$)

This is the minimum gate to emitter voltage required to turn on the IGBT at specified I_C and V_{CE}.

$V_{GE(th)}$ limits are indicated in *Table 8* and to turn on IGBT a higher voltage than $V_{GE(th)}$ has to be applied.

The following diagram shows the variation of the normalized threshold versus temperature

Figure 17. Normalized $V_{GE(th)}$ vs junction temperature



The $V_{GE(th)}$ value decreases by a factor of approximately: -2.2 mV/°C.

2.6 Dynamic characteristics

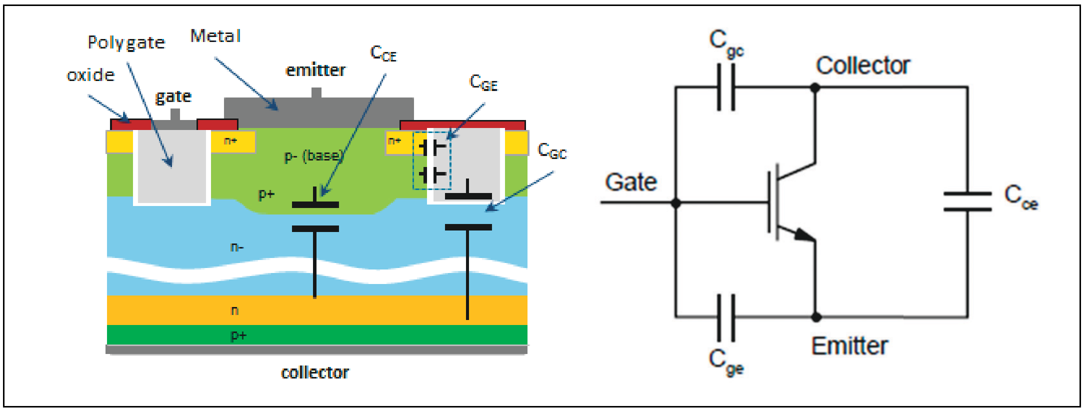
Table 9. Dynamic characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{ies}	Input capacitance	V_{CE} = 25 V, f = 1 MHz, V_{GE} = 0	-	5400	-	pF
C_{oes}	Output capacitance		-	220	-	pF
C_{res}	Reverse transfer capacitance		-	180	-	pF
Q_g	Total gate charge	V_{CC} = 480 V, I_C = 40 A, V_{GE} = 15 V	-	226	-	nC
Q_{ge}	Gate-emitter charge		-	38	-	nC
Q_{gc}	Gate-collector charge		-	95	-	nC

2.6.1 Input, output and reverse transfer capacitances (C_{ies}), (C_{oes}) and (C_{res})

IGBT dynamical characteristics are influenced by parasitic capacitances. The typical values of the capacitance are measured under specific conditions: V_{CE} = 25 V, f = 1 MHz and V_{GE} = 0 V, and its decrease is inversely proportional to the biased voltage introduced in the collector-to-emitter.

Figure 18. IGBT section and equivalent model with parasitic capacitances between terminals



2.6.2 Input capacitance (C_{ies})

This is the input capacitance measured between the gate and emitter terminals with the collector shorted to the emitter for AC signals. C_{ies} is given by the gate to collector capacitance (C_{GC}) in parallel with the gate to emitter capacitance (C_{GE}):

Equation 9

$$C_{ies} = C_{GE} + C_{GC}$$

The input capacitance has to be charged to the threshold voltage before the device begins to turn on, and discharged to the plateau voltage before the device begins to turn off. Therefore both the impedance of the drive circuitry and C_{ies}, have a direct relationship to the turn on and turn off delays.

2.6.3 Output capacitance (C_{oes})

This is the output capacitance measured between the collector and emitter terminals with the gate shorted to the emitter for AC voltages. C_{oes} is given by the collector-to-emitter capacitance (C_{CE}) in parallel with the gate to collector capacitance (C_{GC}):

Equation 10

$$C_{oes} = C_{CE} + C_{GC}$$

For soft switching applications, C_{oes} can affect the resonance of the circuit.

2.6.4 Reverse transfer capacitance (C_{res})

This is the reverse transfer capacitance measured between the collector and gate terminals with the emitter connected to ground. The reverse transfer capacitance is equal to the gate to collector capacitance:

Equation 11

$$C_{res} = C_{GC}$$

The reverse transfer capacitance, often referred to as the Miller capacitance, is one of the major parameters affecting voltage rise and fall times during switching.

Figure 19. STGW40V60DF capacitance variation

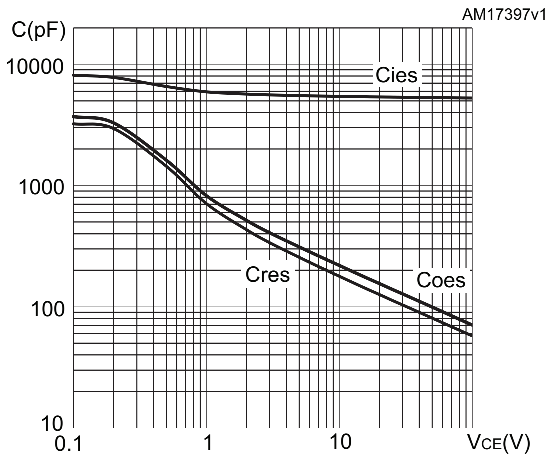


Figure 19 shows a graph of typical capacitance values versus collector-to-emitter voltage.

These capacitances decrease over a range of increasing collector-to-emitter voltage, especially the output and reverse transfer capacitances. This variation is linked to the gate charge data. These parameters are not tested in production.

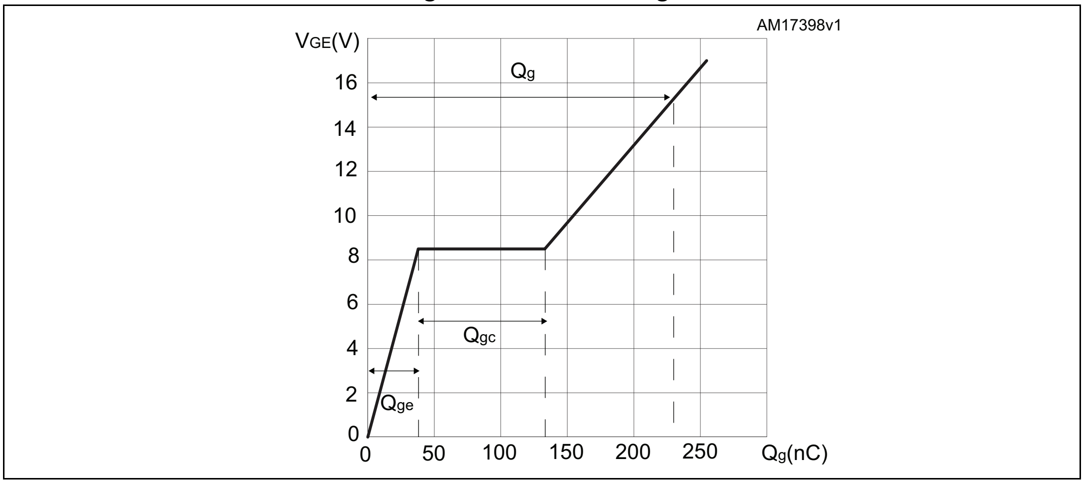
2.6.5 Gate charge (Q_{ge}), (Q_{gc}) and (Q_g)

IGBT gate charge values are useful to design the gate drive circuit, since it takes into account the changes of capacitance and voltage during a switching transient, by estimating gate drive losses.

They cannot be used to predict switching times, because of the minority carrier due to the NPN and PNP structure inside the IGBT.

Q_{ge} is the charge from the origin to the first inflection in the curve, Q_{gc} is the charge from the first to second inflection in the curve (also known as the “Miller” charge), and Q_g is the charge from the origin to the point on the curve at which V_{GE} equals the peak drive voltage. Gate charge values vary with collector current and collector-emitter voltage but not with temperature. The graph of gate charge is typically included in the datasheet showing gate charge curves for a fixed collector current and different collector-emitter voltages. The gate charge values reflect charge stored on capacitances.

Figure 20. Gate charge



These parameters are not tested in production.

2.7 IGBT switching characteristics (inductive load)

This section describes the behavior of the device during the two transitional states: from off-state to on-state and from on-state to off-state. IGBT and Power MOSFET switching characteristics are very similar. The major difference from Power MOSFET is that it has a tailing collector current due to the stored charge in the N-drift region.

Table 10. IGBT switching characteristics (inductive load)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{CE} = 400 V, I_C = 40 A, R_G = 10 Ω, V_{GE} = 15 V	-	52	-	ns
t_r	Current rise time		-	17	-	ns
$(di/dt)_{on}$	Turn-on current slope		-	1850	-	A/µs
$t_d(_{off})$	Turn-off delay time		-	208	-	ns
t_f	Current fall time		-	20	-	ns
E_{on}	Turn-on switching losses		-	456	-	µJ
E_{off}	Turn-off switching losses		-	411	-	µJ
E_{ts}	Total switching losses		-	867	-	µJ
$t_{d(on)}$	Turn-on delay time	V_{CE} = 400 V, I_C = 40 A, R_G = 10 Ω, V_{GE} = 15 V, T_J = 175 °C	-	52	-	ns
t_r	Current rise time		-	21	-	ns
$(di/dt)_{on}$	Turn-on current slope		-	1538	-	A/µs
$t_d(_{off})$	Turn-off delay time		-	220	-	ns
t_f	Current fall time		-	21	-	ns
E_{on}	Turn-on switching losses		-	1330	-	µJ
E_{off}	Turn-off switching losses		-	560	-	µJ
E_{ts}	Total switching losses		-	1890	-	µJ

The switching characteristic provides useful information to determine an appropriate dead time between turn-on and turn-off of the complementary devices in a half-bridge configuration.

Figure 21. Test circuit for switching characteristics (inductive load)

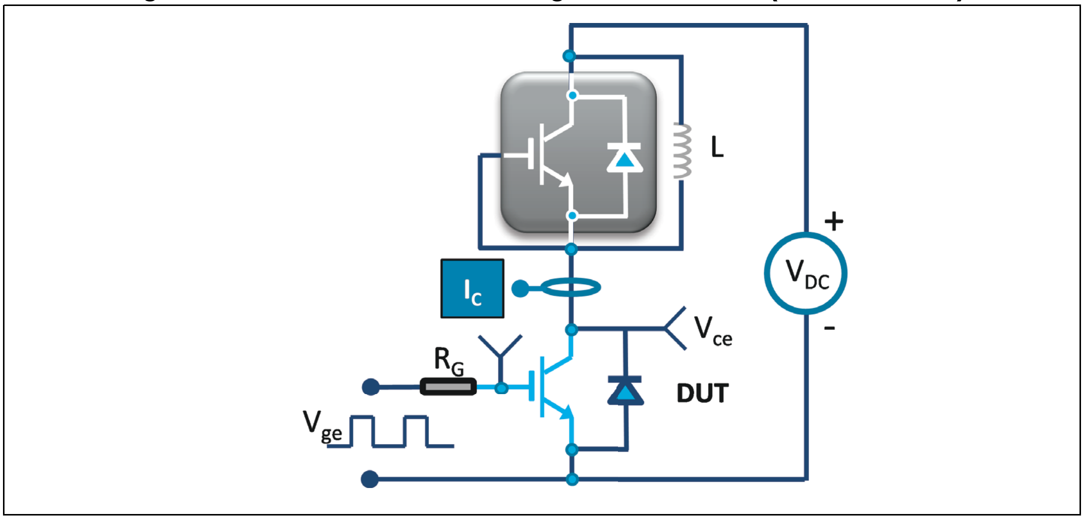
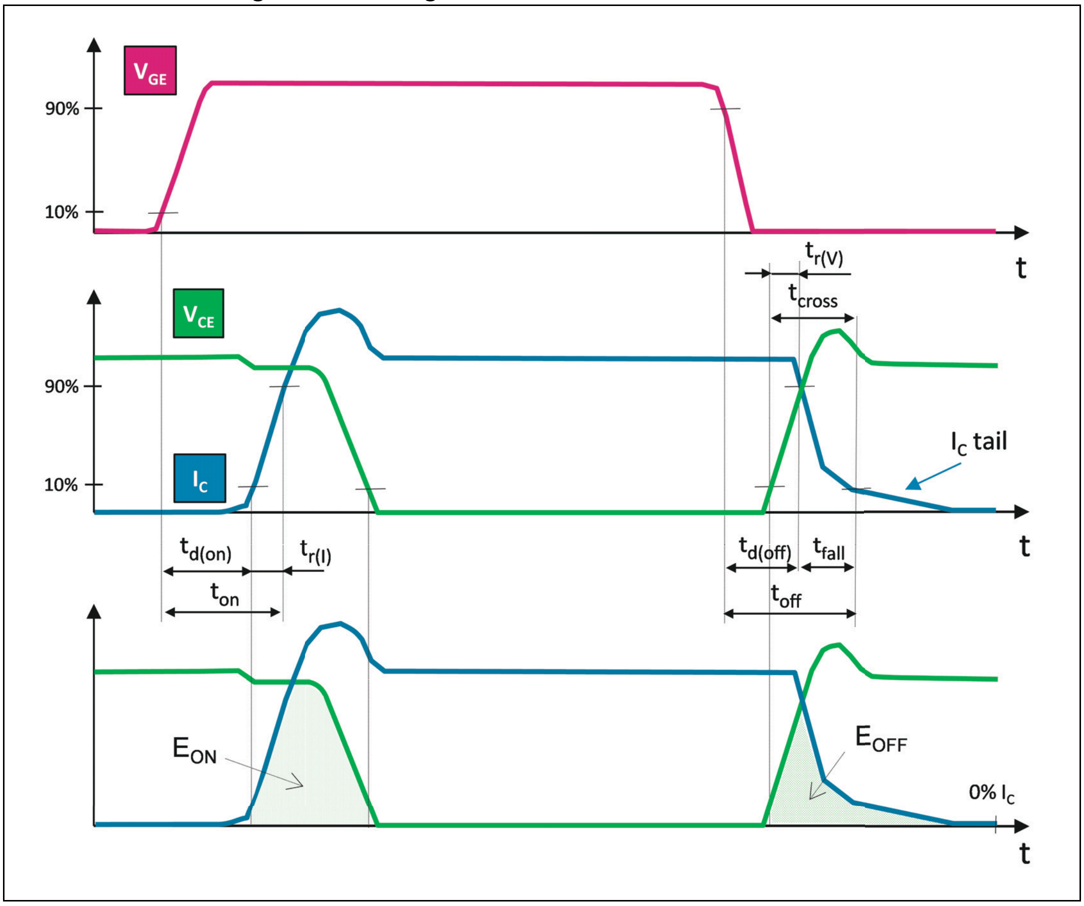


Figure 21 shows a test circuit for switching characteristics on inductive load and *Figure 22* shows the corresponding current and voltage turn-on and turn-off waveforms. IGBTs are tested with a gate voltage switched from +15 V to 0 V, T_J = 25 °C and 175 °C, nominal I_C @ 100 °C and bus voltage (V_{CE}) that is function of B_{VCES} (400 V in case min. B_{VCES} of 600 V / 650 V device or 600 V for a min. B_{VCES} of 1200 V).

Figure 22. Voltage turn-on and turn-off waveforms



2.7.1 Turn-on delay time ($t_{d(on)}$)

It is defined as the time from V_{GE} = 10% to I_C = 10% of its final value. During this time the MOSFET channel is formed.

2.7.2 Current rise time (t_r)

It is the time of I_C to increase from 10% to 90% of its final value. The rise time is influenced by the IGBT gate characteristics.

2.7.3 Turn-on current ($di/dt_{(on)}$) and voltage slope ($dv/dt_{(on)}$)

It is the rate of rise of current (di/dt) and voltage (dv/dt) during turn-on. Both of slopes can be controlled by changing the gate resistance. In particular switching transients are reduced as the gate resistance increases.

2.7.4 Turn-off delay time ($t_{d(off)}$)

It is defined as the time from V_{GE} = 90% of its initial value to IC = 90% of its initial value. During this time the MOSFET channel is removed and further supply of electrons from the emitter is cut.

2.7.5 Fall time (t_f)

it defined as the time between I_C = 90% to 10% of its initial value. The fall time also includes the tail period which stands for the time taken to recombine excess charges stored in N-region. A high current tail introduces high switching losses and limits the operating frequency of the device.

Figure 23. Switching times vs. collector current

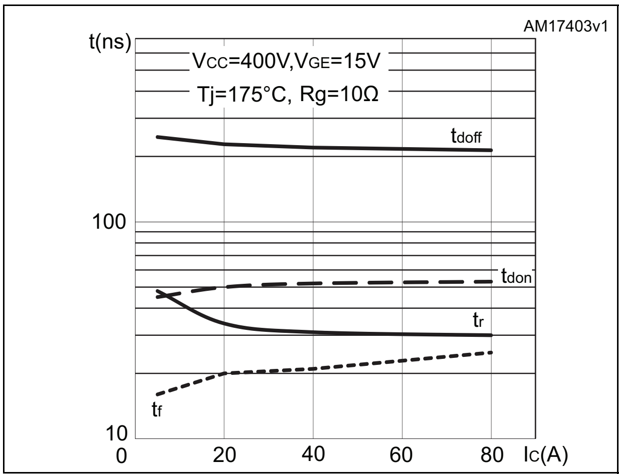
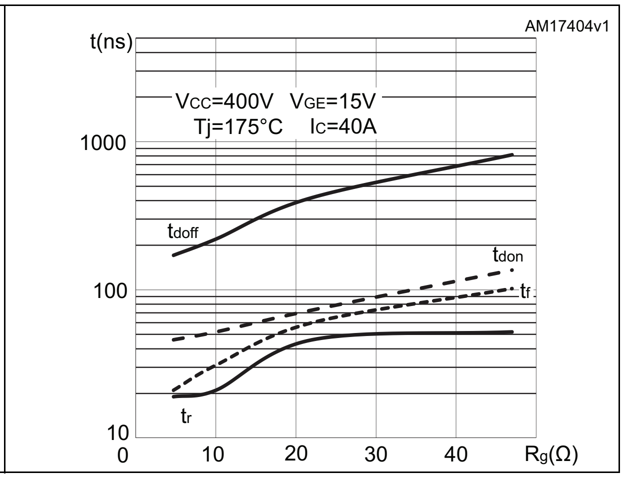


Figure 24. Switching times vs. gate resistance



2.7.6 Switching energy (E_{on}) and (E_{off})

The switching time is not sufficient to calculate the switching loss, as there is a region where some switching losses occur although they are not specifically included in the switching time.

E_{on} is the amount of total energy lost during turn-on under inductive load, and it includes the loss from the diode reverse recovery. It is measured from the point where the collector current begins to flow (10% I_C) to the point where the collector-emitter voltage reaches 10% of V_{CE}.

E_{off} is the amount of total energy lost during turn-off under inductive load. It is measured from the point where the collector-emitter voltage begins to rise (measures starts from 10% V_{CE}) to the point where the collector current falls to zero.

E_{on}, E_{off} are specified at T= 25 °C and 175 °C, I_C @ T= 100 °C, V_{GE}= 15 V, for V_{CC}= 400 V (for 600 V / 650 V devices) and under inductive load conditions. Data for T=175 °C are provided to the user because the temperature of the devices in the system rises during operation. Switching energy rises due to increase of I_C (collector current), R_G (gate resistance), T (case/junction temperature) and V_{CE} (bus voltage). *Figure 25* and *Figure 26* show detailed changes of switching energy in relation to changes of I_C, R_G, T and V_{CE}. These data are not absolute values, but they are included in the datasheet as a reference for design purposes.

Figure 25. Switching losses vs. collector current

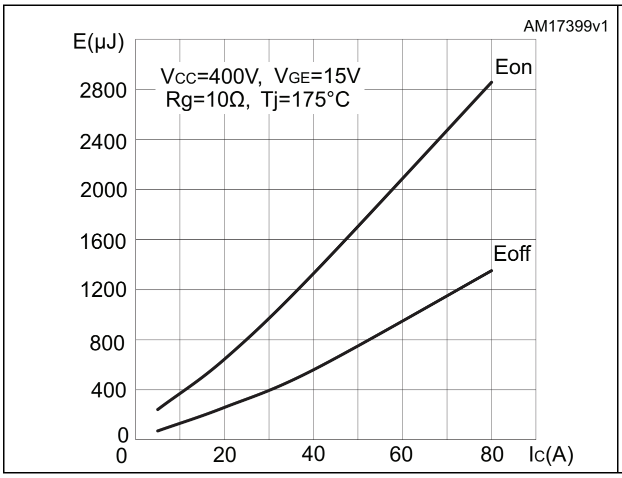


Figure 26. Switching losses vs. gate resistance

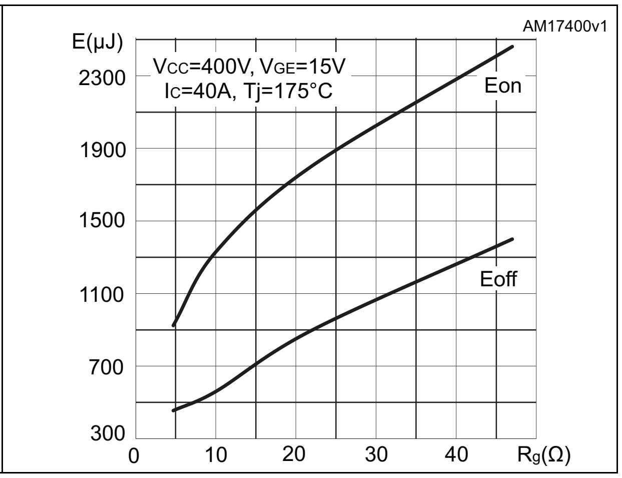


Figure 27. Switching losses vs. junction temperature

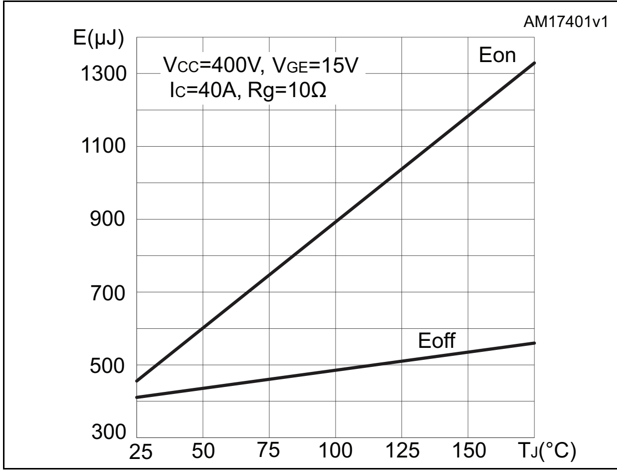
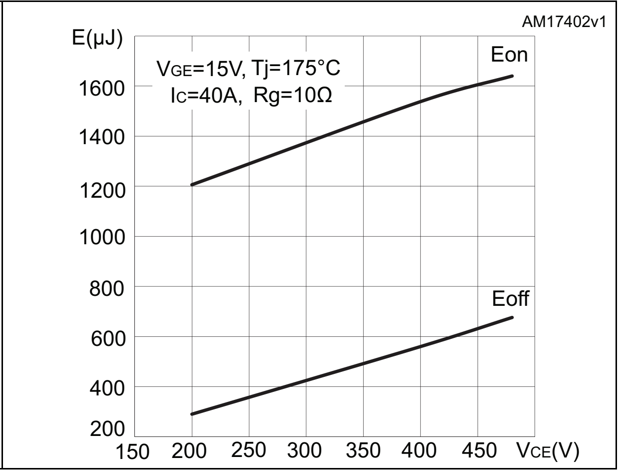


Figure 28. Switching losses vs. collector-emitter voltage



2.7.7 Short-circuit withstand time - t_{sc}

In motor control applications, the ability to turn off safely due to a load or equipment short-circuit is a very important requirement on the power switching device.

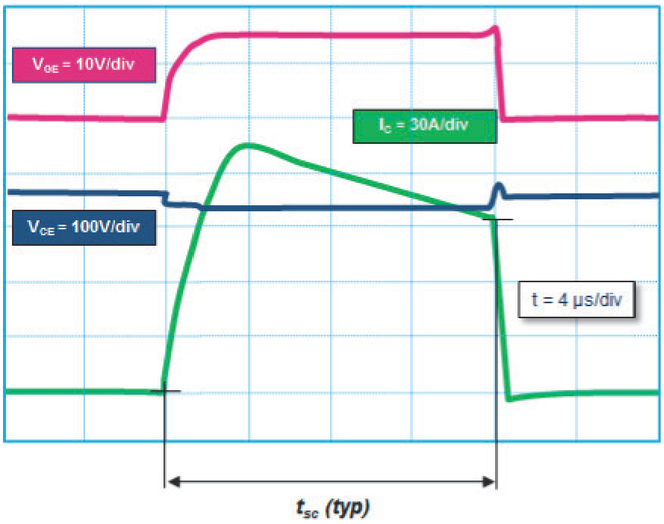
When a current overload occurs, collector current rises rapidly so the power device limits the current amplitude to a safe level for a period of time that allows the control circuit to detect the fault and turn the device off.

Table 11. Maximum ratings for short-circuit withstand time

Symbol	Description	Test conditions	Min.	Typ.	Max.	Unit
t_{sc}	Short-circuit withstand time	$V_{CC} \leq 360$, $V_{GE} = 15$ V, $T_{jstart} \leq 150$ °C	6	-	-	µs

Specific IGBT technology and series are produced to show such features.

Figure 29. Short-circuit performance example



Test conditions: V_{CC} = 360 V, R_G = 22 Ω, V_{GE} = 15 V, T_{Jstart} = 150 °C

2.7.8 Diode switching characteristics (inductive load)

Table 12. Diode switching characteristics (inductive load)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
t_{rr}	Reverse recovery time	I_F = 40 A, V_R = 400 V, V_{GE} = 15 V, di/dt=1000 A/µs	-	41	-	ns
Q_{rr}	Reverse recovery charge		-	440	-	nC
I_{rrm}	Reverse recovery current		-	21.6	-	A
$dI_{rr/}$ /dt	Peak rate of fall of reverse recovery current during t_b		-	1363	-	A/µs
E_{rr}	Reverse recovery energy		-	151	-	µJ
t_{rr}	Reverse recovery time	I_F = 40 A, V_R = 400 V, V_{GE} = 15 V, di/dt=1000 A/µs T_J = 175 °C	-	109	-	ns
Q_{rr}	Reverse recovery charge		-	2400	-	nC
I_{rrm}	Reverse recovery current		-	44.4	-	A
$dI_{rr/}$ /dt	Peak rate of fall of reverse recovery current during t_b		-	670	-	A/µs
E_{rr}	Reverse recovery energy		-	718	-	µJ

A typical reverse recovery waveform is shown in *Figure 30*. The reverse recovery time t_{rr} is defined as the time from diode current zero-crossing to where the current returns within 25% of the peak recovery current I_{RM}(rec). A better way to characterize the rectifier reverse recovery is to divide the reverse recovery time into two different regions, t_a and t_b, where t_a time is a function of the forward current and the applied di/dt. A charge Q_a can be assigned to this region, the area under the curve. t_b portion of the reverse recovery current is not well-fixed, in fact measured t_b times vary according to the switch characteristic, circuit parasitic, load inductance and the applied reverse voltage. A relative softness can be defined as the ratio of t_b to t_a. General purpose rectifiers are very soft (softness factor about 1.0), fast recovery diodes are fairly soft (softness factor about 0.5) and ultrafast rectifiers are not soft (softness factor about 0.2).

Figure 30. Typical reverse recovery waveform

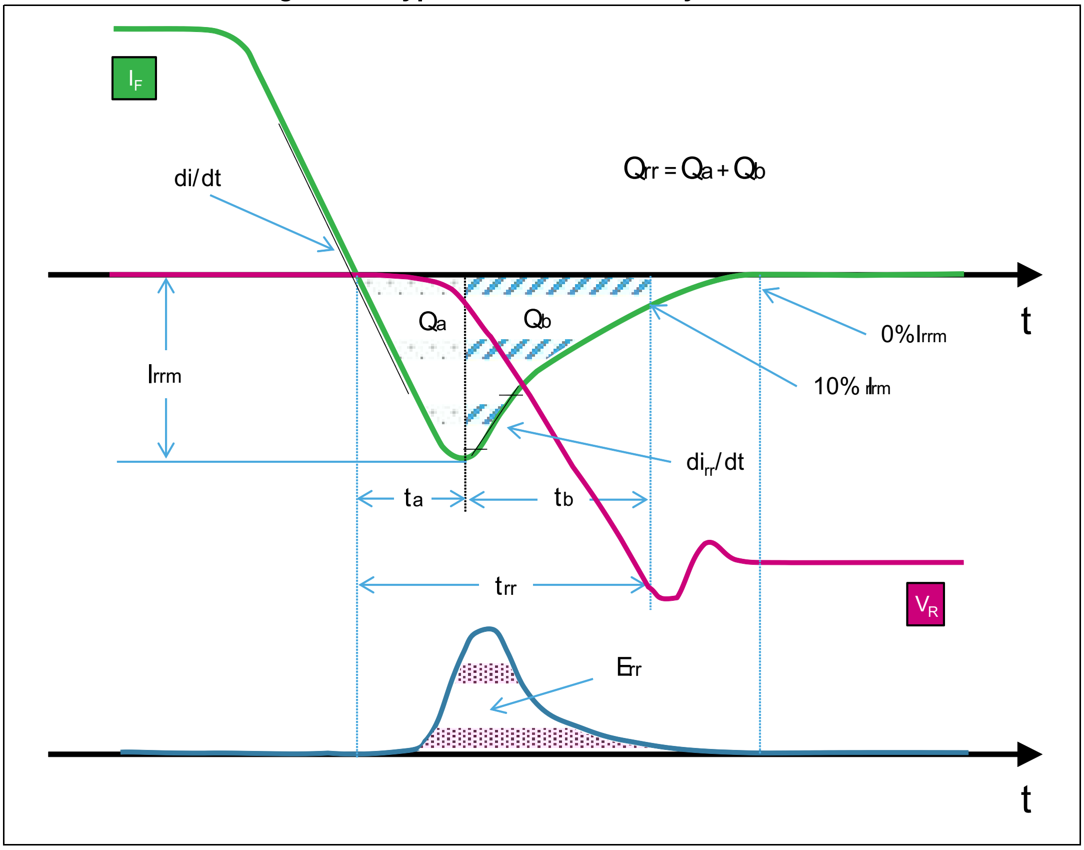


Figure 31. Reverse recovery current vs. diode current slope

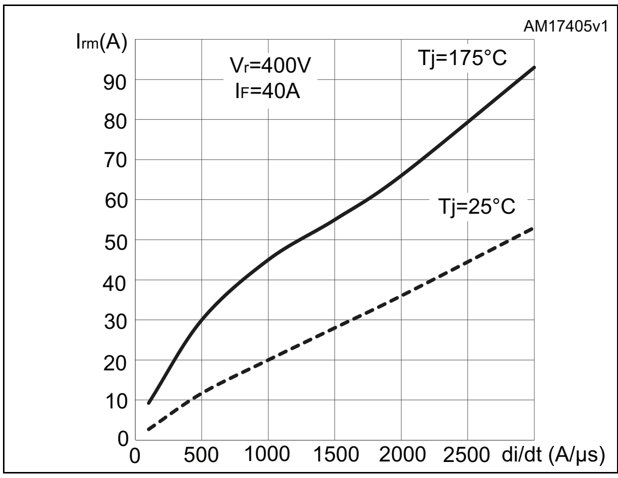


Figure 32. Reverse recovery time vs. diode current slope

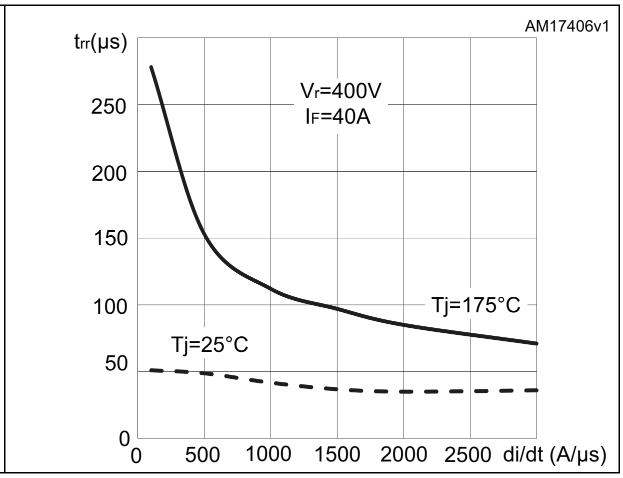


Figure 33. Reverse recovery charge vs. diode current slope

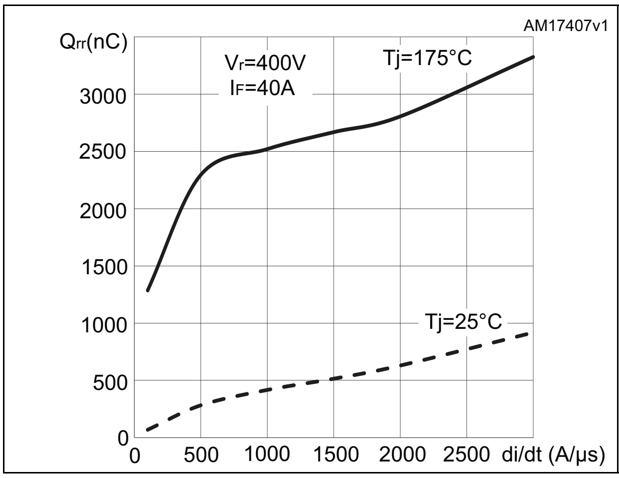
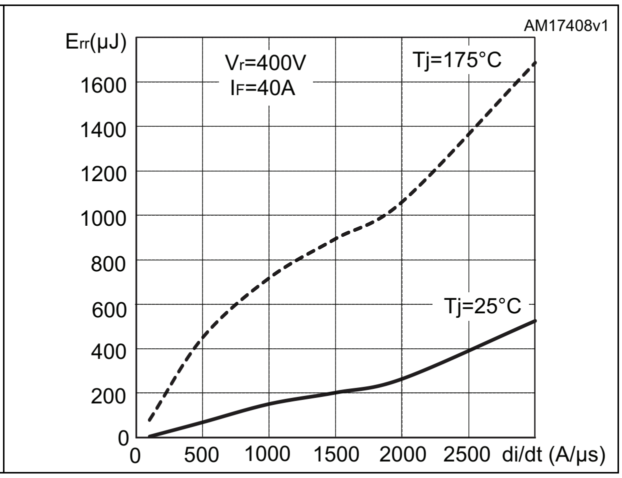


Figure 34. Reverse recovery energy vs. diode current slope



3 Revision history

Table 13. Document revision history

Date	Revision	Changes
16-Sep-2014	1	Initial release.