AN4555
Application note

Getting started with STM32L4 Series and STM32L4+ Series hardware development

Introduction

This application note is intended for system designers who require a hardware implementation overview of the development board features such as power supply, clock management, reset control, boot mode settings and debug management.

It shows how to use the STM32L4 Series and STM32L4+ Series MCUs and describes the minimum hardware resources required to develop an application using the STM32L4 Series and STM32L4+ Series devices.

Detailed reference design schematics are also contained in this document with descriptions of the main components, interfaces and modes.

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The STM32L4 Series and STM32L4+ Series are Arm®[a]-based devices.

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2.1 Power supplies

The STM32L4 Series and STM32L4+ Series devices require a 1.71 V to 3.6 V operating voltage supply (V_{DD}). Several independent supplies (V_{DDA}, V_{DDIO2}, V_{DDUSB}, V_{LCD}[b], V_{DDDSI}), can be provided for specific peripherals:

- V_{DD} = 1.71 V to 3.6 V
  V_{DD} is the external power supply for the I/Os, the internal regulator and the system analog such as reset, power management and internal clocks. It is provided externally through V_{DD} pins.
- V_{DD12} = 1.05 V[c] to 1.32 V
  V_{DD12} is the external power supply bypassing the internal regulator when connected to an external SMPS. It is provided externally through VDD12 pins and only available on packages with the external SMPS supply option. It does not need any external capacitance and cannot drive an external load.
- V_{DDA} = 1.62 V (ADCs/COMPs) / 1.8 V (DACs/OPAMPs) / 2.4 V (VREFBUF) to 3.6 V
  V_{DDA} is the external analog power supply for A/D converters, D/A converters, voltage reference buffer, operational amplifiers and comparators. The V_{DDA} voltage level is independent from the V_{DD} voltage.
- V_{DDUSB} = 3.0 V to 3.6 V (USB used)
  V_{DDUSB} is the external independent power supply for USB transceivers. The V_{DDUSB} voltage level is independent from the V_{DD} voltage.
- V_{DDIO2} = 1.08 V to 3.6 V
  V_{DDIO2} is the external power supply for 14 I/Os (Port G[15:2]). The V_{DDIO2} voltage level is independent from the V_{DD} voltage (V_{DDIO2} is not available on STM32L41xxx/42xxx/43xxx/44xxx/45xxx/46xxx).

Note: *When the functions supplied by V_{DDA}, V_{DDIO2} or V_{DDUSB} are not used, these supplies should preferably be shorted to V_{DD}.*

Note: *On small packages, V_{DDA}, V_{DDIO2} or V_{DDUSB} independent power supplies may not be present as a dedicated pin and are internally bonded to V_{DD}.*

a. Arm is a registered trademark of Arm Limited (or its subsidiaries) in the US and/or elsewhere.

b. Only for STM32L4 Series.

c. For STM32L412xx and STM32L422xx and STM32L4P5xxxxP devices, V_{DD12} could go down to 1.00 V, thus V_{DD12} = 1.00 V to 1.32 V for those devices, when bit EXT_SMPS_ON in the power control register 4 (PWR_CR4) is set.

- V_{LCD} = 2.5 V to 3.6 V

  The LCD controller can be powered either externally through VLCD pin, or internally from an internal voltage generated by the embedded step-up converter. VLCD is multiplexed with PC3 which can be used as GPIO when the LCD is not used.
- V_{BAT} = 1.55 V to 3.6 V

  V_{BAT} is the power supply for RTC, external clock 32 kHz oscillator and backup registers (through power switch) when V_{DD} is not present.
- V_{DDDSI} is an independent DSI power supply dedicated for the DSI regulator and the MIPI D-PHY. This supply must be connected to the global V_{DD}.
- V_{CAPDSI} pin is the output of the DSI regulator (1.2 V) which must be connected externally to $V_{DD12DSI}$.
- $V_{DD12DSI}$ is used to supply the MIPI D-PHY, and to supply the clock and data lanes pins. An external capacitor of 2.2 µF must be connected on the $V_{DD12DSI}$ pin.

Note: V_{DDDSI}, V_{CAPDSI} and $V_{DD12DSI}$ are available only on STM32L4S9xx/4R9xx devices.

- V_{REF-}, V_{REF+}

  V_{REF+} is the input reference voltage for ADCs and DACs. It is also the output of the internal voltage reference buffer when enabled.

  When V_{DDA} < 2 V, V_{REF+} must be equal to V_{DDA}.

  When V_{DDA} ≥ 2 V, V_{REF+} must be between 2 V and V_{DDA}.

  V_{REF+} can be grounded when ADC and DAC are not active.

  The internal voltage reference buffer supports two output voltages, which are configured with VRS bit in the VREF_CSR register:
  - V_{REF+} around 2.048 V. This requires V_{DDA} equal to or higher than 2.4 V.
  - V_{REF+} around 2.5 V. This requires V_{DDA} equal to or higher than 2.8 V.

  V_{REF-} and V_{REF+} pins are not available on all packages. When not available, they are bonded to V_{SSA} and V_{DDA}, respectively.

  When the V_{REF+} is double-bonded with V_{DDA} in a package, the internal voltage reference buffer is not available and must be kept disable (refer to datasheet for packages pinout description).

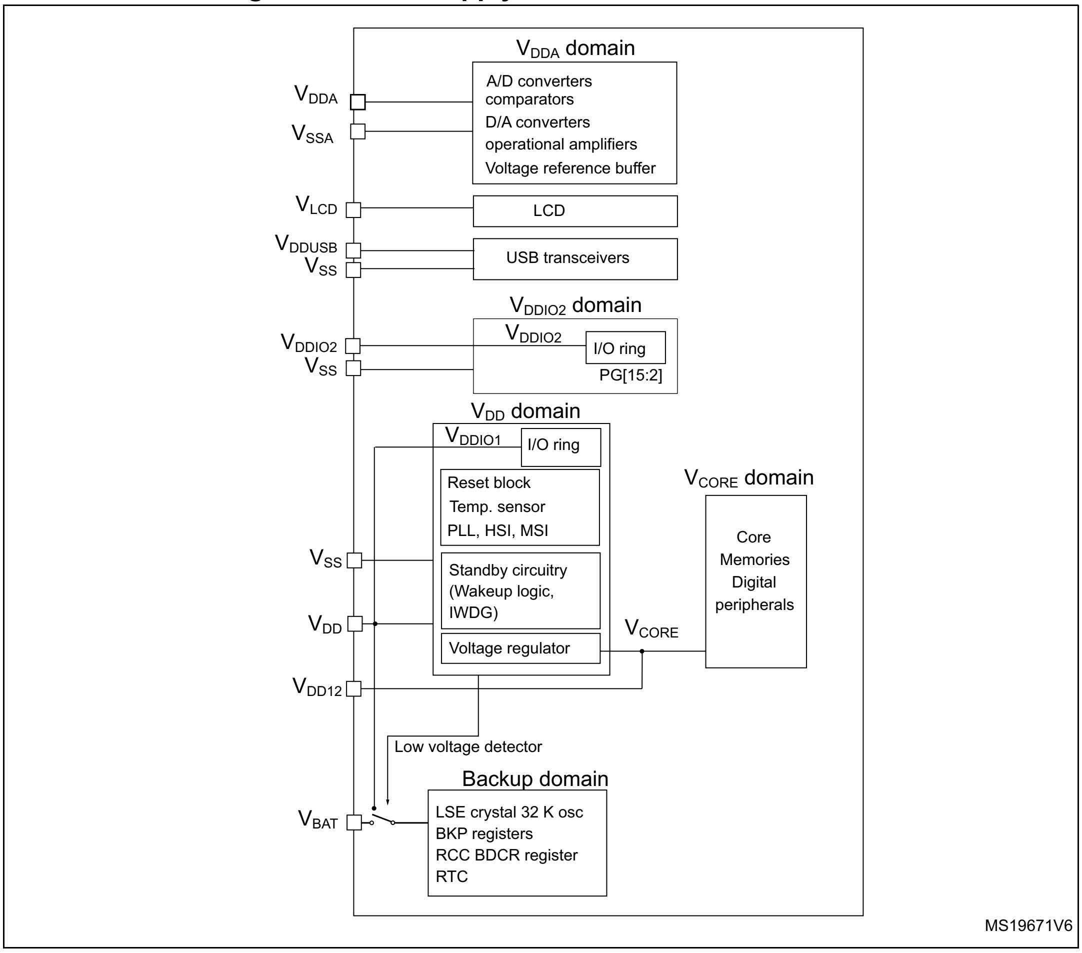
  V_{REF-} must always be equal to V_{SSA}.

Note: Independent power supplies are not present when the related features are not supported on the product, they are not present neither on small packages where they are bonded together with other supply pin.

An embedded linear voltage regulator is used to supply the internal digital power V_{CORE}. V_{CORE} is the power supply for digital peripherals and SRAMs. The Flash is supplied by V_{CORE} and V_{DD}.

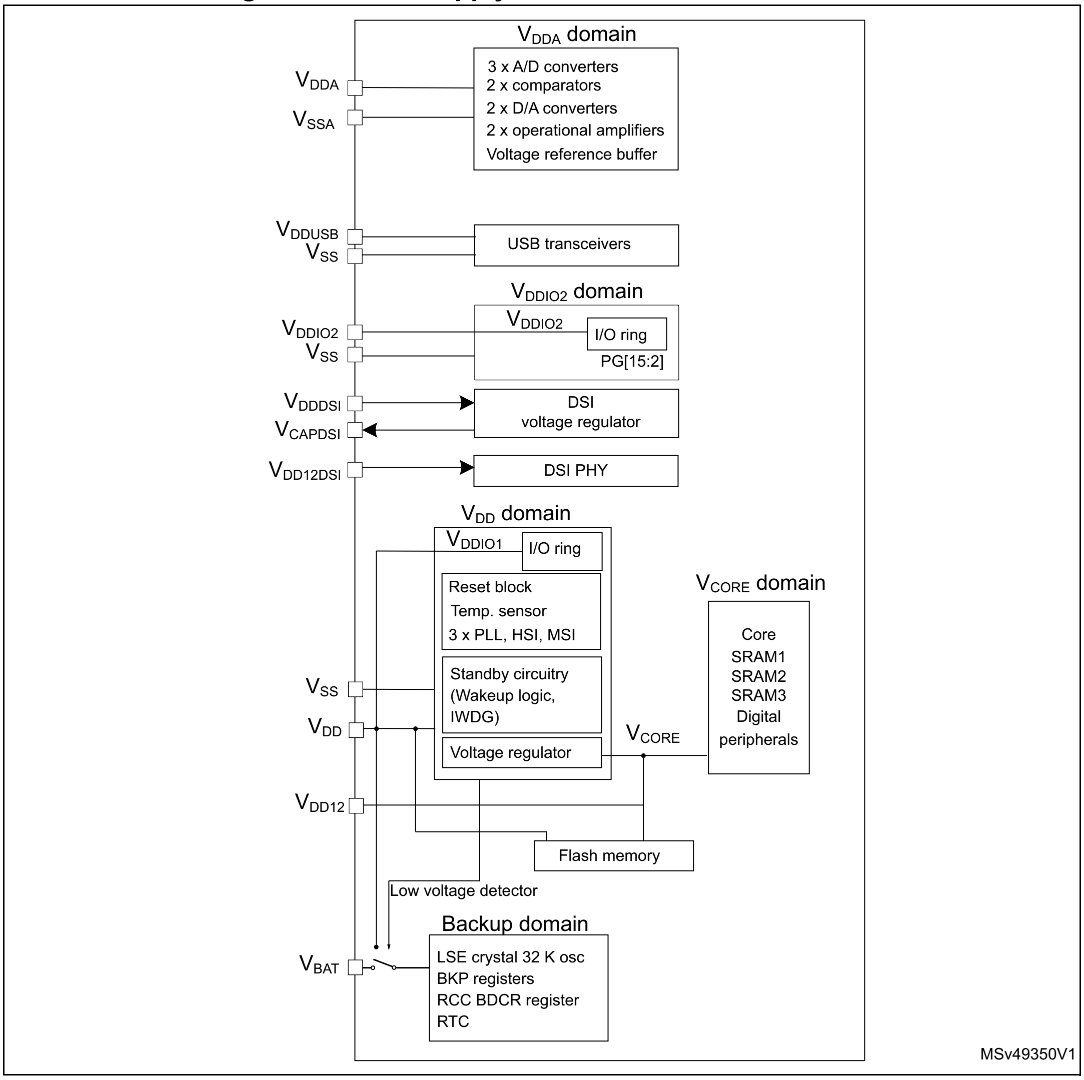
Figure 1 presents the power supply overview of the STM32L4 Series and *Figure 2* the power supply overview of STM32L4+ Series.

Figure 1. Power supply overview: STM32L4 Series



1. On STM32L41xxx/42xxx/43xxx/44xxx/45xxx/46xxx devices there is no V_{DDIO2} power domain.

Figure 2. Power supply overview: STM32L4+ Series



1. V_{DDDSI}, V_{CAPDSI} and $V_{DD12DSI}$ are only available on STM32L4R9xx/S9xx devices.

2.1.1 Independent analog peripherals supply

To improve ADC and DAC conversion accuracy and to extend the supply flexibility, the analog peripherals have an independent power supply which can be separately filtered and shielded from noise on the PCB.

- The analog peripherals voltage supply input is available on a separate V_{DDA} pin.
- An isolated supply ground connection is provided on V_{SSA} pin.

The V_{DDA} supply voltage can be different from V_{DD}. The presence of V_{DDA} must be checked before enabling any of the analog peripherals supplied by V_{DDA} (A/D converter, D/C converter, comparators, operational amplifiers, voltage reference buffer).

The V_{DDA} supply can be monitored by the peripheral voltage monitoring, and compared with two thresholds (1.65 V for PVM3 or 1.8 V for PVM4), refer to reference manual *section: Peripheral voltage monitoring (PVM)* for more details.

When a single supply is used, V_{DDA} can be externally connected to V_{DD} through the external filtering circuit in order to ensure a noise-free V_{DDA} reference voltage.

ADC and DAC reference voltage

To ensure a better accuracy on low-voltage inputs and outputs, the user can connect to V_{REF+} a separate reference voltage lower than V_{DDA}. V_{REF+} is the highest voltage, represented by the full scale value, for an analog input (ADC) or output (DAC) signal.

V_{REF+} can be provided either by an external reference or by an internal buffered voltage reference (V_{REF}).

The internal voltage reference is enabled by setting the ENVR bit in the *V_{REF} control and status register (VREF_CSR)*. The voltage reference is set to 2.5 V when the VRS bit is set and to 2.048 V when the VRS bit is cleared. The internal voltage reference can also provide the voltage to external components through V_{REF+} pin. Refer to the device datasheet or reference manual for further information.

2.1.2 Independent I/O supply rail

Some I/Os from Port G (PG[15:2]) are supplied from a separate supply rail. The power supply for this rail can range from 1.08 V to 3.6 V and is provided externally through the V_{DDIO2} pin. The V_{DDIO2} voltage level is completely independent from V_{DD} or V_{DDA}. The V_{DDIO2} pin is available only for some packages. Refer to the pinout diagrams or tables in the related device datasheet(s) for I/O list(s).

After reset, the I/Os supplied by V_{DDIO2} are logically and electrically isolated and therefore are not available. The isolation must be removed before using any I/O from PG[15:2], by setting the IOSV bit in the PWR_CR2 register, once the V_{DDIO2} supply is present.

The V_{DDIO2} supply is monitored by the peripheral voltage monitoring (PVM2) and compared with the internal reference voltage (3/4 V_{REFINT}, around 0.9 V), refer to reference manual *section: Peripheral voltage monitoring (PVM)* for more details.

Note: This does not apply to STM32L41xxx/42xxx/43xxx/44xxx/45xxx/46xxx devices.

2.1.3 Independent USB transceivers supply

The USB transceivers are supplied from a separate V_{DDUSB} power supply pin. V_{DDUSB} range is from 3.0 V to 3.6 V and its voltage level is completely independent from V_{DD} or V_{DDA}.

After reset, the USB features supplied by V_{DDUSB} are logically and electrically isolated and therefore are not available. The isolation must be removed before using the USB OTG peripheral, by setting the USV bit in the PWR_CR2 register, once the V_{DDUSB} supply is present.

The V_{DDUSB} supply is monitored by the peripheral voltage monitoring (PVM1) and compared with the internal reference voltage (V_{REFINT}, around 1.2 V), refer to reference manual s*ection: Peripheral voltage monitoring (PVM)* for more details.

2.1.4 Independent LCD supply

The V_{LCD} pin is provided to control the contrast of the glass LCD. This pin can be used in two ways:

- It can receive from an external circuitry the desired maximum voltage that is provided on segment and common lines to the glass LCD by the microcontroller.
- It can also be used to connect an external capacitor that is used by the microcontroller for its voltage step-up converter. This step-up converter is controlled by software to provide the desired voltage to segment and common lines of the glass LCD.

The voltage provided to segment and common lines defines the contrast of the glass LCD pixels. This contrast can be reduced when the user configures the dead time between frames.

- When an external power supply is provided to the V_{LCD} pin, it should range from 2.5 V to 3.6 V. It does not depend on VDD.
- When the LCD is based on the internal step-up converter, the V_{LCD} pin should be connected to a capacitor (see the product datasheet for further information).

Note: The independent LCD supply is available only on STM32L496xx/4A6xx/476xx/486xx/433xx/443xx devices.

2.1.5 Independent DSI supply

The DSI (display serial interface) sub-system uses several power supply pins which are independent from the other supply pins:

- V_{DDDSI} is an independent DSI power supply dedicated for the DSI regulator and MIPI D-PHY. This supply must be connected to the global V_{DD}.
- V_{CAPDSI} is the output of DSI regulator (1.2 V) which must be connected externally to $V_{DD12DSI}$.
- $V_{DD12DSI}$ is used to supply the MIPI D-PHY, and to supply clock and data lanes pins. An external capacitor of 2.2 uF must be connected on $V_{DD12DSI}$ pin.
- V_{SSDSI} pin is an isolated supply ground used for DSI sub-system.

If DSI functionality is not used at all, then:

- V_{DDDSI} must be connected to global V_{DD}.
- V_{CAPDSI} can be left floating, otherwise connect it externally to $V_{DD12DSI}$ and the external capacitor is not needed.
- V_{SSDSI} must be grounded.
- V_{DDDSI} and $V_{DD12DSI}$ pins are not available on all packages. When not available, they are bonded to V_{DD} and V_{CAPDSI}, respectively.

Note: The DSI supply is available only on STM32L4R9xx/4S9xx.

2.1.6 Battery backup domain

To retain the content of the backup registers and supply the RTC function when V_{DD} is turned off, the V_{BAT} pin can be connected to an optional backup voltage supplied by a battery or by another source.

The V_{BAT} pin powers the RTC unit, the LSE oscillator and the PC13 to PC15 I/Os, allowing the RTC to operate even when the main power supply is turned off. The switch to the V_{BAT} supply is controlled by the power-down reset embedded in the Reset block.

Warning: During $t_{RSTTEMPO}$ (temporization at V_{DD} startup) or after a PDR has been detected, the power switch between V_{BAT} and V_{DD} remains connected to V_{BAT}.
During the startup phase, if V_{DD} is established in less than $t_{RSTTEMPO}$ (refer to the datasheet for the value of $t_{RSTTEMPO}$) and $V_{DD} > V_{BAT} + 0.6$ V, a current may be injected into V_{BAT} through an internal diode connected between V_{DD} and the power switch (V_{BAT}).
If the power supply/battery connected to the V_{BAT} pin cannot support this current injection, it is strongly recommended to connect an external low-drop diode between this power supply and the V_{BAT} pin.

If no external battery is used in the application, it is recommended to connect V_{BAT} externally to V_{DD} with a 100 nF external ceramic decoupling capacitor.

When the backup domain is supplied by V_{DD} (analog switch connected to V_{DD}), the following pins are available:

- PC13, PC14 and PC15 can be used as GPIO pins or can be configured by RTC or LSE pins (refer to reference manual *section: RTC functional description*)
- PA0/RTC_TAMP2 and PE6/RTC_TAMP3 when they are configured by the RTC as tamper pins.

Note: Due to the fact that the analog switch can transfer only a limited amount of current (3 mA), the use of GPIO PC13 to PC15 in output mode is restricted: the frequency has to be limited to 2 MHz with a maximum load of 30 pF and these I/Os must not be used as a current source (for instance to drive a LED).

When the backup domain is supplied by V_{BAT} (analog switch connected to V_{BAT} because V_{DD} is not present), the following functions are available:

- PC13, PC14 and PC15 can be controlled only by RTC or LSE refer to reference manual *section: RTC functional description*
- PA0 and PE6 can be used as tamper inputs by the RTC (RTC_TAMP2 and RTC_TAMP3 respectively).

Backup domain access

After a system reset, the backup domain (RTC registers and backup registers) is protected against possible unwanted write accesses. To enable access to the backup domain, proceed as follows:

1. Enable the power interface clock by setting the PWREN bits in the *APB1 peripheral clock enable register 1 (RCC_APB1ENR1)*.
2. Set the DBP bit in the *Power control register 1 (PWR_CR1)* to enable access to the backup domain.
3. Select the RTC clock source in the *backup domain control register (RCC_BDCR)*.
4. Enable the RTC clock by setting the RTCEN [15] bit in the *backup domain control register (RCC_BDCR)*.

VBAT battery charging

When V_{DD} is present, It is possible to charge the external battery on V_{BAT} through an internal resistance.

The V_{BAT} charging is done either through a 5 kΩ resistor or through a 1.5 kΩ resistor depending on the V_{BRS} bit value in the PWR_CR4 register. The battery charging is enabled by setting V_{BE} bit in the PWR_CR4 register. It is automatically disabled in V_{BAT} mode.

2.1.7 Voltage regulator

Two embedded linear voltage regulators supply all the digital circuitries, except for the Standby circuitry and the backup domain. The main regulator output voltage (V_{CORE}) can be programmed by software to two different power ranges (Range 1 and Range 2) in order to optimize the consumption depending on the system's maximum operating frequency (refer to reference manual *Section: Clock source frequency versus voltage scaling* and to *Section: Read access latency*. For STM32L4+ Series, the Range 1 can be configured in normal mode or in boost mode.

The voltage regulators are always enabled after a reset. Depending on the application modes, the V_{CORE} supply is provided either by the main regulator (MR) or by the low-power regulator (LPR).

- In Run, Sleep and Stop 0 modes, both regulators are enabled and the main regulator (MR) supplies full power to the V_{CORE} domain (core, memories and digital peripherals).
- In Low-power run and Low-power sleep modes, the main regulator is off and the low-power regulator (LPR) supplies low power to the V_{CORE} domain, preserving the contents of the registers and of internal SRAMs.
- In Stop 1 and Stop 2 modes, the main regulator is off and the low-power regulator (LPR) supplies low power to the V_{CORE} domain, preserving the contents of the registers and internal SRAMs.

- In Standby mode, the SRAM2 content can be fully or partially[a] preserved (depending on RRS[1:0] bits in the PWR_CR3 register). The main regulator (MR) is off and the low-power regulator (LPR) provides the supply only to SRAM2. The core, digital peripherals (except Standby circuitry and backup domain) and SRAM1 are powered off.
- In Standby mode, both regulators are powered off. The contents of the registers and SRAMs is lost except for the Standby circuitry and the backup domain.
- In Shutdown mode, both regulators are powered off. When exiting from Shutdown mode, a power-on reset is generated. Consequently, the contents of the registers and of SRAMx is lost, except for the backup domain.

The packages with external SMPS supply option allows to force an external V_{DD12} supply on the V_{CORE} power domain when the MR is in use.

- When V_{DD12} is forced by an external source and is higher than the output of the internal LDO, the current is taken from this external supply and the overall power efficiency is significantly improved if using an external step down DC/DC converter.

Note: For more details refer to the VDD12 domain in the reference manual and to learn more on VDD12 management, refer to "Design recommendations for STM32L4xxxx with external SMPS, for ultra-low-power applications with high performance" (AN4978).

2.1.8 Dynamic voltage scaling management

The dynamic voltage scaling is a power management technique which consists in increasing or decreasing the voltage used for the digital peripherals (V_{CORE}), according to the application performance and power consumption needs.

Dynamic voltage scaling to increase V_{CORE} is known as overvolting. Overvolting improves the device's performance.

Dynamic voltage scaling to decrease V_{CORE} is known as undervolting. Undervolting is performed to save power, particularly in laptop and other mobile devices where the energy comes from a battery and is thus limited.

- Range 1: High-performance range.
  For STM32L4+ Series the main regulator operates in two modes following the R1MODE bit in the PWR_CR5 register:
  - Main regulator Range 1 boost mode: the main regulator provides a typical output voltage at 1.28 V. It is used when the system clock frequency is greater than 80 MHz.
  - Main regulator Range 1 normal mode: the main regulator provides a typical output at 1.2 V. It is used when the system clock frequency is up to 80 MHz.

  For STM32L4 Series devices, the main regulator provides a typical output voltage at 1.2 V. The system clock frequency can be up to 80 MHz. The Flash access time for read access is minimum, the write and erase operations are possible.
- Range 2: Low-power range.
  The main regulator provides a typical output voltage at 1.0 V. The system clock frequency

a. For STM32L4 Series and STM32L4Rxxx and STM32L4Sxxx devices it is only possible to preserve the full SRAM2 content depending on RRS bit in the PWR_CR3 register. For STM32L4P5xx and STM32L4Q5xx devices it is possible to preserve the full (64 Kbytes) or partial (4 Kbytes) SRAM2 content depending on RRS[1:0] bits in the PWR_CR3 register.

can be up to 26 MHz.The Flash access time for a read access is increased as compared to Range 1; write and erase operations are possible (except for STM32L4+ Series).

Voltage scaling is selected through the V_{OS} bit in the PWR_CR1 register.

The sequence to go from Range 1 (Normal/Boost) to Range 2 is:

1. In case of switching from Range 1 boost mode to Range 2, the system clock must be divided by 2 using the AHB prescaler before switching to a lower system frequency for at least 1 us and then reconfigure the AHB prescaler.
2. Reduce the system frequency to a value lower than 26 MHz.
3. Adjust number of wait states according new frequency target in Range 2 (LATENCY bits in the FLASH_ACR).
4. Program the VOS bits to “10” in the PWR_CR1 register.

The sequence to go from Range 2 to Range 1 is:

1. Program the VOS bits to “01” in the PWR_CR1 register.
2. Wait until the VOSF flag is cleared in the PWR_SR2 register.
3. Adjust number of wait states according to the new frequency target in Range1 (LATENCY bits in the FLASH_ACR).
4. Increase the system frequency by following below procedure:

- If the system frequency is 26 MHz < SYSCLK ≤ 80 MHz, select the Range 1 mode and just configure and switch to PLL for a new system frequency. For STM32L4+ Series, the R1MODE bit must be set in the PWR_CR5 register for Range1 normal mode selection.
- If the system frequency is SYSCLK > 80 MHz, select the Range 1 boost mode (this is only available in STM32L4+ Series):
  - The system clock must be divided by 2 using the AHB prescaler before switching to a higher system frequency.
  - Clear the R1MODE bit in the PWR_CR5 register.
  - Configure and switch to PLL for a new system frequency.
  - Wait for at least 1 us and then reconfigure the AHB prescaler to get the needed HCLK clock frequency.

For more details about how to switch between ranges (i.e. from Range1 normal mode to Range1 boost mode....) refer to the reference manual.

Note: Range1 boost mode is available only in STM32L4+ Series.

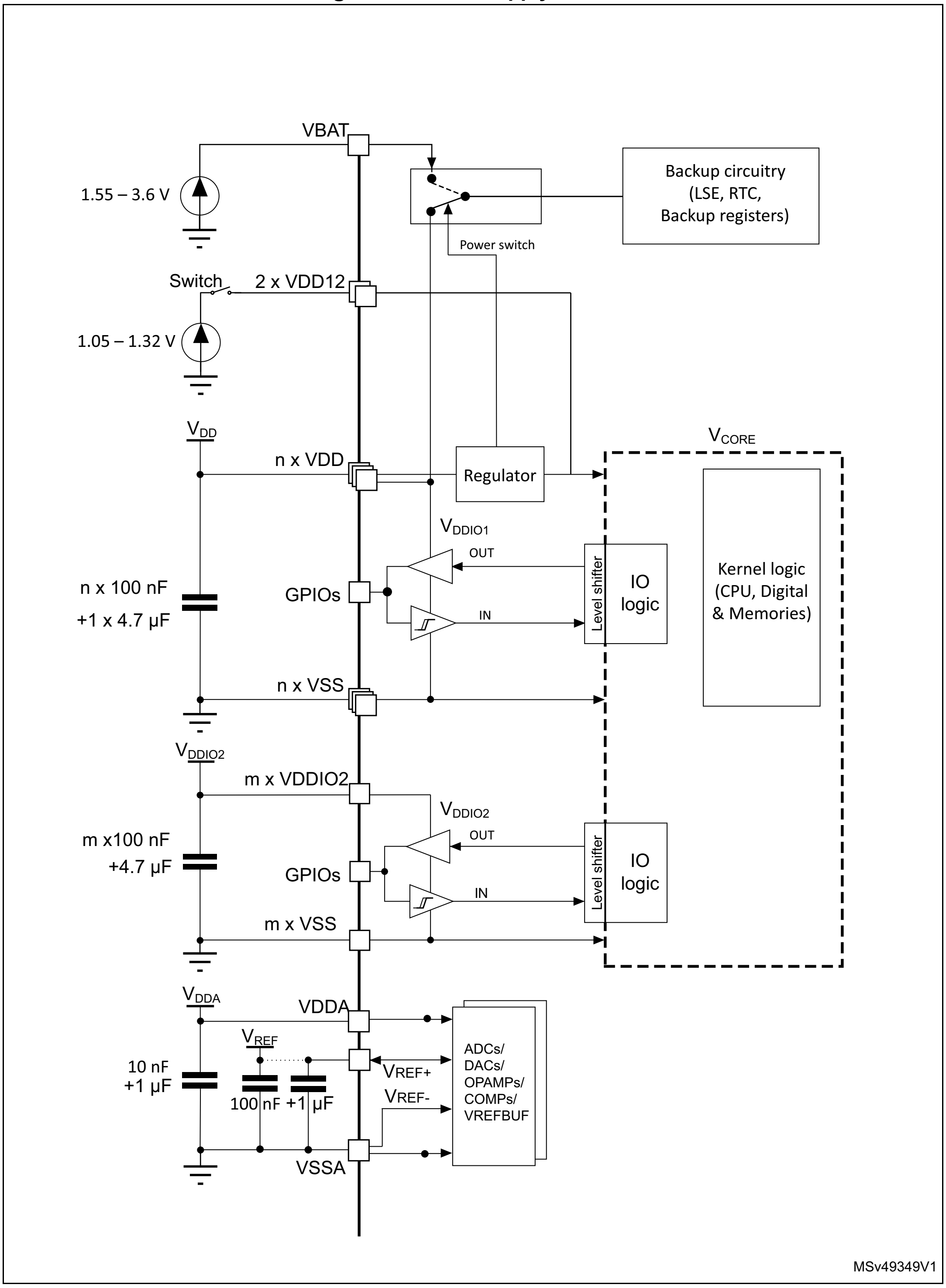
2.2 Power supply schemes

The circuit is powered by a stabilized power supply, V_{DD}.

- The V_{DD} pins must be connected to V_{DD} with external decoupling capacitors; one single Tantalum or ceramic capacitor (minimum 4.7 µF typical 10 µF) for the package + one 100 nF ceramic capacitor for each V_{DD} pin).
- The V_{DD12} pins, when available, can be connected to an external SMPS. As these V_{DD12} pin are also connected to internal regulators, they cannot accommodate a decoupling capacitance, neither can they be shared with an external circuitry for other purposes.
- The V_{DDA} pin must be connected to two external decoupling capacitors (10 nF ceramic capacitor + 1 µF Tantalum or ceramic capacitor).
  Additional precautions can be taken to filter digital noise: V_{DDA} can be connected to V_{DD} through a ferrite bead.
- The V_{REF+} pin can be provided by an external voltage reference in which case an external capacitor of 100 nF and a 1 µF capacitor must be connected on this pin.
  It can also be provided internally by the Voltage Reference Buffer in which case an external capacitor of 1 µF (typical) must be connected on this pin.
- The V_{BAT} pin can be connected to an external battery to preserve backup domain content.
  When V_{DD} is present, it is possible to charge the external battery on V_{BAT} through a 5 kΩ or 1.5 kΩ internal resistor.
  If no external battery is used in the application, it is recommended to connect V_{BAT} externally to V_{DD} with a 100 nF external ceramic decoupling capacitor.
- The V_{LCD} pin can be provided by an external voltage reference in which case an external capacitor of 100 nF and a 1 µF capacitor must be connected on this pin.
  It can also be provided internally by the Step-up Converter in which case an external capacitor of 1 µF (typical) must be connected on this pin.
- $V_{DD12DSI}$ is used to supply the MIPI D-PHY, and to supply clock and data lanes pins. An external capacitor of 2.2 µF must be connected on the $V_{DD12DSI}$ pin.
- V_{DDDSI} is an independent DSI power supply dedicated for the DSI regulator and the MIPI D-PHY. This supply must be connected to the global V_{DD}.
- V_{CAPDSI} pin is the output of the DSI regulator (1.2 V) which must be connected externally to $V_{DD12DSI}$.

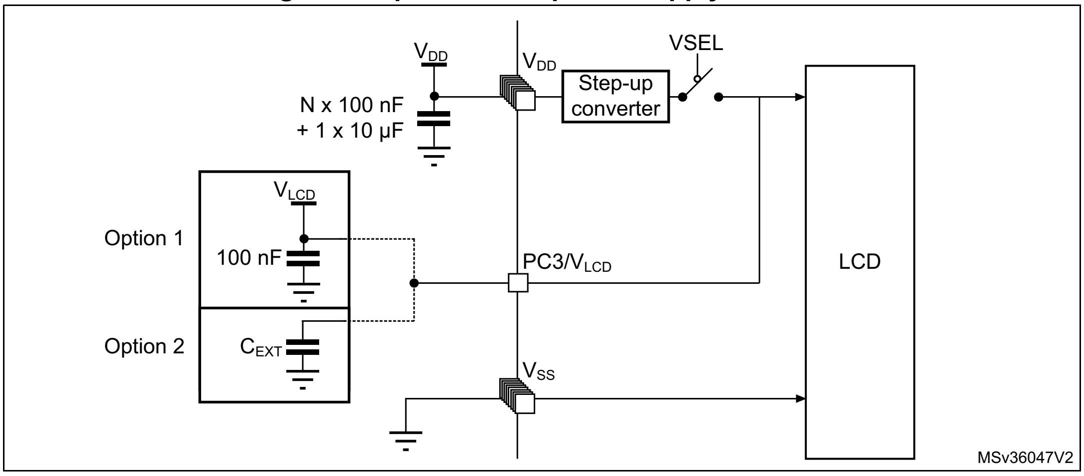
Note: V_{DDDSI}, V_{CAPDSI} and $V_{DD12DSI}$ are available only on STM32L4S9xx/4R9xx devices.

Figure 3. Power supply scheme



1. V_{REF}+ is either connected to V_{DDA} or to V_{REF}.
2. n is the number of V_{DD} inputs.
3. m is the number of V_{DDIO2} inputs.
4. There is no V_{DDIO2} on STM32L41xxx/42xxx/43xxx/44xxx/45xxx/46xxx devices.

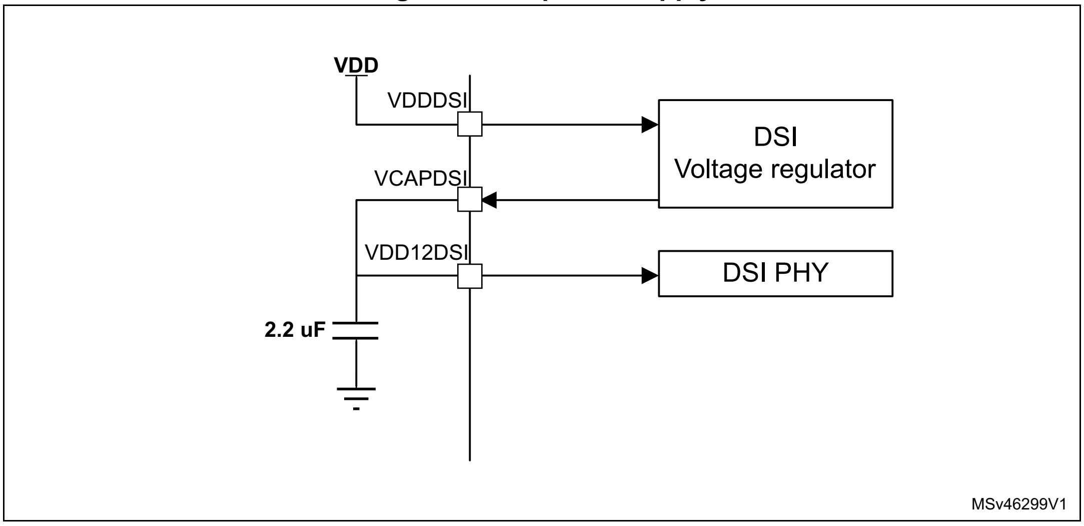
Figure 4. Optional LCD power supply scheme



- **Option 1**: LCD power supply is provided by a dedicated V_{LCD} supply source, V_{SEL} switch is open.
- **Option 2**: LCD power supply is provided by the internal step-up converter, V_{SEL} switch is closed, an external capacitance is needed for correct behavior of this converter.

Note: V_{LCD} is multiplexed on PC3 GPIO that needs to be configured as V_{LCD} alternate function (only available on STM32L496xx/4A6xx/476xx/486xx/433xx/443xx devices).

Figure 5. DSI power supply



Note: V_{DDDSI}, V_{CAPDSI} and $V_{DD12DSI}$ are available only on STM32L4R9xx/4S9xx.

2.3 Power supply sequence between V_{DDA}, V_{DDUSB}, V_{DDIO2}, V_{LCD} and V_{DD}

2.3.1 Power supplies isolation

The STM32L4 Series and STM32L4+ Series features a powerful reset system which ensures that the main power supply (V_{DD}) has reached a valid operating range before releasing the MCU reset. This reset system is also in charge of isolating the independent power domains: V_{DDA}, V_{DDUSB}, V_{DDIO2}, V_{LCD} and V_{DD}. This reset system is supplied by V_{DD} and is not functional before V_{DD} reaches a minimal voltage (1 V in worse case conditions).

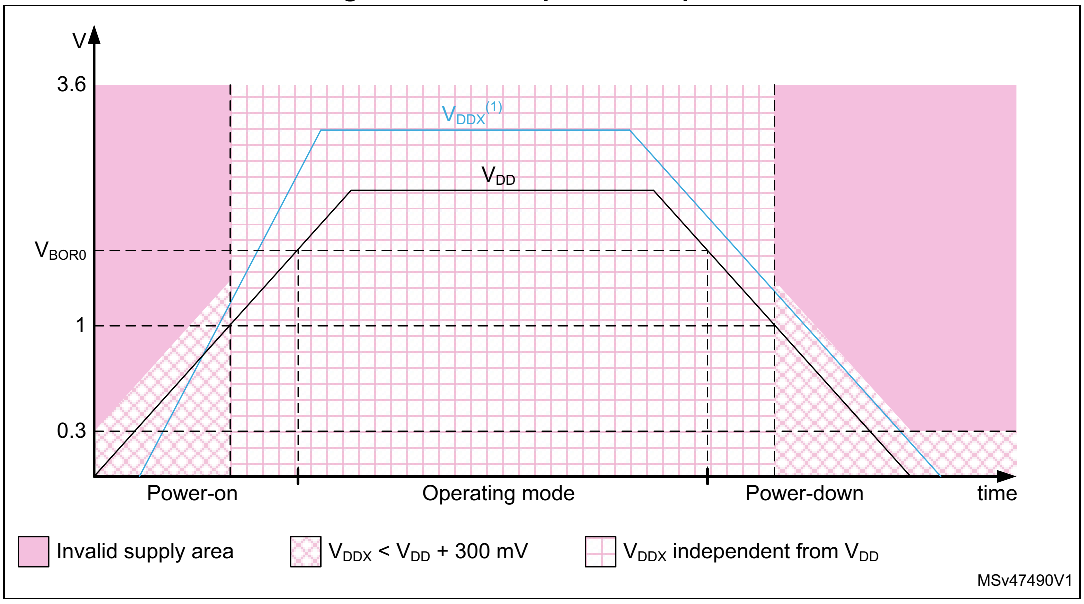
In order to avoid leakage currents between the available supplies and V_{DD} (or ground), V_{DD} must be provided first to the MCU and released last.

2.3.2 General requirements

During power-up and power-down phases, the following power sequence requirements must be respected:

- When V_{DD} is below 1 V, other power supplies (V_{DDA}, V_{DDIO2}, V_{DDUSB} and V_{LCD}) must remain below V_{DD} +300 mV.
- When V_{DD} is above 1 V, all power supplies are independent.

Figure 6. Power-up/down sequence



1. V_{DDX} refers to any power supply among V_{DDA}, V_{DDIO2}, V_{DDUSB} and V_{LCD}.

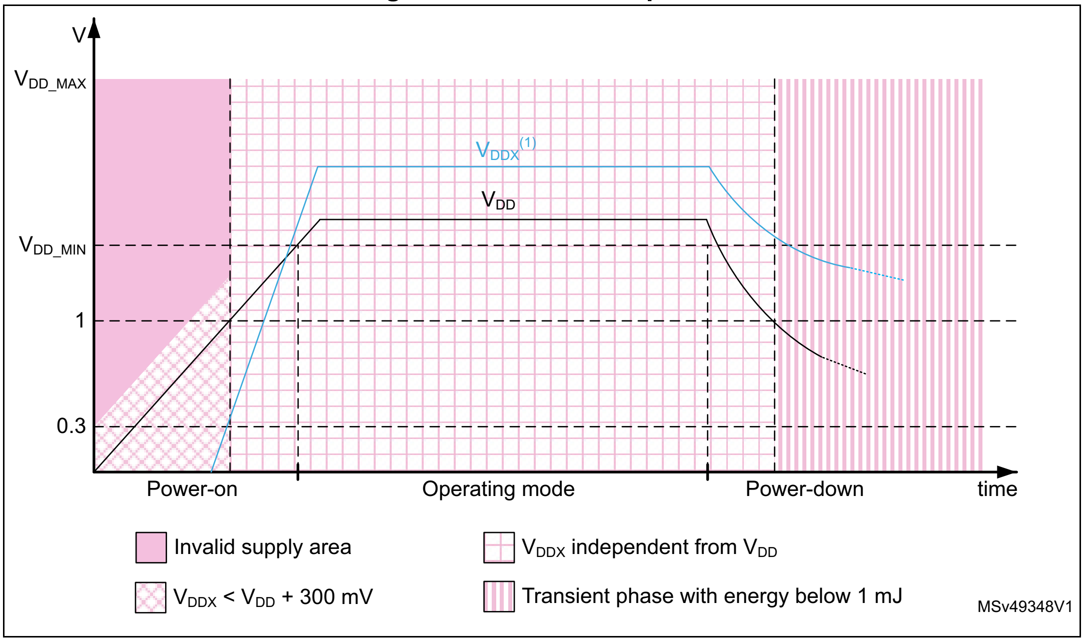
Note: VBAT is an independent supply and has no constraint versus VDD.

Note: All power supply rails can be tied together.

2.3.3 Particular conditions during power-down phase

During the power-down phase, V_{DD} can temporarily become lower than other supplies only if the energy provided to the MCU remains below 1 mJ; this allows external decoupling capacitors to be discharged with different time constants during the power-down transient phase.

Figure 7. Power-down phase



1. V_{DDX} refers to any power supply among V_{DDA}, V_{DDIO2}, V_{DDUSB} and V_{LCD}.

V_{DDX} (V_{DDA}, V_{DDIO2}, V_{DDUSB} and V_{LCD}) power rails must be switched off before V_{DD}. Note that during the power-down transient phase, V_{DDX} can remain temporarily above V_{DD}.

Example of computation of the energy provided to the MCU during the power-down phase:

If the sum of decoupling capacitors on V_{DDX} is 10 µF and V_{DD} drops below 1 V while V_{DDX} is still at 3.3 V, the energy remaining in the decoupling capacitors is:

$$E = ½ C V^2 = ½ \times 10^{-5} \times 3.3^2 = 0.05 \text{ mJ}$$

The energy remaining in the decoupling capacitors is below 1 mJ so it is acceptable for the MCU to absorb it.

2.4 Reset and power supply supervisor

2.4.1 Power-on reset (POR) / power-down reset (PDR) / brown-out reset (BOR)

The device has an integrated power-on reset (POR) / power-down reset (PDR), coupled with a brown-out reset (BOR) circuitry. The BOR is active in all power modes except Shutdown mode, and cannot be disabled.

Five BOR thresholds can be selected through option bytes.

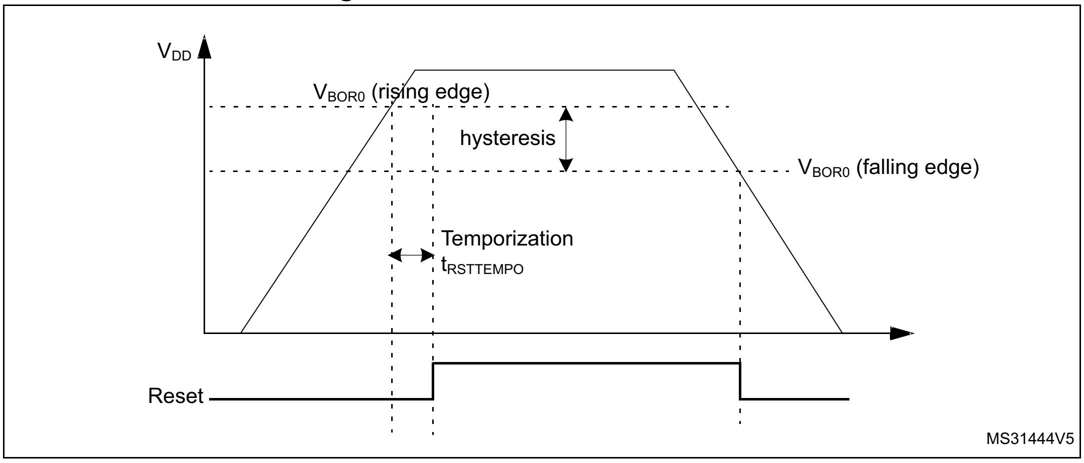
During power-on, the BOR keeps the device under reset until the supply voltage V_{DD} reaches the specified V_{BORx} threshold. When V_{DD} drops below the selected threshold, a device reset is generated. When V_{DD} is above the V_{BORx} upper limit, the device reset is released and the system can start.

On STM32L412xx and STM32L422xx and STM32L4P5xx/STM32L4Q5xx devices, continuous monitoring of the power supply might be changed to periodical sampling to reduce power consumption in Stop2 and Standby modes. This setup can be done by setting ENULP bit in the power control register 3 (PWR_CR3).

Sampling time is controlled by internal temporization, the typical duration is of 12 ms at 25°C; the duration shortens exponentially with an increasing temperature. At around 70°C, the monitoring becomes continuous. When the sampling mode is activated, a fast supply-drop between two samples is not detected. This feature is targeting mainly battery operated devices.

For more details on the brown-out reset thresholds, refer to the electrical characteristics section in the datasheet.

Figure 8. Brown-out reset waveform



2.4.2 Power reset

A power reset is generated when one of the following events occurs:

1. a brown-out reset (BOR).
2. when exiting from Standby or Shutdown mode.

A brown-out reset, including power-on or power-down reset (POR/PDR), sets all registers to their reset values except the backup domain.

When exiting Standby or Shutdown mode, all registers in the V_{CORE} domain are set to their reset value. Registers outside the V_{CORE} domain (RTC, WKUP, IWDG, and Standby/Shutdown modes control) are not impacted.

2.4.3 System reset

A system reset sets all registers to their reset values except the reset flags in the clock control/status register (RCC_CSR) and the registers in the backup domain.

A system reset is generated when one of the following events occurs:

- A low level on the NRST pin (external reset)
- Window watchdog event (WWDG reset)
- Independent watchdog event (IWDG reset)
- A firewall event (FIREWALL reset)
- A software reset (SW reset)
- Low-power management reset
- Option byte loader reset
- A Brown-out reset

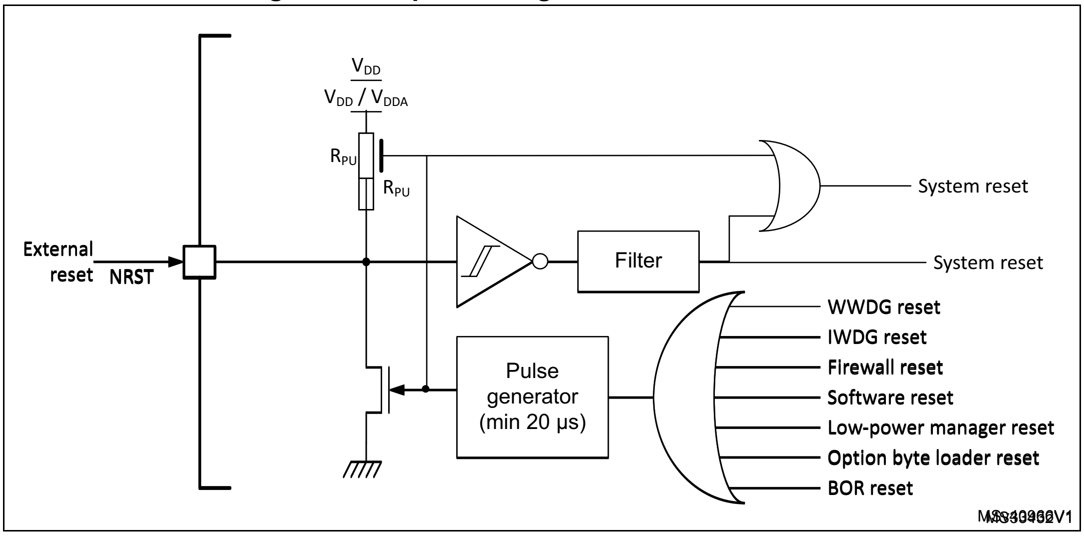
The reset source can be identified by checking the reset flags in the control/status register, RCC_CSR.

These sources act on the NRST pin and it is always kept low during the delay phase. The RESET service routine vector is fixed at address 0x0000_0004 in the memory map.

The system reset signal provided to the device is output on the NRST pin. The pulse generator guarantees a minimum reset pulse duration of 20 µs for each internal reset source. In case of an external reset, the reset pulse is generated while the NRST pin is asserted low.

In case on an internal reset, the internal pull-up R_{PU} is deactivated in order to save the power consumption through the pull-up resistor.

Figure 9. Simplified diagram of the reset circuit



Software reset

The SYSRESETREQ bit in Cortex®-M4 application interrupt and reset control register must be set to force a software reset on the device (as described in *STM32F3, STM32F4, STM32L4 and STM32L4+ Series Cortex®-M4 programming manual* (PM0214)).

Low-power mode security reset

To prevent that critical applications mistakenly enter a low-power mode, two low-power mode security resets are available.

If enabled in option bytes, the resets are generated in the following conditions:

- Entering standby mode: this type of reset is enabled by resetting nRST_STDBY bit in user option bytes. In this case, whenever a standby mode entry sequence is successfully executed, the device is reset instead of entering standby mode.
- Entering stop mode: this type of reset is enabled by resetting nRST_STOP bit in user option bytes. In this case, whenever a stop mode entry sequence is successfully executed, the device is reset instead of entering stop mode.
- Entering shutdown mode: this type of reset is enabled by resetting nRST_SHDW bit in user option bytes. In this case, whenever a shutdown mode entry sequence is successfully executed, the device is reset instead of entering shutdown mode.

For further information on the user option bytes, refer to reference manual *section: Option bytes description*.

Option byte loader reset

The option byte loader reset is generated when the OBL_LAUNCH bit (bit 27) is set in the FLASH_CR register. This bit is used to launch the option byte loading by software.

Charging/discharging the pull-down capacitor through the internal resistor adds to the device power consumption. The recommended value of 100 nF for the capacitor can be reduced to 10 nF to limit power consumption.

2.4.4 Backup domain reset

The backup domain has two specific resets.

A backup domain reset is generated when one of the following events occurs:

1. Software reset, triggered by setting the BDRST bit in the *backup domain control register (RCC_BDCR)*.
2. V_{DD} or V_{BAT} power on, if both supplies have previously been powered off.

A backup domain reset only affects the LSE oscillator, the RTC, the backup registers and the RCC backup domain control register.

3 Packages

3.1 Package selection

Package should be selected by taking into account the constraints that are strongly dependent upon the application.

The list below summarizes the most frequent ones:

- Amount of interfaces required. Some interfaces might not be available on some packages. Some interfaces combinations might not be possible on some packages.
- PCB technology constrains. Small pitch and high ball density could require more PCB layers and higher class PCB.
- Package height.
- PCB available area .
- Noise emission or signal integrity of high speed interfaces.

  Smaller packages usually provide better signal integrity. This is further enhanced as Small pitch and high ball density requires multilayer PCBs which allow better supply/ground distribution.
- Compatibility with other devices.

Table 1. Package summary for STM32L4Rxxx/4Sxxx devices

Package type	LQFP100	UFBGA132	WLCSP144	LQFP144	UFBGA144	UFBGA169
Size (mm)(1)	14 x 14	7 x 7	5.24 x 5.24	20 x 20	10 x 10	7 x 7
Pitch (mm)	0.5	0.5	0.4	0.5	0.8	0.5
Height (mm)(2)	1.6	0.6	0.59	1.6	0.6	0.6

1. Body size, excluding pins for LQFP.
2. Maximum value.

Table 2. Package summary for STM32L49xxx/4Axxx devices

Package type	LQFP64	LQFP100	LQFP144	UFBGA132	UFBGA169	WLCSP100
Size (mm)(1)	10 x 10	14 x 14	20 x 20	7 x 7	7 x 7	4.618 x 4.142
Pitch (mm)	0.5	0.5	0.5	0.5	0.5	0.4
Height (mm)(2)	1.6	1.6	1.6	0.6	0.6	0.405

1. Body size, excluding pins for LQFP.
2. Maximum value.

Table 3. Package summary for STM32L47xxx/48xxx devices

Package type	LQFP64	LQFP100	LQFP144	UFBGA132	UFBGA144	WLCSP81	WLCSP72
Size (mm)(1)	10 x 10	14 x 14	20 x 20	7 x 7	10 x 10	4.4084 x 3.7594	4.4084 x 3.7594
Pitch (mm)	0.5	0.5	0.5	0.5	0.8	0.4	0.4
Height (mm)(2)	1.6	1.6	1.6	0.6	0.6	0.585	0.585

1. Body size, excluding pins for LQFP.
2. Maximum value.

Table 4. Package summary for STM32L45xxx/46xxx devices

Package type	UFQFPN48	LQFP64	LQFP100	UFBGA64	UFBGA100	WLCSP64
Size (mm)(1)	7 x 7	10 x 10	14 x 14	5 x 5	7 x 7	3.357 x 3.657
Pitch (mm)	0.5	0.5	0.5	0.5	0.5	0.35
Height (mm)(2)	0.6	1.6	1.6	0.6	0.6	0.4

1. Body size, excluding pins for LQFP.
2. Maximum value.

Table 5. Package summary for STM32L43xxx/44xxx devices

Package type	UFQFPN32	UFQFPN48	LQFP48	LQFP64	LQFP100	UFBGA64	UFBGA100	WLCSP49	WLCSP64
Size (mm)(1)	5 x 5	7 x 7	7 x 7	10 x 10	14 x 14	5 x 5	7 x 7	3.141 x 3.127	3.141 x 3.127
Pitch (mm)	0.5	0.5	0.5	0.5	0.5	0.5	0.5	0.4	0.35
Height (mm)(2)	0.6	0.6	1.6	1.6	1.6	0.6	0.6	0.585	0.576

1. Body size, excluding pins for LQFP.
2. Maximum value.

Table 6. Package summary for STM32L412xx/422xx devices

Package type	UFQFPN32	UFQFPN48	LQFP32	LQFP48	LQFP64	UFBGA64	WLCSP36
Size (mm)(1)	5 x 5	7 x 7	5 x 5	7 x 7	10 x 10	5 x 5	2.605 x 2.703
Pitch (mm)	0.5	0.5	0.8	0.5	0.5	0.5	0.4
Height (mm)(2)	0.6	0.6	1.6	1.6	1.6	0.6	0.585

1. Body size, excluding pins for LQFP.
2. Maximum value.

Table 7. Package summary for STM32L4P5xx/4Q5xx devices

Package type	UFQFPN48	LQFP48	LQFP64	LQFP100	LQFP144	UFBGA132	UFBGA169	WLCSP100
Size (mm)(1)	7 x 7	7 x 7	10 x 10	14 x 14	20 x 20	7 x 7	5 x 5	4.618 x 4.412
Pitch (mm)	0.5	0.5	0.5	0.5	0.5	0.5	0.5	0.4
Height (mm)(2)	0.6	1.6	1.6	1.6	1.6	0.6	0.6	0.405

1. Body size, excluding pins for LQFP.
2. Maximum value.

3.2 SMPS packages

Some STM32L4 Series and STM32L4+ Series devices offer a package option allowing the connection of an external SMPS.

Such a connection is done through two V_{DD12} pins that are replacing the two existing pins in the baseline package.

For a specific package, the pin to pin compatibility is kept among the various derivatives of STM32L4 Series and STM32L4+ Series.

Note that the pins that are replaced by the two V_{DD12} are different across package types; however, the pins that are replaced in a specific package remain the same within similar packages.

Note that two new bits making SMPS use easier and more efficient were introduced on STM32L412xx and STM32L422xx and STM32L4P5xx/STM32L4Q5xx devices. Bit EXT_SMPS_ON allows operation from 1.00 V connected to VDD12 to improve efficiency and EXT_SMPS_RDY flag indicates status of the regulator to user application.

Refer to the product datasheet for details.

3.3 Pinout compatibility

Table 8 below allows to select the right package depending on required signals.

Table 8. Pinout summary

Pin name	Packages and pin number																		
	UFQFPN		LQFP					UFBGA					WLCSP						
	32	48	32	48	64	100	144	64	100	132	144	169	36	49	64	72	81	100	144
Specific IOs availability																			
PC14/OSC32_IN	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
PC15/OSC32_OUT	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
PH0/OSC_IN	-	x	-	x	x	x	x	x	x	x	x	x	-	x	x	x	x	x	x
PH1/OSC_OUT	-	x	-	x	x	x	x	x	x	x	x	x	-	x	x	x	x	x	x
PC3/VLCD[1]	-	-	-	-	x	x	x	x	x	x	-	x	-	x	x	x	x	x	-
System related pins																			
BOOT0(/PH3)[2]	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
NRST	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
Supplies pins																			
VBAT	-	x	-	x	x	x	x	x	x	x	x	x	-	x	x	x	x	x	x
V_{DDUSB}	-	x	-	x	x	x	x	x	x	x	x	x	-	x	x	x	x	x	x
V_{SSA}	-	x	-	x	x	x	x	x	x	x	x	x	-	x	x	x	x	x	x
V_{REF-}	-	-	-	-	-	x	x	-	x	-	-	-	-	-	-	-	-	x	-
V_{REF+}	-	-	-	-	-	x	x	-	x	x	x	x	x[3]	-	-	x	x	x	x
V_{DDA}	-	x	-	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
V_{DDIO2}	-	-	-	-	-	-	x	-	-	x	x	2	-	-	-	x	x	x	x
V_{DDDSI}[4]	-	-	-	-	-	x	x	-	-	-	-	x	-	-	-	-	-	-	-
$V_{DD12DSI}$[4]	-	-	-	-	-	x	x	-	-	-	-	-	-	-	-	-	-	-	-
V_{CAPDSI}[4]	-	-	-	-	-	x	x	-	-	-	x	x	-	-	-	-	-	-	x
V_{SSDSI}[4]	-	-	-	-	-	x	x	-	-	-	x	x	-	-	-	-	-	-	x
Number of V_{DD}[5]	2	2	2	2	3	5	10/9 (6)	3	5	6	7	11/8 (6)	2	2	3	3	4	6	11/9 (6)
Number of V_{SS}	2	3	2	3	4	5	11/10 (6)	4	5	7	8	12/10 (6)	2	3	4	4	4	5	11/9 (6)

1. VLCD is only available on STM32L496xx/4A6xx/476xx/486xx/433xx/443xx.
2. Pin BOOT0 multiplexed with PH3 on STM32L4+ Series and STM32L4Axxx/49xxx/44xxx/43xxx/42xxx/41xxx devices.
3. On STM32L41xxx and STM32L42xxx devices, VREF+ is only input for the reference. VREFBUF output is not supported.
4. V_{DDDSI}, V_{SSDSI}, $V_{DDA2DSI}$ and V_{CAPDSI} are available only on STM32L4S9xx/4R9xx devices.
5. 1 single tantalum or ceramic capacitor (min. 4.7 uF, typ.10 uF) for the package + one 100 nF ceramic capacitor for each V_{DD} pin.
6. X/Y: X is for all STM32L4 Series and STM32L4+ Series devices and Y is only for STM32L4R9xx/4S9xx and STM32L4P5xx/4Q5xx .

4 Clocks

Four different clock sources can be used to drive the system clock (SYSCLK):

- HSI16 (high speed internal) 16 MHz RC oscillator clock
- MSI (multispeed internal) RC oscillator clock
- HSE oscillator clock, from 4 to 48 MHz
- PLL clock

The MSI is used as system clock source after startup from Reset, configured at 4 MHz.

The devices have the following additional clock sources:

- 32 kHz low speed internal RC (LSI RC) which drives the independent watchdog and optionally the RTC used for Auto-wakeup from Stop and Standby modes.
- 32.768 kHz low speed external crystal (LSE crystal) which optionally drives the real-time clock (RTCCLK).
- RC 48 MHz internal clock sources (HSI48) to potentially drive the USB full speed, the SDMMC and the RNG (not available on STM32L471, STM32L475, STM32L476 and STM32L486 devices).

Each clock source can be switched on or off independently when it is not used, to optimize power consumption.

Several prescalers can be used to configure the AHB frequency, the high speed APB (APB2) and the low speed APB (APB1) domains. The maximum frequency of the AHB, the APB1 and the APB2 domains is 80 MHz and for STM32L4+ Series is 120 MHz.

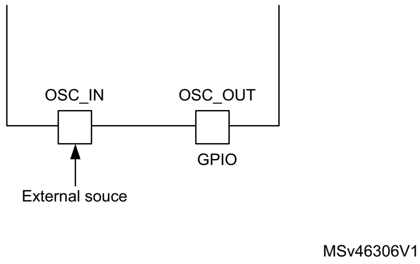
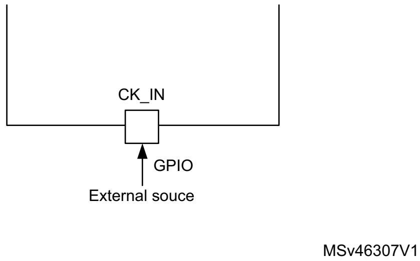
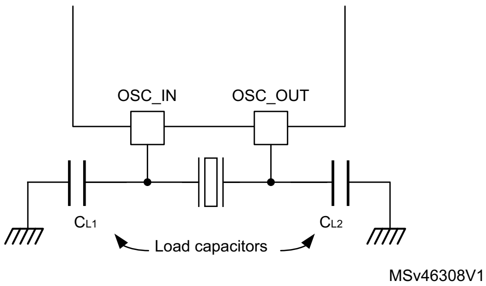
4.1 HSE clock

The high speed external clock signal (HSE) can be generated from two possible clock sources:

- HSE external crystal/ceramic resonator
- HSE user external clock

The resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. The loading capacitance values must be adjusted according to the selected oscillator.

Table 9. HSE/ LSE clock sources

Clock source	Hardware configuration
External clock	
External clock (available on some package, please refer to the corresponding datasheet)	
Crystal/ceramic resonators	

1. The value of R_{EXT} depends on the crystal characteristics. A typical value is in the range of 5 to 6 R_S (resonator series resistance).To fine tune the REXT value, refer to AN2867(Oscillator design guide for ST microcontrollers)
2. Load capacitance, C_L, has the following formula: $C_L = C_{L1} \times C_{L2} / (C_{L1} + C_{L2}) + C_{stray}$ where: C_{stray} is the pin capacitance and board or trace PCB-related capacitance. Typically, it is between 2 pF and 7 pF. Please refer to *Section 7.4: Decoupling* to minimize its value.

4.1.1 External crystal/ceramic resonator (HSE crystal)

The 4- to 48-MHz external oscillator has the advantage of producing a very accurate rate on the main clock.

The associated hardware configuration is shown in *Figure 9*. Refer to the electrical characteristics section of the *datasheet* for more details.

The HSERDY flag in the *clock control register (RCC_CR)* indicates if the HSE oscillator is stable or not. At startup, the clock is not released until this bit is set by hardware. An interrupt can be generated if enabled in the *clock interrupt enable register (RCC_CIER)*.

The HSE crystal can be switched on and off using the HSEON bit in the *clock control register (RCC_CR)*.

4.1.2 External source (HSE bypass)

In this mode, an external clock source must be provided. It can have a frequency of up to 48 MHz. The user selects this mode by setting the HSEBYP and HSEON bits in the *clock control register* (RCC_CR). The external clock signal (square, sinus or triangle) with ~40-60% duty cycle depending on the frequency (refer to the datasheet) has to drive the following pin (see *Figure 9*).

- On devices where OSC_IN and OSC_OUT pins are available: OSC_IN pin must be driven while the OSC_OUT pin can be used as a GPIO.
- Otherwise, the CK_IN pin must be driven.

Note: For details on pin availability, refers to the pinout section in the corresponding device datasheet.

To minimize the consumption, it is recommended to use the square signal.

4.2 HSI16 clock

The HSI16 clock signal is generated from an internal 16 MHz RC oscillator.

The HSI16 RC oscillator has the advantage of providing a clock source at low cost (no external components). It also has a faster startup time than the HSE crystal oscillator however, even with calibration the frequency is less accurate than an external crystal oscillator or ceramic resonator.

The HSI16 signal can also be used as a backup source (auxiliary clock) if the HSE crystal oscillator fails. Refer to reference manual *section: Clock security system (CSS)*.

4.3 MSI clock

The MSI clock signal is generated from an internal RC oscillator. Its frequency range can be adjusted by software by using the MSIRANGE[3:0] bits in the *clock control register (RCC_CR)*. Twelve frequency ranges are available: 100 kHz, 200 kHz, 400 kHz, 800 kHz, 1 MHz, 2 MHz, 4 MHz (default value), 8 MHz, 16 MHz, 24 MHz, 32 MHz and 48 MHz.

The MSI RC oscillator has the advantage of providing a low-cost (no external components) low-power clock source. In addition, when trimmed by the 32.768 kHz external oscillator (LSE), the MSI can provide the USB device with very accurate clock removing the need for an external high speed crystal (HSE).

4.3.1 Hardware auto calibration with LSE (PLL-mode)

When a 32.768 kHz crystal is present in the application, it is possible to configure the MSI in a PLL-mode by setting the MSIPLLEN bit in the *clock control register (RCC_CR)*. When configured in PLL-mode, the MSI automatically calibrates itself thanks to the LSE. This mode is available for all MSI frequency ranges. At 48 MHz, the MSI in PLL-mode can be used for the USB OTG FS device, saving the need of an external high-speed crystal.

For more details on how to calibrate the MSI frequency variation please refer to reference manual *section: Internal/external clock measurement with TIM15/TIM16/TIM17*.

4.4 LSE clock

The LSE crystal is a 32.768 kHz low speed external crystal or ceramic resonator. It has the advantage of providing a low-power but highly accurate clock source to the real-time clock peripheral (RTC) for clock/calendar or other timing functions.

The LSE crystal is switched on and off using the LSEON bit in *backup domain control register (RCC_BDCR)*. The crystal oscillator driving strength can be changed at runtime using the LSEDRV[1:0] bits in the *backup domain control register (RCC_BDCR)* to obtain the best compromise between robustness and short start-up time on one side and low-power-consumption on the other side. The LSE drive can be decreased to the lower drive capability (LSEDRV=00) when the LSE is ON. However, once LSEDRV is selected, the drive capability can not be increased if LSEON=1.

The LSERDY flag in the *backup domain control register (RCC_BDCR)* indicates whether the LSE crystal is stable or not. At startup, the LSE crystal output clock signal is not released until this bit is set by hardware. An interrupt can be generated if enabled in the *clock interrupt enable register (RCC_CIER)*.

On STM32L412xx and STM32L422xx and STM32L4P5xx/STM32L4Q5xx devices, propagation of clock out of RTC structure may be disabled in order to reduce power consumption. Software could disable it by setting bit LSESYSDIS in the RCC_BDCR register. When this bit is set, LSE clock propagation is disabled (even when it is used by any peripheral out of RTC block).

4.4.1 External source (LSE bypass)

In this mode, an external clock source must be provided. It can have a frequency of up to 1 MHz. The user selects this mode by setting the LSEBYP and LSEON bits in the *AHB1 peripheral clocks enable in Sleep and Stop modes register (RCC_AHB1SMENR)*. The external clock signal (square, sinus or triangle) with ~50 % duty cycle has to drive the OSC32_IN pin while the OSC32_OUT pin can be used as GPIO. See *Figure 9*.

5 Boot configuration

5.1 Boot configuration for STM32L47xxx/48xxx devices

In STM32L47xxx/48xxx devices, three different boot modes can be selected through the BOOT0 pin and nBOOT1 bit in the User option byte, as shown in the following table.

Table 10. Boot modes

Boot mode selection		Boot mode	Aliasing
BOOT1(1)	BOOT0		
x	0	Main Flash memory	Main Flash memory is selected as boot space
0	1	System memory	System memory is selected as boot space
1	1	Embedded SRAM1	Embedded SRAM1 is selected as boot space

1. The BOOT1 value is the opposite of the nBOOT1 Option Bit.

The values on both BOOT0 pin and nBOOT1 bit are latched after a reset. It is up to the user to set nBOOT1 and BOOT0 to select the required boot mode.

The BOOT0 pin and nBOOT1 bit are also re-sampled when exiting from Standby mode. Consequently they must be kept in the required Boot mode configuration in Standby mode. After this startup delay has elapsed, the CPU fetches the top-of-stack value from address 0x0000 0000, then starts code execution from the boot memory at 0x0000 0004.

Depending on the selected boot mode, main Flash memory, system memory or SRAM1 is accessible as follows:

- Boot from main Flash memory: the main Flash memory is aliased in the boot memory space (0x0000 0000), but still accessible from its original memory space (0x0800 0000). In other words, the Flash memory contents can be accessed starting from address 0x0000 0000 or 0x0800 0000.
- Boot from system memory: the system memory is aliased in the boot memory space (0x0000 0000), but still accessible from its original memory space (0x1FFF 0000).
- Boot from the embedded SRAM1: the SRAM1 is aliased in the boot memory space (0x0000 0000), but it is still accessible from its original memory space (0x2000 0000).

Note: When the device boots from SRAM, in the application initialization code, the user has to relocate the vector table in SRAM using the NVIC exception table and the offset register.

When booting from the main Flash memory, the application software can either boot from bank 1 or from bank 2. By default, boot from bank 1 is selected.
To select boot from Flash memory bank 2, set the BFB2 bit in the user option bytes. When this bit is set and the boot pins are in the boot from main Flash memory configuration, the device boots from system memory, and the boot loader jumps to execute the user application programmed in Flash memory bank 2. For further details, please refer to AN2606.

Note: When booting from bank 2, in the application initialization code, the user has to relocate the vector table to bank 2 base address. (0x0808 0000) using the NVIC exception table and offset register.

5.1.1 Physical remap

Once the boot pins are selected, the application software can modify the memory accessible in the code area (in this way the code can be executed through the ICode bus in place of the System bus). This modification is performed by programming the *SYSCFG memory remap register (SYSCFG_MEMRMP)* in the SYSCFG controller.

The following memories can thus be remapped:

- Main Flash memory
- System memory
- Embedded SRAM1 (96 Kbytes)
- FSMC bank 1 (NOR/PSRAM 1 and 2)
- Quad SPI memory

Table 11. Memory mapping versus boot mode/physical remap

Addresses	Boot/remap in main Flash memory	Boot/remap in embedded SRAM1	Boot/remap in system memory	Remap in FSMC	Remap in QUADSPI
0x2000 0000 - 0x2001 7FFF	SRAM1	SRAM1	SRAM1	SRAM1	SRAM1
0x1FFF 0000 - 0x1FFF FFFF	System memory/OTP/ Options bytes	System memory/OTP/ Options bytes	System memory/OTP/ Options bytes	System memory/OTP/ Options bytes	System memory/OTP / Options bytes
0x1000 8000 - 0x1FFE FFFF	Reserved	Reserved	Reserved	Reserved	Reserved
0x1000 0000 - 0x1000 7FFF	SRAM2	SRAM2	SRAM2	SRAM2	SRAM2
0x0810 0000 - 0x0FFF FFFF	Reserved	Reserved	Reserved	Reserved	Reserved
0x0800 0000 - 0x080F FFFF	Flash memory	Flash memory	Flash memory	Flash memory	Flash memory
0x0400 0000 - 0x07FF FFFF	Reserved	Reserved	Reserved	FSMC bank 1 NOR/ PSRAM 2 (128 Mbytes) Aliased	QUADSPI bank (128 Mbytes) Aliased
0x0010 0000 - 0x03FF FFFF	Reserved	Reserved	Reserved	FSMC bank 1 NOR/ PSRAM 1 (128 Mbytes) Aliased	QUADSPI bank (128 Mbytes) Aliased
0x0000 0000 - 0x000F FFFF(1)	Flash (1 Mbyte) Aliased	SRAM1 (96 Kbytes) Aliased	System memory (28 Kbytes) Aliased	FSMC bank 1 NOR/ PSRAM 1 (128 Mbytes) Aliased	QUADSPI bank (128 Mbytes) Aliased

1. When the FSMC is remapped at address 0x0000 0000, only the first two regions of bank 1 memory controller (bank 1 NOR/PSRAM 1 and NOR/PSRAM 2) can be remapped. When the QUADSPI is remapped at address 0x0000 0000, only 128 Mbytes are remapped. In remap mode, the CPU can access the external memory via ICode bus instead of system bus which boosts up the performance. Even when aliased in the boot memory space, the related memory is still accessible at its original memory space.

5.1.2 Embedded boot loader

The embedded boot loader is located in the System memory, programmed by ST during production. It is used to reprogram the Flash memory using one of the following serial interfaces:

- USART1 on pins PA9/PA10, USART2 on pins PA2/PA3, USART3 on pins PC10/PC11
- I2C1 on pins PB6/PB7, I2C2 on pins PB10/PB11, I2C3 on pins PC0/PC1
- SPI1 on pins PA4/PA5/PA6/PA7, SPI2 on pins PB12/PB13/PB14/PB15
- USB DFU interface on pins PA11/PA12
- CAN1 on pins PB8/PB9

For details concerning the boot loader serial interface corresponding I/O, refer to the device datasheet.

If the boot loader is used by the application, avoid toggling signals during the boot sequence on pins used by the boot loader. Activity on boot loader output pins may conflict with GPIO configuration; activity on boot loader input pins may be interpreted as a communication start on this interface.

For further details on STM32 boot loader, please refer to AN2606.

5.1.3 BOOT0 pin connection

The BOOT0 pin of the STM32L4 Series has a lower V_{IL} than the other GPIO, (for details see datasheet I/O static characteristics), thus as it does not fit CMOS requirement, when driven by another CMOS circuit the signal level must be verified.

5.2 Boot configuration for STM32L4+ Series and STM32L4Axxx/41xxx/42xxx/43xxx/44xxx/45xxx/46xxx/49xxx devices

In STM32L4+ Series and STM32L4Axxx/41xxx/42xxx/43xxx/44xxx/45xxx/46xxx/49xxx devices, three different boot modes can be selected through the BOOT0 pin or the nBOOT0 bit into the FLASH_OPTR register (if the nSWBOOT0 bit is cleared into the FLASH_OPTR register), and nBOOT1 bit in the FLASH_OPTR register, as shown in the following table:

Table 12. Boot modes

nBOOT1 FLASH_OPTR [23]	nBOOT0 FLASH_OPTR [27]	BOOT0 pin PH3	nSWBOOT0 FLASH_OPTR [26]	Main Flash empty(1)	Boot Memory Space Alias
X	X	0	1	0	Main Flash memory is selected as boot area
X	X	0	1	1	System memory is selected as boot area(2)
X	1	X	0	X	Main Flash memory is selected as boot area(3)
0	X	1	1	X	Embedded SRAM1 is selected as boot area

Table 12. Boot modes (continued)

nBOOT1 FLASH_OPTR [23]	nBOOT0 FLASH_OPTR [27]	BOOT0 pin PH3	nSWBOOT0 FLASH_OPTR [26]	Main Flash empty(1)	Boot Memory Space Alias
0	0	X	0	X	Embedded SRAM1 is selected as boot area
1	X	1	1	X	System memory is selected as boot area
1	0	X	0	X	System memory is selected as boot area

1. On STM32L41xxx/42xxx/43xxx/44xxx/45xxx/46xxx devices a Flash empty check mechanism is implemented to force the boot from system Flash if the first Flash memory location is not programmed (0xFFFF FFFF) and if the boot selection is configured to boot from the main Flash. Refer to *Section 5.2.2: Embedded boot loader* for more details.
2. On STM32L49xxx/4Axxx/4Rxxx/4Sxxx, an empty Flash is also handled by the boot loader. Refer to *Section 5.2.2: Embedded boot loader* for more details.
3. On STM32L49xxx/4Axxx/4Rxxx/4Sxxx, an empty Flash generates a hard fault.

The values on both BOOT0 pin (coming from the pin or the option bit) and nBOOT1 bit are latched upon reset release. It is up to the user to set nBOOT1 and BOOT0 to select the required boot mode.

The BOOT0 pin or user option bit (depending on the nSWBOOT0 bit value in the FLASH_OPTR register), and nBOOT1 bit are also re-sampled when exiting from Standby mode. Consequently they must be kept in the required Boot mode configuration in Standby mode. After this startup delay has elapsed, the CPU fetches the top-of-stack value from address 0x0000 0000, then starts code execution from the boot memory at 0x0000 0004.

Depending on the selected boot mode, main Flash memory, system memory or SRAM1 is accessible as follows:

- Boot from main Flash memory: the main Flash memory is aliased in the boot memory space (0x0000 0000), but still accessible from its original memory space (0x0800 0000). In other words, the Flash memory contents can be accessed starting from address 0x0000 0000 or 0x0800 0000.
- Boot from system memory: the system memory is aliased in the boot memory space (0x0000 0000), but still accessible from its original memory space (0x1FFF 0000).
- Boot from the embedded SRAM1: the SRAM1 is aliased in the boot memory space (0x0000 0000), but it is still accessible from its original memory space (0x2000 0000).

PH3/BOOT0 GPIO is configured in:

- Input mode during the complete reset phase if the option bit nSWBOOT0 is set into the FLASH_OPTR register and then switches automatically in analog mode after reset is released (BOOT0 pin).
- Input mode from the reset phase to the completion of the option byte loading if the bit nSWBOOT0 is cleared into the FLASH_OPTR register (BOOT0 value coming from the option bit). It switches then automatically to the analog mode even if the reset phase is not complete.

Note: *When the device boots from SRAM, in the application initialization code, the user has to relocate the vector table in SRAM using the NVIC exception table and the offset register.*

5.2.1 Physical remap

Once the boot mode is selected, the application software can modify the memory accessible in the code area (in this way the code can be executed through the ICode bus in place of the System bus). This modification is performed by programming the SYSCFG memory remap register (SYSCFG_MEMRMP) in the SYSCFG controller.

The following memories can thus be remapped:

- Main Flash memory
- System memory
- Embedded SRAM1 (256 Kbytes for STM32L49xxx/4Axxx, 128 Kbytes for STM32L45xxx/46xxx, 48 Kbytes for STM32L43xxx/44xxx, 32 Kbytes for STM32L41xxx/42xxx, 192 Kbytes for STM32L4Rxxx/4Sxxx and 128 Kbytes for STM32L4P5xx/4Q5xx)
- FSMC bank 1 (NOR/PSRAM 1 and 2) (for STM32L4+ Series and STM32L49xxx/4Axxx devices only)
- Quad-SPI memory (not available on STM32L4+ Series)
- Octo-SPI (OCTOSPI1 or OCTOSPI2) memory (available only on STM32L4+ Series).

Table 13. Memory mapping vs. Boot mode/Physical remap for STM32L4 Series

Addresses	Boot/remap in main Flash memory	Boot/remap in embedded SRAM1	Boot/remap in System memory	Remap in QUADSPI
0x2000 0000 - 0x2000 BFFF	SRAM1	SRAM1	SRAM1	SRAM1
0x1FFF 0000 - 0x1FFF FFFF	System memory/ OTP/ Options bytes	System memory/ OTP/ Options bytes	System memory/ OTP/ Options bytes	System memory/ OTP/ Options bytes
0x1000 4000 - 0x1FFE FFFF	Reserved	Reserved	Reserved	Reserved
0x1000 0000 - 0x1000 3FFF	SRAM2	SRAM2	SRAM2	SRAM2
0x0804 0000 - 0x0FFF FFFF	Reserved	Reserved	Reserved	Reserved
0x0800 0000 - 0x0803 FFFF	Flash memory	Flash memory	Flash memory	Flash memory
0x0400 0000 - 0x07FF FFFF	Reserved	Reserved	Reserved	QUADSPI bank (128 Mbytes) Aliased
0x0010 0000 - 0x03FF FFFF	Reserved	Reserved	Reserved	QUADSPI bank (128 Mbytes) Aliased
0x0000 0000 - 0x000F FFFF(1)	Flash (256 Kbytes) Aliased	SRAM1 (256 Kbytes STM32L49xxx/4Axxx, 128 Kbytes STM32L45xxx/46xxx, 48 Kbytes STM32L43xxx/44xxx, 32 Kbytes STM32L41xxx/42xxx) Aliased	System memory (28 Kbytes) Aliased	QUADSPI bank (128 Mbytes) Aliased

1. When the QUADSPI is remapped at address 0x0000 0000, only 128 Mbytes are remapped. In remap mode, the CPU can access the external memory via ICode bus instead of System bus which boosts up the performance.

   Even when aliased in the boot memory space, the related memory is still accessible at its original memory space.

Table 14. Memory mapping versus Boot mode/Physical remap for STM32L4+ Series

Addresses	Boot/Remap in main Flash memory	Boot/Remap in embedded SRAM1	Boot/Remap in System memory	Remap in FSMC	Remap in OCTOSPI
0x2000 0000 - 0x2002 FFFF	SRAM1	SRAM1	SRAM1	SRAM1	SRAM1
0x1FFF 7000 - 0x1FFF FFFF	System memory/OTP/ Options bytes	System memory/OTP/ Options bytes	System memory/OTP/ Options bytes	System memory/OTP/ Options bytes	System memory/OTP/ Options bytes
0x1000 8000 - 0x1FFE FFFF	Reserved	Reserved	Reserved	Reserved	Reserved
0x1000 0000 - 0x1000 FFFF	SRAM2	SRAM2	SRAM2	SRAM2	SRAM2
0x0820 0000 - 0x0FFF FFFF	Reserved	Reserved	Reserved	Reserved	Reserved
0x0800 0000 - 0x081F FFFF	Flash memory	Flash memory	Flash memory	Flash memory	Flash memory
0x0400 0000 - 0x07FF FFFF	Reserved	Reserved	Reserved	FSMC bank 1 NOR/ PSRAM 2 (128 Mbytes) Aliased	OCTOSPI bank (128 Mbytes) Aliased
0x0010 0000 - 0x03FF FFFF	Reserved	Reserved	Reserved	FSMC bank 1 NOR/ PSRAM 2 (128 Mbytes) Aliased	OCTOSPI bank (128 Mbytes) Aliased
0x0000 0000 - 0x001F FFFF(1) (2)	Flash (2 Mbytes)(3) Aliased	SRAM1 (192 Kbytes)(4) Aliased	System memory (28 Kbytes) Aliased	FSMC bank 1 NOR/ PSRAM 2 (128 Mbytes) Aliased	OCTOSPI bank (128 Mbytes) Aliased

1. When the FSMC is remapped at address 0x0000 0000, only the first two regions of bank 1 memory controller (bank 1 NOR/PSRAM 1 and NOR/PSRAM 2) can be remapped. When the OCTOSPI is remapped at address 0x0000 0000, only 128 Mbytes are remapped. In remap mode, the CPU can access the external memory via ICode bus instead of system bus, which boosts up the performance.
2. Even when aliased in the boot memory space, the related memory is still accessible at its original memory space.
3. 2 Mbytes for STM32L4Rxxx and STM32L4Sxxx devices and 1 Mbytes for STM32L4P5xx and STM32L4Q5xx devices.
4. 192 Kbytes for STM32L4Rxxx and STM32L4Sxxx devices and 128 Kbytes for STM32L4P5xx and STM32L4Q5xx devices.

5.2.2 Embedded boot loader

The embedded boot loader is located in the System memory and programmed by ST during production. It is used to reprogram the Flash memory using one of the following serial interfaces:

- USART1 on pins PA9/PA10, USART2 on pins PA2/PA3, USART3 on pins PC10/PC11
- I2C1 on pins PB6/PB7, I2C2 on pins PB10/PB11, I2C3 on pins PC0/PC1
- I2C4 on pins PD12/PD13 (STM32L4+ Series and STM32L49xxx/4Axxx/45xxx/46xxx devices only)
- SPI1 on pins PA4/PA5/PA6/PA7, SPI2 on pins PB12/PB13/PB14/PB15
- USB DFU interface on pins PA11/PA12
- CAN1 on pins PB8/PB9 (except on STM32L41xxx/42xxx devices)
- CAN2 on pins PB5/PB6 (STM32L49xxx/4Axxx devices only)

For details concerning the boot loader serial interface corresponding I/O, refer to the device's datasheet.

If the boot loader is used by the application or if the device boots on the main Flash while it is still empty, avoid toggling signals during the boot sequence on pins used by the boot loader. Activity on boot loader output pins may conflict with GPIO configuration; activity on boot loader input pins may be interpreted as a communication start on this interface.

For further details on STM32 boot loader, please refer to AN2606.

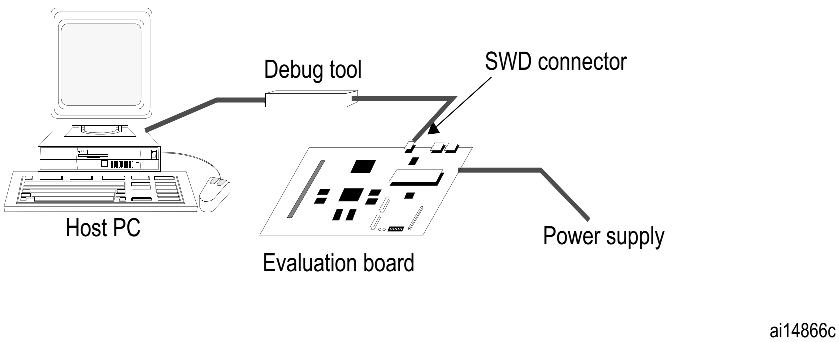
6 Debug management

In the SWJ-DP, the two JTAG pins of the SW-DP are multiplexed with some of the five JTAG pins of the JTAG-DP.

The host/target interface is the hardware equipment that connects the host to the application board. This interface is made of three components: a hardware debug tool, a SW connector and a cable connecting the host to the debug tool.

Figure 10 shows the connection of the host to a development board.

Figure 10. Host-to-board connection



The Nucleo demonstration board embeds the debug tools (ST-LINK) so it can be directly connected to the PC through an USB cable. The ST-LINK requires by default to have an enumeration with a host that is able to supply 100 mA to power the STM32L4/STM32L4+ MCU, hence user shall use jumper JP1 on the Nucleo board which can be set in case maximum current consumption on U5V does not exceed 100 mA.

6.1 SWJ debug port (JTAG and serial wire)

The STM32L4 Series and STM32L4+ Series core integrates the serial wire / JTAG debug port (SWJ-DP). It is an ARM® standard CoreSight™ debug port that combines a JTAG-DP (5-pin) interface and a SW-DP (2-pin) interface.

- The JTAG debug port (JTAG-DP) provides a 5-pin standard JTAG interface to the AHP-AP port
- The serial wire debug port (SW-DP) provides a 2-pin (clock + data) interface to the AHP-AP port

6.2 Pinout and debug port pins

The STM32L4 Series and STM32L4+ Series devices are offered in various packages with different numbers of available pins. As a result, some functionality related to the pin availability may differ from one package to another.

6.2.1 SWJ debug port pins

Five pins are used as outputs for the SWJ-DP as *alternate functions* of general-purpose I/Os (GPIOs). These pins, shown in *Table 15*, are available on all packages.

Table 15. Debug port pin assignment

SWJ-DP pin name	JTAG debug port		SW debug port		Pin assignment
	Type	Description	Type	Debug assignment	
JTMS/SWDIO	I	JTAG test mode selection	I/O	Serial wire data input/output	PA13
JTCK/SWCLK	I	JTAG test clock	I	Serial wire clock	PA14
JTDI	I	JTAG test data input	-	-	PA15
JTDO/TRACESWO	O	JTAG test data output	-	TRACESWO if async trace is enabled	PB3
JNTRST	I	JTAG test nReset	-	-	PB4

6.2.2 Flexible SWJ-DP pin assignment

After reset (SYSRESETn or PORESETn), all five pins used for the SWJ-DP are assigned as dedicated pins which are immediately usable by the debugger host (note that the trace outputs are not assigned except if explicitly programmed by the debugger host).

However, the STM32L4 Series and STM32L4+ Series devices implement a register to disable all or part of the SWJ-DP port, and so releases the associated pins for general-purpose I/O usage. This register is mapped on an APB bridge connected to the Cortex®-M4 system bus. It is programmed by the user software program and not by the debugger host.

Table 16 shows the different possibilities for releasing some pins. For more details, see the related STM32L4 Series and STM32L4+ Series reference manual.

Table 16. SWJ I/O pin availability

Available debug ports	SWJ I/O pin assigned				
	PA13 / JTMS/ SWDIO	PA14 / JTCK/ SWCLK	PA15 / JTDI	PB3 / JTDO	PB4/ JNTRST
Full SWJ (JTAG-DP + SW-DP) - reset state	X	X	X	X	X
Full SWJ (JTAG-DP + SW-DP) but without JNTRST	X	X	X	X	-
JTAG-DP disabled and SW-DP enabled	X	X	-		
JTAG-DP disabled and SW-DP disabled	Released				

6.2.3 Internal pull-up and pull-down resistors on JTAG pins

The JTAG input pins must *not* be floating since they are directly connected to flip-flops which control the debug mode features. Special care must be taken with the SWCLK/TCK pin that is directly connected to the clock of some of these flip-flops.

To avoid any uncontrolled I/O levels, the STM32L4 Series embeds internal pull-up and pull-down resistors on the JTAG input pins:

- JNTRST: internal pull-up
- JTDI: internal pull-up
- JTMS/SWDIO: internal pull-up
- TCK/SWCLK: internal pull-down

Once a JTAG I/O is released by the user software, the GPIO controller takes control again. The reset states of the GPIO control registers put the I/Os in the following equivalent states:

- JNTRST: input pull-up
- JTDI: input pull-up
- JTMS/SWDIO: input pull-up
- JTCK/SWCLK: input pull-down
- JTDO: input floating

The software can then use these I/Os as standard GPIOs.

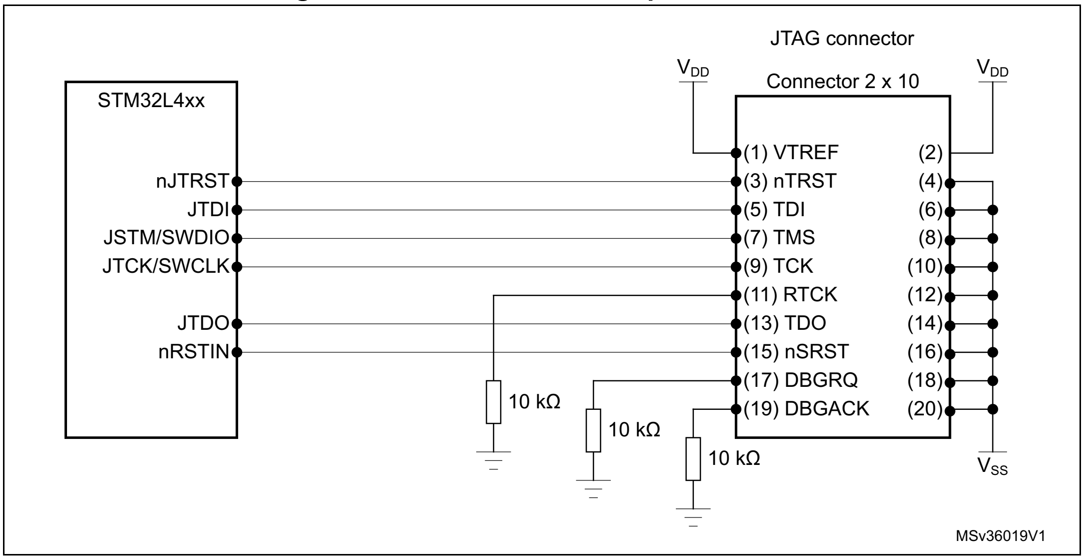
Note: *The JTAG IEEE standard recommends to add pull-up resistors on TDI, TMS and nTRST but, there is no special recommendation for TCK. However, for the STM32L4 Series and the STM32L4+ Series, an integrated pull-down resistor is used for JTCK.*

Having embedded pull-up and pull-down resistors removes the need to add external resistors.

6.2.4 SWJ debug port connection with standard JTAG connector

Figure 11 shows the connection between the STM32L4 Series / STM32L4+ Series devices and a standard JTAG connector.

Figure 11. JTAG connector implementation



6.3 Serial wire debug (SWD) pin assignment

The same SWD pin assignment is available on all STM32L4 Series and STM32L4+ Series packages.

Table 17. SWD port pins

SWD pin name	SWD port		Pin assignment
	Type	Debug assignment	
SWDIO	I/O	Serial wire data input/output	PA13
SWCLK	I	Serial wire clock	PA14

6.3.1 SWD pin assignment

After reset (SYSRESETn or PORESETn), the pins used for the SWD are assigned as dedicated pins which are immediately usable by the debugger host.

However, the MCU offers the possibility to disable the SWD, therefore releasing the associated pins for general-purpose I/O (GPIO) usage. For more details on how to disable SWD port, refer to the I/O pin alternate function multiplexer and mapping section of the related STM32L4 Series and STM32L4+ Series reference manual.

6.3.2 Internal pull-up and pull-down on SWD pins

Once the SWD I/O is released by the user software, the GPIO controller takes control of these pins. The reset states of the GPIO control registers put the I/Os in the equivalent states:

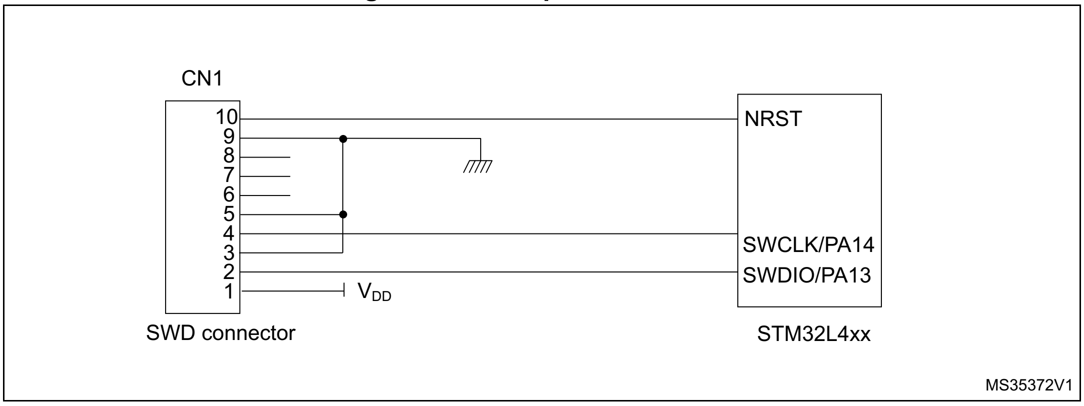
- SWDIO: alternate function pull-up
- SWCLK: alternate function pull-down

Having embedded pull-up and pull-down resistors removes the need to add external resistors.

6.3.3 SWD port connection with standard SWD connector

Figure 12 shows the connection between the STM32L4 Series / STM32L4+ Series and a standard SWD connector.

Figure 12. SWD port connection



7 Recommendations

7.1 Printed circuit board

For technical reasons, it is best to use a multilayer printed circuit board (PCB) with a separate layer dedicated to ground (V_{SS}) and another dedicated to the V_{DD} supply. This provides good decoupling and a good shielding effect. For many applications, economical reasons prohibit the use of this type of board. In this case, the major requirement is to ensure a good structure for ground and for the power supply.

7.2 Component position

A preliminary layout of the PCB must separate circuits into different blocks:

- High-current circuits
- Low-voltage circuits
- Digital component circuits
- Circuits separated according to their EMI contribution in order to reduce noise due to cross-coupling on the PBC.

7.3 Ground and power supply (V_{SS}, V_{DD}, V_{SSA}, V_{DDA}, V_{DDUSB}, V_{DDIO2}, V_{DDDSI})

Respect the following rules related to grounding:

- Ground every block (noisy, low-level sensitive, digital or others) individually
- Return all grounds to a single point
- Avoid loops (or ensure they have a minimum area)

In order to improve analog performance, the user must use separate supply sources for V_{DD} and V_{DDA}, and place the decoupling capacitors as close as possible to the device.

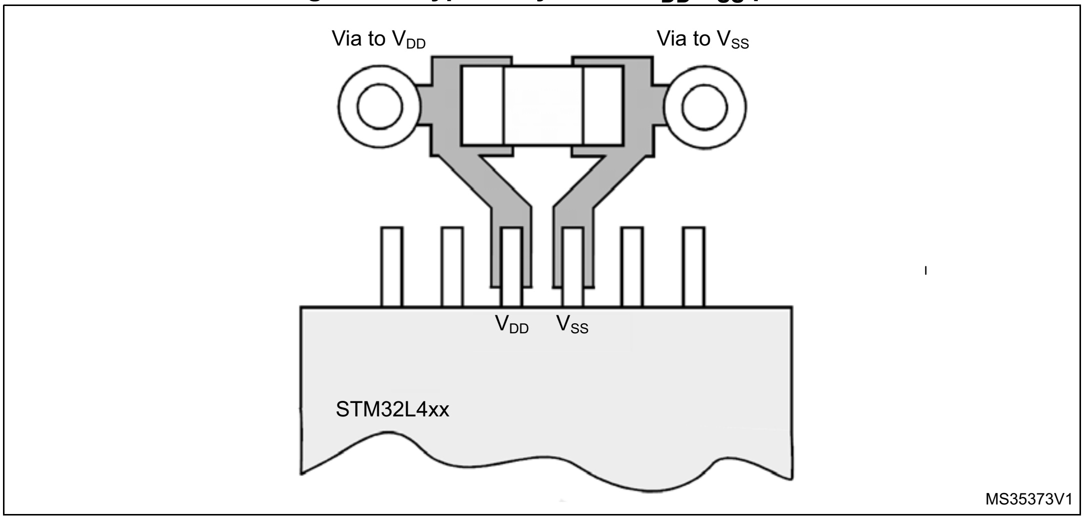
The power supplies should be implemented close to the ground line to minimize the area of the supplies loop. This is due to the fact that the supply loop acts as an antenna, and acts as the main transmitter and receiver of EMI. All component-free PCB areas must be filled with additional grounding to create a kind of shielding (especially when using single-layer PCBs).

7.4 Decoupling

All power supply and ground pins must be properly connected to the power supplies. These connections (including pads, tracks and vias) must have an impedance as low as possible. This is typically achieved with thick track widths and, preferably, the use of dedicated power supply planes in multilayer PCBs.

In addition, each power supply pair should be decoupled with filtering ceramic capacitors (100 nF) and a Tantalum or ceramic capacitor of about 10 µF connected in parallel on the STM32L4/STM32L4+ Series devices. Some package use a common V_{SS} for several V_{DD} instead of a pair of power supply (one V_{SS} for each V_{DD}), in that case the capacitors must be between each V_{DD} and the common V_{SS}.These capacitors need to be placed as close as possible to, or below, the appropriate pins on the underside of the PCB. Typical values are 10 nF to 100 nF, but exact values depend on the application needs. *Figure 13* shows the typical layout of such a V_{DD}/V_{SS} pair.

Figure 13. Typical layout for V_{DD}/V_{SS} pair



7.5 Other signals

When designing an application, the EMC performance can be improved by closely studying the following:

- Signals for which a temporary disturbance affects the running process permanently (which is the case for interrupts and handshaking strobe signals but, not the case for LED commands).
  For these signals, a surrounding ground trace, shorter lengths, and the absence of noisy and sensitive traces nearby (crosstalk effect) improve EMC performance.
  For digital signals, the best possible electrical margin must be reached for the two logical states and slow Schmitt triggers are recommended to eliminate parasitic states.
- Noisy signals (example, clock)
- Sensitive signals (example, high impedance)

7.6 Unused I/Os and features

All microcontrollers are designed for a variety of applications and often a particular application does not use 100% of the MCU resources.

To increase EMC performance and avoid extra power consumption, the unused features of the device should be disabled and disconnected from the clock tree. The unused clock source should be disabled and the unused I/Os should not be left floating. The unused I/O pins should be configured as analog input by software; they should also be connected to a fixed logic level 0 or 1 by an external or internal pull-up or pull-down or configured as output mode using software.

8 Reference design

8.1 Description

The reference design shown in *Figure 14*, is based on the STM32L4 Series / STM32L4+ Series LQFP144.

This reference design can be tailored to any STM32L4 Series or STM32L4+ Series device with a different package, using the pin correspondence given in *Table 20*.

8.1.1 Clock

Two clock sources are used for the microcontroller:

- LSE: X2– 32.768 kHz crystal for the embedded RTC
- HSE: X1– 8 MHz crystal for the STM32L4 Series microcontroller

Refer to *Section 4*.

8.1.2 Reset

The reset signal in *Figure 14* is active low. The reset sources include:

- Reset button (B1)
- Debugging tools via the connector CN1

Refer to *Section 2.4*.

8.1.3 Boot mode

The boot option is configured by setting switches SW1 (Boot 0). Refer to *Section 5*.

Note: When waking up from Standby mode, the Boot pin is sampled. In this situation, the user needs to pay attention to its value.

8.1.4 SWD interface

The reference design shows the connection between the STM32L4 Series / STM32L4+ Series and a standard SWD connector. Refer to *Section 6*.

Note: It is recommended to connect the reset pins so as to be able to reset the application from the tools.

8.1.5 Power supply

Refer to *Section 2*.

8.2 Component references

Table 18. Mandatory components

Reference	Component name	Value	Quantity	Comments
U1A	Microcontroller	STM32L4/STM32L4+ LQFP144	1	144-pin package
C8, C11, C13	Capacitor	100 nF	10 + 2	Ceramic capacitors (decoupling capacitors)
C9, C10	Capacitor	4.7 µF	1	Tantalum / chemical / ceramic capacitor (decoupling capacitor)
C12	Capacitor	1 µF	1	Ceramic capacitor (LCD booster) only needed if LCD is used
C6, C16	Capacitor	1 µF	3	Ceramic capacitor (decoupling capacitor)
C14, C15	Capacitor	1 µF	1	Ceramic capacitor (decoupling capacitor) used for internal voltage reference buffer

Table 19. Optional components

Reference	Component name	Value	Quantity	Comments
R1	Resistor	390 Ω	1	Used for HSE: the value depends on the crystal characteristics, refer to application note AN2687
R3, R4, R5	Resistor	10 kΩ	3	Used for ST Link interface
C5	Capacitor	100 nF	1	Ceramic capacitor
C7	Capacitor	10 nF	1	Ceramic capacitor
C1, C2	Capacitor	6.8 pF	2	Used for LSE: the value depends on the crystal characteristics. Fits for MC-306 32.768K-E3, which has a load capacitance of 6 pF.
C3, C4	Capacitor	20 pF	2	Used for HSE: the value depends on the crystal characteristics, refer to application note AN2687
X1	Quartz	8 MHz	1	Used for HSE
X2	Quartz	32.764 kHz	1	Used for LSE
SW1	Switch	-	1	Used to select the right boot mode
B1	Push-button	-	1	-
L1	Ferrite bead	-	1	For EMC reduction on V_{DDA} supply, can be replaced by a direct connection between V_{DD} and V_{DDA}

Figure 14. Reference design STM32L4 Series / STM32L4+ Series

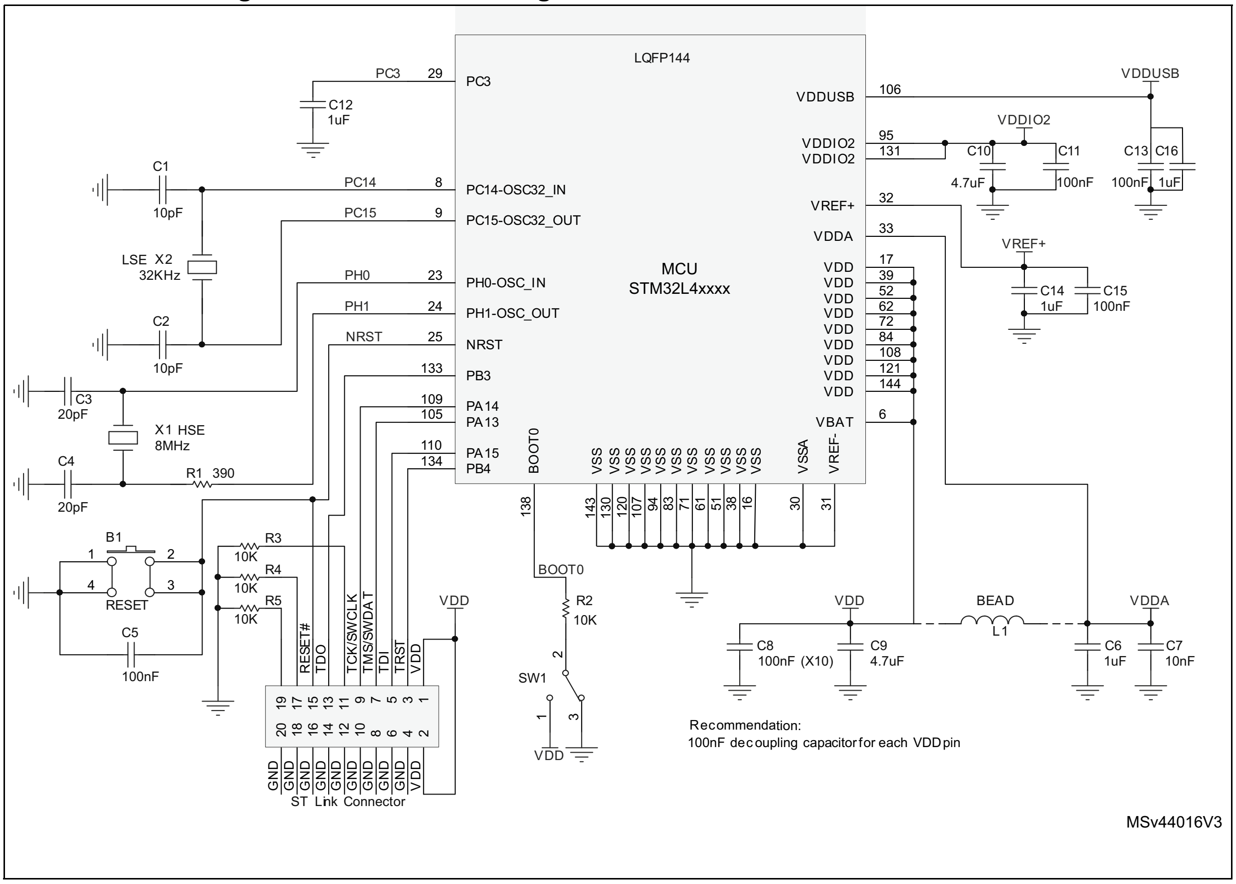


Table 20. Reference connection for all packages(1)

Pin Name	Pin Number per Package																
	UFQFPN		LQFP					UFBGA				WLCSP					
	32	48	32	48	64	100	144	64	100	132	169	36	49	64	72	81	100	144
Specific IOs availability																		
PC14/ OSC32_IN	2	3	2	3	3	8	8	A1	D1	D1	F1	B6	C7	C8	C9	C9	D10	E11
PC15/ OSC32_OUT	3	4	3	4	4	9	9	B1	E1	E1	G1	C6	C6	C7	C8	C8	E10	E12
PH0/OSC_IN	-	5	-	5	5	12	23	C1	F1	F1	H1	-	D7	D8	D9	D9	F10	H12
PH1/ OSC_OUT	-	6	-	6	6	13	24	D1	G1	G1	J1	-	D6	D7	D8	D8	G10	J12
PC3/VLCD(2)	-	-	-	-	11	18	29	G1	K2	K2	K1	-	E6	E6	G7	G7	F7	J10
System related pins																		
BOOT0 (/PH3)(3)	31	44	31	44	60	94	138	B4	A4	A4	E5	C5	A5	C5	D7	D7	E6	B9
NRST	4	7	4	7	7	14	25	E1	H2	H2	H3	D6	D5	25	E9	E9	E8	H11

Table 20. Reference connection for all packages(1) (continued)

Pin Name	Pin Number per Package																	
	UFQFPN		LQFP					UFBGA				WLCSP						
	32	48	32	48	64	100	144	64	100	132	169	36	49	64	72	81	100	144
Debug pin																		
PA13 (JTMS-SWDIO)	23	34	23	34	46	72	105	A8	A11	A11	A11	B2	B2	C2	C2	C2	C2	B3
PA14 (JTCK-SWCLK)	24	37	24	37	49	76	109	A7	A10	A10	A10	A2	A2	B2	B2	B2	B2	A2
Supply pins																		
VBAT	-	1	-	1	1	6	6	B2	E2	E2	E2	-	B6	x	B9	B9	C10	E10
VDDUSB	-	36	-	36	48	73	106	E5	C11	C11	E12	-	A1	A1	A1	A1	A1	B2
VSSA	-	8	-	8	12	19	30	F1	J1	J1	K2	-	E7	F8	G9	G9	H9	K11
VREF-	-		-			20	31		K1			-					G8	
VREF+	-	9	-	9	13	21	32	H1	L1	L1	L1	E6 (4)	F7	G8	G8	G8	G7	L11
VDDA	-		-			22	33		M1	M1	L2	F6			H9	H9	J10	L12
VDDIO2	-	-	-	-	-	-	131 95	-	-	G7	B6	-	-	-	B6	B6	A6	A8
VDD	2	2	2	2	19, 32, 64	11, 28, 50, 75, 100	17, 39, 52, 62, 72, 84, 108, 121, 144	3	5	C4, G2, G6, G11, G12, H3	A3, A8, C1, C13, G2, G13, H13, L12, N3, N7, N11	A6, E1	2	3	J8, J1, A9	J8, J1, A9, E4	A4, A10, E9, F1, J8, K1	A6, B1, B12, G2, G12, L7, M1, M2, M11
VSS	2	3	2	3	18, 31, 47, 63	10, 27, 49, 74, 99	16, 38, 51, 61, 71, 83, 94, 107, 120, 130, 143	4	5	D3, E3, F2, F6, F7, F11, F12	A7, B3, C2, C12, F2, F13, H2, H12, L13, M3, M7, M11	A5, F1	3	4	J9, J2, B1, A8	J9, J2, B1, A8	A9, B1, D9, K2, K10	A1, A12, B6, D12, G1, G11, K3, L3, M3, M12

1. This table is not applicable for STM32L4R9xx/4S9xx as they are not compatible with STM32L4 Series.
2. PC3/VLCD not applicable on devices without LCD feature.
3. Pin BOOT0 multiplexed with PH3 on STM32L4Axxx/41xxx/42xxx/43xxx/44xxx/45xxx/46xxx/49xxx devices.

4. On STM32L41xxx and STM32L42xxx devices, VREF+ is only input for the reference. VREFBUF output is not supported.

9 Revision history

Table 21. Document revision history

Date	Revision	Changes
16-Jul-2015	1	Initial release.
05-Jan-2016	2	*Section 4.2: HSI16 clock* updated: Stop 0 mode added. *Section 4.3: MSI clock* updated: Stop 0 mode added.
07-Mar-2016	3	Updated document with Category 2 and 4 for STM32L4 Series.
31-Jan-2017	4	Replaced Cat. 1, Cat. 2, Cat. 3 and Cat. 4 categories by the corresponding product references throughout the document. Updated BGA169 and WLCSP100 ball numbers in *Table 20*. *Section 4.3: MSI clock* updated for LSE trimming description. SMPS usage description added to *Section 2.1*, to *Section 2.1.7* and to *Section 2.2*. *Figure 1: Power supply overview: STM32L4 Series* and *Figure 3: Power supply scheme* updated for SMPS.
04-Sep-2017	5	The whole document was updated to add STM32L4+ Series information. Updated *Table 9: HSE/ LSE clock sources* (from figure to table) Added: – *Table 1: Package summary for STM32L4Rxxx/4Sxxx devices* – *Table 14: Memory mapping versus Boot mode/Physical remap for STM32L4+ Series* – *Figure 2: Power supply overview: STM32L4+ Series* – *Figure 5: DSI power supply* – *Section 2.1.5: Independent DSI supply*

Table 21. Document revision history (continued)

Date	Revision	Changes
14-May-2018	6	Added: – Section 1: General information – Section 2.3: Power supply sequence between V_{DDA}, V_{DDUSB}, V_{DDIO2}, V_{LCD} and V_{DD} – Figure 6: Power-up/down sequence – Figure 7: Power-down phase – Footnotes 2 and 3 on Table 12: Boot modes – Updated: – Section 2.1: Power supplies – Section 2.1.1: Independent analog peripherals supply – Section 2.1.3: Independent USB transceivers supply – Section 2.1.4: Independent LCD supply – Section 2.1.7: Voltage regulator – Section 2.1.8: Dynamic voltage scaling management – Section 2.2: Power supply schemes – Section 3.2: SMPS packages – Section 4: Clocks – Section 5.1.2: Embedded boot loader – Section 5.2: Boot configuration for STM32L4+ Series and STM32L4Axxx/41xxx/42xxx/43xxx/44xxx/45xxx/46xxx/49xxx devices – Section 5.2.2: Embedded boot loader – Section 7.2: Component position – Section 7.3: Ground and power supply (V_{SS}, V_{DD}, V_{SSA}, V_{DDA}, V_{DDUSB}, V_{DDIO2}, V_{DDDSI}) – Section 7.4: Decoupling – Figure 2: Power supply overview: STM32L4+ Series – Figure 3: Power supply scheme – Table 3: Package summary for STM32L47xxx/48xxx devices – Footnotes on Table 8: Pinout summary – Table 11: Memory mapping versus boot mode/physical remap was moved from Section 5.1.2: Embedded boot loader to Section 5.1.1: Physical remap – Footnote 1 on Table 12: Boot modes

Table 21. Document revision history (continued)

Date	Revision	Changes
16-Aug-2018	7	Updated all document to include information concerning STM32L41xxx/42xxx devices impacting: – Content on *Section 2.1: Power supplies*, *Section 2.4.1: Power-on reset (POR) / power-down reset (PDR) / brown-out reset (BOR)*, *Table 8: Pinout summary*, *Section 3.2: SMPS packages*, *Section 4.4: LSE clock*, *Section 5.2: Boot configuration for STM32L4+ Series and STM32L4Axxx/41xxx/42xxx/43xxx/44xxx/45xxx/46xxx/49xxx devices*, *Section 5.2.1: Physical remap*, *Table 13: Memory mapping vs. Boot mode/Physical remap for STM32L4 Series*, *Section 5.2.2: Embedded boot loader*, *Table 20: Reference connection for all packages* – Footnotes on *Figure 1: Power supply overview: STM32L4 Series* and *Table 12: Boot modes* – Note on *Section 2.1.2: Independent I/O supply rail* – Added *Table 6: Package summary for STM32L412xx/422xx devices*
13-Dec-2019	8	Updated: – *Section 2.1: Power supplies*, *Section 2.1.5: Independent DSI supply*, *Section 2.1.6: Battery backup domain*, *Section 2.1.7: Voltage regulator*, *Section 2.1.8: Dynamic voltage scaling management*, *Section 2.4.1: Power-on reset (POR) / power-down reset (PDR) / brown-out reset (BOR)*, *Section 2.4.3: System reset*, *Section 4.4: LSE clock*, *Section 6.2.1: SWJ debug port pins*, *Section 6: Debug management*, *Section 7.4: Decoupling*, – *Figure 8: Brown-out reset waveform*, *Figure 9: Simplified diagram of the reset circuit* – *Table 8: Pinout summary*, *Table 14: Memory mapping versus Boot mode/Physical remap for STM32L4+ Series*, *Table 18: Mandatory components*, *Table 20: Reference connection for all packages* Added: – *Table 7: Package summary for STM32L4P5xx/4Q5xx devices*
02-Nov-2022	9	Updated *Section 2.1: Power supplies* Added missing information *Section 2.2: Power supply schemes* Updated *Figure 14* Updated cross-references *Chapter 8*