AN4625
Application note

STEVAL-IFP023V1 evaluation board for CLT01-38S4 input termination

Introduction

The CLT01-38S4 is an 8-channel industrial protected current limiter and a serializer for interfacing automation digital inputs. It meets type 1, 2 and 3 input characteristics in accordance with the IEC 61131-2, programmable controller international standard.

It integrates the SPI serializer, which is important for applications with high channel counts. The serial communication allows the number of lines to be reduced which, in most applications, need to be galvanically isolated. Furthermore, its structure allows the transfer of the data and the additional information including thermal alarm, undervoltage indication and checksum bits.

The device optimizes input VI characteristic shape to reduce power dissipation. This becomes critical when the application enclosure requires higher protection levels with closed cabinets. The power dissipated inside the module is very limited, no air circulation is present inside the box. Current limitation also reduces power losses on the sensor side.

LED drivers, providing input states and using current from sensors, are energy-less.

5 V regulator is included to drive opto-coupler when galvanic isolation is needed.

Another important parameter is the electrical protection and susceptibility of the application. The CLT01-38S4 implements large protection diodes on each input and supply voltage line.

Thanks to its compact package, the CLT01-38S4 is smaller, in terms of PCB area, than a discrete solution.

Contents

1 Description

The STEVAL-IFP023V1 evaluation board (*Figure 1*) allows designers to evaluate the CLT01-38S4 device behavior in industrial conditions. The board accommodates two CLT01-38S4 chips connected to the SPI bus in a daisy chain configuration. It offers a 16-bit digital input interface and indicates each sensor logic state with the LED.

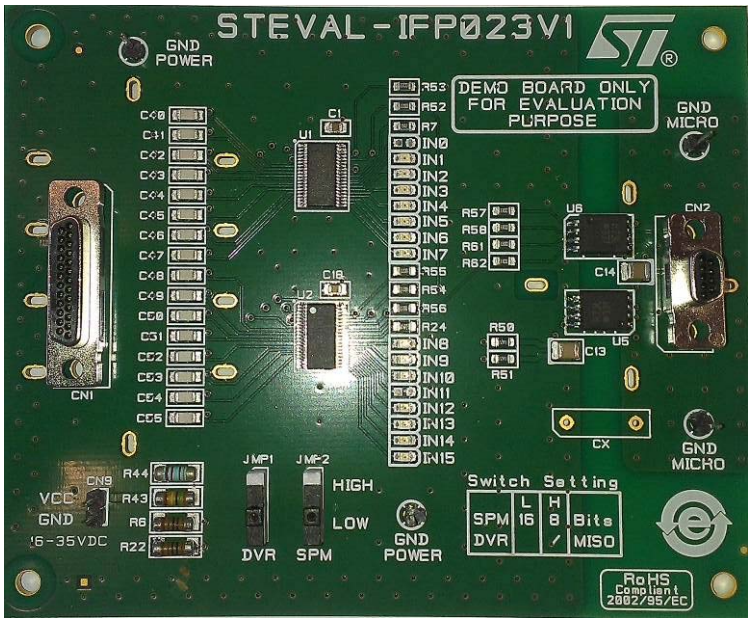
Features:

- 8/16 input channel topology (CLT01-38S4 chip / STEVAL-IFP023V1 board)
- Fully integrated current limiter
- Termination for IEC 61131-2 type 1 and 3 inputs
- SPI communication peripheral working at high frequency
- Voltage regulator integrated on the chip
- Thermal / voltage alarms and checksum
- Wide range supply voltage operation

Benefits:

- Low power dissipation compared to discrete solutions
- Small external component count
- Overvoltage protection
- ESD in accordance with IEC 61000-4-2, class 4, 15 kV air discharge, 8 kV contact discharge
- Excellent EMC immunity
  - High energy surge (IEC 61000-4-5), 2 kV / criteria “B” without any external protection
  - Fast transient burst (IEC 61000-4-4), +-3 kV criteria “A”
  - RF amplitude modulation (IEC 61000-4-6), 150 kHz - 80 MHz, 3 V / criteria “A”
- Cost-effective isolation thanks to SPI bus
- Overall dissipation reduced
- Compact HTSSOP-38 package

Figure 1. STEVAL-IFP023V1 evaluation board



2 The CLT01-38S4 presentation

Typical applications for the CLT01-38S4 include PLCs (programmable logic controllers), PACs (programmable automation controllers), distributed I/O systems, etc. The device works as a serializer for mechanical switches, relay contacts and two-wire or three-wire digital sensors (also known as proximity switches). Protected digital input characteristics are in accordance with type 1, 2 and 3 of the IEC 61131-2 (programmable controller international standard).

Available in 8-channel configuration, it offers a high-density termination by minimizing the external component count. It is housed in HTSSOP-38 surface mount package to reduce the printed circuit board size.

The CLT01-38S4 features are: eight parallel voltage protected inputs, a current limiting circuit that regulates the channel current and feeds the indicator LEDs, a voltage regulator and the SPI communication peripheral.

The CLT01-38S4 device is connected between sensors and microcontroller, FPGA or ASIC. Current limiting circuit is compensated over the entire temperature range. Thanks to its low tolerance, current limitation allows drastic reduction of power dissipation in comparison with a resistive input (discrete solution); the overall module requires less cooling capability and is smaller than a discrete solution.

Thanks to the integrated SPI communication, the CLT01-38S4 reduces number of lines that typically need to be galvanically isolated, making the application more cost-effective. In a 16-bit input interface, conventional solutions require 16 isolators to isolate the control part from the industrial environment. With the CLT01-38S4, the two-chip solution (16-bit interface) connected in a daisy chain configuration requires 3 isolators only. In addition to input data, it also provides device status information including thermal alarm and undervoltage indication. Control bits for higher reliability can also be included in the frame extension.

The CLT01-38S4 device block diagram and recommended application diagram are shown in *Figure 2* and *Figure 3*.

Figure 2. CLT01-38S4 block diagram

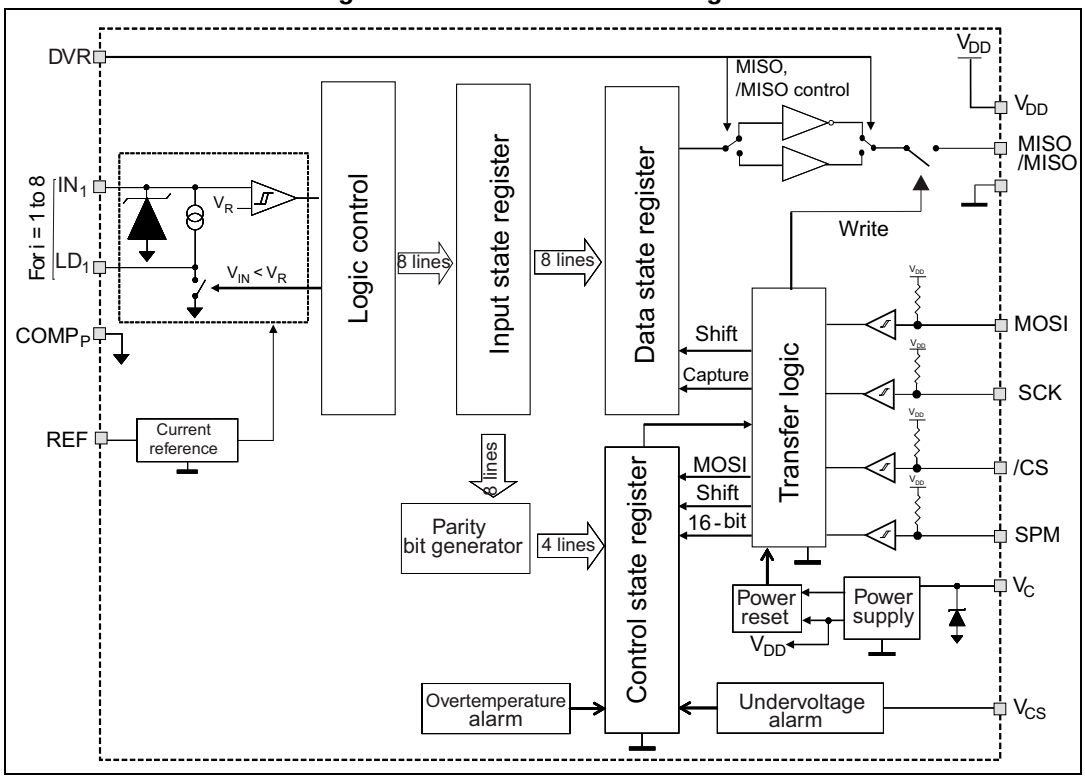
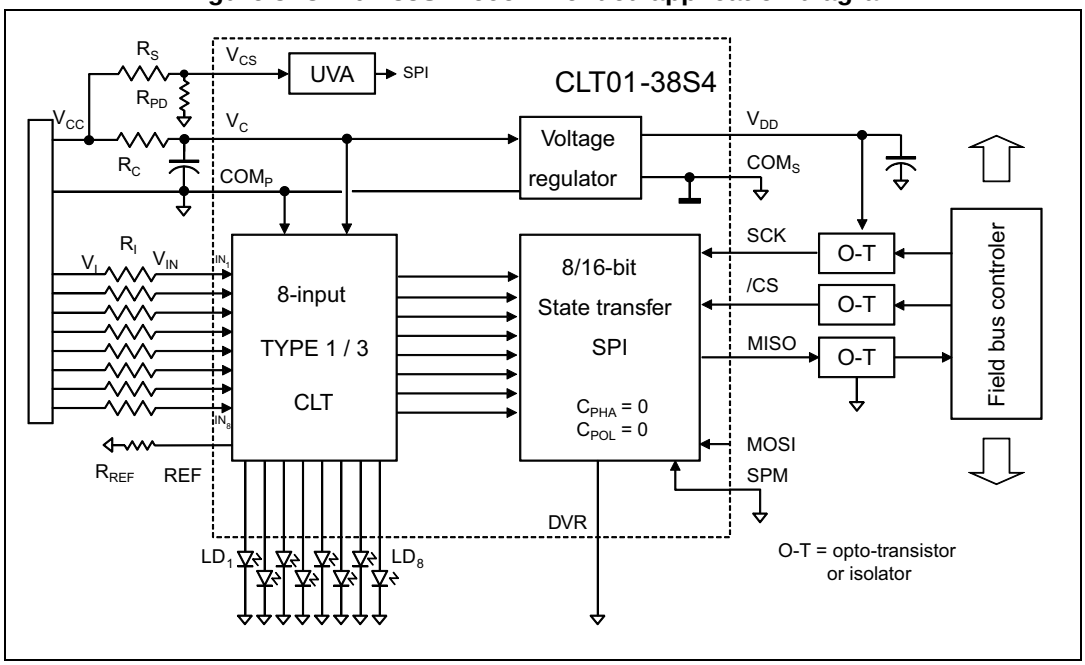


Figure 3. CLT01-38S4 recommended application diagram



3 STEVAL-IFP023V1 evaluation board

The STEVAL-IFP023V1 evaluation board schematic is showed in *Figure 4*, bill of material is available in *Table 1* and PBC layouts are listed from *Figure 5* to *Figure 10*.

Figure 4. STEVAL-IFP023V1 schematic

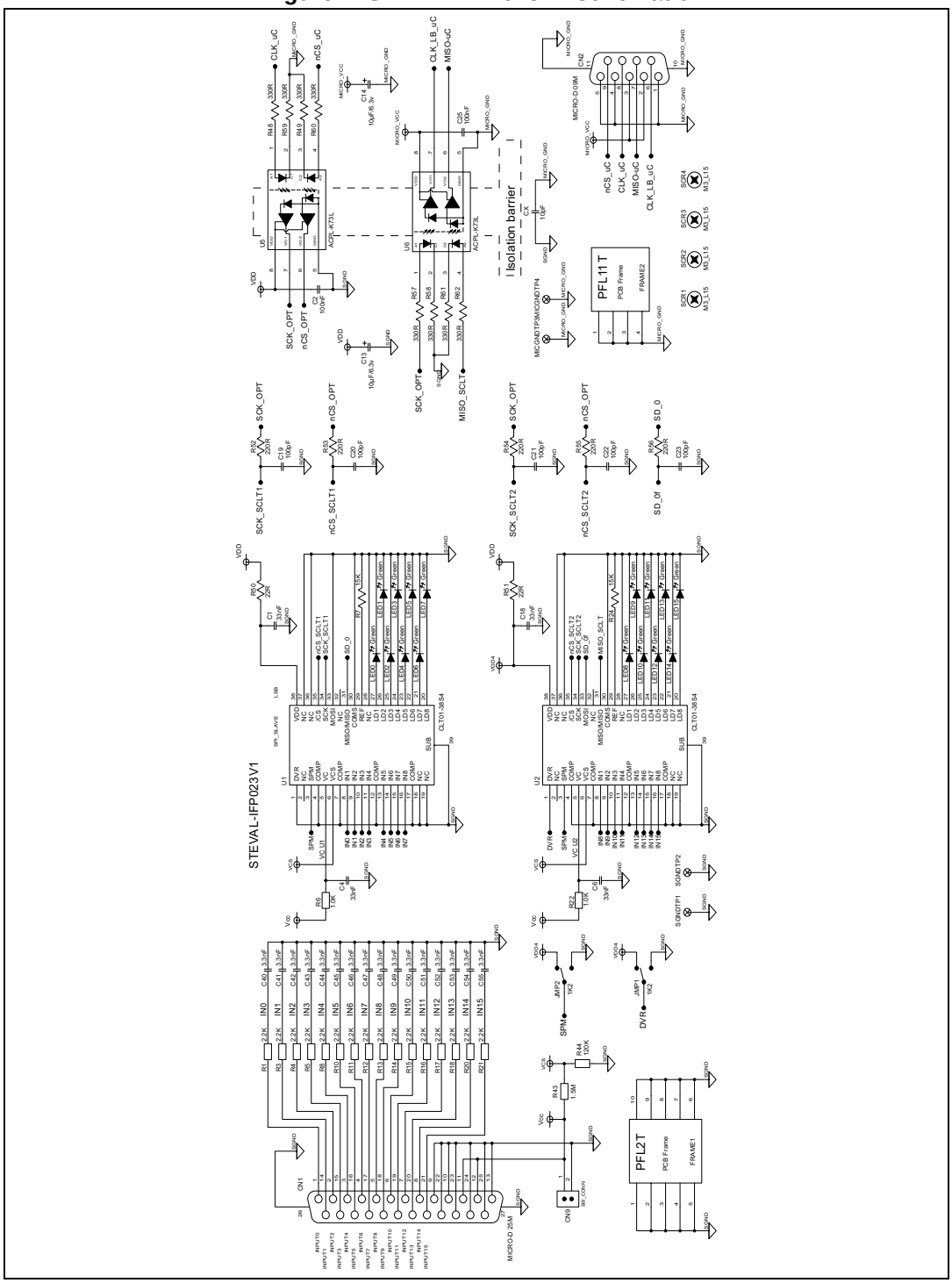


Table 1. STEVAL-IFP023V1 bill of material

Designator	Value	Package / footprint	Manufacturer / order code	Quantity
R1,R3, R5, R8, R10, R18, R20, R21	Resistor 2.2 kΩ 1% 0.4 W MELF MMB0207	SMD MELF 0207	Vishay BEYSCHLAG MMB02070C22	16
R6,R22	Resistor 1.0 kΩ 1% 0.4 W MELF MMB0207	SMD MELF 0207	Vishay BEYSCHLAG MMB02070C10	2
R7,R24	Resistor 15 kΩ 1% 0805	SMD 0805	Any	2
R43	Resistor 1.5 MΩ 1% 0.4 W MELF MMB0207	SMD MELF 0207	Vishay BEYSCHLAG MMB02070C15	1
R44	Resistor 120 kΩ 1% 0.4 W MELF MMB0207	SMD MELF 0207	Vishay BEYSCHLAG MMB02070C12	1
R48,R49,R57,R58R59,R60,R61,R62	Resistor 330 Ω 1% 0805	SMD 0805	Any	8
R50,R51	Resistor 22 Ω 1% 0805	SMD 0805	Any	2
R52,R53,R54,R55,R56	Resistor 220 Ω 1% 0805	SMD 0805	Any	5
SGNDTP1-2, MICGNDTP3-4,	Test-point	Through hole	Terminal assembly 1.02 mm	4
CN1	MICRO-D plug straight THT 25	MICRO D-sub connector male 25P	NORCOMP 380-025-113L001	1
CN2	MICRO-D plus straight THT 9	MICRO D-sub connector male 09P	NORCOMP 380-009-113L001	1
CN9	Strip line male single row 2.54 mm	Through hole	Any	1
LED0, LED15	LED SMD 0805 green	SMD 0805	Any	16
U1, U2	CLT01-38S4	HTSSOP38	ST	2
U5, U6	ACPL-K73L	SO8-wide	AVAGO technologies	2
C1,C4,C6,C18	Capacitor 33 nF/50 V 0805	SMD 0805	Any	4
C2,C25	Capacitor 100 nF/50 V 0805	SMD 0805	Any	2
C19,C20,C21,C22,C23	Capacitor 100 pF/50 V 0805	SMD 0805	Any	5
C13,C14	Capacitor tantalium 10 µF/6.3 V	SMD 1210	Any	2

Table 1. STEVAL-IFP023V1 bill of material (continued)

Designator	Value	Package / footprint	Manufacturer / order code	Quantity
C40, C55	Capacitor 3.3 nF/50 V 5% 1206	SMD 1206	Any	16
JMP1, JMP2	PCB switch 1K2 straight black	Through hole	EAO: ref 09-03290.01	2
SCR1, SCR4	Screw M3		Any	4
Frame1	PCB frame PFL2T	55x30x16 mm	PERANCEA	1
Frame2	PCB frame PFL11T	30x30x11 mm	PERANCEA	1
25 poles micro-D female (assembled) to blunt cut cable			NORCOMP	1
9 poles micro-D female (assembled) to blunt cut cable			NORCOMP	1

3.1 PCB layer set

The following figures show layers and silkscreen layouts.

Figure 5. Top layer PCB layout

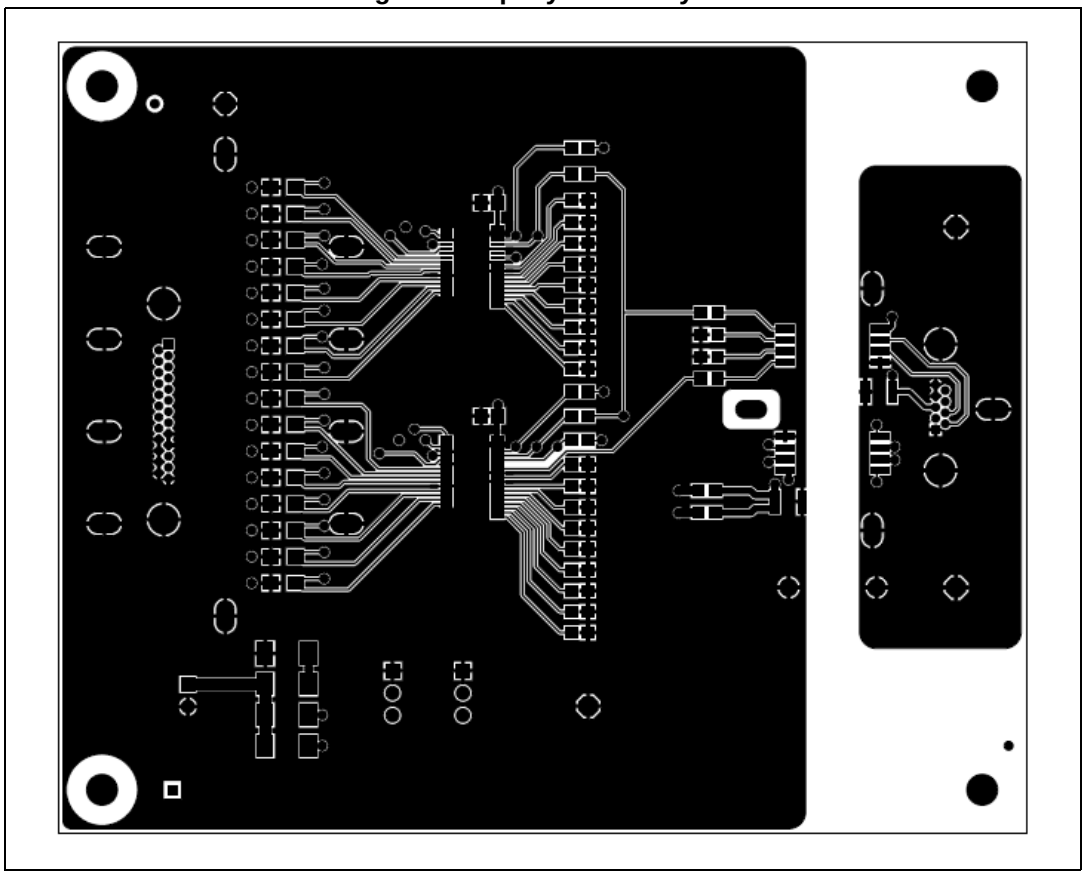


Figure 6. Top inner PCB layout

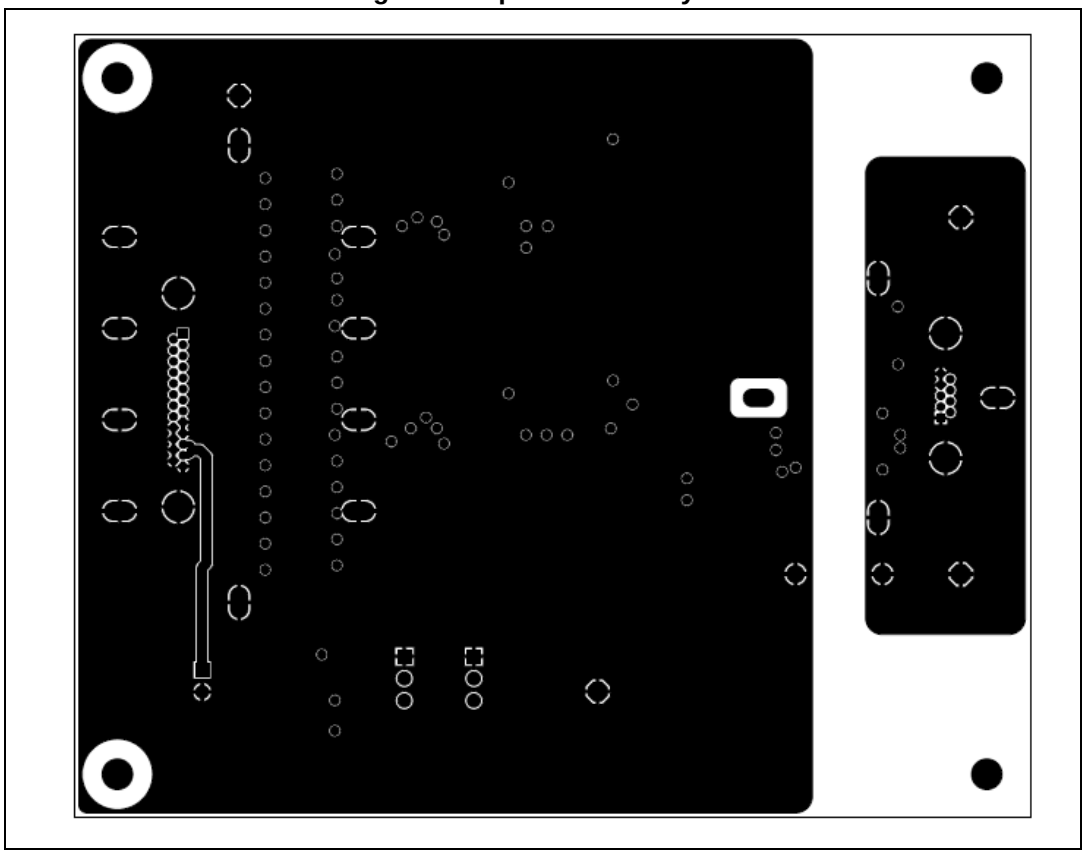


Figure 7. Bottom inner PCB layout

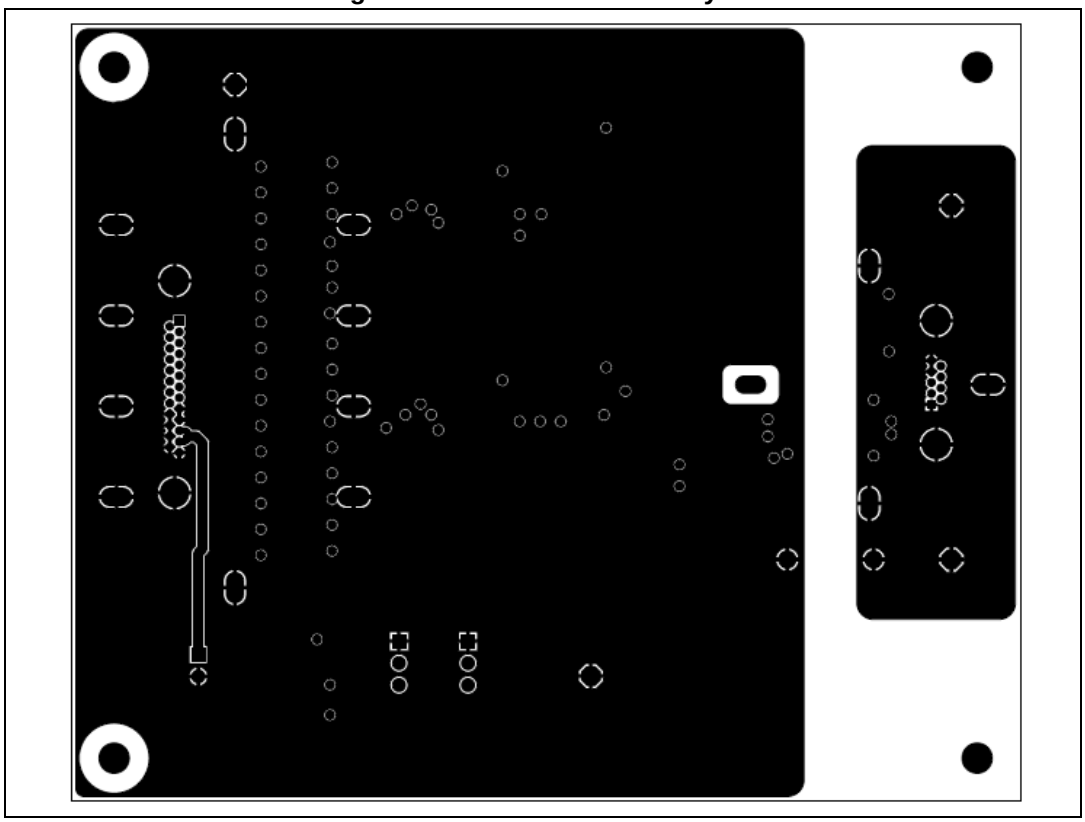


Figure 8. Bottom layer PCB layout

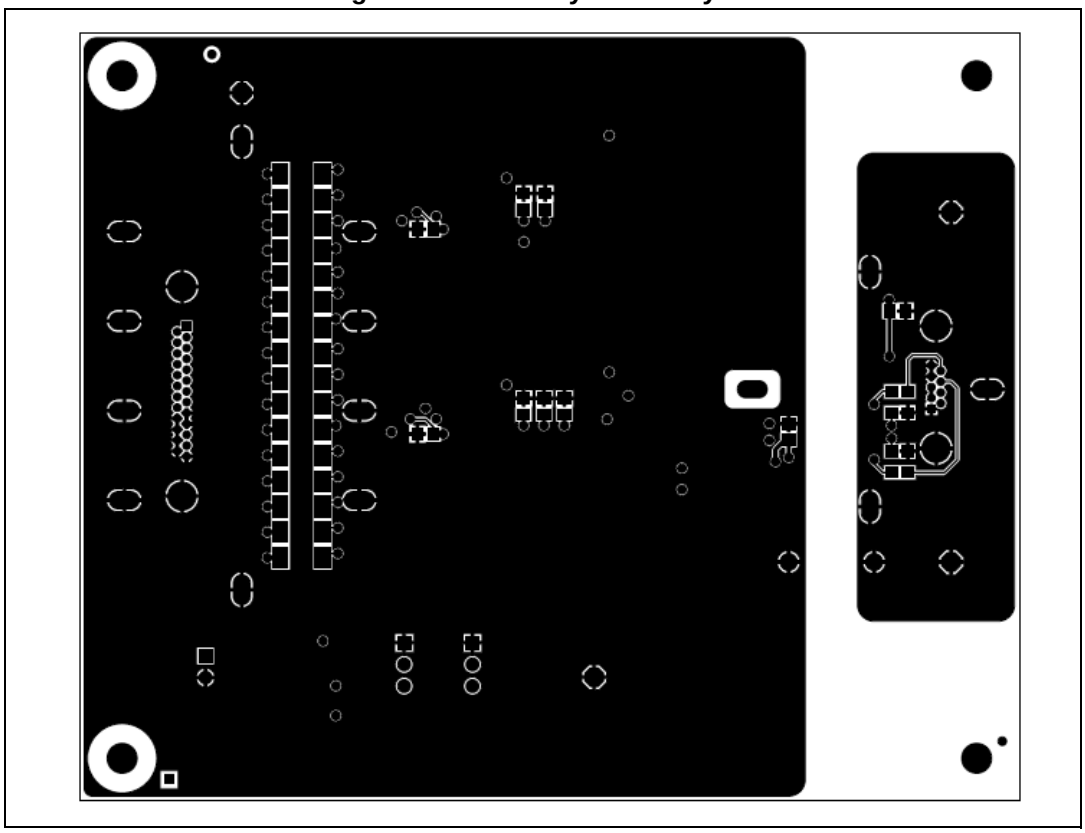


Figure 9. Top silk PCB layout

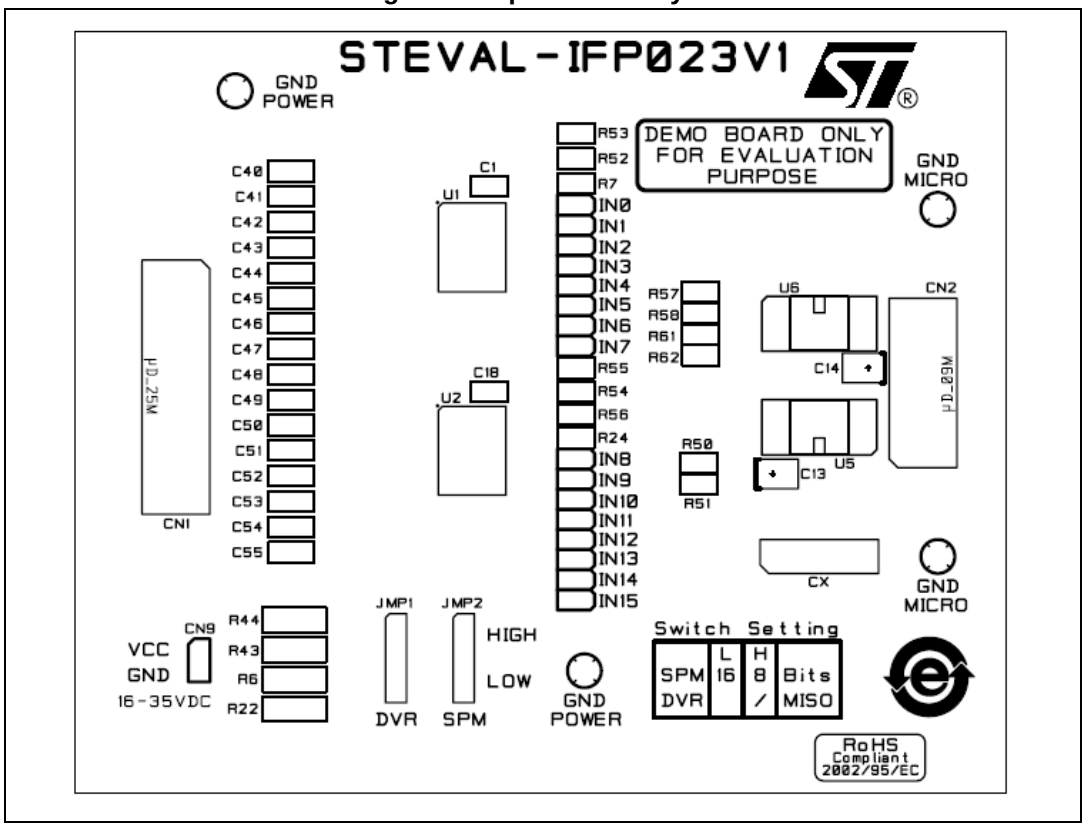
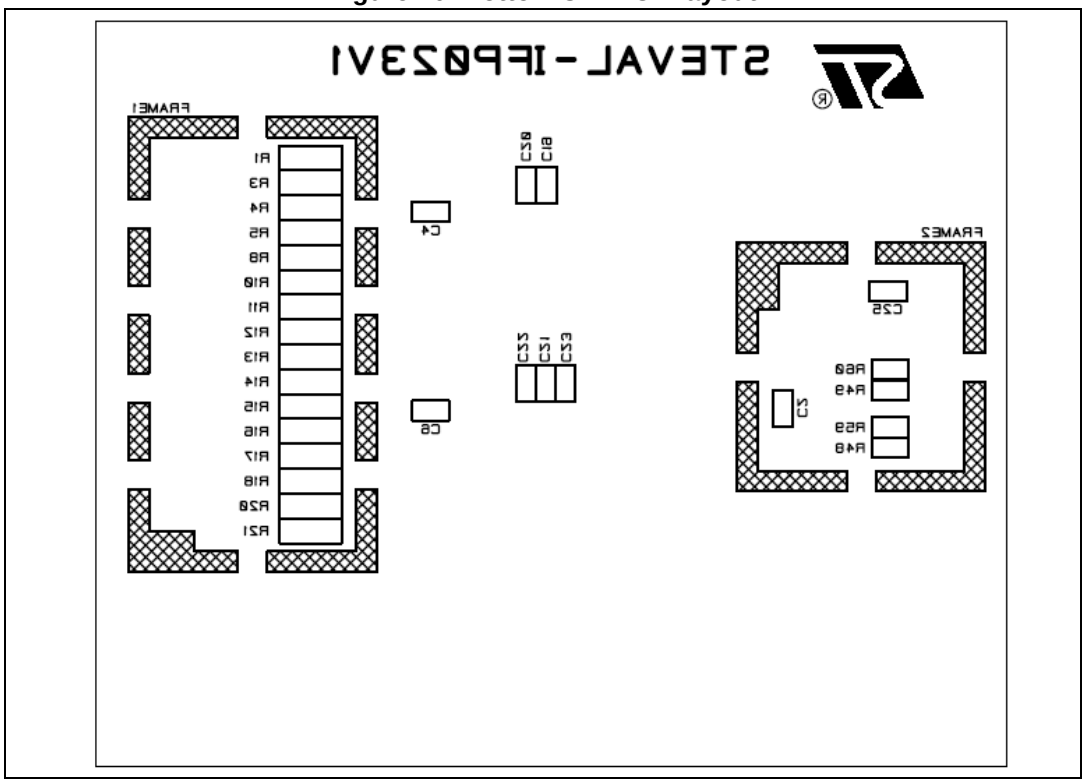


Figure 10. Bottom silk PCB layout



3.2 PCB layout considerations

Micro sub-D connectors (CN1 and CN2) grant the continuity of cable shielding to the PCB. To insulate input from external electromagnetic perturbation, all input tracks are internal.

The signal lines are continuously shielded from cable lines to input capacitor (C40 to C55) in order to increase EMC robustness to IEC 61000 4-4.

3.3 Power supplies

The application is supplied by two sides using two independent power supplies: primary and secondary. The primary power supply is typically 24 VDC (functional range from 16 to 35 VDC), and is connected to CN1 connector. The secondary supply is connected through CN2 (SPI) connector and it comes from microcontroller or control logic supply voltage.

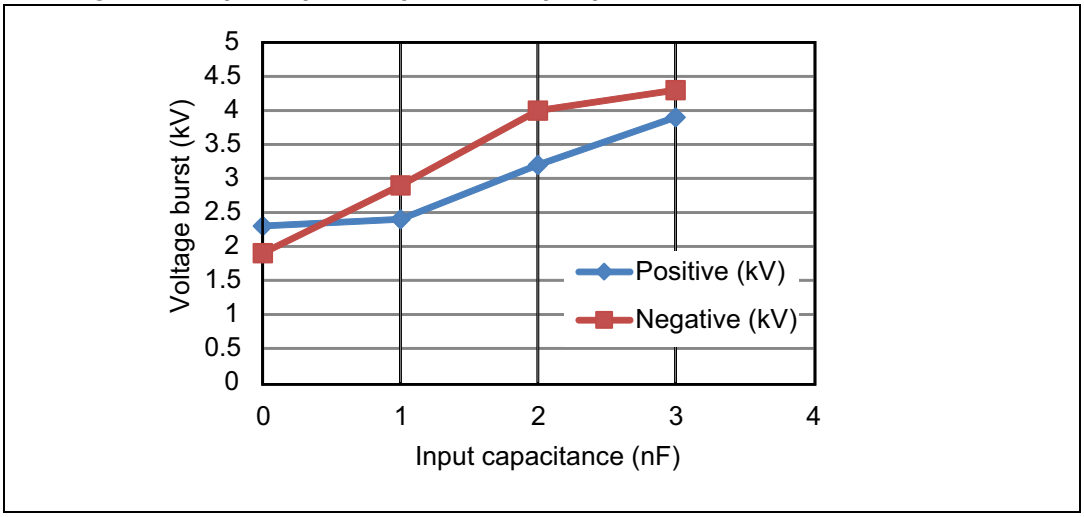
3.4 Input resistors

Special care should be given to the input and supply line resistors (R1, R3 to R5, R8, R10 to R18, R20, R21 and R22). Their type dramatically influences EMC of the application and high voltage surge robustness (IEC 61000-4-5). Resistors should sustain high peak voltage and current levels. A suitable type is, for example, MELF MMB0207 from Vishay. Standard SMD 1206 resistors are not recommended, as their peak ratings are much lower.

3.5 Input capacitor

Each CLT01-38S4 input signal is filtered by an input capacitor of 3.3 nF (C40 to C55) to maximize EFT immunity. *Figure 11* presents the IEC 61000 4-4 robustness as a function of the input capacitor value.

Figure 11. Input capacitor (C40 to C55) impact on IEC 61000 4-4 robustness

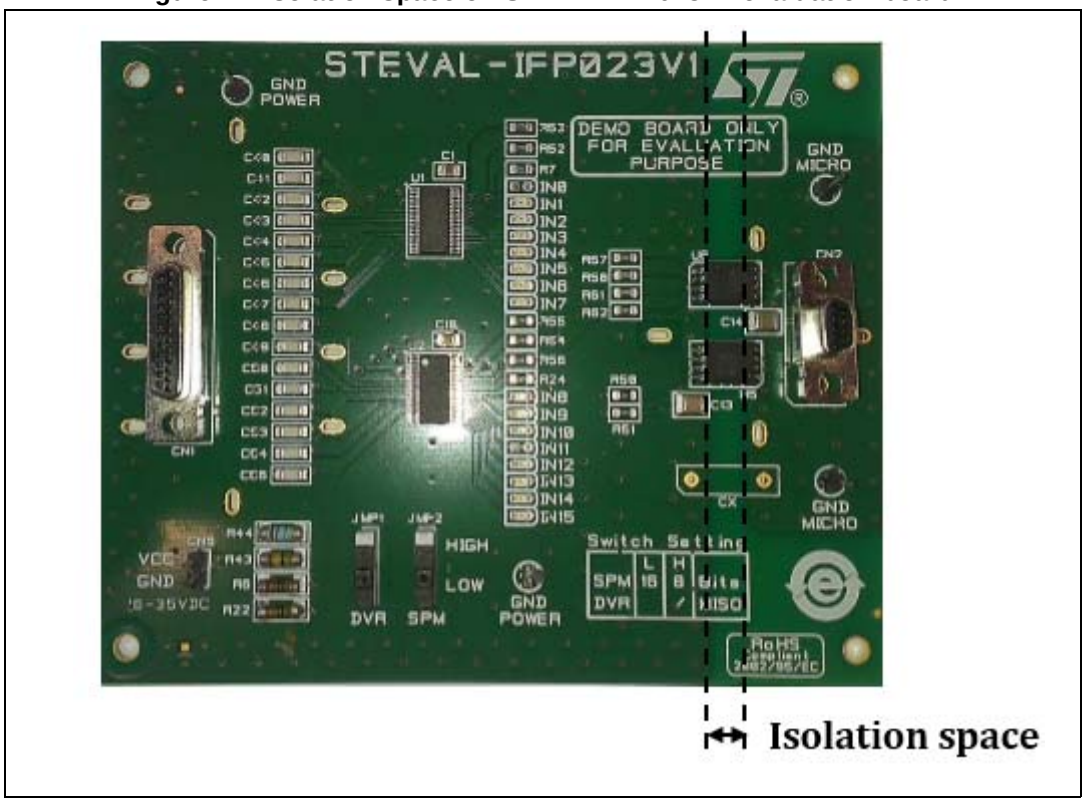


Capacitor values can be increased up to 22 nF, for example, to achieve even higher immunity levels, but with an input bandwidth reduction. These input capacitors can be compared to an immunity barrier, the IEC 61000 4-4, in addition to the overall shielding.

3.6 Isolation space

An isolation space (without routes, copper areas and components) is present between the primary (sensor-side) and secondary (microcontroller) application parts. Due to the isolator (opto-couplers: U5 and U6) sensitivity on fast common mode transitions, both application sections could be additionally coupled with high voltage ceramic capacitors. This increases overall application robustness. EMC tests show immunity rise when a 10 pF capacitor (Cx) is placed between SGND and MICRO_GND.

Figure 12. Isolation space on STEVAL-IFP023V1 evaluation board



Filters are implemented on each SPI signal (CS, SCK, and MOSI), close to each CLT0138-S4, with an R-C cell that limits the bandwidth to suppress noise sensitivity. Values used in the application are 220 Ω, 100 pF (R52 to R56 and C19 to C23), which correspond to the maximum communication baud rate of approximately 3 Mbps.

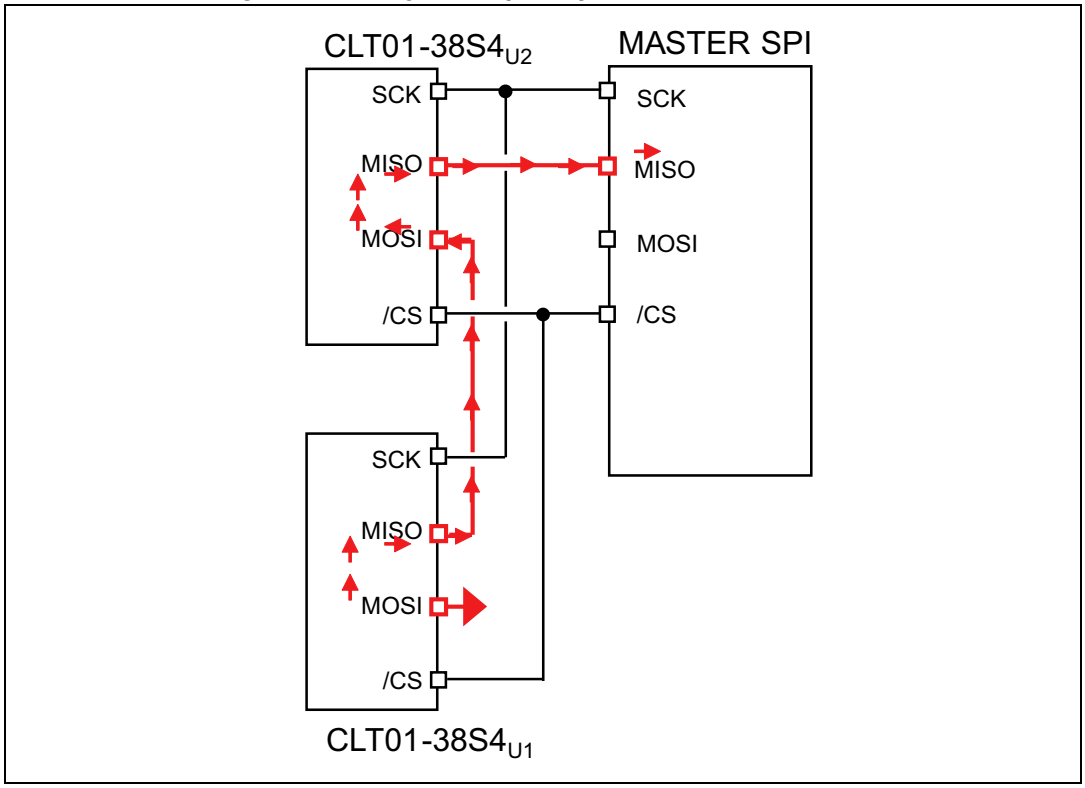
The application designer sets the appropriate R-C values in order to suppress high frequency noise. By increasing the capacitor values, a higher signal stability is ensured; it has a positive effect on the immunity, but reduces the communication baud rate.

3.7 Daisy chain

There are 16 parallel sensor inputs on the STEVAL-IFP023V1. To read them, two CLT01-38S4 are necessary (U1 and U2). 16 LED display input states. However, only one single SPI port is used to transmit information to the field bus controller. Indeed, MISO output of U1 CLT01-38S4 goes on MOSI input of U2 CLT01-38S4 (SD_0f signal on schematic). This link is a “daisy chain”. Input signals CLK and CS are common between the CLT01-38S4 (see *Figure 13*). MOSI input of U1 CLT01-38S4 must be connected to GND to avoid floating high

impedance state. MISO-/MISO output of U1 CLT01-38S4 must be forced to MISO and DVR input must be grounded.

Figure 13. Daisy chain principle for two CLT01-38S4



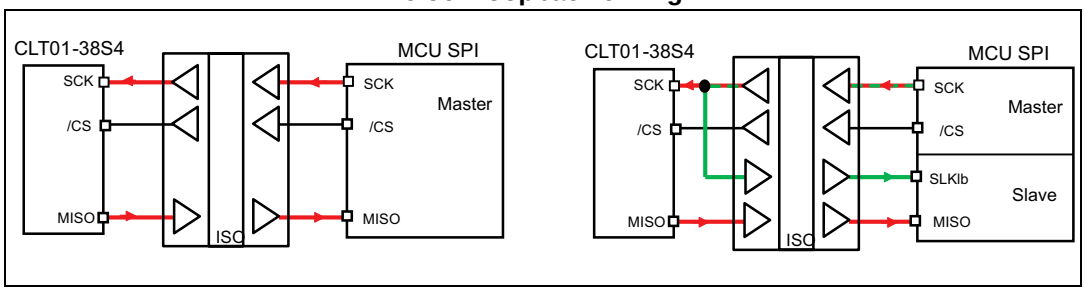
This configuration presents some advantages such as: the reduction of opto-coupler numbers and one CS address only. Indeed, the U2 CLT01-38S4 sends information to the field bus controller. The drawback is an increased access time to read a single input, because 16 inputs need to be read instead of 8. However, if all inputs have to be read, access time is similar.

This example presents two CLT01-38S4 on daisy chain configuration but this principle can be extended to any number of the CLT01-38S4.

3.8 Clock loopback

On standard SPI configuration, delay induced by opto-coupler between SCK and MISO signal (on MCU SPI master) is twice the opto-coupler delay (one time on SCK line and one time on MISO line). *Figure 14* illustrates timing principle.

Figure 14. On the left, CLT01-38S4 timing principle/ on the right, CLT01-38S4 with clock loopback timing



AVAGO ACPL-K73L propagation maximal delay is 55 ns: then, maximal delay offset induced by opto-couplers could be as high as 110 ns. This value is not compatible with the CLT01-384S4 max. frequency, equal to 6.25 MHz (80 ns for a half period) and due to delay offset caused by opto-coupler, synchronization is not possible anymore. Faster opto-couplers with higher current consumption do not solve this issue.

Implementation of a clock loopback enables high datarate to be achieved, whatever the opto-coupler delay is (see *Figure 14*, on the right). Two SPI ports are required by MCU, one in master mode while the other is in slave mode. The slave is independent of opto-coupler propagation delays because the clock signal (CLTI) goes through the same opto-coupler than MOSI signal. The tradeoff is two SPI ports and a dual channel opto-coupler instead of a single channel one for data incoming on MCU SPI slave.

3.9 Thermal management

The CLT01-38S4 has three functional blocks generating thermal losses:

- Input current limiters
- Voltage regulator
- Quiescent current

Each part generates a voltage drop between I/O of the CLT01-38S4 and a flowing current is associated. Product corresponds to the CLT01-38S4 losses. Total losses are the sum of these thermal losses.

Figure 15 shows thermal losses and the associated circuitry.

Figure 15. Thermal loss blocks on CLT01-38S4

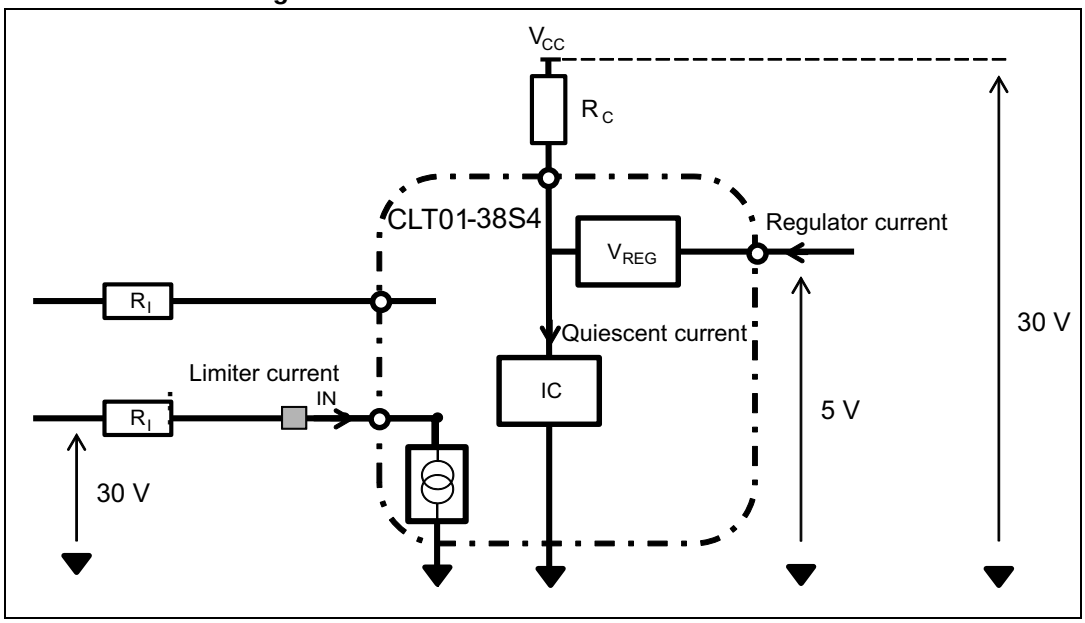


Table 2 shows thermal losses on the CLT01-38S4. All values are worst cases in terms of power losses to secure all used cases.

Table 2. Thermal loss values

Circuit	Count	Drop voltage (V)	Flowing current (mA)	Loss (mW)
Quiescent current	1	30 – 0.5 kΩ x (7+3) mA = 25.6	3	46
Current limiter	8	30- 2.2 kΩ x 2.6 mA = 24.3	< 2.6	505
Voltage regulator	1	30 – 0.5 kΩ x (7+3) mA – 5 = 18.7	7	144
Total				**695**

Power dissipation on the CLT01-38S4 increases the junction temperature.

The allowed maximal junction temperature of the CLT01-38S4 is 150 °C.

HTSSOP38 package gives a thermal resistance (junction-to-ambient) of 80 °C/W when mounted on 40 mm² copper surface.

The thermal equation is: $\Delta T_{j\text{-}a} = T_j - T_a = Pd*Rth_{j\text{-}a}$

where:

- T_j: junction temperature
- T_a: ambient temperature
- P_d: power to dissipate
- $Rth_{j\text{-}a}$: junction-to-ambient thermal resistance

As example, an 80 °C ambient temperature with 40 mm² copper surface and all functions used on worst thermal case lead to 130 °C junction temperature. It is lower than the 150 °C defined in the datasheet.

3.10 Reverse polarity

One-channel has to be connected to the negative voltage.

With negative biasing of the input, the current flows through the protection diode. The voltage between the reverse I/O is then equal to the forward voltage of the protection diode and it is approximately 0.7 V. All other inputs work correctly.

The flowing on the reverse I/O is (30 - 0.7) / 2.2 kΩ = 13 mA and the associated losses are 10 mW. The dissipated power in that case is lower than in normal operation (63 mW by I/O). The CLT01-38S4 is protected from input reverse polarity.

Special care must be taken on the serial resistor rating. During the normal operation or worst case conditions, the power ratings of the serial resistors are:

- 16 mW for the input serial resistors
- 36 mW for the supply serial resistors

During the reverse polarity connection, the resistors must be able to dissipate:

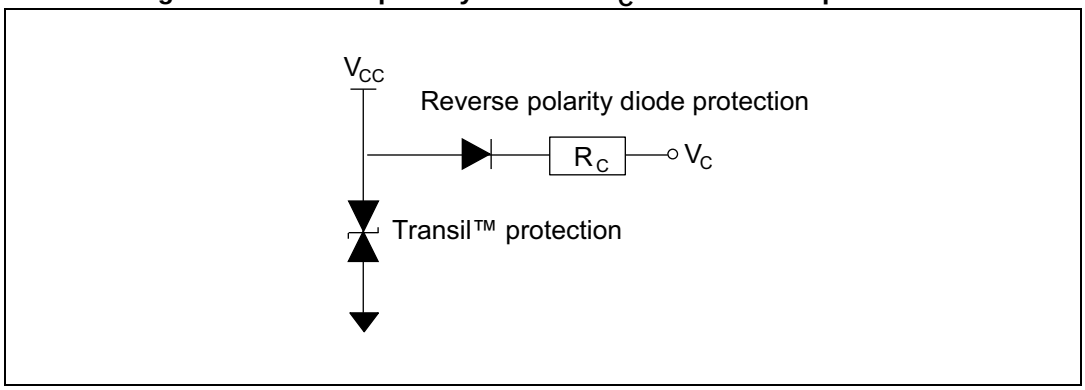
- 372 mW, the input serial resistors
- 858 mW, the supply serial resistor

To increase reliability of the resistors, by considering long-term reverse polarity, the following options are suggested:

1. Parallel connection of two (or more) resistors
2. Use of high power rating resistors
3. Reverse polarity diode connection in series with supply serial resistor

Concerning this last option (point 3), it is important to choose the diode with VR rating higher than the required surge immunity voltage (e.g. 1 or 2 kV) or to use additional Transil™ protection (bi-directional) to the application supply voltage terminal (for example the SM15T36CA) as shown in *Figure 16*.

Figure 16. Reverse polarity diode on V_C with Transil™ protection



4 EMC requirements

4.1 Procedure to evaluate the robustness of the CLT01-38S4

The IEC 61131-2 international standard is the reference to evaluate the CLT01-38S4 robustness. This standard provides all requirements and test conditions for programmable logic controllers (PLCs) and their associated peripherals. It specifies the electromagnetic compatibility (EMC) requirements and the nature of the tests to perform and to determine if the system meets these requirements. The levels of each test depend on the zone where the system is installed. The most typical industrial environmental levels correspond to zone B: local power distribution zone and dedicated power distribution zone (see EMC immunity zones of the IEC 61131-2-Ed2 standard). The following sections deal with the test levels for this zone.

4.2 ESD tests (IEC 61000-4-2)

Electrostatic discharge test is applied to operator accessible devices. This means that these tests have to be performed on each connector pin. The required levels are air discharge: ± 8 kV and contact discharge: ± 4 kV.

PLC system continues operating. Temporary degradation of the performance is acceptable during the test, but the system must recover after the test (criteria “B” according to the IEC61131-2 standard).

4.3 Burst tests (IEC 61000-4-4)

The fast transient burst tests must be applied to all input pins of the system. A capacitive clamp-coupling device (50-200 pF) must be used as described in the IEC 61000-4-4 standard. The required burst voltage levels are the analog or DC I/O: ± 1 kV, DC power line: ± 2 kV. PLC system continues operating. Temporary degradation of the performance is acceptable during the test, but the system must recover after the test (criteria “B” according to the IEC 61131-2 standard).

4.4 Surge test (IEC 61000-4-5)

Since the voltage surge consists of a single but energetic pulse, the CLT01-38S4 embeds an overvoltage protection on each point. The absorbed energy complies at least with the IEC 61131-2 standard requirements. The high energy surge test must be applied on all input pins of the system. For all analog inputs, the coupling method is a 42 Ω serial resistor and a capacitor of 0.5 µF. For DC power line, the coupling is 2 Ω, 18 µF for differential mode, and 12 Ω, 9 µF for common mode. Required voltage surge levels are:

- Analog or DC I/O: 0.5 kV (differential and common coupling modes)
- DC power line: 0. 5 kV (differential mode)
- DC power line: 1 kV (common mode)

The PLC system continues operating. Temporary degradation of the performance is acceptable during the test, but the system must recover after the test (criteria “B” according to the IEC 61131-2 standard).

4.5 Conducted disturbance tests (IEC 61000-4-6)

The conducted radio frequency interference test must be applied to all input pins of the system. The frequency range is from 150 kHz to 80 MHz, with 80% amplitude modulation 1 kHz sinusoidal wave. A CDN (coupling/decoupling network) or a current coupling clamp (as described in the IEC 61000-4-6 standard) must be used to apply stress to the system. The required level is: 3 VRMS, whatever the tested system input is. The PLC system continues operating. No loss of function or performance is acceptable (criteria “A” according to the IEC 61131-2 standard).

4.6 Reverse analog input polarity tests

The test procedure is described in the IEC 61131-2 standard (section 5.4.4.5 of Ed2 of the standard). A signal of reverse polarity (negative voltage) for unipolar analog inputs is applied for 10 seconds. The result of this test is stated by the manufacturer. Each input of the CLT01-38S4 device may be biased to a reverse polarity. This case corresponds either to a connection mistake, or a reverse biasing that is generated by the demagnetization of a monitored inductive solenoid. The involved input withstands the high reverse current up to 20 mA; its corresponding bit in the data frame remains in a logic low-state. The other inputs remain operative. By considering the supply operation, a reverse blocking diode can be connected between the module ground and the common COM pin to protect the application (especially the serial resistors) from a spurious reverse supply connection.

4.7 EMC testing

The EMC requirements according to the IEC 61131-2 standard have been verified. Application tests show much better results than those given by the industrial standard. Test requirements and results are listed in the table below. No additional protection device has been used in the application.

Table 3. EMC immunity test requirements and results

	Minimum requirements of international standards *		**CLT01-38S4 robustness**	
	Tests conditions	Level/criteria	Test conditions	Level/ criteria
ESD test IEC61000-4-2	Air discharge	±8 kV B	On product + R_{IN}=2.2 kΩ / R_C=0.5 kΩ	±15 kV B
	Contact discharge	±4 kV B	On product + R_{IN}=2.2 kΩ / R_C=0.5 kΩ	±8 kV B
Burst test IEC61000-4-4	Analog input	±1 kV B	STEVAL-IFP023V1, 2 MHz	±3 kV A
	DC power line	±2 kV B		

Table 3. EMC immunity test requirements and results (continued)

	Minimum requirements of international standards *			CLT01-38S4 robustness	
Surge test IEC61000-4-5	Analog input	42 Ω, 0.5 µF different and common	±0.5 kV B	On single CLT01 board R_{IN}=2.2 kΩ	±2 kV B
	DC power line	2 Ω, 18 µF different mode	±0.5 kV B	On single CLT01 board R_C=0.5 kΩ R_C=2.2 kΩ	±1 kV B ±2.5 kV B
		12 Ω, 9 µF common	±1 kV B		
RF test IEC61000 4-6	Analog input		3 V A	STEVAL-IFP023V1, 2 MHz	3 V A
	DC power line		3 V A		3 V A
Reverse input polarity test	-V_{CC} applied to one input during 10 seconds			-30 VDC CW applied to one input +VDC CW applied on the others	

5 Ordering information

The evaluation board is available through the standard ordering system, with the order code: STEVAL-IFP023V1. The complete kit contains:

- Evaluation board
- Cables to connect the board
- Evaluation board documentation
- PCB fabrication data, such as Gerber files
- Assembly files (pick-and-place)
- Component documentation

6 Conclusion

This document illustrates that the CLT01-38S4, implemented in the STEVAL-IFP023V1 evaluation board, works in harsh environments without problems. All industrial standard requirements are fulfilled. Besides, test levels are higher than those required for the majority of final products. No additional protection device is necessary and this increases the cost-effectiveness of the application. Finally, the device has passed the reverse polarity tests, including the thermal management considerations.

7 Revision history

Table 4. Document revision history

Date	Revision	Changes
26-Jan-2015	1	Initial release.