AN4651
Application note

STM32F3 series peripheral interconnect matrix

Introduction

STM32F3 series peripherals communicate autonomously without any intervention from the CPU, via a network known as peripheral interconnect matrix.

STM32F3 series peripheral interconnect matrix offers multiple benefits:

- autonomous communication between peripherals,
- efficient synchronization between peripherals,
- discarded software latency and minimized GPIOs configuration,
- optimal available pins even with small packages,
- connector usage avoidance leading to optimized PCB design with less dissipated energy.

The present document first describes the peripheral interconnect matrix, then provides an overview of the peripheral interconnections and how to configure them with respect to user applications.

This application note has to be read in conjunction with STM32F3 series datasheets and reference manuals:

- STM32F303xB/C/D/E, STM32F303x6/8, STM32F328x8, STM32F358xC, STM32F398xE advanced ARM®-based MCUs (RM0316)
- STM32F302xB/C/D/E and STM32F302x6/8 advanced ARM®-based 32-bit MCUs (RM0365)
- STM32F301x6/8 and STM32F318x8 advanced ARM®-based 32-bit MCUs (RM0366)
- STM32F334xx advanced ARM®-based 32-bit MCUs (RM0364)
- STM32F37xx advanced ARM-based 32-bit MCUs (RM0313)

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1 Peripheral availability in STM32F3 series devices

The interconnection feature is available for many peripherals in the STM32F3 series devices. *Table 1* presents the peripheral availability in the respective devices of STM32F3 series. Users should refer to this table in the coming sections in which the interconnections are mostly described without referring to any specific device of STM32F3 series.

Table 1. Peripheral availability in STM32F3 series devices(1) (2)

Peripheral	STM32F303xD/E STM32F398VE	STM32F303xB/C STM32F358xC	STM32F303x6/8 STM32F328x8	STM32F302xD/E	STM32F302xB/C	STM32F302x6/8 STM32F301x6/8 STM32F318x8	STM32F334x4/6/8	STM32F373x8/B/C STM32F378xC
DMA1	x	x	x	x	x	x	x	x
DMA2	x	x		x	x			x
ADC1	x	x	x	x	x	x	x	x
ADC2	x	x	x	x	x		x	
ADC3	x	x						
ADC4	x	x						
SDADC1								x
SDADC2								x
SDADC3								x
COMP1	x	x		x	x			x
COMP2	x	x	x	x	x	x	x	x
COMP3	x	x						
COMP4	x	x	x	x	x	x	x	
COMP5	x	x						
COMP6	x	x	x	x	x	x	x	
COMP7	x	x						
OPAMP1	x	x		x	x			
OPAMP2	x	x	x	x	x	x	x	
OPAMP3	x	x						
OPAMP4	x	x						

Table 1. Peripheral availability in STM32F3 series devices(1) (2) (continued)

Peripheral	STM32F303xD/E STM32F398VE	STM32F303xB/C STM32F358xC	STM32F303x6/8 STM32F328x8	STM32F302xD/E	STM32F302xB/C	STM32F302x6/8 STM32F301x6/8 STM32F318x8	STM32F334x4/6/8	STM32F373x8/B/C STM32F378xC
TIM1	x	x	x	x	x	x	x	
HRTIM1							x	
SPI1	x	x	x	x	x		x	x
TIM8	x	x						
USART1	x	x	x	x	x	x	x	x
SPI4	x			x				
TIM12								x
TIM13								x
TIM14								x
TIM15	x	x	x	x	x	x	x	x
TIM16	x	x	x	x	x	x	x	x
TIM17	x	x	x	x	x	x	x	x
TIM18								x
TIM19								x
TIM20	x							
TIM2	x	x	x	x	x	x	x	x
TIM3	x	x	x	x	x		x	x
TIM4	x	x		x	x			x
TIM5								x
TIM6	x	x	x	x	x	x	x	x
TIM7	x	x	x				x	x
SPI2/I2S	x	x		x	x	x		x
SPI3/I2S	x	x		x	x	x		x
USART2	x	x	x	x	x	x	x	x
USART3	x	x	x	x	x	x	x	x

Table 1. Peripheral availability in STM32F3 series devices(1) (2) (continued)

Peripheral	STM32F303xD/E STM32F398VE	STM32F303xB/C STM32F358xC	STM32F303x6/8 STM32F328x8	STM32F302xD/E	STM32F302xB/C	STM32F302x6/8 STM32F301x6/8 STM32F318x8	STM32F334x4/6/8	STM32F373x8/B/C STM32F378xC
UART4	x	x		x	x			
UART5	x	x		x	x			
I2C1	x	x	x	x	x	x	x	x
I2C2	x	x		x	x	x		x
DAC1	x	x	x	x	x	x	x	x
DAC2			x				x	x
I2C3	x			x		x		
IRTIM	x	x	x	x	x	x	x	x

1. Only peripherals concerned by the interconnect matrix are listed in the table.
2. Table cells with gray shading indicate that the peripheral is not available.

2 Peripheral interconnect matrix

STM32F3 series peripherals are interconnected through the peripheral interconnect matrix that allows to directly connect one peripheral to another. *Table 2* summarizes the peripheral interconnections in STM32F3 series devices. *Section 3: Interconnection descriptions* provides the details on the interconnections.

Table 2. STM32F3 series peripherals interconnect matrix(1)

Source/ Destination	DMA1	DMA2	ADC1	ADC2	ADC3	ADC4	COMP1	COMP2	COMP3	COMP4	COMP5	COMP6	COMP7	OPAMP	OPAMP	OPAMP	OPAMP	TIM1	TIM8	TIM14	TIM15	TIM16	TIM17	TIM19	TIM20	TIM2	TIM3	TIM4	TIM5	TIM12	DAC1	DAC2	IRTIM	SDADC	SDADC	SDADC	HRTIM1
ADC1	x			x																																	x
ADC2	x(2)	x																	x																		x
ADC3		x				x													x						x												
ADC4		x																							x												
COMP1																		x	x		x(3)				x	x	x		x(3)								
COMP2																		x	x			x(3)			x	x	x	x(3)									x
COMP3																		x	x		x				x	x	x										
COMP4																			x		x				x		x	x									x
COMP5																			x			x	x		x	x	x	x									
COMP6																			x			x			x	x		x									x
COMP7																			x				x		x	x											
OPAMP1			x																																		
OPAMP2				x																																	x
OPAMP3					x																																
OPAMP4						x																															
TIM1	x		x	x	x	x	x	x	x				x	x	x	x	x		x						x	x	x	x									x

Table 2. STM32F3 series peripherals interconnect matrix(1) (continued)

Source/ Destination	DMA1	DMA2	ADC1	ADC2	ADC3	ADC4	COMP1	COMP2	COMP3	COMP4	COMP5	COMP6	COMP7	OPAMP	OPAMP	OPAMP	OPAMP	TIM1	TIM8	TIM14	TIM15	TIM16	TIM17	TIM19	TIM20	TIM2	TIM3	TIM4	TIM5	TIM12	DAC1	DAC2	IRTIM	SDADC	SDADC	SDADC	HRTIM1
SPI1	x																																				
TIM8		x	x	x	x	x				x	x	x	x												x	x		x			x						
USART1	x																																				
SPI4		x																																			
TIM12																																		x	x		
TIM13																													x				x				
TIM14																										x	x		x				x				
TIM15	x		x(4)	x	x	x				x	x	x	x					x						x	x	x(3)	x(4)	x(3)	x		x	x		x			x
TIM16	x																				x			x									x		x	x	
TIM17	x																	x			x												x		x		x
TIM18	x	x																																			
TIM19	x		x																							x	x	x						x	x	x	
TIM20		x	x	x	x	x																															
TIM2	x		x	x	x	x	x	x	x		x	x						x	x		x			x			x	x	x		x	x			x	x	x
TIM3	x		x	x	x	x	x	x		x								x	x		x			x		x		x	x		x	x		x	x	x	x
TIM4	x		x	x	x	x												x	x						x	x(4)	x(4)			x	x			x	x	x	
TIM5	x																										x			x							
TIM6	x	x	x(4)	x																											x	x					x
TIM7	x	x			x	x																									x	x					x
SPI2/I2S	x																																				
SPI3/I2S		x																																			

Table 2. STM32F3 series peripherals interconnect matrix[1] (continued)

Source/ Destination	DMA1	DMA2	ADC1	ADC2	ADC3	ADC4	COMP1	COMP2	COMP3	COMP4	COMP5	COMP6	COMP7	OPAMP	OPAMP	OPAMP	OPAMP	TIM1	TIM8	TIM14	TIM15	TIM16	TIM17	TIM19	TIM20	TIM2	TIM3	TIM4	TIM5	TIM12	DAC1	DAC2	IRTIM	SDADC	SDADC	SDADC	HRTIM1
USART2	x																																				
USART3	x																																				
UART4		x																																			
UART5		x																																			
I2C1	x																																				
I2C2	x																																				
DAC1	x	x					x	x	x	x	x	x	x	x		x	x																					
DAC2	x	x[3]					x[3]	x		x		x																										
I2C3	x																																				
TS			x																																		
VBAT			x																																		
V_{REFINT}			x	x	x	x	x	x	x	x	x	x	x																								
CSS																		x	x		x				x												x
PVD																		x	x		x				x												x
SRAM Parity error																		x	x		x				x												x
CPU Hard-fault																		x	x		x				x												x
HSE																				x		x[4]															
HSI																				x		x[4]															
LSE																				x		x[4]															

Table 2. STM32F3 series peripherals interconnect matrix(1) (continued)

Source/ Destination	DMA1	DMA2	ADC1	ADC2	ADC3	ADC4	COMP1	COMP2	COMP3	COMP4	COMP5	COMP6	COMP7	OPAMP	OPAMP	OPAMP	OPAMP	TIM1	TIM8	TIM14	TIM15	TIM16	TIM17	TIM19	TIM20	TIM2	TIM3	TIM4	TIM5	TIM12	DAC1	DAC2	IRTIM	SDADC	SDADC	SDADC	HRTIM1
LSI																				x		x(4)															
MCO																				x		x(4)															
RTC																				x		x(4)															
SDADC1		x																																			
SDADC2		x																																			
SDADC3		x																																			
HRTIM1	x		x	x																										x	x					

1. The cells with gray shading indicate that there is no interconnection.
2. Only in STM32F303x6/8 and STM32F328x8.
3. Only in STM32F37x.
4. Not applicable for STM32F37x.

3 Interconnection descriptions

3.1 DMA interconnections

Peripherals manage the hardware DMA requests. *Table 3* lists the DMA channels dedicated to each peripheral.

Table 3. DMA interconnections in STM32F3 series devices(1)

Peripheral	STM32F303xB/CD/E STM32F302xB/C/D/E STM32F398xE STM32F358xC	STM32F303x6/8 STM32F328x8 STM32F334x4/6/8	STM32302x6/8	STM32F373x8/B/C STM32F378xC
ADC1	DMA1_Ch1			
ADC2	DMA2_Ch1 DMA2_Ch3	DMA1_Ch2 DMA1_Ch4		
ADC3	DMA2_Ch5			
ADC4	DMA2_Ch2 DMA2_Ch4			
SPI1	DMA1_Ch2 (SPI1_RX) DMA1_Ch3 (SPI1_TX)	DMA1_Ch2/Ch4/Ch6 (SPI1_RX) DMA1_Ch3/Ch5/CH7 (SPI1_TX)		DMA1_Ch2 (SPI1_RX) DMA1_Ch3 (SPI1_TX)
SPI2	DMA1_Ch4 (SPI2_RX) DMA1_Ch5 (SPI2_TX)		DMA1_Ch4 (SPI2_RX) DMA1_Ch5 (SPI2_TX)	
SPI3	DMA2_Ch1 (SPI3_RX) DMA2_Ch2 (SPI3_TX)		DMA1_Ch2 (SPI3_RX) DMA1_Ch3 (SPI3_TX)	DMA2_Ch1 (SPI3_RX) DMA2_Ch2 (SPI3_TX)
SPI4	DMA2_Ch4 (SPI4_RX) DMA2_Ch5 (SPI4_TX)			
USART1	DMA1_Ch4 (USART1_TX) DMA1_Ch5 (USART1_RX)			
USART2	DMA1_Ch6 (USART2_RX) DMA1_Ch7 (USART2_TX)			
USART3	DMA1_Ch2 (USART3_TX) DMA1_Ch3 (USART3_RX)			
UART4	DMA2_Ch3 (UART4_RX) DMA2_Ch5 (UART4_TX)			
I2C1	DMA1_Ch6 (I2C1_TX) DMA1_Ch7 (I2C1_RX)	DMA1_Ch2/Ch4/Ch6 (I2C1_TX) DMA1_Ch3/Ch5/Ch7 (I2C1_RX)	DMA1_Ch6 (I2C1_TX) DMA1_Ch7 (I2C1_RX)	
I2C2	DMA1_Ch4 (I2C2_TX) DMA1_Ch5 (I2C2_RX)		DMA1_Ch4 (I2C2_TX) DMA1_Ch5 (I2C2_RX)	

Table 3. DMA interconnections in STM32F3 series devices(1) (continued)

Peripheral	STM32F303xB/CD/E STM32F302xB/C/D/E STM32F398xE STM32F358xC	STM32F303x6/8 STM32F328x8 STM32F334x4/6/8	STM32302x6/8	STM32F373x8/B/C STM32F378xC
I2C3	DMA1_Ch1 (I2C3_TX) DMA1_Ch2 (I2C3_RX)		DMA1_Ch1 (I2C3_TX) DMA1_Ch2 (I2C3_RX)	
TIM1	DMA1_Ch2(TIM1_CH1) DMA1_Ch3 (TIM1_CH2) DMA1_Ch4 (TIM1_CH4/TRIG/COM) DMA1_Ch5 (TIM1_UP) DMA1_Ch6 (TIM1_CH3)			
TIM8	DMA2_Ch1 (TIM8_CH3/UP) DMA2_Ch2 (TIM8_CH4/TRIG/COM) DMA2_Ch3 (TIM8_CH1) DMA2_Ch5 (TIM8_CH2)			
TIM20	DMA2_Ch1 (TIM20_CH1) DMA2_Ch2 (TIM20_CH2) DMA2_Ch3 (TIM20_CH3/UP) DMA2_Ch4 (TIM20_CH4/TRIG/COM)			
TIM2	DMA1_Ch1 (TIM2_CH3) DMA1_Ch2 (TIM2_UP) DMA1_Ch5 (TIM2_CH1) DMA1_Ch7 (TIM2_CH2/CH4)			
TIM3	DMA1_Ch2 (TIM3_CH3) DMA1_Ch3 (TIM3_CH4/UP) DMA1_Ch6 (TIM3_CH1/TRIG)			DMA1_Ch2 (TIM3_CH3) DMA1_Ch3 (TIM3_CH4/UP) DMA1_Ch6 (TIM3_CH1/TRIG)
TIM4	DMA1_Ch1 (TIM4_CH1) DMA1_Ch4 (TIM4_CH2) DMA1_Ch5 (TIM4_CH3) DMA1_Ch7 (TIM4_UP)			DMA1_Ch1 (TIM4_CH1) DMA1_Ch4 (TIM4_CH2) DMA1_Ch5 (TIM4_CH3) DMA1_Ch7 (TIM4_UP)
TIM5				DMA2_Ch1 (TIM5_CH4/TRIG) DMA2_Ch2 (TIM5_CH3/UP) DMA2_Ch4 (TIM5_CH2) DMA2_Ch5 (TIM5_CH1)
TIM6	DMA1/2_Ch3 (TIM6_UP)	DMA1_Ch3 (TIM6_UP)		DMA1/2_Ch3 (TIM6_UP)
TIM7	DMA1/2_Ch4 (TIM7_UP)	DMA1_Ch4 (TIM7_UP)		DMA1/2_Ch4 (TIM7_UP)

Table 3. DMA interconnections in STM32F3 series devices(1) (continued)

Peripheral	STM32F303xB/CD/E STM32F302xB/C/D/E STM32F398xE STM32F358xC	STM32F303x6/8 STM32F328x8 STM32F334x4/6/8	STM32302x6/8	STM32F373x8/B/C STM32F378xC
TIM15	DMA1_Ch5 (TIM15_CH1/UP/TRIG/COM)			
TIM16	DMA1_Ch3 (TIM16_CH1/UP) DMA1_Ch6 (TIM16_CH1/UP)			
TIM17	DMA1_Ch1 (TIM17_CH1/UP) DMA1_Ch7 (TIM17_CH1/UP)			
TIM18				DMA1/2_Ch5 (TIM18_UP)
TIM19				DMA1_Ch1 (TIM19_CH3/CH4) DMA1_Ch2 (TIM19_CH1) DMA1_Ch3 (TIM19_CH2) DMA1_Ch4 (TIM19_UP)
DAC1	DMA1/2_Ch3 (DAC1_CH1) DMA1/2_Ch4 (DAC1_CH2)	DMA1_Ch3 (DAC1_CH1) DMA1_Ch4 (DAC1_CH2)	DMA1_Ch3 (DAC1_CH1)	DMA1/2_Ch3 (DAC1_CH1) DMA1/2_Ch4 (DAC1_CH2)
DAC2		DMA1_Ch5 (DAC2_CH1)		DMA1/2_Ch5 (DAC2_CH1)
SDADC1				DMA2_CH3
SDADC2				DMA2_CH4
SDADC3				DMA2_CH5
HRTIM1		DMA1_Ch2 (HRTIM1_M) DMA1_Ch3 (HRTIM1_A) DMA1_Ch4 (HRTIM1_B) DMA1_Ch5 (HRTIM1_C) DMA1_Ch6 (HRTIM1_D) DMA1_Ch7 (HRTIM1_E)		

1. The cells with gray shading indicate that there is no interconnection.

3.2 From ADC to ADC

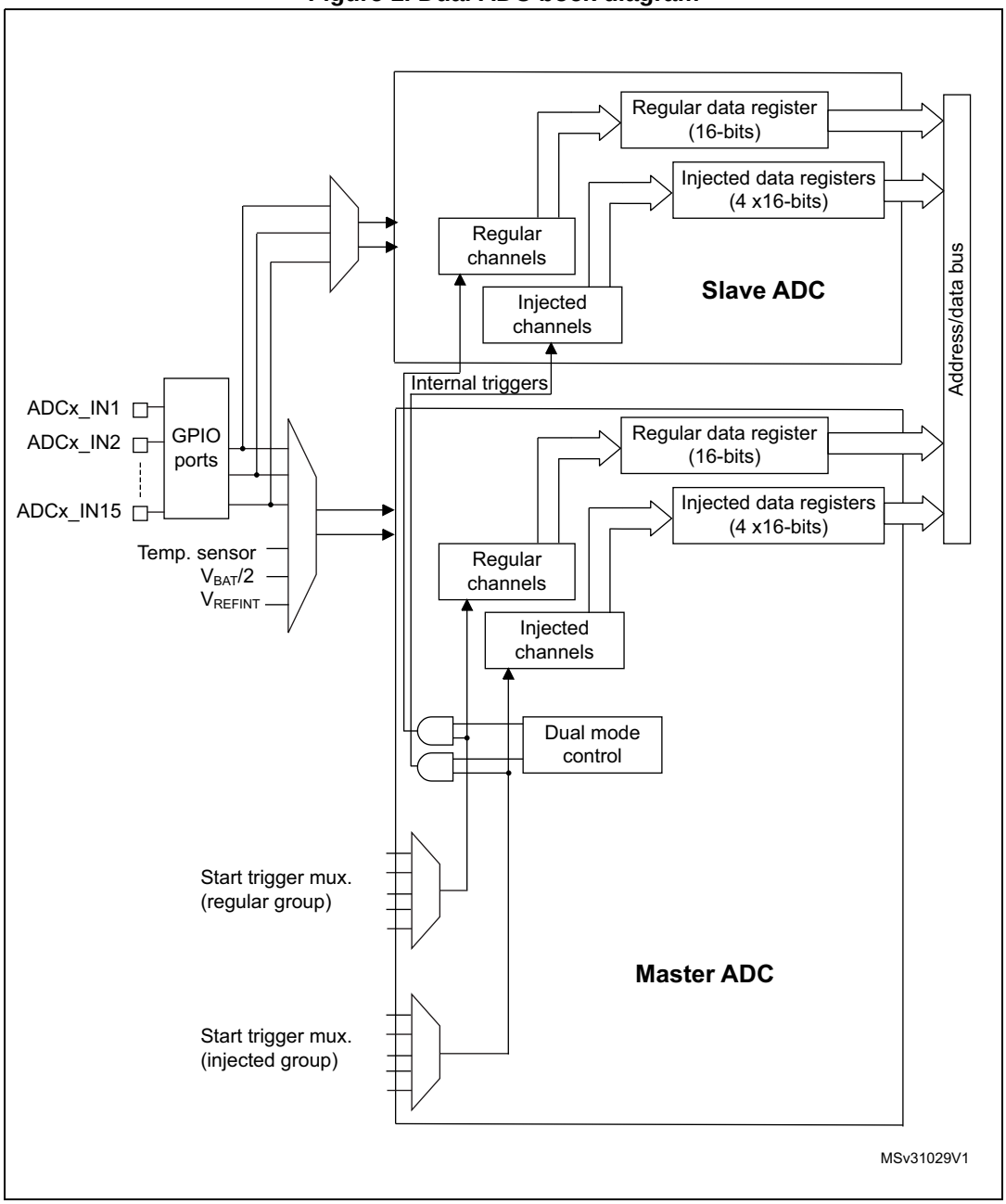
In the devices of STM32F3 series that feature two ADCs or more, the dual ADC modes can be used:

- ADC1 can be used as a “master” to trigger ADC2 “slave” start of conversion.
- ADC3 can be used as “master” to trigger ADC4 “slave” start of conversion.

In dual ADC mode, the converted data of the master and slave ADCs can be read in parallel.

Figure 1 depicts the internal connection of the master ADC and the slave ADC.

Figure 1. Dual ADC bock diagram



3.3 From ADC to TIM

ADCx (x=1 to 4) provides the trigger event through watchdog signals to advanced-control timers (TIM1/TIM8/TIM20).

The output (from ADC) is on signals ADCx_AWDy_OUT (x = 1 to 4, y = 1 to 3 as there are three analog watchdogs per ADC) and the input (to timer) on signal TIMx_ETR (external trigger).

ADCx_AWDy_OUT is activated when the associated analog watchdog is enabled. This internal hardware signal is set when a guarded conversion is outside the programmed thresholds.

ADCx_AWDy_OUT signal is reset after the end of the next guarded conversion which is inside the programmed thresholds or when disabling the ADC (when setting ADDIS=1).

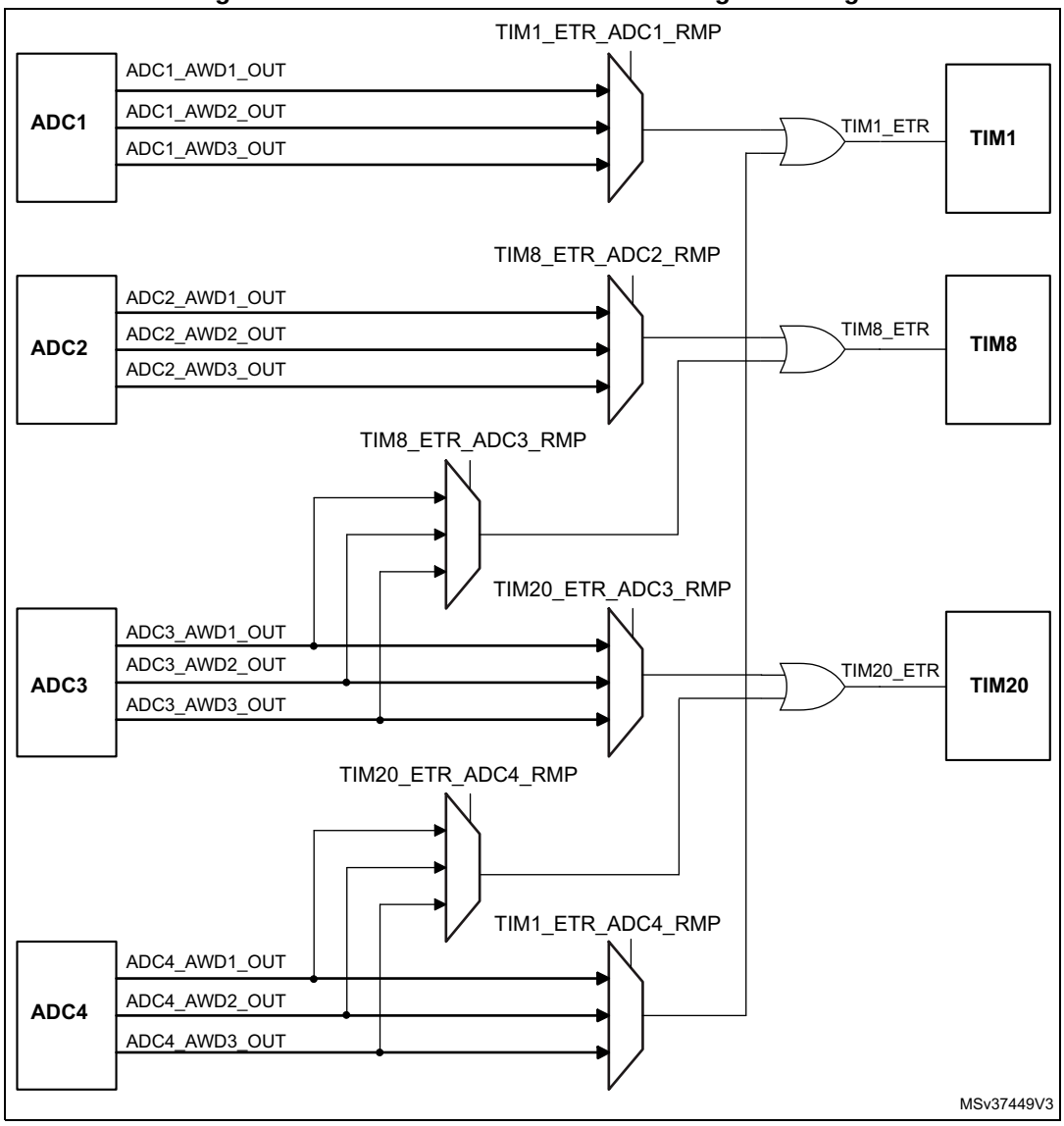
Table 4. TIM1/8/20_ETR connection to ADCx analog watchdogs(1)

	TIM1	TIM8	TIM20
ADC1	x		
ADC2		x	
ADC3		x	x
ADC4	x		x

1. x means that there is a connection. Table cells with gray shading indicate that there is no connection.

TIMx_ETR is connected to ADCx_AWDy_OUT through bits in TIMx_OR registers. *Figure 2* details the connections between TIMx and ADCx analog watchdogs.

Figure 2. TIMx connections to ADCx analog watchdogs



3.4 From TIM and EXTI to ADC

General-purpose timers (TIM2/TIM3/TIM4/TIM19), basic timers (TIM6/TIM7), advanced-control timers (TIM1/TIM8/TIM20), general-purpose timer (TIM15/TIM16/TIM17) and EXTI can be used to generate an ADC triggering event.

The output (from timer) is on signal TIMx_TRGO, TIMx_TRGO2 or TIMx_CCx event.

The input (to ADC) is on signal EXT[15:0] for regular channels and JEXT[15:0] for injected ones.

Table 5 details the connection between timers and ADCs for all STM32F3 series devices except STM32F37x.

Table 5. Internal signals from timers to ADCs(1)

	ADC1/ADC2	ADC3/ADC4
TIM1	TIM1_CC1 (Regular) TIM1_CC2 (Regular) TIM1_CC3 (Regular) TIM1_TRGO (Regular/Injected) TIM1_TRGO2 (Regular/Injected) TIM1_CC4 (Injected)	TIM1_CC3 (Regular/Injected) TIM1_TRGO (Regular/Injected) TIM1_TRGO2 (Regular/Injected) TIM1_CC4 (Injected)
TIM2	TIM2_CC2 (Regular) TIM2_TRGO (Regular/Injected) TIM2_CC1 (Injected)	TIM2_CC3 (Regular) TIM2_TRGO (Regular/Injected) TIM2_CC1 (Regular)
TIM3	TIM3_TRGO (Regular/Injected) TIM3_CC4 (Regular/Injected) TIM3_CC3 (Injected) TIM3_CC1 (Injected)	TIM3_TRGO (Regular/Injected) TIM3_CC1 (Regular)
TIM4	TIM4_CC4 (Regular) TIM4_TRGO (Regular/Injected)	TIM4_CC1 (Regular) TIM4_TRGO (Regular/Injected) TIM4_CC3 (Injected) TIM4_CC4 (Injected)
TIM6	TIM6_TRGO (Regular/Injected)	
TIM8	TIM8_TRGO (Regular/Injected) TIM8_TRGO2 (Regular/Injected) TIM8_CC4 (Regular/Injected)	TIM8_CC1 (Regular) TIM8_TRGO (Regular/Injected) TIM8_TRGO2 (Regular/Injected) TIM8_CC2 (Injected) TIM8_CC4 (Injected)
TIM15	TIM15_TRGO (Regular/Injected)	TIM15_TRGO (Regular/Injected)
TIM20	TIM20_TRGO (Regular/Injected) TIM20_TRGO2 (Regular/Injected) TIM20_CC1 (Regular) TIM20_CC2 (Regular) TIM20_CC3 (Regular)	TIM20_TRGO (Regular/Injected) TIM20_TRGO2 (Regular/Injected) TIM20_CC1 (Regular) TIM20_CC2 (Injected)
TIM7		TIM7_TRGO (Regular/Injected)

1. The gray shading in table cells means Not Applicable.

Table 6 shows the timers to ADC1 connections for STM32F37x devices.

Table 6. STM32F37x: Internal signals from timers to ADC1

	Regular channels	Injected channels
TIM2	TIM2_CC2	TIM2_TRGO TIM2_CC1
TIM3	TIM3_TRGO	TIM3_CC4
TIM4	TIM4_CC4	TIM4_TRGO
TIM19	TIM19_TRGO TIM19_CC3 TIM19_CC4	TIM19_CC1 TIM19_CC2

3.5 From OPAMP to ADC

There are two interconnection types:

- Connection of OPAMP output reference voltage to an internal ADC channel,
- Connection of OPAMPx (x = 1 to 4) output to ADCy (y = 1 to 4) channels.

1. Connection of OPAMP output reference voltage to an internal ADC channel.
   This connection can be used for OPAMP calibration.
   Table 7 provides information on the channels to use for the connections.

Table 7. VREFOPAMPx to ADC channel

VREFOPAMPx	ADC channel	Description
VREFOPAMP1	ADC1_IN15	Reference Voltage for the Operational Amplifier 1
VREFOPAMP2	ADC2_IN17	Reference Voltage for the Operational Amplifier 2
VREFOPAMP3	ADC3_IN17	Reference Voltage for the Operational Amplifier 3
VREFOPAMP4	ADC4_IN17	Reference Voltage for the Operational Amplifier 4

2. Connection of OPAMPx (x = 1 to 4) output to ADCy (y = 1 to 4) channels.
   Table 8 details the connection settings.

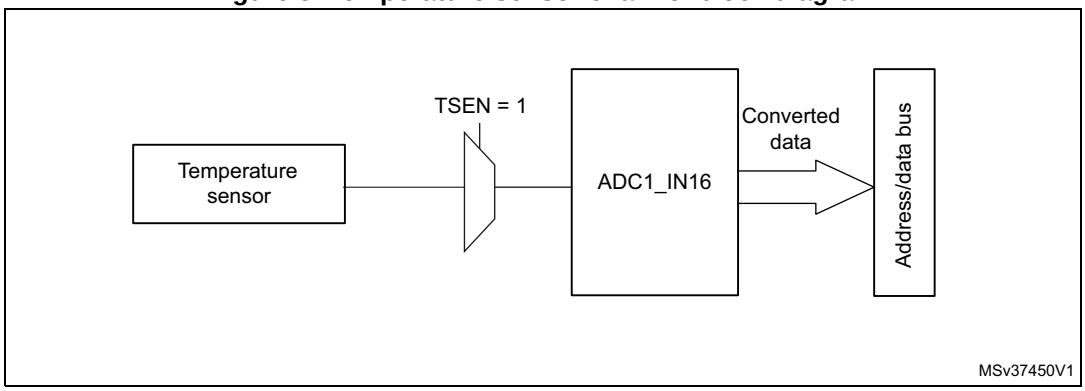
Table 8. OPAMP output to ADC input

OPAMPx output	ADC channel	Used pins
OPAMP1_VOUT	ADC1_IN3	PA2
OPAMP2_VOUT	ADC2_IN3	PA6
OPAMP3_VOUT	ADC3_IN1	PB1
OPAMP4_VOUT	ADC4_IN3	PB12

3.6 From TS to ADC

The internal temperature sensor (VTS) is connected internally to ADC1_IN16. *Figure 3* illustrates the connection between VTS and ADC1_IN16.

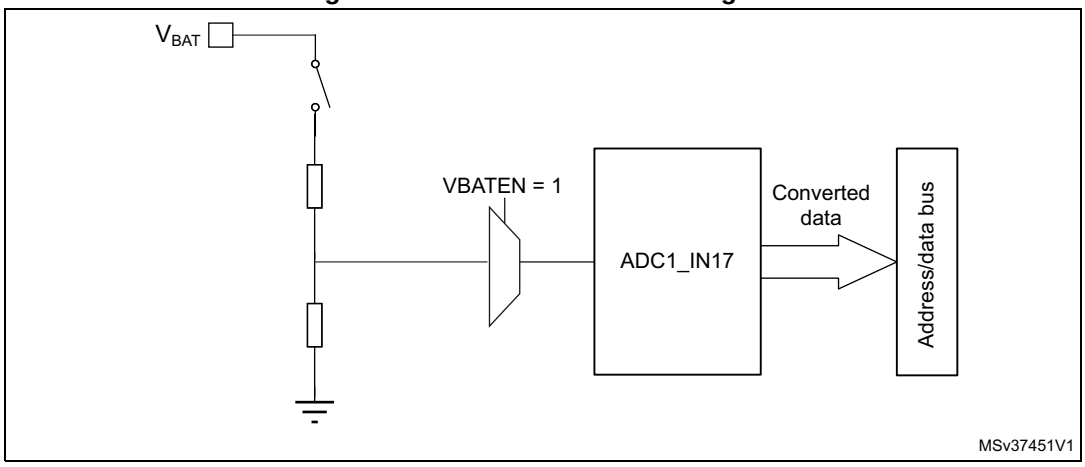
Figure 3. Temperature sensor channel block diagram



3.7 From VBAT to ADC

VBAT/2 output voltage can be converted using ADC1_IN17 as illustrated in *Figure 4*.

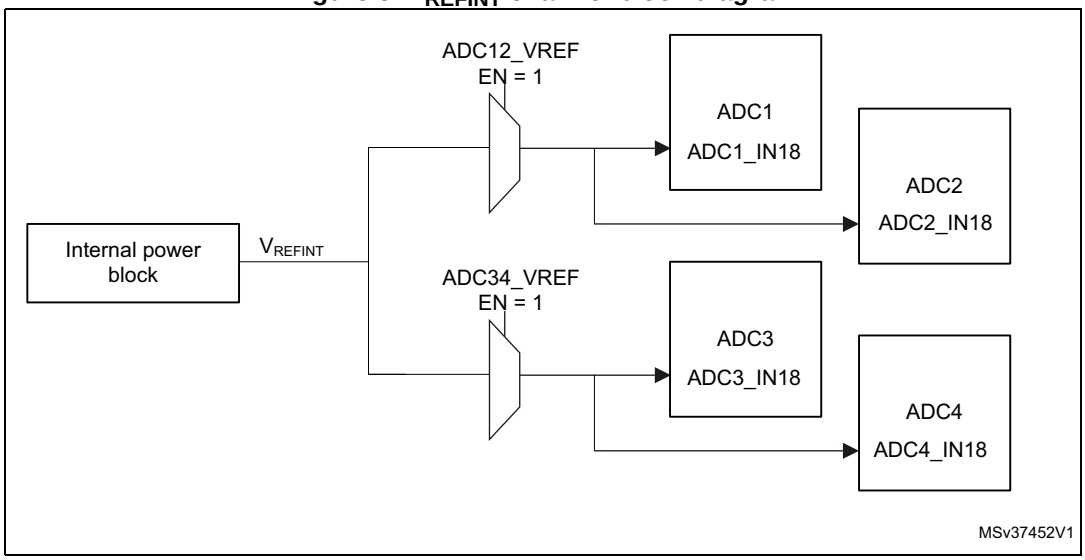
Figure 4. VBAT channel block diagram



3.8 From V_{REFINT} to ADC

V_{REFINT} is internally connected to channel 18 of the four ADCs. This allows the monitoring of its value. *Figure 5* shows the block diagram of the V_{REFINT} sensing feature.

Figure 5. V_{REFINT} channel block diagram



3.9 From COMP to TIM

The comparators outputs can be redirected internally to different timer inputs:

- break input 1/2 for fast PWM shutdowns,
- OCREF_CLR input,
- input capture .

The bit field COMPxOUTSEL in the COMPx_CSR register (COMP_CSR register for STM32F37x products) is used to select which timer input must be connected to the comparator output.

Table 9 lists the possible comparator output redirections to the timer inputs.

Table 9. Comparator outputs to TIM inputs(1)

COMP output selection										
	TIM1	**TIM8**	**TIM2**	**TIM3**	**TIM4**	**TIM5**	**TIM15**	**TIM16**	**TIM17**	**TIM20**
COMP1	TIM1_BRK_ACTH TIM1_BRK2 TIM1_OCrefClear TIM1_IC1	TIM8_BRK_ACTH TIM8_BRK2	TIM2_IC4 TIM2_OCrefClear	TIM3_IC1 TIM3_OCrefClear		TIM5_IC4 TIM5_OCrefClear	TIM15_BRK_ACTH (2)			TIM20_BRK_ACTH TIM20_BRK2
COMP2	TIM1_BRK_ACTH TIM1_BRK2 TIM1_OCrefClear TIM1_IC1	TIM8_BRK_ACTH TIM8_BRK2	TIM2_IC4 TIM2_OCrefClear	TIM3_IC1 TIM3_OCrefClear	TIM4_IC1 (2) TIM4_OCrefClear (2)			TIM16_BRK_ACTH(2)		TIM20_BRK_ACTH TIM20_BRK2 TIM20_OCrefClear
COMP3	TIM1_BRK_ACTH TIM1_BRK2 TIM1_OCrefClear	TIM8_BRK_ACTH TIM8_BRK2	TIM2_OCrefClear	TIM3_IC2	TIM4_IC1		TIM15_IC1 TIM15_BRK_ACTH			TIM20_BRK_ACTH TIM20_BRK2
COMP4	TIM1_BRK TIM1_BRK2	TIM8_BRK TIM8_BRK2 TIM8_OCrefClear		TIM3_IC3 TIM3_OCrefClear	TIM4_IC2		TIM15_OCrefClear TIM15_IC2			TIM20_BRK TIM20_BRK2

Table 9. Comparator outputs to TIM inputs(1)

COMP output selection										
	TIM1	**TIM8**	**TIM2**	**TIM3**	**TIM4**	**TIM5**	**TIM15**	**TIM16**	**TIM17**	**TIM20**
COMP5	TIM1_BRK_ACTH TIM1_BRK2	TIM8_BRK_ACTH TIM8_BRK2 TIM8_OCrefClear	TIM2_IC1	TIM3_OCrefClear	TIM4_IC3			TIM16_BRK_ACTH	TIM17_IC1	TIM20_BRK_ACTH TIM20_BRK2
COMP6	TIM1_BRK_ACTH TIM1_BRK2	TIM8_BRK_ACTH TIM8_BRK2 TIM8_OCrefClear	TIM2_IC2 TIM2_OCrefClear		TIM4_IC4			TIM16_OCrefClear TIM16_IC1		TIM20_BRK_ACTH TIM20_BRK2
COMP7	TIM1_BRK TIM1_BRK2 TIM1_OCrefClear TIM1_IC2	TIM8_BRK TIM8_BRK2 TIM8_OCrefClear	TIM2_IC3						TIM17_OCrefClear TIM17_BRK_ACTH	TIM20_BRK TIM20_BRK2

1. The gray shading in table cells means Not Applicable.
2. Only in STM32F37x devices.

Note: When the comparator output is configured to be connected internally to the timer break input, the following must be considered:

1/ COMP1/2/3/5/6 can be used to control TIM1/8/20_BRK_ACTH (this break is always active high with no digital filter) and also to control TIM1/8/20_BRK2 input.

2/ COMP4/7 can be used to control TIM1/8/20_BRK and the TIM1/8/20_BRK2 input.

3/ COMP3/5/7 can be used to control TIMx_BRK_ACTH, x=15;16;17 respectively (this break is always active high with no digital filter).

3.10 From TIM to COMP

For all STM32F3 series devices except STM32F37x devices, the timers output can be selected as comparators outputs blanking signals using the “COMPx_BLANKING” bits in “COMPx_CSR” register.

Table 10. Timer outputs used as comparators blanking sources(1)

	COMP blanking source						
	COMP1	**COMP2**	**COMP3**	**COMP4**	**COMP5**	**COMP6**	**COMP7**
TIM1	TIM1 OC5	TIM1 OC5	TIM1 OC5				TIM1 OC5
TIM8				TIM8 OC5	TIM8 OC5	TIM8 OC5	TIM8 OC5
TIM15				TIM15 OC1		TIM15 OC2	TIM15 OC2
TIM2	TIM2 OC3	TIM2 OC3	TIM2 OC4			TIM2 OC4	
TIM3	TIM3 OC3	TIM3 OC3		TIM3 OC4	TIM3 OC3		

1. The gray shading in table cells means Not Applicable.

3.11 From DAC to COMP

For all STM32F3 series devices except STM32F37x devices, the comparators inverting input may be a DAC channel output (DAC1_CH1 or DAC1_CH2). DAC2_CH1 may be selected for COMP2, COMP4 and COMP6 in case the device belongs to STM32F303x6/8 or STM32F328x8 families.

“COMPxINMSEL” bits value in “COMPx_CSR” register are used for the selection.

Table 11 details the interconnections between DAC and COMP.

Table 11. DAC output selection as comparator inverting input(1)

	COMP inverting inputs						
	COMP1(2)	**COMP2(2)**	**COMP3**	**COMP4**	**COMP5**	**COMP6**	**COMP7**
DAC1_CH1	X	X	X	X	X	X	X
DAC1_CH2	X	X	X	X	X	X	X
DAC2_CH1		X		X		X	

1. The gray shading in table cells means Not Applicable.
2. For STM32F37x products, COMP1 and COMP2 inverting input may be DAC1_CH1, DAC1_CH2 or DAC2_CH1 output. The selection is made based on COMPxINSEL (x=1,2) bits value in COMP_CSR register.

3.12 From VREFINT to COMP

Besides to the DAC channel output, Vrefint (x1, x3/4, x1/2, x1/4) can be selected as comparator inverting input using:

- COMPxINSEL bits in COMP_CSR register for STM32F37x devices,
- COMPxINMSEL bits in COMPx_CSR register for other STM32F3 devices.

3.13 From DAC to OPAMP

The DAC outputs are connected internally to OPAMP1, OPAMP3 and OPAMP4 non inverting inputs as shown in *Table 12*.

Table 12. DAC output selection as OPAMP non inverting input

	Non inverting input		
	OPAMP1	**OPAMP3**	**OPAMP4**
DAC channel	DAC1_CH2	DAC1_CH2	DAC1_CH1

3.14 From TIM to OPAMP

The selection of the OPAMP inverting and non-inverting inputs can be done automatically. In this case the switch from one input to another is done automatically. This automatic switch is triggered by the TIM1 CC6 output arriving on the OPAMP input multiplexers.

3.15 From TIM to TIM

Some STM32F3 timers are linked together internally for timer synchronization or chaining.

When one timer is configured in Master Mode, it can reset, start, stop or clock the counter of another timer configured in Slave Mode.

Depending on the selected synchronization mode, a configuration sequence is applied. This is detailed in the *Timer synchronization* chapter in the reference manuals.

The slave mode selection is made using “SMS” bits in the selected timer slave mode control register (TIMx_SMCR).

Table 13 presents the possible master/slave connections and indicates the internal trigger connection in each case.

Table 13. Timers synchronization(1)

Master/ Slave		SLAVE									
		TIM1	**TIM8**	**TIM20**	**TIM2**	**TIM3**	**TIM4**	**TIM15**	**TIM5**	**TIM19**	**TIM12**
MASTER	**TIM1**		TIM8_ ITR0	TIM20_ ITR0	TIM2_ ITR0	TIM3_ ITR0	TIM4_ ITR0				
	TIM8			TIM20_ ITR1	TIM2_ ITR1		TIM4_ ITR3				
	TIM2	TIM1_ ITR1	TIM8_ ITR1			TIM3_ ITR1	TIM4_ ITR1	TIM15_ ITR0	TIM5_ ITR0	TIM19_ ITR0	
	TIM3	TIM1_ ITR2	TIM8_ ITR3		TIM2_ ITR2		TIM4_ ITR2	TIM15_ ITR1	TIM5_ ITR1	TIM19_ ITR1	
	TIM4	TIM1_ ITR3	TIM8_ ITR2	TIM20_ ITR2	TIM2_ ITR3(2)	TIM3_ ITR3(2)			TIM5_ ITR2		TIM12_ ITR0
	TIM5					TIM3_ ITR2					TIM12_ ITR1
	TIM13										TIM12_ ITR2
	TIM14				TIM2_ ITR3	TIM3_ ITR3					TIM12_ ITR3
	TIM15	TIM1_ ITR0		TIM20_ ITR3	TIM2_ ITR1 (3)	TIM3_ ITR2(3)	TIM4_ ITR3 (3)		TIM5_ ITR3	TIM19_ ITR2	
	TIM16							TIM15_ ITR2		TIM19_ ITR3	
	TIM17	TIM1_ ITR3						TIM15_ ITR3			
	TIM19				TIM2_ ITR0	TIM3_ ITR0	TIM4_ ITR0				

1. The gray shading in table cells means Not Applicable.
2. Not applicable for STM32F37x.
3. Only for STM32F37x.

3.16 From system errors to TIM

Besides the comparators outputs, there are other sources that may be used as trigger for the internal break events of some timers (TIM1/TIM8/TIM20/TIM15/TIM16/TIM17). These sources are:

- the clock failure event generated by the clock security system (CSS),
- the PVD output (this feature is not available in STM32F3x8 devices),
- the SRAM parity error signal,
- the Cortex-M4 LOCKUP (Hardfault) output.

The above-mentioned sources can be connected internally to TIMx_BRK_ACTH input, with x = 1,8,15,16,17,20.

The purpose of the break function is to protect power switches driven by PWM signals generated by the timers.

3.17 From HSE, HSI, LSE, LSI, MCO, RTC to TIM

For all STM32F3 series devices except STM32F37x devices, TIM16 can be used for the measurement of internal/external clock sources. TIM16 channel1 input capture is connected to HSE/32, GPIO, RTC clock and MCO to output clocks among (HSE, HSI, LSE, LSI, SYSCLK, PLLCLK, PLLCLK/2).

The selection is performed through the TI1_RMP [1:0] bits in the TIM16_OR register.

This allows calibrating the HSI/LSI clocks.

TIM14 is used in STM32F37x devices for the same purpose.

3.18 From TIM and EXTI to DAC

A timer counter can be used as a trigger for DAC conversions.

The TRGO event is the internal signal that will trigger conversion.

Table 14 provides a summary of DAC interconnections with timers.

Table 14. Timer and EXTI signals triggering DAC conversions(1)

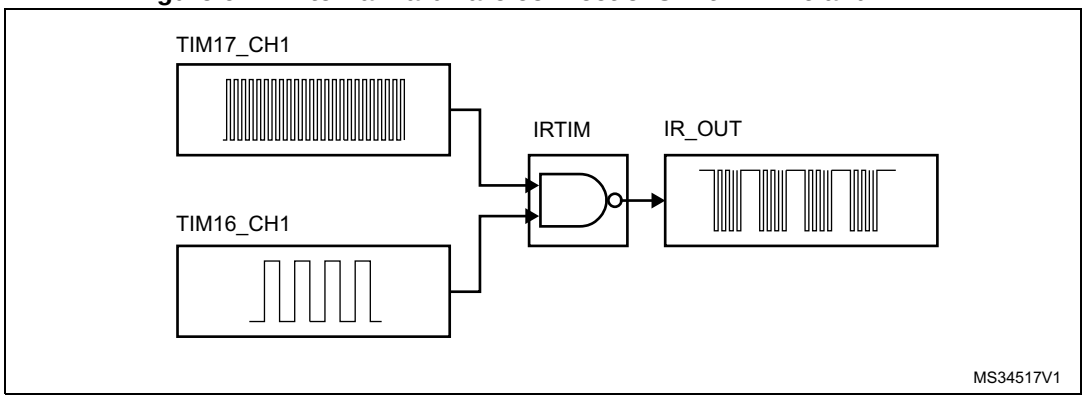
	DAC1	DAC2
TIM8	x	
TIM2	x	x
TIM3	x	x
TIM4	x	x(2)
TIM6	x	x
TIM7	x	x
TIM15	x(3)	x(3)
TIM18		x
EXTI line9	x	x

1. The gray shading in table cells means Not Applicable.
2. Only for STM32F37x devices.
3. Not applicable for STM32F37x.

3.19 From TIM to IRTIM

General-purpose timers (TIM16/TIM17) output channels TIMx_OC1 are used to generate the waveform of infrared signal output.

Figure 6. IR internal hardware connections with TIM16 and TIM17



3.20 From TIM and EXTI to SDADC

General-purpose timers (TIM2, TIM3, TIM4, TIM12, TIM13, TIM14, TIM15, TIM16, TIM17, TIM19), EXTI11 and EXTI15 can be used to generate a SDADC triggering event for injected conversions selection.

Table 15 details the connection between timers and SDADCs.

Table 15. Internal signals from timers to SDADCs(1)

	SDADC1	SDADC2	SDADC3
TIM2		TIM2_CH3	TIM2_CH4
TIM3	TIM3_CH1	TIM3_CH2	TIM3_CH3
TIM4	TIM4_CH1	TIM4_CH2	TIM4_CH3
TIM12		TIM12_CH1	TIM12_CH2
TIM13	TIM13_CH1		
TIM14	TIM14_CH1		
TIM15	TIM15_CH2		
TIM16			TIM16_CH1
TIM17		TIM17_CH1	
TIM19	TIM19_CH2	TIM19_CH3	TIM19_CH4

1. The gray shading in table cells means Not Applicable.

3.21 From ADC to HRTIM1

ADCx (x=1, 2) provides the trigger event through watchdog signals to the high resolution timer HRTIM1.

Table 16. HRTIM1_EEx connection to ADC analog watchdogs

	Feature	HRTIM1 event
ADC1	ADC1_AWD1	HRTIM1_EEV1
	ADC1_AWD2	HRTIM1_EEV2
	ADC1_AWD3	HRTIM1_EEV3
ADC2	ADC2_AWD1	HRTIM1_EEV4
	ADC2_AWD2	HRTIM1_EEV5
	ADC2_AWD3	HRTIM1_EEV6

3.22 From system faults to HRTIM1

The HRTIM1 system fault input (SYSFLT) gathers MCU internal fault events coming from:

- the clock failure event generated by the clock security system (CSS),
- the PVD output,
- the SRAM parity error signal,
- the Cortex-M4 LOCKUP (Hardfault) output.

3.23 From COMP to HRTIM1

The comparator output can be redirected internally to HRTIM1 inputs.

The comparator outputs are connected directly to HRTIM1 in order to speed-up the propagation delay.

Table 17. Comparator outputs to HRTIM1 inputs

COMP#	Internal events
COMP2	HRTIM1_EEV1 HRTIM1_EEV6 HRTIM1_FLT1
COMP4	HRTIM1_EEV2 HRTIM1_EEV7 HRTIM1_FLT2
COMP6	HRTIM1_EEV3 HRTIM1_EEV8 HRTIM1_FLT3

3.24 From OPAMP to HRTIM1

The OPAMP2_VOUT can be used as a HRTIM1 internal event source connected to HRTIM1_EEV4 or HRTIM1_EEV9.

In this case, the software must set OPAMP2_DIG as of PA6 alternate function (AF13) to redirect OPAMP2_VOUT signal to the HRTIM1 external events through the Schmitt trigger.

3.25 From TIM to HRTIM1

The table below summarizes the list of possible connections between timers and HRTIM1.

Table 18. Internal signals from timers to HRTIM1

Timer signal	HRTIM1 signal	Description
TIM1_TRGO	HRTIM1_EEV1	Internal event
TIM2_TRGO	HRTIM1_EEV2	Internal event
TIM3_TRGO	HRTIM1_EEV3	Internal event
TIM6_TRGO	HRTIM1_EEV6	Internal event
	UPD_EN3	Update enable 3
TIM7_TRGO	HRTIM1_EEV7	Internal event
	BMTRIG	Burst mode trigger event
	BMCLK3	Burst mode clock
TIM15_TRGO	HRTIM1_EEV9	Internal event
TIM16_OC	UPD_EN1	Update enable 1
	BMCLK1	Burst mode clock
TIM17_OC	UPD_EN2	Update enable 2
	BMCLK2	Burst mode clock

3.26 From HRTIM1 to ADC

The high resolution timer can be used to generate an ADC trigger event.

The output from HRTIM1 is on signal HRTIM1_ADCTRG1/2/3/4.

The input (to ADC) is on signal EXT[15:0] for regular channels and JEXT[15:0] for injected ones.

Table 19 details the connection between HRTIM1 and ADCs.

Table 19. Internal signals from HRTIM1 to ADCs

	ADC1/2 regular channels	ADC1/2 injected channels
HRTIM1	HRTIM1_ADCTRG1 event HRTIM1_ADCTRG3 event	HRTIM1_ADCTRG2 event HRTIM1_ADCTRG4 event

3.27 From HRTIM1 to DAC

Besides the timers events and the external interrupt line, the HRTIM1 DACTRGx events can be selected as internal signals to trigger DAC conversion depending on the value of TSELx[2:0] control bits in DAC_CR register.

Table 20. HRTIM1 signals triggering DAC conversions

	DAC1	DAC2
HRTIM1	HRTIM1_DACTRG1 event HRTIM1_DACTRG2 event	HRTIM1_DACTRG3 event

4 Revision history

Table 21. Document revision history

Date	Revision	Changes
20-Mar-2015	1	Initial release.