Cycling endurance and data retention of STMicroelectronics EEPROMs

Introduction

Electronic applications, based on several single electronic products (integrated circuits) are looking for a global high level of reliability and robustness, each single electronic product must therefore offer a very high level of quality.

To fulfill these requirements STMicroelectronics developed the family of CMOSF8H EEPROM and now upgrade it with a new improved architecture with the CMOSF9V process.

This application note details the improved cycling and data retention performances of the STMicroelectronics EEPROM industrial range 6 (temperature range -40°C to +85°C) products, listed in Table 1.

Table 1. Applicable products

Type	Serial interface	Root part numbers
Standard serial EEPROM	I2C bus	M24256-BF, M24256-BR, M24256-BW, M24256-DF, M24256-DR, M24256E-F, M24256X-F-M24256E-U, M24256X-G
		M24512-DF, M24512-R, M24512-W, M24512E-F, M24512E-U
		M24M01-DF, M24M01-R, M24M01E-F, M24M01X-F, M24M01E-U
		M24M02-DR, M24M02E-F, M24M02E-U
	SPI bus	M95256-DF, M95256-R, M95256-W
		M95512-DF, M95512-R, M95512-W
		M95M01-DF, M95M01-R, M95M01E-F
		M95M02-DR, M95M02E-F
		M95M04-DR

1 Cycling endurance

This section intends to offer all details concerning the cycling capabilities of the high-density EEPROMs based on the CMOSF8H & CMOSF9V process technologies, industrial range 6 (temperature range -40°C to +85°C).

1.1 Cycling values specified in high-density EEPROM datasheets

Table 2. CMOS F8H process devices (-40°C to +85°C)

Root part numbers	Number of cycles for each cell
M24256-BF, M24256-BR, M24256-BW, M24256-DF, M24256-DR, M24256E-F, M24256X-F-M24256E-U, M24256X-G	4 million cycles (at 25°C) 1.2 million cycles (at 85°C)
M24512-DF, M24512-R, M24512-W, M24512E-F, M24512E-U	
M24M01-DF, M24M01-R, M24M01E-F, M24M01X-F, M24M01E-U	
M24M02-DR, M24M02E-F, M24M02E-U	
M95256-DF, M95256-R, M95256-W	
M95512-DF, M95512-R, M95512-W	
M95M01-DF, M95M01-R, M95M01E-F	
M95M02-DR, M95M02E-F	
M95M04-DR	

1.2 High-density EEPROM cycling performances

1.2.1 Cycling and temperature dependence

Note:
- ***Cycle** = Internal write cycle executed inside the EEPROM.*
- ***Cycling** = cumulated number of write cycles*

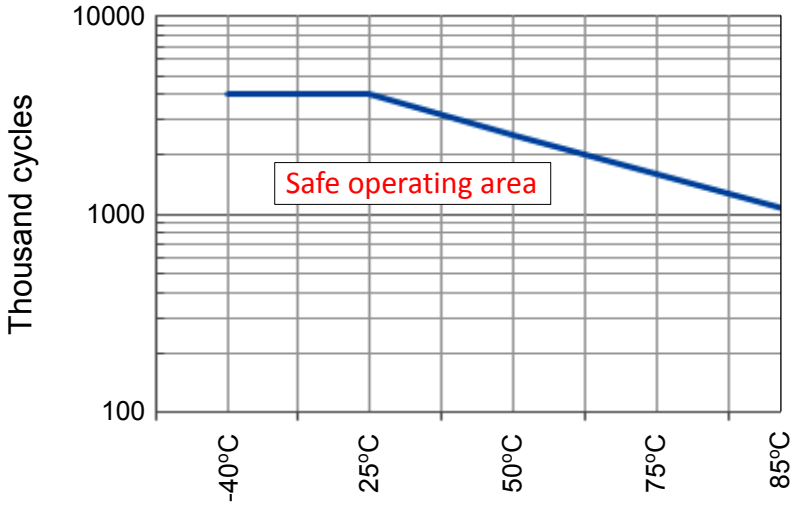
As specified in the related datasheets, the cycling endurance depends on the operating temperature (and is independent of the value of the supply voltage): The higher the temperature, the lower the cycling performance.

This safe cycling operating area can be represented by the following equation and/or by Figure 1

$$Number\ of\ cycles = 4\ Million * e^{(k * (t° - 25))}$$

Where:
- k = 0.018971
- t° is defined in celsius degree and is greater than +25°C

Figure 1. **Safe cycling operating conditions (per byte) vs. temperature**



Note: For temperatures lower than 25°C, the safe operating conditions are considered as 4 million cycles (the real limit is actually higher).

For a robust application design, the safe cycling operating area shown in Figure 1 has to be considered as a maximum cycling value for each byte of the memory, going above this safe operating area is not recommended.

Note: On CMOSF8H & CMOSF9V devices, the cycling limits (wear-out) observed during the internal qualification are much more above the safe conditions offered in Figure 1.

1.2.2 Cycling qualification method

The qualification procedure identifies the cell cycling intrinsic performance over the full temperature range.

Note: intrinsic = belonging to the essential nature or constitution of the EEPROM die
(extrinsic = originating from random event)

During the qualification phase, the parts are cycled and then read in order to locate eventual failing bit.
In STMicroelectronics, the intrinsic failure criterion is defined as 1 failing cell (or less) over 10 million cells.

1.2.3 Overall number of write cycles

When evaluating the cycling performances of an application, it must be stressed out that the number of cycles can be defined either for each memory cell or for the overall number of cycles decoded by the whole memory:

- The max cycling value defined in the datasheet is the max number of cycles for each byte;
- The overall number of cycles is the number of cycles correctly decoded and executed by the device, spread over all addressed locations in the memory.

The characterization trials performed on high density CMOSF8H & CMOSF9V process products have demonstrated that the overall number of write cycles can reach 1 Billion without failure, at 25°C (test performed on M95M01, 1Mbit device).

1.3 Cycling strategy

1.3.1 Cycling strategy and application temperature profile

To ensure the safest EEPROM cycling conditions, it is recommended to evaluate the number of write cycles and the relative temperature profile of the cycling performed by the EEPROM during the life of the application, that is:

- Define the main temperature ranges at which the EEPROM is operating in the end application.
- For each temperature range, estimate the number of write cycles executed for each data block.
- For each data block (with different cycling profiles), calculate the cumulated cycling effect using the following equation or Table 3 .

$$\sum_{i=1}^{n} \frac{Number\ of\ cycles\ at\ temp(i)}{Max\ number\ of\ cycles\ specified\ at\ temp(i)} \leq 1$$

Table 3. Application cycling profile evaluation

Temperature	Number of cycles(2)	% of the max cycling value specified in Table 2
25°C	w	(w/4M) x 100 = a %
85°C	y	(y/1.2M) x 100 = b%
Total	w + y	(a + b) %

Note:
1. *The table can be adapted according to the temperature profile by taking care of putting down the maximum cycling for each temperature.*
2. *w and y are the forecast number of cycles for a specific data block.*

If the total percentage of cumulated cycles (last row in Table 3) is lower than 100%, the data stored in the EEPROM are safely cycled.

If the total percentage of cumulated cycles is above 100%, the intrinsic safe margin for cycling is exceeded and a data relocation strategy must be defined. This can be done by distributing the number of cycles over several memory locations as follows:

- Define a cycling limit for each data block according to the application needs and product performance (as shown in Table 3).
- Count the numbers of cycles executed on each data block (counter value can be stored in the EEPROM).
- When the counter exceeds the defined limit, the cycled data block must be relocated to another physically independent memory address. The software developer should define this new data block to be duplicated in a location inside a different page and, when possible, not with the same byte address inside the new page. The counter itself must also be stored in a new location.

In addition, to optimize the number of cycles in the EEPROM and keep the other data blocks safe in the memory array:

- Define data classes (located in the same page) where data with similar update rates are gathered. This optimizes the use of the Page mode instead of the byte mode.
- The areas containing the read-only parameters and the cycled items should be separated and made as much as possible independent from each other. Two types of data should not share the same pages and, where possible, the same locations inside the related page.

1.3.2 Cycling with error correction code (ECC)

The CMOSF8H & CMOSF9V process high-density devices offer an error correction code (ECC) logic.

The ECC logic is implemented on each group of four EEPROM bytes(c). Inside a group, if a single bit out of the four bytes happens to be erroneous during a Read operation, the ECC detects this bit and replaces it with the correct value. The read reliability is therefore much improved.

Even if the ECC function is performed on groups of four bytes, a single byte can be written/cycled independently. In this case, the ECC function also writes/cycles the three other bytes located in the same group. As a consequence, the maximum cycling budget is defined at group level and the cycling can be distributed over the four bytes of the group: the sum of the cycles seen by byte0, byte1, byte2, and byte3 of the same group must remain below the maximum value defined in Table 3. Application cycling profile evaluation.

2 Data retention

This section intends to offer all details concerning the data retention capabilities of the high-density EEPROM based on CMOSF8H and CMOSF9V process, industrial range 6 (temperature range -40°C to +85°C).

Note: ***Data retention***

At t_0, bytes are written after what no Write is executed on these bytes. The data retention time is the time after t0 during which the bytes can still be correctly read (the EEPROM devices being DC supplied or not).

2.1 Data retention values specified in high-density devices datasheets

Table 4. Data retention for high-density devices

Root part numbers	Data retention
M24256-BF, M24256-BR, M24256-BW, M24256-DF, M24256-DR, M24256E-F, M24256X-F-M24256E-U, M24256X-G	More than 200 years at 55°C
M24512-DF, M24512-R, M24512-W, M24512E-F, M24512E-U	
M24M01-DF, M24M01-R, M24M01E-F, M24M01X-F, M24M01E-U	
M24M02-DR, M24M02E-F, M24M02E-U	
M95256-DF, M95256-R, M95256-W	
M95512-DF, M95512-R, M95512-W	
M95M01-DF, M95M01-R, M95M01E-F	
M95M02-DR, M95M02E-F	
M95M04-DR	

2.2 Data retention performance

2.2.1 Data retention and temperature dependence

The data retention is temperature dependent and is independent of the value of V_{CC}: the higher is the temperature, the lower is the data retention time.

The data retention safe values are:

- more than 200 years (at 55°C or less);
- more than 50 years (at 85°C).

Note: For M95M04-DR, 40 years at 55°C (or less) and 10 years at 85°C.

2.2.2 Data retention qualification method

The data retention qualification procedure checks that the data written into the EEPROM remain readable with a safe programming level. The STMicroelectronics qualification method is the following:

- The part is stored in an oven at 250°C during 1000h (or during an equivalent time/temperature combination), with no DC voltage on pin V_{CC}.
- The part content is then checked.

The data retention follows an Arrhenius law, this allows to extrapolate, from the different qualification tests performed at different temperatures, the data retention limits.These limits are above the safe value defined in datasheets.

2.3 Data retention strategy in the end application

The data retention time is defined in the datasheets with specific temperatures. To ensure the safest EEPROM data retention, evaluate the amount of time during which the end application remains within some temperature range to evaluate the data retention profile. To do so:

- Define the time (in years) during which the EEPROM remains inside each temperature range (that is a typical temperature profile of the end application),
- Estimate the data retention value, in percentage, for each temperature range, as defined in the equation below, or in Table 5.

$$\sum_{i=1}^{n} \frac{Number\ of\ years\ at\ temp(i)}{Max\ number\ of\ years\ specified\ at\ temp(i)} \leq 1$$

Table 5. Data retention profile evaluation example

Temperature	Data retention (max)	Application ambient temperature in years(2)	Data retention capability percentage
55°C	V = 200 years	v	(v/V) x 100 = a
85°C	W = 50 years	w	(w/W) x 100 = b
Total		v + w	(a + b)

Note:
1. *The table can be adapted according to the temperature profile by taking care of putting down the maximum cycling for each temperature.*
2. *v and w are the forecasted number of years for a specific data block.*

Example

An EEPROM is used in an application with a temperature profile defined as:

- 10 years at 85°C, that is 20% of the max data retention time at 85°C.
- 20 years at 55°C, that is 10% of the max data retention time at 55°C.

The data will be safe for 30 years, with only 30% of data retention capability (10 years + 20 years is 30 years, with 20% + 10% = 30% of data retention capability): this simple example demonstrates the excellent data retention capability of the CMOSF8H & CMOSF9V process EEPROMs.

Revision history

Table 6. **Document revision history**

Date	Version	Changes
23-Feb-2015	1	Initial release.
04-Feb-2026	2	• General document update. • Addition of products manufactured in CMOSF9V.

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