AN4674
Application note

SRK2001 adaptive synchronous rectification controller for LLC resonant converter evaluation board family

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Introduction

The STEVAL-SRK2001 in *Figure 1* is a family of demonstration boards intended for evaluation of SRK2001 controller in LLC resonant converters with synchronous rectification (SR) at secondary side of a center-tap transformer.

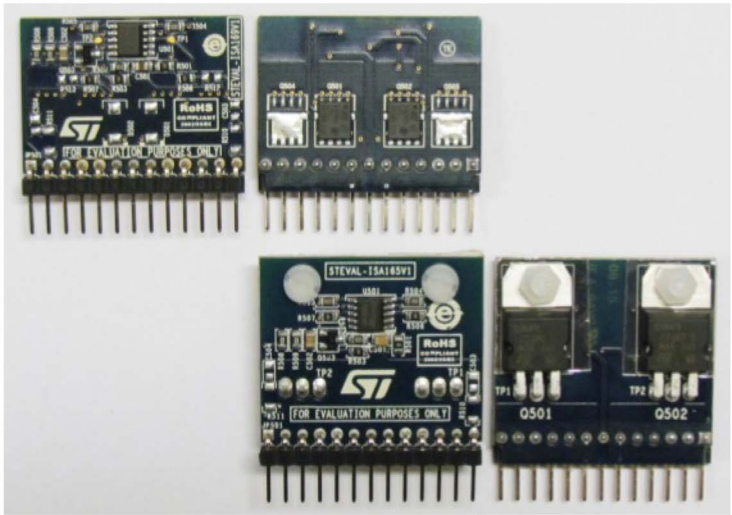
The first part of this note is a brief description of the IC features. The second part is dedicated to board description and implementation on an existing LLC converter. Finally, some consideration about circuit/layout optimization and thermal aspects are reported.

The board layout was realized in two different configurations depending on the mounted SR MOSFET package. The version with the STL140N4LLF5 type MOSFET is available both with standard and logic level SR controller (SRK2001 and SRK2001L respectively). The various board codes are reported in *Table 1*.

Table 1. Demonstration board ordering codes

Ordering code	SR MOSFET P/N	MOSFET package	MOSFET		Controller
			V_{DSS}	R_{DS_on}	
STEVAL-ISA165V1	STP120N4F6	TO220	40 V	4.3 mΩ	SRK2001
STEVAL-ISA166V1	STP77N6F6	TO220	60 V	7.0 mΩ	SRK2001
STEVAL-ISA167V1	STL85N6F3	PowerFLAT	60 V	6.5 mΩ	SRK2001
STEVAL-ISA168V1	STL140N4LLF5	PowerFLAT	40 V	2.75 mΩ	SRK2001
STEVAL-ISA169V1	STL140N4LLF5	PowerFLAT	40 V	3.1 mΩ	SRK2001L

Figure 1. STEVAL-SRK2001 - adaptive SR control for LLC resonant converter



GSPG2703151110SG

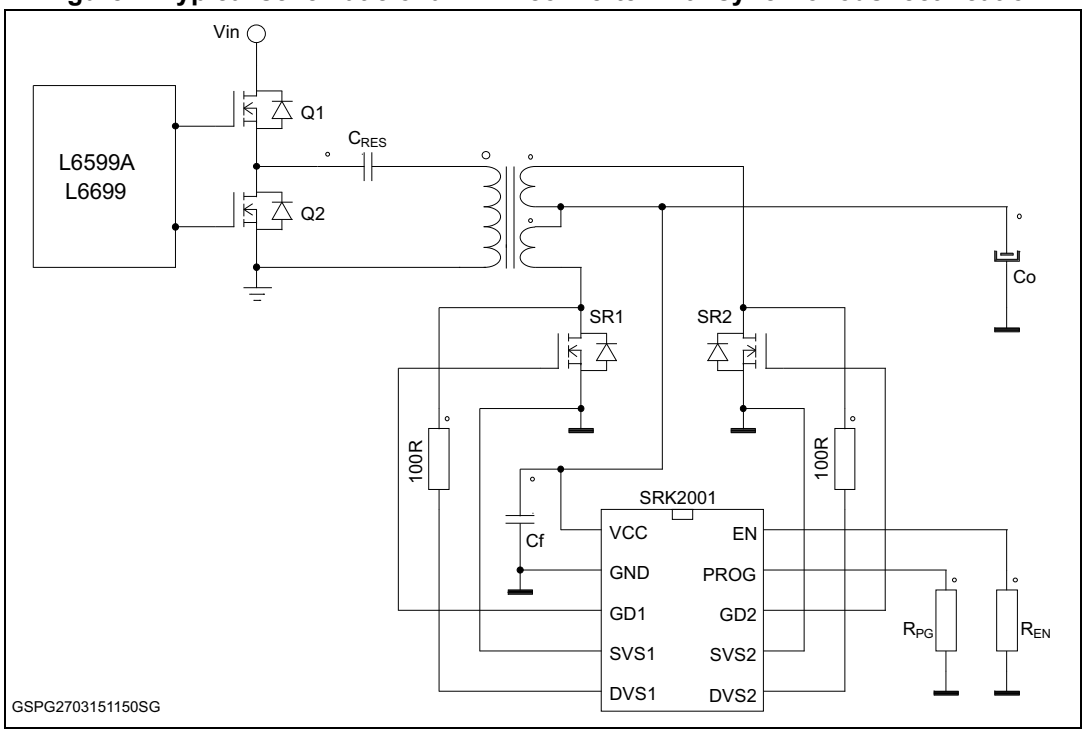
Contents

1 SRK2001 main characteristics

SRK2001 main features are described below. The values of the parameters mentioned in the following text are reported in the SRK2001 datasheet - *1.* in *Section 7: References on page 24*.

The SRK2001 implements a control scheme specific for secondary-side synchronous rectification in LLC resonant converters that use a transformer with center-tap secondary winding for full-wave rectification (refer to typical application schematic in *Figure 2*). It provides two high-current gate-drive outputs, each capable of driving one or more N-channel power MOSFETs in parallel. Each gate driver is controlled separately and an interlock logic circuit prevents the two synchronous rectifier MOSFETs from conducting simultaneously.

Figure 2. Typical schematic of an LLC converter with synchronous rectification



1.1 MOSFET drain-source voltage sensing and driving logic

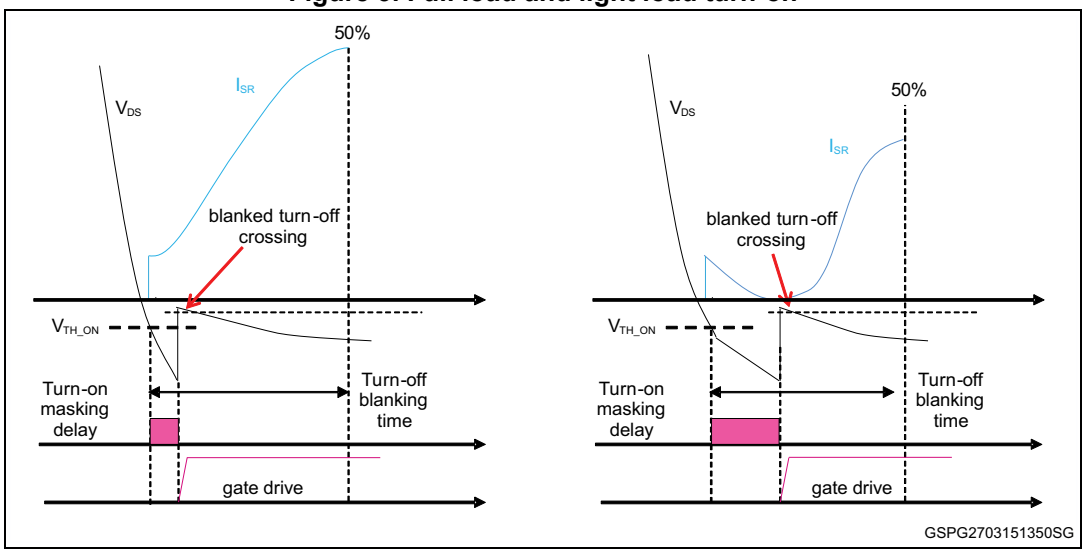
The IC core function is switching on each synchronous rectifier MOSFET whenever the corresponding transformer half-winding starts conducting (i.e. when the MOSFET body diode starts conducting) and then switching it off when the flowing current approaches zero. For this purpose, the IC is provided with two couples of pins (DVS1-SVS1 and DVS2-SVS2 Kelvin sensing), able to sense the MOSFET drain-source voltage level. Because each MOSFET is turned on when its body diode is conducting, zero voltage switching (ZVS) is achieved at turn-on. The same ZVS operation is found obviously also at turn-off.

Device operation bases on adaptive algorithms for both turn-on and turn-off and is described below (refer to device datasheet *1.* in *Section 7: References on page 24* for further details).

1. Adaptive turn-on:

When the current ISR starts flowing through the body diode, the voltage across the MOSFET drain-source becomes negative; as it reaches the negative threshold V_{TH_ON}, (refer to *Figure 3*), the power MOSFET is switched on: to avoid false triggering, an adaptive delay T_{D_On} is inserted: this is minimum at high load ($T_{D\_On\_min}$) and is progressively increased (adapted) at light loads (up to $T_{D\_On\_max}$, equal to 40% of half the switching cycle), this in order to prevent premature turn-on triggered by capacitive current pulses and not really by current through the body diode.

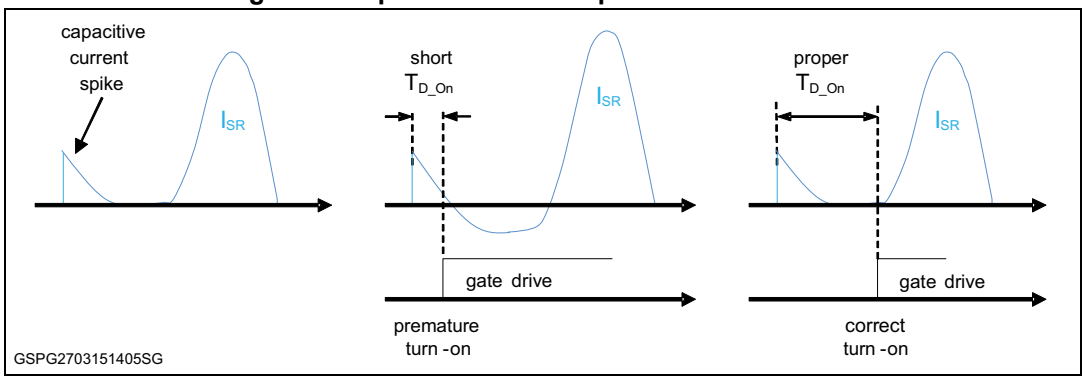
Figure 3. Full load and light load turn-on



In fact, premature turn-on at light load due to capacitive current spikes would cause undesired current inversions that, in turn, would affect efficiency (see *Figure 4*).

Turn-on is allowed only during the first 50% of half the switching cycle for either MOSFET.

Figure 4. Capacitive current spike effect at turn-on



2. Adaptive turn-off:

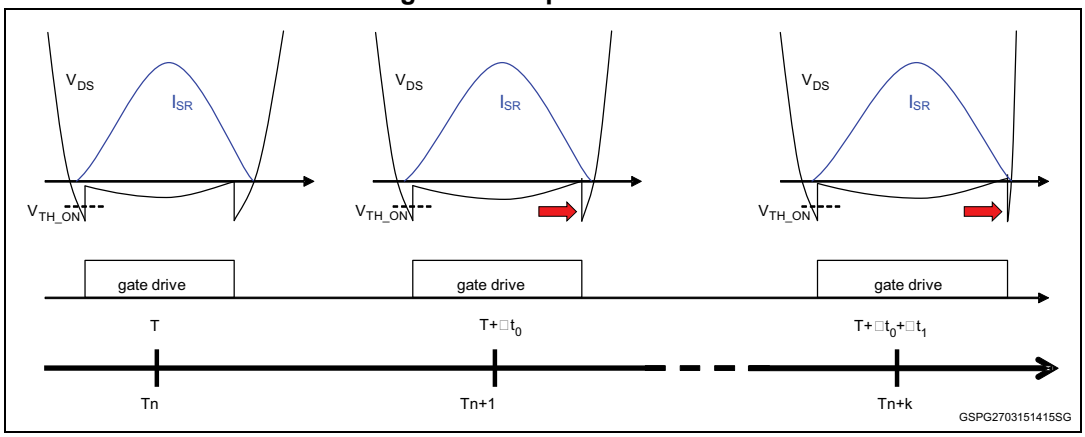
The sensed drain-source voltage is not really proportional to the current flowing through the MOSFET: in fact, after turn-on, it is the summation of the drop across R_{DS_ON} and the drop across the stray inductance, always present in series to the MOSFET (mainly its package inductance). Therefore, the sensed drain-source signal always anticipates the time instant where flowing current reaches zero and would cause a premature turn-off in case the circuit based on a simple comparator.

The adaptive turn-off algorithm (refer to *Figure 5*) overcomes this problem by progressively changing the turn-off time instant to get the maximum conduction period (minimizing the residual conduction of the MOSFET body diode, after turn-off, to T_{diode_off}). The adaptive turn-off is blanked during the first 50% of half the switching cycle (see *Figure 3*).

3. ZCD_OFF comparator turn-off:

Turn-off is prevalently managed by adaptive algorithm in steady state operation or during slow load variations. During fast load transitions or during above resonance operation, a further turn-off mechanism is available, which bases on a ZCD_OFF comparator with self-adaptive threshold and triggers the gate drive circuit for a very fast MOSFET turn-off (with a total delay time T_{D_Off}). The ZCD_OFF comparator is blanked for 450 ns after turn-on.

Figure 5. Adaptive turn-off



During converter start-up phase and on sleep-mode exiting, the control circuit starts turning on the SR MOSFETs at 30% of half the switching cycle and turning off at 50% and then it progressively adapts the driving in order to maximize the SR MOSFET conduction time. This helps reducing system perturbations, both during start-up and while exiting sleep-mode during a fast zero to full load transition.

Adaptive turn-on and turn-off algorithms allow maximizing efficiency in each load condition and doesn't need any external component for compensating circuit stray inductance, thus allowing a very low component count with consequent saving in BOM cost and PCB space.

In order to avoid current inversions, the SRK2001 stops driving the SR MOSFETs during any operating condition where the converter enters deeply into below resonance region (i.e. switching frequency gets lower than 60% of resonance frequency).

1.2 Light load operation and EN-PROG programming pins

At the reduced load the SRK2001 provides the user with various operating modes that can be programmed through EN and PROG pins. In each of these modes, the IC enters a low consumption state that allows to be compliant with the most stringent energy save standards and no-load consumption requirements.

1. Automatic sleep-mode operation:

It is selected by setting R_{EN} equal to 100 kΩ or 180 kΩ: by reducing the load, the controller enters sleep-mode when the SR MOSFET duty cycle is detected lower than D_{OFF} for 512 consecutive half switching cycles; then, as the load increases, it exits sleep-mode when the MOSFET body diode conduction duty cycle exceeds D_{ON}. Duty cycle values for D_{OFF} and D_{ON} are selected by R_{EN} and RPG resistors according to *Table 2*.

Table 2. Automatic sleep-mode programming

R_{EN} = 100 kΩ => D_{OFF} = 40%		R_{EN} = 180 kΩ => D_{OFF} = 25%	
R_{PG}	D_{ON}	R_{PG}	D_{ON}
Zero	80%	Zero	75%
100 kΩ	75%	100 kΩ	70%
180 kΩ	65%	180 kΩ	60%
Open	60%	open	55%

2. Burst-mode from primary side controller:

With R_{EN} = open, automatic sleep-mode is disabled and the IC enters low consumption state when it detects switching activity stop (as primary controller enters burst-mode). On switching activity resuming, the SRK2001 recovers operation when the SR MOSFET body diode conduction duty cycle becomes higher than D_{ON}. Duty cycle value for D_{ON} is selected by R_{PG} resistor according *Table 3* to below.

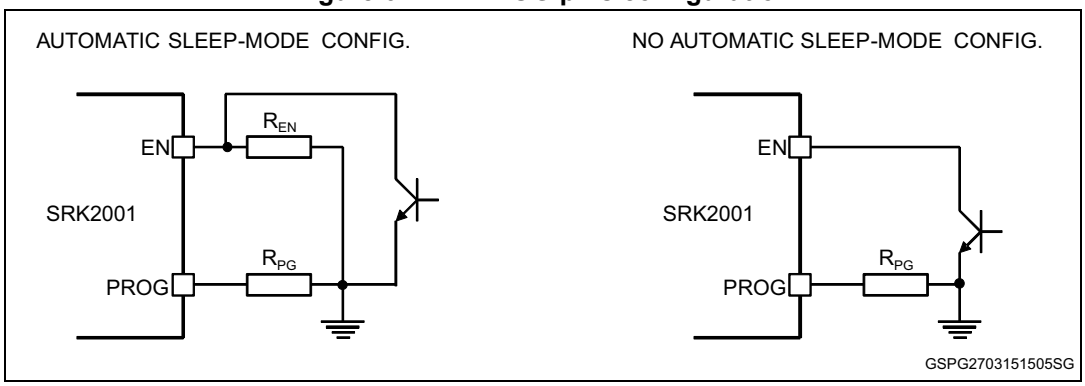
Table 3. Burst-mode exiting programming

	R_{PG}	D_{ON}
R_{EN} open	Zero	80%
	100 kΩ	75%
	180 kΩ	65%
	Open	0%

3. Remote ON/OFF:

During run mode, the EN pin can be used as remote on-off input as well (for both operating modes above described), using a small signal transistor connected to the pin as shown in *Figure 6*: when the switch is closed, the pin voltage goes below the V_{EN_OFF} threshold, the controller stops operating and enters a low consumption state; it resumes operation when the switch is opened and the pin voltage surpasses the V_{EN_ON} threshold: also in this case, the IC has to detect that the SR MOSFET body diode conduction duty cycle becomes higher than D_{ON} (according to *Table 2* or *Table 3*).

Figure 6. EN - PROG pins configuration



2 Electrical diagram description

The board electrical schematic is reported in *Figure 7*: it refers to the STEVAL-ISA165V1; the other boards in *Table 1* have similar schematics, mainly differing in SR MOSFET part number.

SR MOSFETs were selected supposing to implement the SR on a 12 V output converter and using the converter output as supply bus for the SRK2001. In case the board is used with different supply voltage, some modification might be required as well as different MOSFET selection. After start-up, operation with V_{CC} floating (or disconnected by supply voltage) while pins DVS1,2 are switching is not allowed: this in order to avoid that a dV/dt on DVS pin may cause high flowing current with possible damage of the IC.

C501 is a bypass capacitor mounted between V_{CC} and GND pins, to be placed as close as possible to the IC's pin, in order to get a clean supply voltage for the internal circuitry; it is also an energy buffer for the pulsed gate drive currents.

R504 and R505 connect the SR MOSFET drains to DVS1,2 pins: in order to limit dynamic current injection in any condition, at least 100 Ω resistors in series to DVS1,2 pins must be used.

Across either SR MOSFET drain-source, the technical positions for two RC snubber (R510-C503 and R511-C504) are available: these components are foreseen but not mounted because their values depend on the particular application (resonant tank, integrated resonant transformer, secondary side parasitics). They are intended to dump the ringing across drain-source and reduce its peak voltage and might be helpful at reduced load levels, (especially with lower R_{DS_ON} MOSFETs) in order to improve the signal to noise ratio and avoid premature turn-off triggered by ZCD_OFF comparator just after its blanking time.

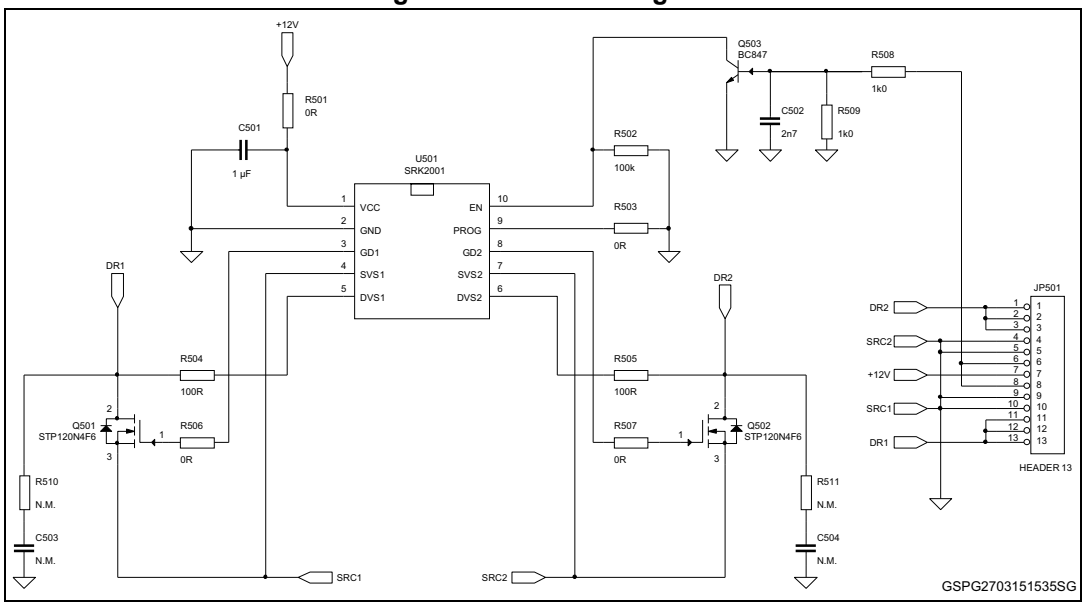
Components Q503-C502-R508-R509 allows user to access EN pin, through R508 connected to board terminals 6 and 8: a signal asserted high (> 2 V) applied to these terminals pulls EN pin low, stopping SRK2001 operation and reducing its consumption to a very low level (I_q).

In case user is not going to use remote ON/OFF function, terminal 6 and 8 can be left floating or connected to GND.

No resistor in series to MOSFET gate is required, since drivers are already optimized for the ZVS operation, both at turn-on and at turn-off (typical in synchronous rectification application), with adaptive control algorithm.

EN and PROG pin resistors are set to 100 kΩ and zero, R502 and R503 respectively (i.e. D_{OFF} = 40% and D_{ON} = 80%): the user can change values according to application needs (referring to *Table 2* and *Table 3*).

Figure 7. Electrical diagram

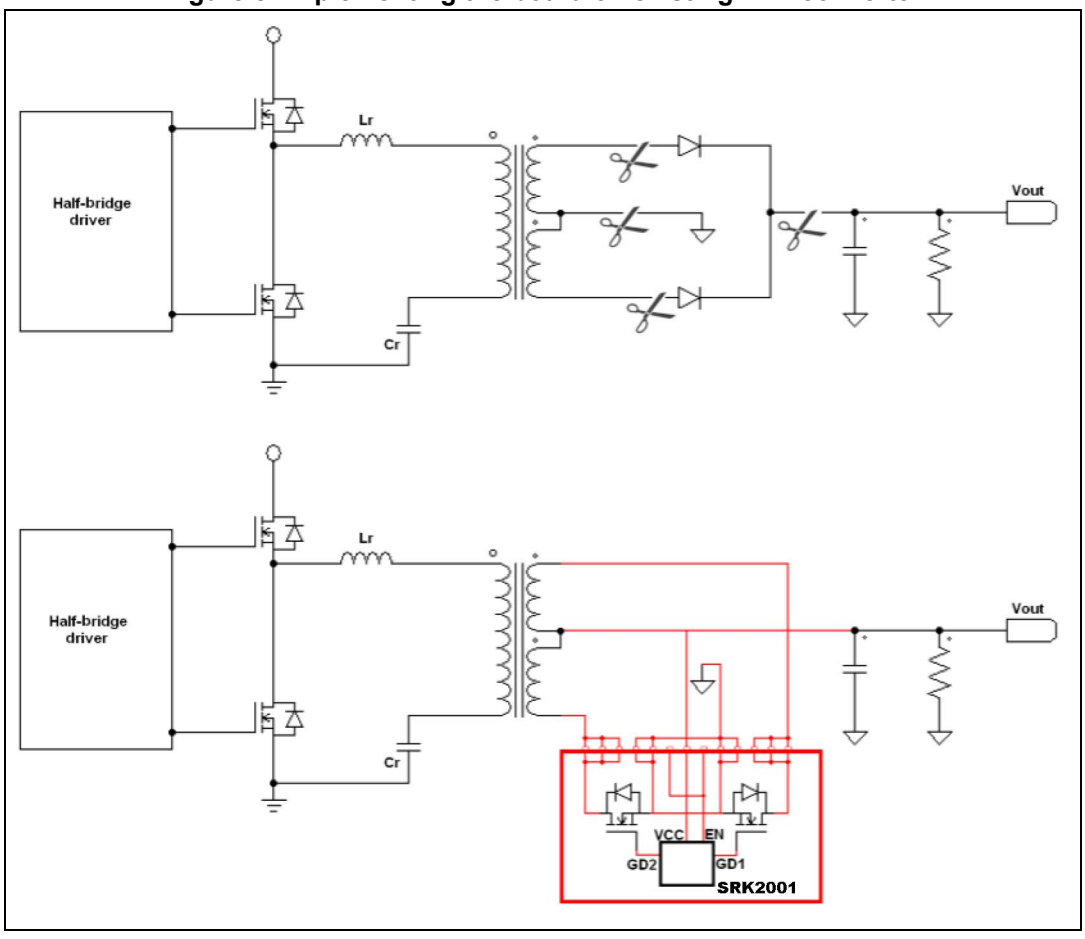


3 How to implement the board in the converter

The demonstration board is intended to implement synchronous rectification in a LLC resonant converter with center-tap secondary winding. If the LLC converter main board implements diode rectification, rectifiers must be removed and the SRK2001 demonstration board has to be connected as indicated in *Figure 8*.

Connect transformer center-tap to the converter output. Tie the other two secondary outputs respectively to terminals 1, 2, 3 and to terminals 11, 12, 13. Bond terminals 4, 5, 9, 10 to secondary ground. The central terminal 7 is for the SRK2001 supplying and can be connected to the converter output. Terminals 6 and 8 are connected to the EN pin and can be used to inhibit the IC remotely. The board connector pinout is perfectly symmetrical and, if necessary for mechanical issues, the board tie to the converter can be rotated by 180°.

Figure 8. Implementing the board on existing LLC converter



4 Power losses and thermal design

SR dramatically reduces the output rectification power losses enabling the design of more efficient power supplies and, even more significant, with a considerable reduction of converter secondary side size.

To get a better idea of the improvement obtained by implementing SR with the SRK2001, power loss calculation in a 12 V - 150 W application - see *2.* in *Section 7: References on page 24* is illustrated below.

4.1 Power losses calculation

The average output current of a 12 V - 150 W LLC resonant converter at nominal load is:

Equation 1

$$I_o = \frac{P_o}{V_o} = 12.50\ A$$

The average current flowing through each output rectifier is:

Equation 2

$$I_{avg} = \frac{I_o}{2} = 6.25\ A$$

while the rms current through each output rectifier is approximately:

Equation 3

$$I_{rms} = \frac{\pi}{4} I_o = 9.82\ A$$

To evaluate power losses, we have selected suitable diode and MOSFET part numbers.

In case of diode rectification we selected the STPS20L45C see - *3.* in *Section 7: References*. The power losses associated to each rectifier can be calculated using the formula indicated in the diode datasheet (which takes into account both of the diode forward drop V_f = 0.28 V and of the dynamic resistance effect Rd = 0.022 Ω):

Equation 4

$$P_{Diode} = 0.28 \cdot I_{avg} + 0.022 \cdot {I_{rms}}^2 = 3.87\ W$$

In case of SR, the selected MOSFET is the STL140N4LLF5 - see *4.* in *Section 7: References*, (PowerFLAT package) which is actually mounted on the STEVAL-ISA168V1 (and STEVAL-ISA169V1 for logic level IC).

Capacitive losses associated to the MOSFET turn-on are negligible because each MOSFET is turned on after its body diode starts conducting. Also losses at turn-off are of minor concern because, after the MOSFET is turned off, current still goes on flowing through the body diode.

Thanks to adaptive turn-on and turn-off algorithms, the SR MOSFET conduction angle is maximized so that losses associated to the current flowing through the body diodes (before turn-on and after turn-off) can be neglected too. Therefore, the most part of SR MOSFET losses can be summarized into conduction losses; for each SR MOSFET the power dissipation is calculated by:

Equation 5

$$P_{MOS} = R_{DS\_on} \cdot I_{rms}^{2} = 265\ mW$$

4.2 IC consumption and driving losses calculation

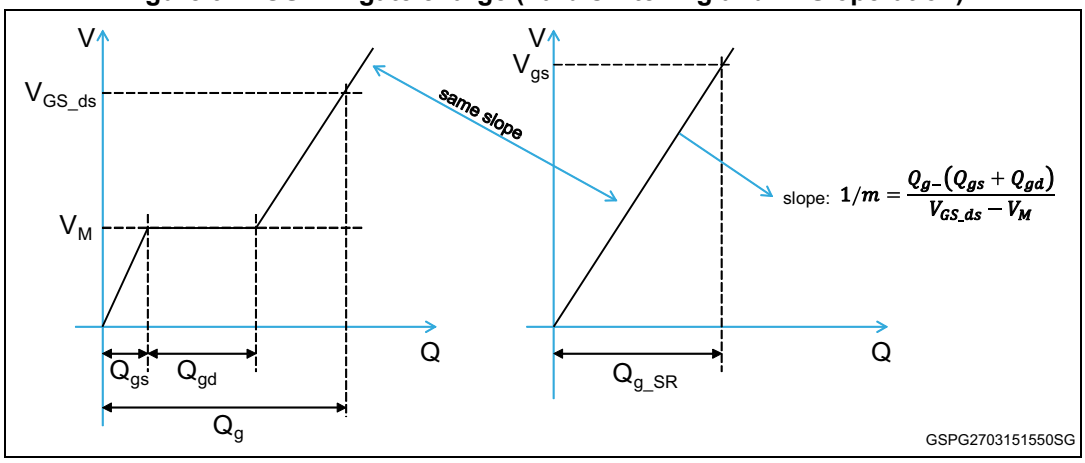
The power consumption of the SRK2001 and the driving losses must be taken into account: for a rough estimation we can consider the IC quiescent current indicated in the datasheet (I_q) and the energy per cycle required for SR MOSFET driving (E_{ZVS}).

Figure 9 shows the curve of the MOSFET gate charge versus the gate-source voltage:

- the part on the left is related to MOSFET operated in hard switching.
- the part on the right is related to MOSFET operated in ZVS, like in the case of SR application.

Note that, in SR application, MOSFET has no Miller effect both at turn-on and at turn-off.

Figure 9. MOSFET gate charge (hard switching and ZVS operation)



From *Figure 9* above, the gate charge for each SR MOSFET of the application can be found as follows, at a generic gate-source voltage V_{gs}:

Equation 6

$$Q_{g\_SR}(V_{gs}) = V_{gs} \frac{Q_g - (Q_{gs} + Q_{gd})}{V_{GS\_ds} - V_M}$$

Where V_{gs} is the gate-source generic level, V_M is the Miller plateau voltage (i.e the voltage of the flat part in the plot of *Figure 9*) and Q_g, Q_{gd}, Q_{gs} are the charges associated to MOSFET gate driving, specified on MOSFET datasheet at a fixed gate-source voltage V_{GS_ds}.

In some cases the MOSFET datasheet directly provides for the gate charge data related to SR applications, generally indicated as Q_{sync}, at a fixed V_{GS_ds} voltage (usually 10 V or 4.5 V); in this case the gate charge at a generic V_{gs} can be found as:

Equation 7

$$Q_{g\_SR}(V_{gs}) = V_{gs}\frac{Q_{sync}}{V_{GS\_ds}}$$

In cases where only the MOSFET input capacitance is known, the gate charge at a generic V_{gs} can be found as:

Equation 8

$$Q_{g\_SR}(V_{gs}) = V_{gs} \cdot C_{in}$$

where C_{in} is basically the summation of the MOSFET gate-source capacitance C_{gs} and of the gate-drain capacitance C_{gd}.

The above calculated gate charge allows to find the expression of the energy per cycle required for SR MOSFET driving:

Equation 9

$$E_{ZVS}(V_{gs}) = V_{dd} \cdot Q_{g\_SR}(V_{gs})$$

where V_{dd} is the IC supply voltage. More detailed explanation on calculating energy per cycle required to drive MOSFETs in ZVS is reported in the Appendix A of the AN2644 see *5.* in *Section 7: References on page 24*.

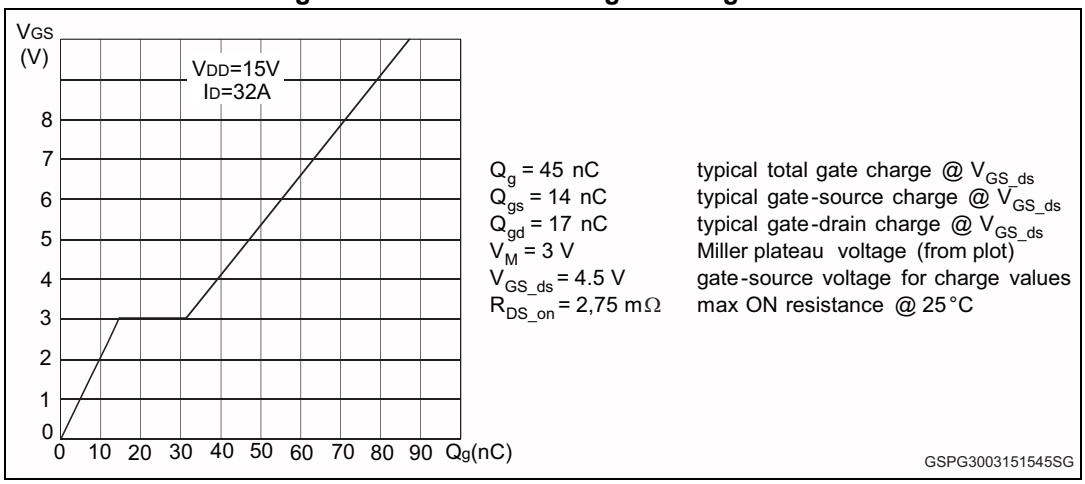
Now, let's split the calculations into the two cases of logic-level and standard-level driver (SRK2001L and SRK2001 respectively), referring to the IC and application data in *Table 4*.

For the MOSFET STL140N4LLF5, gate charge data are shown in *Figure 10*.

Table 4. IC and application data

Value	Description
V_{dd} = 12 V	IC supply voltage (= Vout)
$V_{gd\_high\_LL}$ = 5.5 V	Driver high level for logic-level IC version (SRK2001L)
$V_{gd\_high\_SL}$ = 11 V	Driver high level for standard-level IC version (SRK2001)
I_q = 700 µA	Current consumption in run mode (excluding driver current)
f_{op} = 100 kHz	Operating frequency

Figure 10. STL140N4LLF5 gate charge data



- Logic-level gate drive case:

At: $V_{gs} = V_{gd\_high\_LL} = 5.5\ V \Rightarrow E_{ZVS\_LL} = E_{ZVS(Vgs)} = 0.616\ \mu J$

The above calculated energy per switching cycle allows to find the expression of the total IC consumption and driving power:

Equation 10

$$P_{D\_SRK2001\_LL} = V_{dd} \cdot I_q + 2 \cdot E_{ZVS\_LL} \cdot f_{op} = 132\ mW$$

- Standard-level gate drive case:

At: $V_{gs} = V_{gd\_high\_SL} = 11\ V \Rightarrow E_{ZVS\_SL} = E_{ZVS}(V_{gs}) = 1.232\ \mu J$

The above calculated energy per switching cycle allows to find the expression of the total IC consumption and driving power:

Equation 11

$$P_{D\_SRK2001\_SL} = V_{dd} \cdot I_q + 2 \cdot E_{ZVS\_SL} \cdot f_{op} = 255\ mW$$

The power calculated for the two above cases (neglecting MOSFET internal gate resistance) is almost completely dissipated inside the SRK2001. The factor 2 in above formulas takes into account for the two MOSFETs of the center tap configuration.

Finally, considering the worst case of standard-level gate drive, at full load the total power saving obtained by implementing SR with respect to diode rectification is calculated as follows:

Equation 12

$$\Delta P = 2 \cdot P_{Diode} - \left(2 \cdot P_{MOS} + P_{D\_SRK2001\_SL}\right) = 6.955\ W$$

A power saving of 6.955 W corresponds to a 4.6% efficiency boost on a 150 W converter.

4.3 Thermal design consideration

The efficiency improvement obtained by implementing SR allows dramatic squeezing of the converter secondary side. This becomes evident comparing the heatsink required in case of diode rectification with that required if SR is employed.

Considering the diode rectification, the maximum junction temperature of the selected diode is 150 °C. We can consider 125 °C as maximum tolerable temperature keeping some margin to improve system reliability. Supposing an ambient temperature of 60 °C, the maximum allowed thermal rise is 65 °C. Considering the power dissipation per diode calculated in *Equation 4*, the maximum junction to ambient thermal resistance allowed is:

Equation 13

$$R_{th(j-amb)} = \frac{65°C}{P_{Diode}} = 17\ °C/W$$

We can assume that the thermal resistance between the TO220 case and the heatsink is $R_{th(c-hs)}$ = 1 °C/W and the case to junction thermal resistance of a TO220 package is $R_{th(j-c)}$ = 1 °C/W. As a consequence each diode rectifier needs a heatsink with a maximum thermal resistance of:

Equation 14

$$R_{th(hs-amb)} = R_{th(j-amb)} - R_{th(j-c)} - R_{th(c-hs)} = 15\ °C/W$$

Considering now the case with SR: again the maximum thermal rise is 65 °C. Basing on the power dissipation per MOSFET calculated in *Equation 5*, the maximum junction to ambient thermal resistance allowed is:

Equation 15

$$R_{th(j-amb)} = \frac{65°C}{P_{MOS}} = 245\ °C/W$$

That means that a heatsink is not required, just some PCB copper area is needed, calculated according to the data sheet indication.

In the same way, for the SRK2001, still considering a maximum thermal rise of 65 °C, in the worst case of *Equation 11*, the maximum junction to ambient thermal resistance allowed is:

Equation 16

$$R_{th(j-amb)} = \frac{65°C}{P_{D\_SRK2001\_SL}} = 255\ °C/W$$

This is much higher than the controller junction to ambient thermal resistance on datasheet ($R_{thj-amb}$ = 130 °C/W), meaning also in this case that no heatsink is required.

A straightforward calculation of the junction temperature increase from the calculated power dissipation and from junction to ambient thermal resistance $R_{thj\text{-}amb}$ (JEDEC definition) on datasheet leads to:

Equation 17

$$\Delta T_j = R_{th\ j-amb} \cdot P_{D\_SRK2001\_SL} = 33.15\ °C$$

Anyway, the junction temperature obtained from the above calculated temperature increase above ambient temperature is not a reliable data, since the heat generated internally to the IC is dissipated not only through the device package, but also through the copper track connected to the GND pin, while in JEDEC definition of $R_{thj\text{-}amb}$ heat is only dissipated through the package: therefore, the real junction temperature should be somewhat lower than the calculated one.

Considering the other thermal data available on IC datasheet, that is the junction/case-top thermal resistance, $R_{thj\text{-}case}$ = 10 °C/W (where the generated heat is dissipated both through package and through the pins and therefore strongly depends on the PCB copper area), and measuring the package top temperature, the device junction temperature can be calculated as follows, supposing the temperature measured on the case top is T_{case} = 100 °C:

Equation 18

$$\Delta T_j = T_{case} + R_{th\ j-case} \cdot P_{D\_SRK2001\_SL} = 102.55\ °C$$

It is worth noticing that the IC junction/case-top thermal resistance on datasheet refers to a copper area connected to GND pin of 25 mm² and thickness of 35 µm, with the FR4 PCB material, 1.6 mm thickness.

5 Layout consideration

The GND pin is the return of the device bias current and return of the gate drive currents. It has to be routed to the common point where the source terminals of both synchronous rectifier MOSFETs are connected. A larger copper area connected to the GND pin (located below the device package) helps heat dissipation generated inside the IC, keeping lower junction temperature.

Below the main recommendations that should be taken into account designing the PCB:

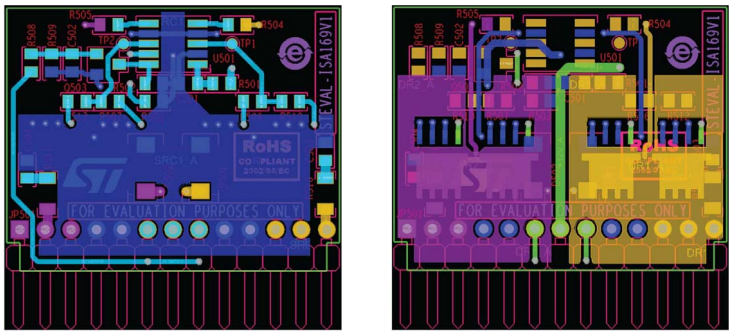
- Close the output current loop as short as possible by connecting the SR MOSFET drains as close as possible to the transformer termination.
- Connect the MOSFET sources close to the output capacitor ground terminals.
- Design the PCB as more geometrically symmetrical as possible to help make the circuit operation as much electrically symmetrical as possible.
- Route the connection between the two MOSFET drains and transformer terminals symmetrically each other.
- Connect the DVS and SVS kelvin sensing inputs as physically close as possible to the drain and source terminals of SR MOSFETs, respectively.
- Keep the source terminals of both SR MOSFETS as close to one another as possible.
- Route the trace that connects MOSFET sources to SRK2001 GND pin as short as possible and separately from the load current return path.
- Use bypass ceramic capacitors between V_{CC} and GND, located as close to the IC pins as possible.

Small capacitors (few nanofarads) between each SVS pin and GND pin may be helpful in case of current injection from SVS pins to ground and, especially when using SR MOSFETs with very lower R_{DS_ON}, even connecting SVS1,2 pins to GND (below the IC body) might be effective to improve operation at light loads, shorting to ground the high frequency noise that affects the circuit.

Figure 11. Board layout

Top Bottom

STEVAL-ISA165V1
STEVAL-ISA166V1



STEVAL-ISA167V1
STEVAL-ISA168V1
STEVAL-ISA169V1

GSPG3003151430SG

6 Bill of material

Table 5. STEVAL-ISA165V1 bill of material

Ref.	Value / PN	Description	Supplier	Case
C501	1 µF	50 V cercap X7R - general purpose	BC COMPONENTS	SMD 0805
C502	2.7 nF	50 V cercap X7R - general purpose	BC COMPONENTS	SMD 0805
JP501	HEADER 13	Strip connector	-	STRIP254P-M-13-90
Q501	STP120N4F6	N-channel power MOSFET	STMicroelectronics	TO220
Q502	STP120N4F6	N-channel power MOSFET	STMicroelectronics	TO220
Q503	BC847C	NPN small signal transistor	VISHAY	SOT23
R501	0 Ω	SMD standard film res. - 1/8 W - 5% - 200 ppm/°C	BC COMPONENTS	SMD 0805
R502	100 kΩ	SMD standard film res. - 1/8 W - 1% - 200 ppm/°C	BC COMPONENTS	SMD 0805
R503	0 Ω	SMD standard film res. - 1/8 W - 5% - 200 ppm/°C	BC COMPONENTS	SMD 0805
R504	100 Ω	SMD standard film res. - 1/8 W - 5% - 200 ppm/°C	BC COMPONENTS	SMD 0805
R505	100 Ω	SMD standard film res. - 1/8 W - 5% - 200 ppm/°C	BC COMPONENTS	SMD 0805
R506	0 Ω	SMD standard film res. - 1/8 W - 5% - 200 ppm/°C	BC COMPONENTS	SMD 0805
R507	0 Ω	SMD standard film res. - 1/8 W - 5% - 200 ppm/°C	BC COMPONENTS	SMD 0805
R508	1 kΩ	SMD standard film res. - 1/8 W - 5% - 200 ppm/°C	BC COMPONENTS	SMD 0805
R509	1 kΩ	SMD standard film res. - 1/8 W - 5% - 200 ppm/°C	BC COMPONENTS	SMD 0805
U501	SRK2001	SRK2001 SR controller	STMicroelectronics	SSOP10

Table 6. STEVAL-ISA166V1 bill of material

Ref.	Value / PN	Description	Supplier	Case
C501	1 µF	50 V cercap X7R - general purpose	BC COMPONENTS	SMD 0805
C502	2.7 nF	50 V cercap X7R - general purpose	BC COMPONENTS	SMD 0805
JP501	HEADER 13	STRIP connector	-	STRIP254P-M-13-90
Q501	STP77N6F6	N-channel power MOSFET	STMicroelectronics	TO220
Q502	STP77N6F6	N-channel power MOSFET	STMicroelectronics	TO220
Q503	BC847C	NPN small signal transistor	VISHAY	SOT23
R501	0 Ω	SMD standard film res. - 1/8 W - 5% - 200 ppm/°C	BC COMPONENTS	SMD 0805
R502	100 kΩ	SMD Standard film res. - 1/8 W - 1% - 200 ppm/°C	BC COMPONENTS	SMD 0805
R503	0 Ω	SMD standard film res. - 1/8 W - 5% - 200 ppm/°C	BC COMPONENTS	SMD 0805
R504	100 Ω	SMD standard film res. - 1/8 W - 5% - 200 ppm/°C	BC COMPONENTS	SMD 0805
R505	100 Ω	SMD standard film res. - 1/8 W - 5% - 200 ppm/°C	BC COMPONENTS	SMD 0805
R506	0 Ω	SMD standard film res. - 1/8 W - 5% - 200 ppm/°C	BC COMPONENTS	SMD 0805
R507	0 Ω	SMD standard film res. - 1/8 W - 5% - 200 ppm/°C	BC COMPONENTS	SMD 0805
R508	1 kΩ	SMD standard film res. - 1/8 W - 5% - 200 ppm/°C	BC COMPONENTS	SMD 0805
R509	1 kΩ	SMD standard film res. - 1/8 W - 5% - 200 ppm/°C	BC COMPONENTS	SMD 0805
U501	SRK2001	SRK2001 SR controller	STMicroelectronics	SSOP10

Table 7. STEVAL-ISA167V1 bill of material

Ref.	Value / PN	Description	Supplier	Case
C501	1 µF	50 V cercap X7R - general purpose	BC COMPONENTS	SMD 0805
C502	2.7 nF	50 V cercap X7R - general purpose	BC COMPONENTS	SMD 0805
JP501	HEADER 13	STRIP connector	-	STRIP254P-M-13-90
Q501	STL85N6F3	N-channel power MOSFET	STMicroelectronics	PowerFLAT
Q502	STL85N6F3	N-channel power MOSFET	STMicroelectronics	PowerFLAT
Q503	BC847C	NPN small signal transistor	VISHAY	SOT23
R501	0 Ω	SMD standard film res. - 1/8 W - 5% - 200 ppm/°C	BC COMPONENTS	SMD 0805
R502	100 kΩ	SMD standard film res. - 1/8 W - 1% - 200 ppm/°C	BC COMPONENTS	SMD 0805
R503	0 Ω	SMD standard film res. - 1/8 W - 5% - 200 ppm/°C	BC COMPONENTS	SMD 0805
R504	100 Ω	SMD standard film res. - 1/8 W - 5% - 200 ppm/°C	BC COMPONENTS	SMD 0805
R505	100 Ω	SMD standard film res. - 1/8 W - 5% - 200 ppm/°C	BC COMPONENTS	SMD 0805
R506	0 Ω	SMD standard film res. - 1/8 W - 5% - 200 ppm/°C	BC COMPONENTS	SMD 0805
R507	0 Ω	SMD standard film res. - 1/8 W - 5% - 200 ppm/°C	BC COMPONENTS	SMD 0805
R508	1 kΩ	SMD standard film res. - 1/8 W - 5% - 200 ppm/°C	BC COMPONENTS	SMD 0805
R509	1 kΩ	SMD standard film res. - 1/8 W - 5% - 200 ppm/°C	BC COMPONENTS	SMD 0805
U501	SRK2001	SRK2001 SR controller	STMicroelectronics	SSOP10

Table 8. STEVAL-ISA168V1 bill of material

Ref.	Value / PN	Description	Supplier	Case
C501	1 µF	50 V cercap X7R - general purpose	BC COMPONENTS	SMD 0805
C502	2.7 nF	50 V cercap X7R - general purpose	BC COMPONENTS	SMD 0805
JP501	HEADER 13	STRIP connector	-	STRIP254P-M-13-90
Q501	STL140N4LLF5	N-channel power MOSFET	STMicroelectronics	PowerFLAT
Q502	STL140N4LLF5	N-channel power MOSFET	STMicroelectronics	PowerFLAT
Q503	BC847C	NPN small signal transistor	VISHAY	SOT23
R501	0 Ω	SMD standard film res. - 1/8 W - 5% - 200 ppm/°C	BC COMPONENTS	SMD 0805
R502	100 kΩ	SMD standard film res. - 1/8 W - 1% - 200 ppm/°C	BC COMPONENTS	SMD 0805
R503	0 Ω	SMD standard film res. - 1/8 W - 5% - 200 ppm/°C	BC COMPONENTS	SMD 0805
R504	100 Ω	SMD standard film res. - 1/8 W - 5% - 200 ppm/°C	BC COMPONENTS	SMD 0805
R505	100 Ω	SMD standard film res. - 1/8 W - 5% - 200 ppm/°C	BC COMPONENTS	SMD 0805
R506	0 Ω	SMD standard film res. - 1/8 W - 5% - 200 ppm/°C	BC COMPONENTS	SMD 0805
R507	0 Ω	SMD standard film res. - 1/8 W - 5% - 200 ppm/°C	BC COMPONENTS	SMD 0805
R508	1 kΩ	SMD standard film res. - 1/8 W - 5% - 200 ppm/°C	BC COMPONENTS	SMD 0805
R509	1 kΩ	SMD Standard film res.- 1/8 W - 5% - 200 ppm/°C	BC COMPONENTS	SMD 0805
U501	SRK2001	SRK2001 SR controller	STMicroelectronics	SSOP10

Table 9. STEVAL-ISA169V1 bill of material

Ref.	Value / PN	Description	Supplier	Case
C501	1 µF	50 V cercap X7R - general purpose	BC COMPONENTS	SMD 0805
C502	2.7 nF	50 V cercap X7R - general purpose	BC COMPONENTS	SMD 0805
JP501	HEADER 13	STRIP connector	-	STRIP254P-M-13-90
Q501	STL140N4LLF5	N-channel power MOSFET	STMicroelectronics	PowerFLAT
Q502	STL140N4LLF5	N-channel power MOSFET	STMicroelectronics	PowerFLAT
Q503	BC847C	NPN small signal transistor	VISHAY	SOT23
R501	0 Ω	SMD standard film res. - 1/8 W - 5% - 200 ppm/°C	BC COMPONENTS	SMD 0805
R502	100 kΩ	SMD standard film res.- 1/8 W - 1% - 200 ppm/°C	BC COMPONENTS	SMD 0805
R503	0 Ω	SMD standard film res.- 1/8 W - 5% - 200 ppm/°C	BC COMPONENTS	SMD 0805
R504	100 Ω	SMD standard film res. - 1/8 W - 5% - 200 ppm/°C	BC COMPONENTS	SMD 0805
R505	100 Ω	SMD standard film res. - 1/8 W - 5% - 200 ppm/°C	BC COMPONENTS	SMD 0805
R506	0 Ω	SMD standard film res. - 1/8 W - 5% - 200 ppm/°C	BC COMPONENTS	SMD 0805
R507	0 Ω	SMD standard film res. - 1/8 W - 5% - 200 ppm/°C	BC COMPONENTS	SMD 0805
R508	1 kΩ	SMD standard film res.- 1/8 W - 5% - 200 ppm/°C	BC COMPONENTS	SMD 0805
R509	1 kΩ	SMD standard film res.- 1/8 W - 5% - 200 ppm/°C	BC COMPONENTS	SMD 0805
U501	SRK2001L	SRK2001L SR controller (logic level)	STMicroelectronics	SSOP10

7 References

1. SRK20001 datasheet: available at www.st.com.
2. AN3233 - 12 V - 150 W resonant converter with synchronous rectification using the L6563H, L6599A and SRK2000A: available at www.st.com.
3. STPS20L45C datasheet: available at www.st.com.
4. STL140N4LLF5 datasheet: available at www.st.com.
5. AN2644 - An introduction to LLC resonant half-bridge converter: available at www.st.com.

8 Revision history

Table 10. Document revision history

Date	Revision	Changes
25-May-2015	1	Initial release.
27-Jun-2017	2	Replaced “SRK2000” by “SRK2000A” in *2.* of *Section 7 on page 24*. Minor modifications throughout document.