AN4675
Application note

Migration of microcontroller applications from STM32F42xxx/STM32F43xxx to STM32F469xx/STM32F479xx

Introduction

For more and more applications using STM32 products, it is important to migrate a project easily to a different microcontroller in the same product family.

Migrating an application to a different microcontroller is often needed, when product requirements grow, putting extra demands on memory size, or increasing the number of I/Os. On the other hand, cost reduction objectives may force you to switch to smaller components and shrink the PCB area.

This application note is intended to help you to analyze the steps you need to migrate from an existing STM32F42xxx/STM32F43xxx devices based design to STM32F469xx/STM32F479xx devices. It groups together all the most important information and lists the vital aspects that you need to address.

The current document lists “full set” of features for STM32F42xxx/STM32F43xxx and STM32F469xx/STM32F479xx series in the comparisons made (some products may have less features depending on their part number).

Migrating between the two devices within the same family could require hardware and/or software changes in some cases. Changes that might be required are described in this document.To fully benefit from the information in this application note, the user should be familiar with the STM32 microcontroller family.

This application note has to be read in conjunction with STM32F42xxx/STM32F43xxx and STM32F469xx/STM32F479xx reference manuals (RM0090 and RM0386) and datasheets available at *www.st.com.*

Table 1. Applicable devices

Type	Reference	Part numbers or product lines
Microcontrollers	STM32F427xx STM32F437xx	STM32F427/437 line
	STM32F429xx	STM32F429AG, STM32F429AI, STM32F429BE, STM32F429BG, STM32F429BI, STM32F429IE, STM32F429IG, STM32F429II, STM32F429NE, STM32F429NG, STM32F429NI, STM32F429VE, STM32F429VG, STM32F429VI, STM32F429ZE, STM32F429ZG, STM32F429ZI
	STM32F439xx	STM32F439AI, STM32F439BG, STM32F439BI, STM32F439IG, STM32F439II, STM32F439NG, STM32F439NI, STM32F439VG, STM32F439VI, STM32F439ZG, STM32F439ZI
	STM32F469xx	STM32F469AE, STM32F469AG, STM32F469AI, STM32F469BE, STM32F469BG, STM32F469BI, STM32F469IE, STM32F469IG, STM32F469II, STM32F469NE, STM32F469NG, STM32F469NI
	STM32F479xx	STM32F479AG, STM32F479AI, STM32F479BG, STM32F479BI, STM32F479IG, STM32F479II, STM32F479NG, STM32F479NI

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1 Hardware migration guide

1.1 PCB design compatibility

The STM32F469xx/STM32F479xx devices are not identical with the STM32F42xxx/STM32F43xxx devices in term of MCU port assignment to package terminals, that is, in term of pinout or ballout. This holds for all common package types of the package list in *Table 2*, ordered from biggest to smallest. For migrating from STM32F42xxx or STM32F43xxx to STM32F469xx or STM32F479xx, the differences in pinout or ballout have to be reflected in the PCB design. Keeping the same LQFP176, UFBGA169 or LQFP208 package, a new PCB design can hardly be avoided. Keeping the same TFBGA216 or UFBGA176 package, it is easier to use the same PCB design as the pinout / ballout differences are weaker. Therefore, for the latter packages, the microcontrollers from either series allow PCB design compatibility.

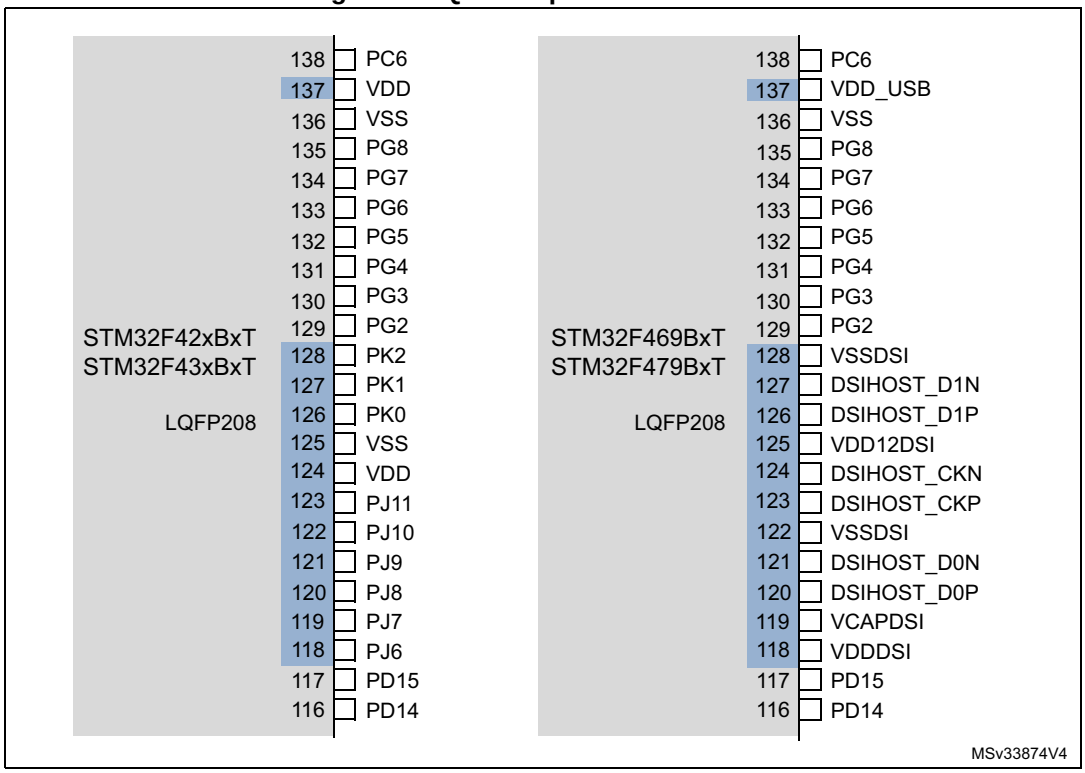
Table 2. Package availability and PCB design compatibility

Package	STM32F42xxx STM32F43xxx	STM32F469xx STM32F479xx	Pinout / ballout difference	PCB design modification
LQFP208 (28 × 28 mm)	X	X	Weak	Mandatory
LQFP176 (24 × 24 mm)	X	X	Medium	Mandatory
LQFP144 (20 × 20 mm)	X	-	-	-
LQFP100 (14 × 14 mm)	X	-	-	-
TFBGA216 (13 x 13 mm)	X	X	Weak	Not mandatory(1)
UFBGA176 (10 × 10 mm)	X	X	Weak	Not mandatory(1)
UFBGA169 (7 × 7 mm)	X	X	Strong	Mandatory
WLCSP143	X	-	-	-
WLCSP168	-	X	-	-

1. Light modification may be required. Refer to *Figure 3* and *Figure 4* for details on ballout differences.

1.1.1 LQFP208 package

Figure 1. LQFP208 pinout differences



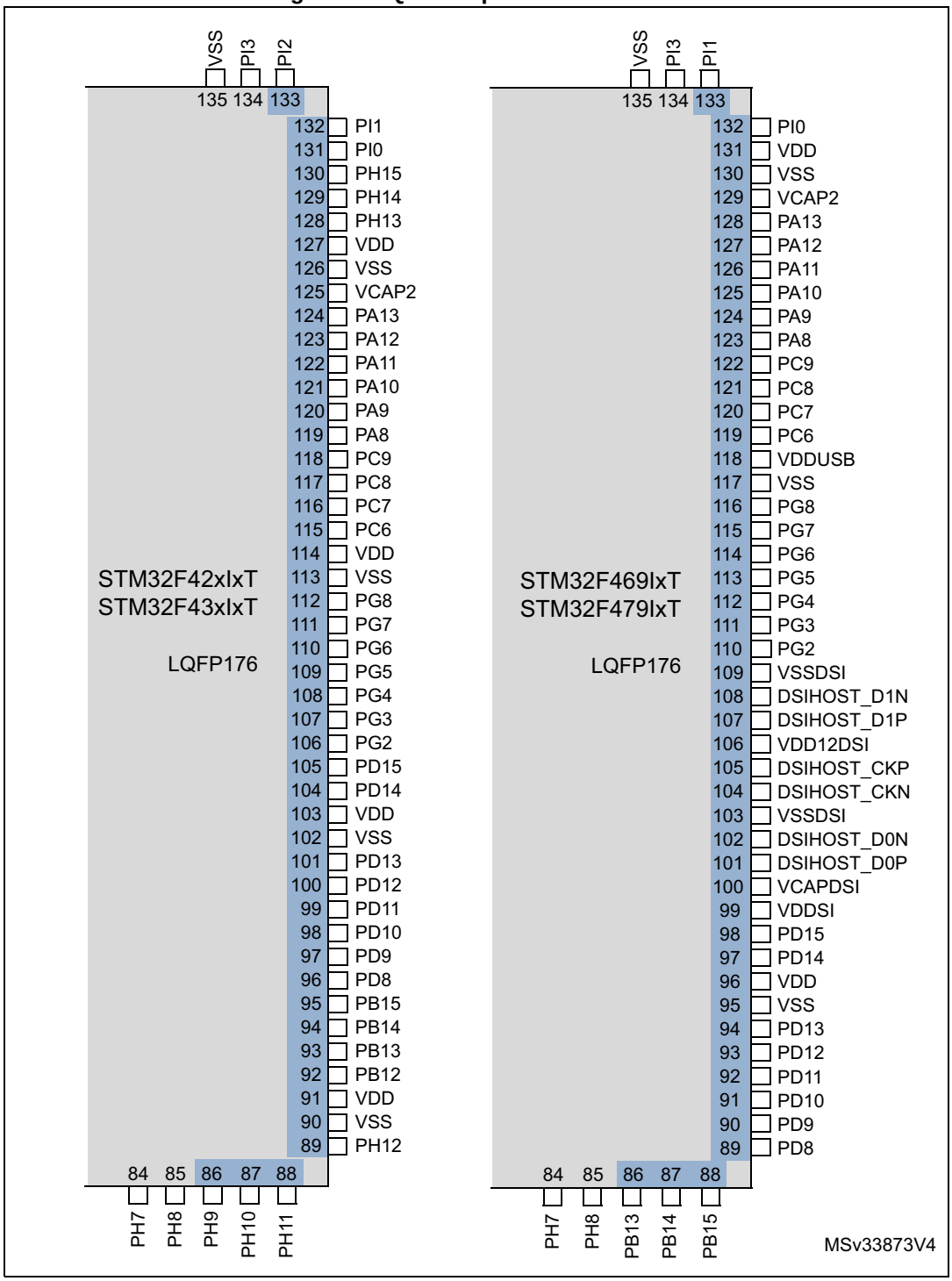
For the highlighted (blue) terminals, DSIHOST dedicated IOs on STM32F469BxT/STM32F479BxT substitute some of STM32F42xBxT/STM32F43xBxT IO ports.

Table 3. List of LQFP208 pinout differences

Terminal	STM32F42xBxT STM32F43xBxT	STM32F469BxT STM32F479BxT	Terminal	STM32F42xBxT STM32F43xBxT	STM32F469BxT STM32F479BxT
128	PK2	VSSDSI	122	PJ10	VSSDSI
127	PK1	DSIHOST_D1N	121	PJ9	DSIHOST_D0N
126	PK0	DSIHOST_D1P	120	PJ8	DSIHOST_D0P
125	VSS	VDD12DSI	119	PJ7	VCAPDSI
124	VDD	DSIHOST_CKN	118	PJ6	VDDDSI
123	PJ11	DSIHOST_CKP	137	VDD	VDD_USB

1.1.2 LQFP176 package

Figure 2. LQFP176 pinout differences



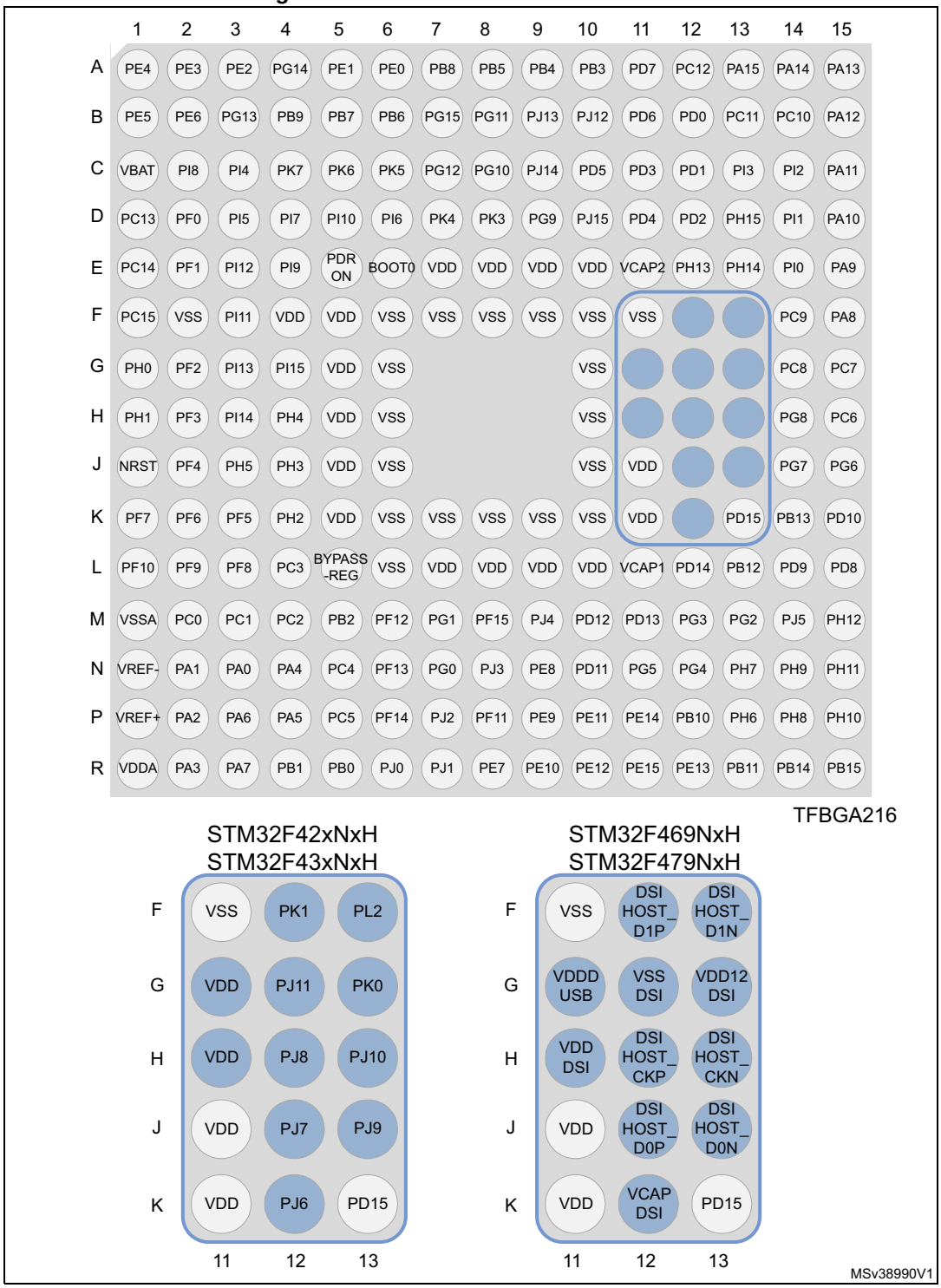
The highlighted (blue) terminals have different IO port assignment.

Table 4. List of LQFP176 pinout differences

Terminal	STM32F42xIxT STM32F43xIxT	STM32F469IxT STM32F479IxT	Terminal	STM32F42xIxT STM32F43xIxT	STM32F469IxT STM32F479IxT
133	PI2	PI1	109	PG5	VSSDSI
132	PI1	PI0	108	PG4	DSIHOST_D1N
131	PI0	VDD	107	PG3	DSIHOST_D1P
130	PH15	VSS	106	PG2	VDD12DSI
129	PH14	VCAP2	105	PD15	DSIHOST_CKP
128	PH13	PA13	104	PD14	DSIHOST_CKN
127	VDD	PA12	103	VDD	VSSDSI
126	VSS	PA11	102	VSS	DSIHOST_D0N
125	VCAP2	PA10	101	PD13	DSIHOST_D0P
124	PA13	PA0	100	PD12	VCAPDSI
123	PA12	PA8	99	PD11	VDDDSI
122	PA11	PC9	98	PD10	PD15
121	PA10	PC8	97	PD9	PD14
120	PA9	PC7	96	PD8	VDD
119	PA8	PC6	95	PB15	VSS
118	PC9	VDDUSB	94	PB14	PD13
117	PC8	VSS	93	PB13	PD12
116	PC7	PG8	92	PB12	PD11
115	PC6	PG7	91	VDD	PD10
114	VDD	PG6	90	VSS	PD9
113	VSS	PG5	89	PH12	PD8
112	PG8	PG4	88	PH11	PB15
111	PG7	PG3	87	PH10	PB14
110	PG6	PG2	86	PH9	PB13

1.1.3 TFBGA216 package

Figure 3. TFBGA216 ballout differences



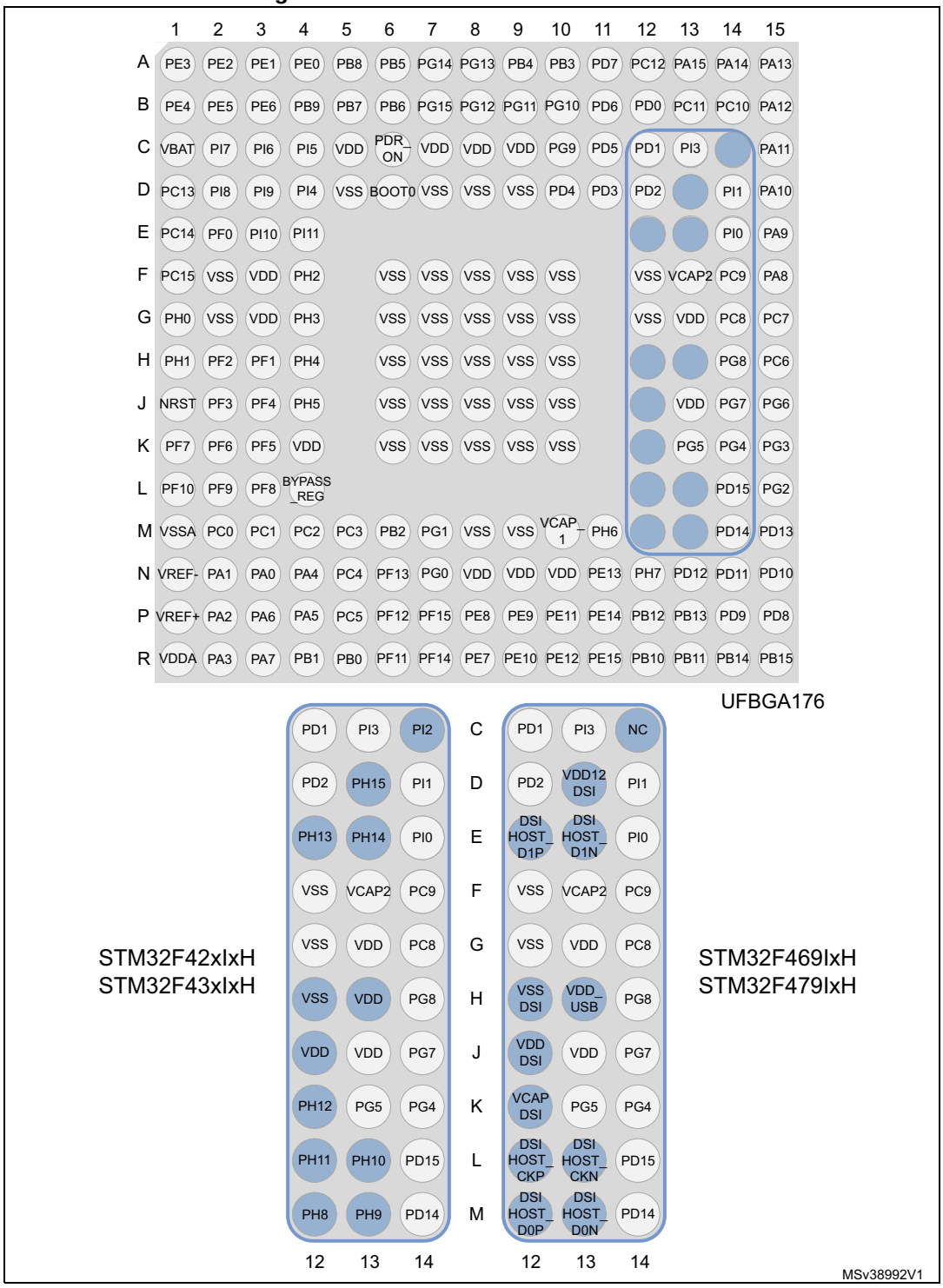
For the highlighted (blue) terminals, DSIHOST dedicated IOs on STM32F469NxH/STM32F479NxH substitute some of STM32F42xNxH/STM32F43xNxH IO ports.

Table 5. List of TFBGA216 ballout differences

Terminal	STM32F42xNxH STM32F43xNxH	STM32F469NxH STM32F479NxH	Terminal	STM32F42xNxH STM32F43xNxH	STM32F469NxH STM32F479NxH
11G	VDD	VDDDUSB	12K	PJ6	VCAPDSI
11H	VDD	VDDDSI	13F	PL2	DSIHOST_D1N
12F	PK1	DSIHOST_D1P	13G	PK0	VDD12DSI
12G	PJ11	VSSDSI	13H	PJ10	DSIHOST_CKN
12H	PJ8	DSIHOST_CKP	13J	PJ9	DSIHOST_D0N
12J	PJ7	DSIHOST_D0P	-	-	-

1.1.4 UFBGA176 package

Figure 4. UFBGA176 ballout differences



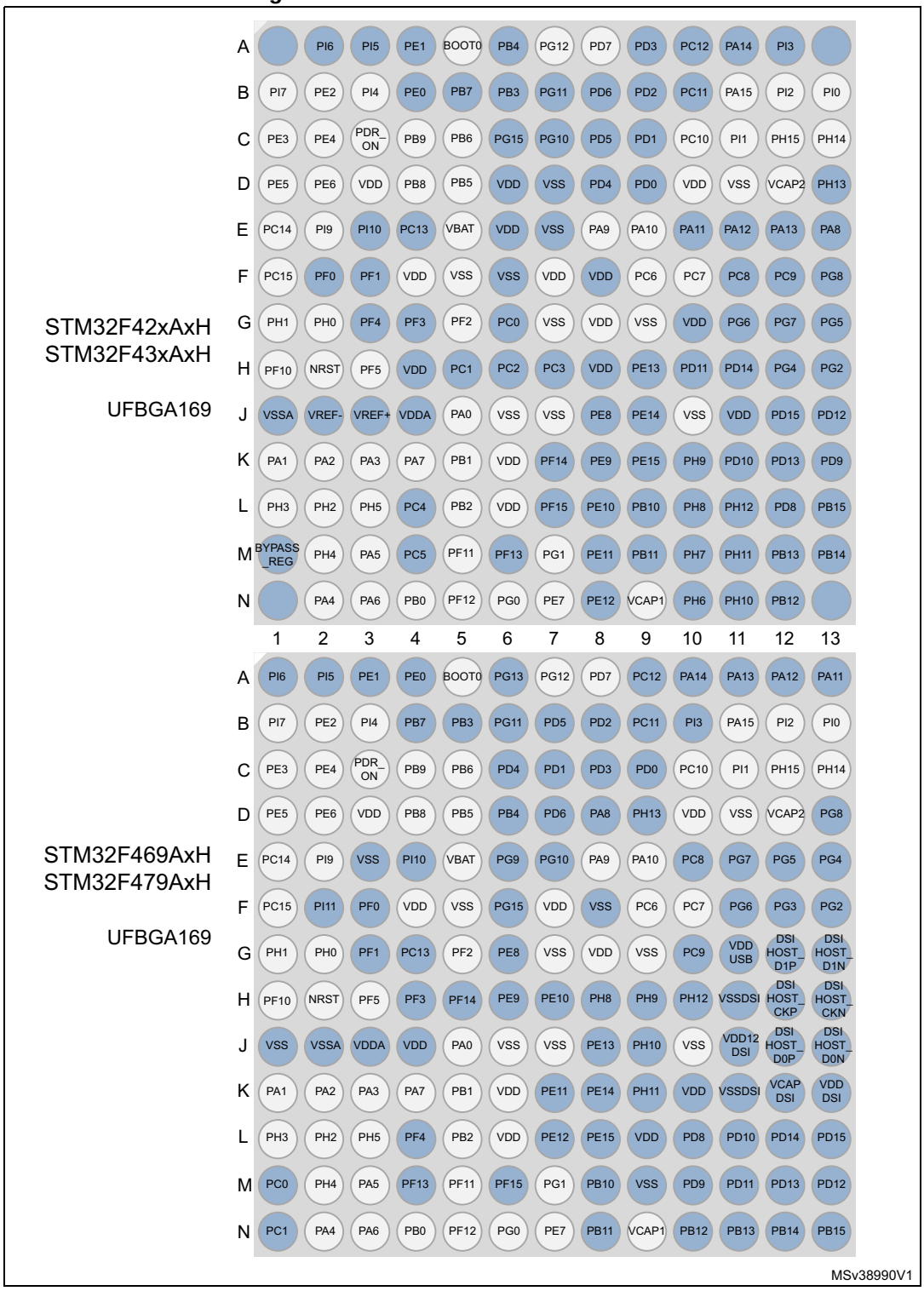
For the highlighted (blue) terminals, DSIHOST dedicated IOs on STM32F469IxH/STM32F479IxH substitute some of STM32F42xIxH/STM32F43xIxH IO ports.

Table 6. List of UFBGA176 ballout differences

Terminal	STM32F42xIxH STM32F43xIxH	STM32F469IxH STM32F479IxH	Terminal	STM32F42xIxH STM32F43xIxH	STM32F469IxH STM32F479IxH
12E	PH13	DSIHOST_D1P	13D	PH15	VDD12DSI
12H	VSS	VSSDSI	13E	PH14	DSIHOST_D1N
12J	VDD	VDDDSI	13H	VDD	VDD_USB
12K	PH12	VCAPDSI	13L	PH10	DSIHOST_CKN
12L	PH11	DSIHOST_CKP	13M	PH9	DSIHOST_D0N
12M	PH8	DSIHOST_D0P	14C	PI2	NC

1.1.5 UFBGA169 package

Figure 5. UFBGA169 ballout differences



The highlighted (blue) terminals have different IO port assignment.

Table 7. List of UFBGA169 ballout differences

Terminal	STM32F42xAxH STM32F43xAxH	STM32F469AxH STM32F479AxH	Terminal	STM32F42xAxH STM32F43xAxH	STM32F469AxH STM32F479AxH
1A	NC	PI6	9B	PD2	PC11
1J	VSSA	VSS	9C	PD1	PD0
1M	BYPASS_REG	PC0	9D	PD0	PH13
1N	NC	PC1	9H	PE13	PH9
2A	PI6	PI5	9J	PE14	PH10
2F	PF0	PI11	9K	PE15	PH11
2J	VREF-	VSSA	9L	PB10	VDD
3A	PI5	PE1	9M	PB11	VSS
3E	PI10	VSS	10A	PC12	PA14
3F	PF1	PF0	10B	PC11	PI3
3G	PF4	PF1	10E	PA11	PC8
3J	VREF+	VDDA	10G	VDD	PC9
4A	PE1	PE0	10H	PD11	PH12
4B	PE0	PB7	10K	PH9	VDD
4E	PC13	PI10	10L	PH8	PD8
4G	PF3	PC13	10M	PH7	PD9
4H	VDD	PF3	10N	PH6	PB12
4J	VDDA	VDD	11A	PA14	PA13
4L	PC4	PF4	11E	PA12	PG7
4M	PC5	PF13	11F	PC8	PG6
5B	PB7	PB3	11G	PG6	VDDUSB
5H	PC1	PF14	11H	PD14	VSSDSI
6A	PB4	PG13	11J	VDD	VDD12DSI
6B	PB3	PG11	11K	PD10	VSSDSI
6C	PG15	PD4	11L	PH12	PD10
6D	VDD	PB4	11M	PH11	PD11
6E	VDD	PG9	11N	PH10	PB13
6F	VSS	PG15	12A	PI3	PA12
6G	PC0	PE8	12E	PA13	PG5
6H	PC2	PE9	12F	PC9	PG3
6M	PF13	PF15	12G	PG7	DSIHOST_D1P
7B	PG11	PD5	12H	PG4	DSIHOST_CKP
7C	PG10	PD1	12J	PD15	DSIHOST_D0P
7D	VSS	PD6	12K	PD13	VCAPDSI

Table 7. List of UFBGA169 ballout differences (continued)

Terminal	STM32F42xAxH STM32F43xAxH	STM32F469AxH STM32F479AxH	Terminal	STM32F42xAxH STM32F43xAxH	STM32F469AxH STM32F479AxH
7E	VSS	PG10	12L	PD8	PD14
7H	PC3	PE10	12M	PB13	PD13
7K	PF14	PE11	12N	PB12	PB14
7L	PF15	PE12	13A	NC	PA11
8B	PD6	PD2	13D	PH13	PG8
8C	PD5	PD3	13E	PA8	PG4
8D	PD4	PA8	13F	PG8	PG2
8F	VDD	VSS	13G	PG5	DSIHOST_D1N
8H	VDD	PH8	13H	PG2	DSIHOST_CKN
8J	PE8	PE13	13J	PD12	DSIHOST_D0N
8K	PE9	PE14	13K	PD9	VDDDSI
8L	PE10	PE15	13L	PB15	PD15
8M	PE11	PB10	13M	PB14	PD12
8N	PE12	PB11	13N	NC	PB15
9A	PD3	PC12	-	-	-

2 Peripheral migration guide

2.1 STM32 product cross-compatibility

The STM32 series embeds a set of peripherals which can be classed in three categories:

- The first category is for the peripherals which are by definition common to all products. Those peripherals are identical, so they have the same structure, registers and control bits. There is no need to perform any firmware change to keep the same functionality at the application level after migration. All the features and behavior remain the same.
- The second category is for the peripherals which are shared by all products but have only minor differences (in general to support new features), so migration from one product to another is very easy and does not need any significant new development effort.
- The third category is for peripherals which have been considerably changed from one product to another (new architecture, new features...). For this category of peripherals, migration will require new development at application level.

The *Table 8* summarizes the available peripherals of the STM32F42xxx/STM32F43xxx and STM32F469xx/STM32F479xx families and their compatibility.

Table 8. Peripheral compatibility analysis: STM32F42xxx/STM32F43xxx vs STM32F469xx/STM32F479xx

Peripherals		STM32F42xxx/ STM32F43xxx	STM32F469xx/ STM32F479xx	Compatibility	
				SW	Comments
Flash memory (Mbytes)		2	2	-	-
SRAM (Kbytes)	System	256 (112+16+64+64)	384 (160+32+128+64)	-	-
	Backup	4	4	-	-
Timers	General purpose	10	10	YES	-
	Advanced control	2	2	YES	-
	Basic	2	2	YES	-
Comunication interfaces	SPI/I2S	6/2(full duplex)	6/2(full duplex)	YES	-
	I2C	3	3	YES	-
	USART/UART	4/4	4/4	YES	-
	USB OTG FS	YES	YES	YES	– Dedicated VDDUSB supply – More endpoints and host channels – New Clock source PLLSAI – Link power management
	USB OTG HS	YES	YES	YES	
	CAN	2	2	YES	-
	SAI	1	1	YES	Additional SPDIF Output
	SPDIF-TX	NO	YES	NA	New peripheral
	SDIO	YES	YES	YES	New clock sources: – SYSCLK and PLLSAI
Quad-SPI		NO	YES	NA	New peripheral with dual/quad mode feature
RNG		YES	YES	YES	New Clock source PLLSAI
FMC		YES	YES	YES	-
Ethernet		YES	YES	YES	-
WWDG		YES	YES	YES	-
IWDG		YES	YES	YES	-
CRC		YES	YES	YES	-
DMA		DMA1-DMA2(8 stream each)		YES	Enhanced dynamic power consumption
Crypto		YES	YES	YES	-
Hash		YES	YES	YES	-

Table 8. Peripheral compatibility analysis: STM32F42xxx/STM32F43xxx vs STM32F469xx/STM32F479xx (continued)

Peripherals		STM32F42xxx/ STM32F43xxx	STM32F469xx/ STM32F479xx	Compatibility	
				SW	Comments
GPIOs		Up to 168	Up to 161	YES	-
12 bit ADC	Instances	3	3	YES	-
	Number of channels	16/24	16/24	-	-
12 bit DAC	Instances	1	1	YES	-
	Number of channels	2	2	-	-
RCC(1)		YES	YES	YES	New LSE modes: – High drive mode – Low power mode New Clock sources
RTC		YES	YES	YES	-
EXTI		YES	YES	YES	-
PWR(2)		YES	YES	YES	New feature: Power supply supervisor management in static way
SYSCFG		YES	YES	YES	-
Chrom-Art-Accelerator™ DMA2D		YES	YES	-	-
DCMI		YES	YES	-	New features : – Half resolution image extraction – Black and White image
LCD-TFT		YES	YES	-	-
MIPI-DSI Host		NO	YES	-	New peripheral

1. For more details on RCC please refer to *Section 2.5: Reset and Clock Control (RCC)*.
2. For more details on PWR please refer to *Section 2.6: Power controller*.

2.2 Register boundary addresses of peripherals

Table 9 compares register boundary addresses of peripherals on STM32F42xxx/STM32F43xxx versus STM32F469xx/STM32F479xx.

Table 9. Peripherals register boundary addresses comparison

Peripheral	Bus	STM32F42xxx/STM32F43xxx Base address	STM32F469xx/STM32F479xx Base address
Quad-SPI Register	AHB3	NA	0xA000 1000 - 0xA000 1FFF
DSI Host	APB2	NA	0x4001 6C00 - 0x4001 73FF

2.3 Flexible memory controller (FMC)

Table 10 presents differences between STM32F42xxx/STM32F43xxx and STM32F469xx/STM32F479xx, in term of FMC.

Table 10. FMC differences between STM32F42xxx/STM32F43xxx and STM32F469xx/STM32F479xx

FMC		STM32F42xxx/STM32F43xxx	STM32F469xx/STM32F479xx
External memory interfaces		SRAM NOR/NAND memories PSRAM (4 memory banks) Two banks of NAND Flash memory with ECC hardware 16-bit PC Card compatible devices	SRAM NOR/NAND memories PSRAM (4 memory banks) NAND Flash memory with ECC hardware
Data bus width		8-, 16- or 32-bit	
FMC Bank memory mapping	BANK1 4x64 Mbyte	NOR/PSRAM/SRAM	NOR/PSRAM/SRAM
	BANK2 4x64 Mbyte	NAND Flash memory	Reserved
	BANK3 4x64 Mbyte		NAND Flash memory
	BANK4 4x64 Mbyte	PC card	Reserved
	SRAM BANK1 4x64 Mbyte	SDRAM	SDRAM
	SRAM BANK2 4x64 Mbyte		
Memory mapping swap: (SYSCFG_MEMRMP) Bit 11:10 SWP_FMC[1:0] = 01b		NOR/PSRAM/SRAM 256 Mbyte	SDRAM Bank1 256 Mbyte
		NAND Bank1 256 Mbyte	SDRAM Bank2 256 Mbyte
		SDRAM Bank1 256 Mbyte	NAND Bank3 256 MByte
		SDRAM Bank2 256 Mbyte	Reserved
		Reserved	Reserved
		NAND Bank2 256 Mbyte	NOR/PSRAM/SRAM 256 MByte
		PC card 256 Mbyte	Reserved

2.4 Interrupt vector

Table 11 presents differences between STM32F42xxx/STM32F43xxx and STM32F469xx/STM32F479xx, in term of interrupt vectors.

Table 11. Interrupt vector differences between STM32F42xxx/STM32F43xxx and STM32F469xx/STM32F469xx

Position	STM32F42xxx/STM32F43xxx	STM32F469xx/STM32F479xx
91	NA	QUADSPI
92	NA	DSI host controller

2.5 Reset and Clock Control (RCC)

Main differences related to RCC (reset and clock controller) on STM32F469xx/F479xx versus STM32F42xxx/F43xxx are presented in the *Table 12*.

Table 12. RCC differences between STM32F42xxx/STM32F43xxx and STM32F469xx/STM32F479xx

Peripherals	STM32F42xxx/STM32F43xxx	STM32F469xx/STM32F479xx
	Clock sources	
USB OTG FS	– PLL48MHz derived from main PLL VCO (PLLQ Clock)	– PLL48MHz derived from: main PLL or PLLSAI (PLLQ or PLLSAIP)
RNG		
SDIO	– PLL48CLK	– PLL48CLK (PLLQ or PLLSAIP) – SYSCLK
USART/UARTs	– APB1 or APB2 clock (PCLK1 or PCLK2)	
I2Cs	– APB1 clock (PCLK1)	
I2S	– PLLI2S – External clock mapped on I2S_CKIN pin	
SAI1	– PLLI2S_Q – PLLSAI_Q – External clock mapped on the I2S_CKIN pin	
LTDC	– PLLSAI_R	
USB OTG FS	– 24 to 60 MHz to External PHY	
ETHERNET MAC	– 25 to 50 MHz External PHY	
RTC	– LSE clock – LSI clock – HSE clock divided by 32	
IWDG	– LSI	

Table 12. RCC differences between STM32F42xxx/STM32F43xxx and STM32F469xx/STM32F479xx (continued)

Peripherals		STM32F42xxx/STM32F43xxx	STM32F469xx/STM32F479xx
		Clock sources	
LSE		NA	Configurable LSE drive in RCC_BDCR register : – LSEMOD = 0: Low power mode – LSEMOD = 1: High drive mode
RCC Dedicated Clock Configuration Register		– RCC_DCKCFGR	
DSI host	DSI Lanebyte clock	NA	Derived from : – Main PLL (PLLDSICLK) if DSI-PHY is off – DSI-PHY output
	DSI RX escape mode clock	NA	– Derived from DSI-PHY

2.6 Power controller

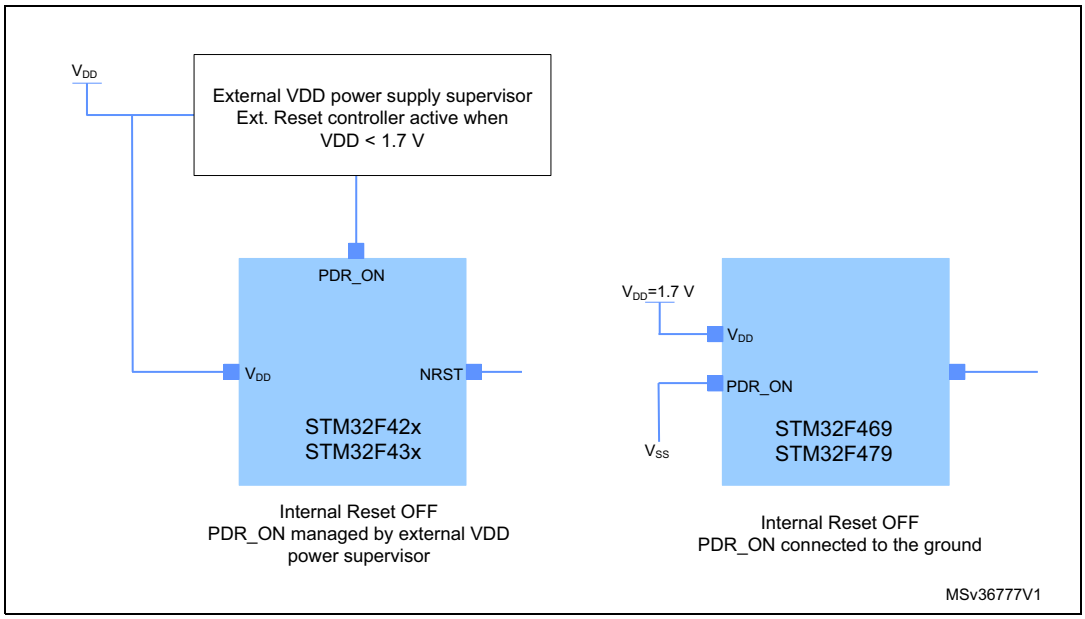
Table 13 summarizes new power controller features integrated on STM32F469xx/STM32F479xx, compared to STM32F42xxx/ STM32F43xxx.

Table 13. PWR controller: STM32F469xx/STM32F479xx vs STM32F42xxx/STM32F43xxx

PWR	STM32F42xxx/STM32F43xxx	STM32F469xx/STM32F479xx
Power supplies	NA	Dedicated USB power rail enabling on-chip PHYs operation throughout the entire MCU power supply range
Power supplies supervisor(1)	PDR_ON: power supervisor enable pin managed by external VDD power supervisor	PDR_ON: power supervisor pin managed in static way. (Disable internal Reset without the need of external VDD power supervisor)
Power control registers	PWR_CR	
	WUF bit: Wakeup flag for the WKUP pin, RTC alarm (Alarm A or Alarm B), RTC Tamper event, RTC TimeStamp event or RTC Wakeup	WUPF bit: dedicated flag for wake-up pin PA0
	PWR_CR	
	CWUF: Clear wakeup flag	CWUPF: Clear Wakeup Flag for PA0 Pin

1. Please refer to *Figure 6* for more details on Power supply differences.

Figure 6. Power supply supervisor: STM32F42xxx/STM32F43xxx vs STM32F469xx/STM32F479xx



2.7 Audio interfaces

The STM32F42xxx/STM32F43xxx and STM32F469xx/STM32F479xx series embed almost the same audio interface features. An SPDIF-Tx output was added to STM32F469xx/STM32F479xx lines.

Table 14. Audio interfaces comparison

Audio interfaces	STM32F42xxx/STM32F43xxx	STM32F469xx/STM32F479xx
SPDIF-Tx	NA	SPDIF-Tx output

2.8 USB OTG

The STM32F42xxx/STM32F43xxx and STM32F469xx/STM32F479xx series implement similar USB OTG peripherals.Some enhancements were done for STM32F469xx/STM32F479xx series which are listed in *Table 15*.

Table 15. USB OTG differences between STM32F469xx/STM32F479xx and STM32F42xxx/STM32F43xxx

USB	STM32F42xxx/STM32F43xxx	STM32F469xx/STM32F479xx
Features	Universal Serial Bus Revision 2.0 Full support for the USB On-The-Go (USB OTG)	
	USB internal connect/disconnect feature with an internal pull-up resistor on the USB D + (USB_DP) line	
	NA	Dedicated USB power rail enabling on-chip PHYs operation throughout the entire MCU power supply range (allowing lower VDD down to 1.8 V while using USB)
	FS mode	
	1 bidirectional control endpoint 3 IN endpoints (Bulk, Interrupt, Isochronous) 3 OUT endpoints (Bulk, Interrupt, Isochronous 8 Host mode channels	1 bidirectional control endpoint 5 IN endpoints (Bulk, Interrupt, Isochronous) 5 OUT endpoints (Bulk, Interrupt, Isochronous) 12 Host mode channels
	HS mode	
	1 bidirectional control endpoint 5 IN endpoints (Bulk, Interrupt, Isochronous) 5 OUT endpoints (Bulk, Interrupt, Isochronous 12 Host mode channels	1 bidirectional control endpoint 7 IN endpoints (Bulk, Interrupt, Isochronous) 7 OUT endpoints (Bulk, Interrupt, Isochronous) 16 Host mode channels
Buffer memory	FS mode	
	Management of up to 4 Tx FIFOs (1 for each IN end point) + 1 Rx FIFO	Management of up to 6 Tx FIFOs (1 for each IN end point) + 1 Rx FIFO
	HS mode	
	Management of up to 6 Tx FIFOs (1 for each IN end point) + 1 Rx FIFO	Management of up to 8 Tx FIFOs (1 for each IN end point) + 1 Rx FIFO
Low-power modes	FS mode	
	USB suspend and resume LPM not supported	USB suspend and resume Link Power Management (LPM) support
	HS mode	
	LPM not supported	Link Power Management (LPM) support

2.9 Digital camera interface (DCMI)

The STM32F42xxx/STM32F43xxx and STM32F469xx/STM32F479xx series embed similar DCMI peripherals. Some new features were added to STM32F469xx/STM32F479xx series which are listed in the *Table 16*.

Table 16. DCMI features: STM32F469xx/STM32F479xx vs STM32F42xxx/STM32F43xxx

DCMI	STM32F42xxx/STM32F43xxx	STM32F469xx/STM32F479xx
Parallel interface	8-, 10-, 12- and 14-bit	
Embedded synchronization	Yes	
External line and frame synchronization	Yes	
Crop feature	Yes	
Supported data format	8/10,12,14 bit progressive video (monochrome or raw Bayer)	
	RGB565 progressive video	
	YCbCr4:2:2 format	
	NA	YCbCr format – Y only (Black and White)
	NA	Half resolution image extraction
	Compressed JPEG	
DCMI control register	NA	New bits added in DCMI_CR register: – BSM and OEBS bits: allow configuring the byte selection for capture – LSM and OELS bits: allow configuring the line selection for capture

2.10 Secure digital input/output interface (SDIO)

The STM32F42xxx/STM32F43xxx and STM32F469xx/STM32F479xx series embed very similar SDIO module. The differences are listed in the *Table 17*.

Table 17. SDIO comparison: STM32F469xx/STM32F479xx vs STM32F42xxx/STM32F43xxx

SDIO	STM32F42xxx/STM32F43xxx	STM32F469xx/STM32F479xx
Features	Full compliance with MultiMediaCard System Specification Version 4.2 Full compliance with SD Memory Card Specifications Version 2.0 Full compliance with SD I/O Card Specification Version 2.0	
	Full support of the CE-ATA features	NA
SDIO registers	-	CE-ATA protocol related features are removed from specification (SDIO_STA, SDIO_ICR and SDIO_CMD registers have been updated)

3 Conclusion

This application note is a useful complement to datasheets and reference manuals which gives a simple guide to migrate an existing product based on the STM32F42xxx/STM32F43xxx device to the STM32F469xx/F479xx device.

4 Revision history

Table 18. Document revision history

Date	Revision	Changes
12-May-2015	1	Initial release.
30-Jul-2015	2	Deep change of *Section 1* related with adding information on pinout / ballout differences for all common package types.
16-Oct-2015	3	SDMMC renamed in SDIO and SDIO/SDMMC in SDIO in the whole document. “DSI lines” changed in DSIHOST dedicated IOs, in comments for *Figure 1*, *Figure 3* and *Figure 4*. “Ports” and “port” substituted with “IO ports” and “IO port”, respectively, in comments for *Figure 1*, *Figure 2*, *Figure 3*, *Figure 4* and *Figure 5*.