AN4717

STEVAL-ILD005V1: Trailing edge phase control rotary wall dimmer based on STF17N62K3 power MOSFET

Anselmo Liberti

Introduction

The STEVAL-ILD005V1 evaluation board implements a simple and cost-effective MOS-based reverse phase cut dimming solution for analog wall dimmers using a pair of STF17N62K3 power MOSFETs controlled by a triple 3-input NOR gate to effectively dim resistive or capacitive lighting loads available for domestic or industrial use (i.e. halogen lamps, electronic low voltage transformers and various dimmable CFL/LED lamps). The AC analog control dimming technique allows on/off power switching and up/down dimming functions through a single linear rotary potentiometer equipped with a mechanical switch which opens the circuit at the minimum setting. Control of the board is achieved with a triple 3-input NOR gate (pin-to-pin compatible with ST's HCF4025BE 14-lead dual in-line CMOS gate logic device in a plastic SO-14 micropackage), which acts as a gate driving voltage signal source and performs zero crossing detection and timing through the use of a few other passive components and diodes.

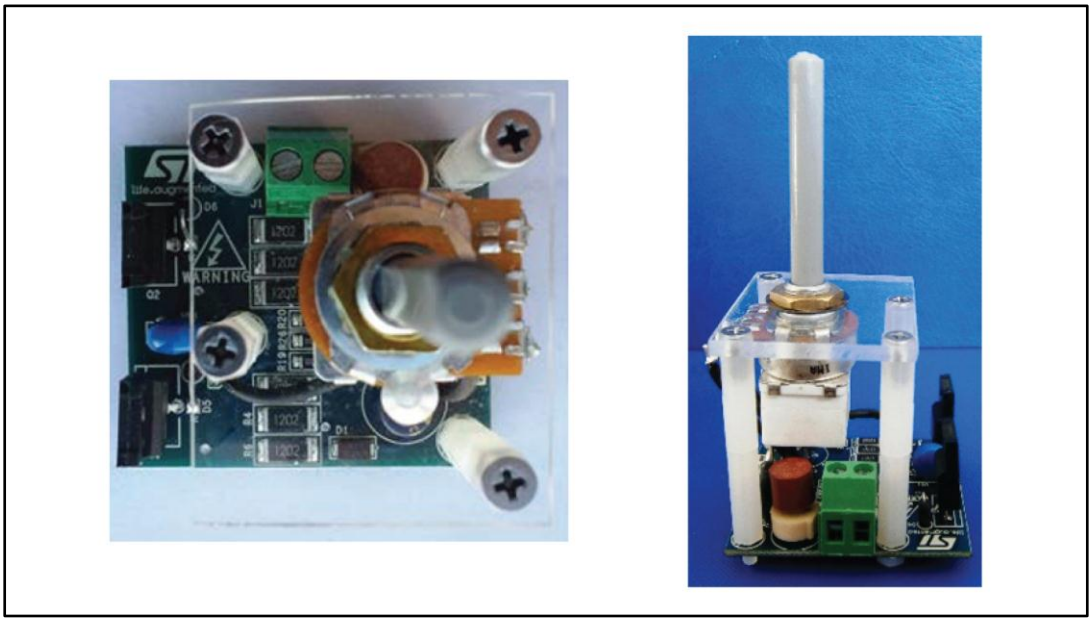
The 15.5 A /620 V SuperMESH3 MOSFET STF17N62K3 in the TO-220 full package used for the lamp current commutations is the most suitable device for the requirements of this trailing edge phase cut dimmer switch application operating at line frequency (50/60 Hz) because its high total input capacitance and sufficiently low on-resistance at the operating currents provides the best trade-off between efficiency and EMI in a particularly simplified dimmer design solution.

The main features of this dimmer are:

- operation for 2-wire wall dimmer
- trailing-edge control only (compatible with all lamps commonly found on the market)
- operation on 110 V_{rms} or 230 V_{rms} line voltage (±10 %) and 50 Hz or 60 Hz line frequency
- dimmable power range (without heatsinks mounted on power MOSFETs)
  - 40 W to 300 W for 230 V_{rms} line
  - 15 W to 90 W for 110 V_{rms} line
- maximum operating ambient temperature: 50 °C
- power efficiency @ Max power - 230 V_{AC} > 95%
- power factor @ Max power > 0.98
- control and regulation interface with a switched type single linear rotary potentiometer
- compliance with EMC standards:
  - EN55015 (for European market): compliant with 300 W - 230 V_{AC} halogen lamp
  - IEC 61000-4-5: criteria A for 2 kV surge tests
- RoHS compliant
  Other features include:
  - flicker-free dimming performance
  - smooth dimming operation and silent dimming control with no buzzing or audible noise
  - acceptable levels of EMI noise without the need for LC filters to reduce conducted emission disturbances
  - low inrush current generation

This application note describes the operating principle and working conditions of the STEVAL-ILD005V1 board. An electrical evaluation of the dimmer performance is also given in terms of temperatures, turn-off energies and EMC standard testing.

Figure 1: STEVAL-ILD005V1 board: top and side views



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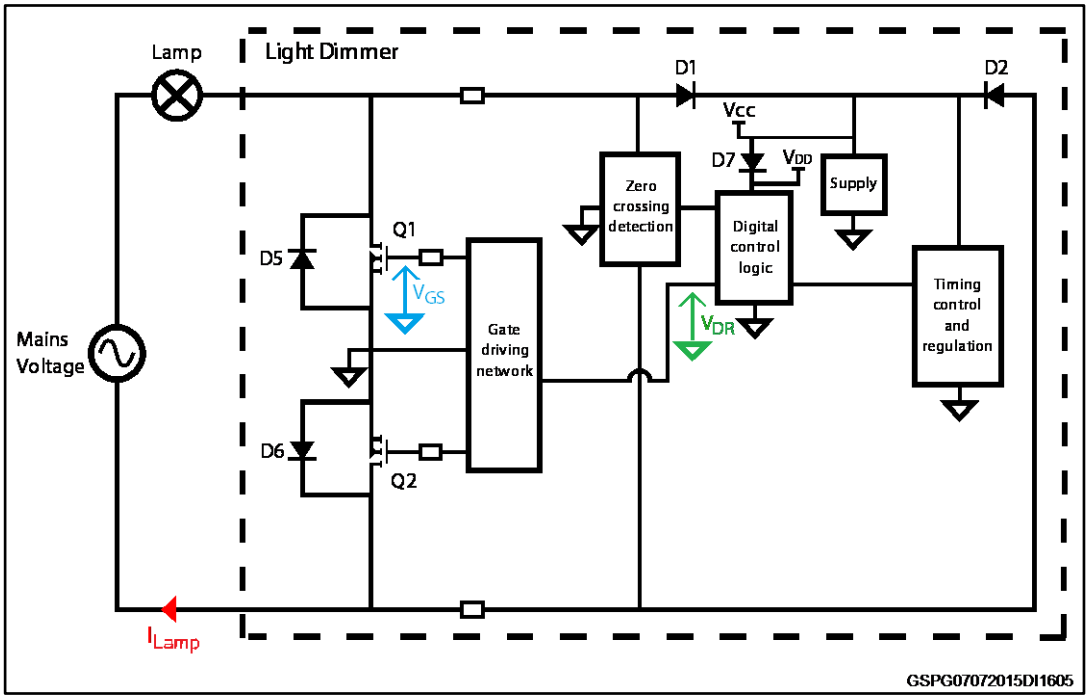
1 Operation principle

1.1 Functional block diagram

The simplified functional diagram of the board is shown in the figure below. In this dimmer design, a single source driving network is used to simultaneously activate and deactivate both gates of the two STF17N62K3 MOSFETs (Q1 and Q2) having sufficiently low $R_{DS(on)}$ at the operating currents ($R_{DS(on)\ max}$ = 0.34 Ω @ V_{GS} = 10 V and I_D = 7.5 A at T_C = 25 °C) and connected to each other in an anti-series configuration or common source electrical topology.

In steady state working conditions, the digital control logic stage supplies the gate driving network with a voltage signal V_{DR} equal to 15 V and pulsed at twice the mains frequency in order to properly drive the MOSFETs with a PWM gate to source voltage signal V_{GS} ~ 14V. The dimmer operates in trailing edge operation mode and each MOSFET is therefore always turned on instantanly at the beginning of the half line cycle in both positive and negative main envelopes and maintains the on-state condition up to a controllable time instant set internally to the same half cycle.

Figure 2: STEVAL-ILD005V1 functional block diagram



From the block diagram above, the following distinct functional stages interact with each other to perform the overall dimming functionality:

- **Zero crossing detection network:** consists of two passive sub-networks (each consisting of resistors, capacitors and diodes) connected separately to both phase and neutral lines and symmetrically arranged with respect to the ground plan. It allows detection of the crossing point of the input main voltage with the zero level in the ascendant or descendant slope phases for the respective positive and negative portions of the main line envelope in order to properly activate the conduction phases of the two MOSFETs.

- **Supply stage:** allows the generation of the dc voltage signal V_{CC} clamped to around 15 V by a Zener diode in order to provide the V_{DD} supply voltage necessary for the triple 3-input NOR gate logic activation.
- **Gate driving network:** consists of resistances only with an appropriate setting to guarantee the proper driving condition for the MOSFET gates and to achieve the best trade-off between efficiency and EMI performance.
- **Timing control and regulation stage:** consists of the potentiometer and other passive components (resistances and capacitances) opportunely set to allow the regulation and control of the conduction time of the MOSFETs in order to perform the dimming function.
- **Digital control logic stage:** implemented with a triple 3-Input NOR Gate logic to detect the zero crossing point instant time and activate the switch on phases of the MOSFETs with the application of the gate driving voltage signal for an interval set by the *Timing control and regulation* stage and depending on the specific operating condition for the dimming function.

No EMI filtering stage (capacitor + inductor) is required at the input of the dimmer because the gate driving network is set to slow the current falling edge down at the turn-off switching transients in order to reduce the conducted electromagnetic noise and meet the requirements of the EN55015 standard.

The electrical design is also optimized to limit the MOSFET power losses during conduction phases and maximize the overall efficiency for the best trade-off between power dissipation and EMI. Due to the alternating trend of both line mains and lamp current, as the two MOSFETs are connected to each other in an *anti-series* configuration with a single gate driving network implemented to simultaneously control both devices, in every half cycle of the main voltage, the current always flows through one MOSFET in *forward conduction* mode (or in the first quadrant operation and crossed by a positive drain current) and simultaneously through the other MOSFET in *reverse conduction* mode (or in the third quadrant operation and crossed by a negative drain current). In this way, it is also possible to exploit the ohmic resistance reverse conduction capability of the MOSFET channel when conducting a reverse direction current (from source to drain) by maintaining the same $R_{DS(on)}$ characteristic as the conventional first quadrant operation.

Obviously, the reverse drain current flows through the MOSFET channel resistance by shunting the parasitic body diode, provided that the $V_{DS(on)}$ value is small enough and lower than the forward drop voltage of the intrinsic reverse diode, due to the appropraite low on-resistance value in that particular operating condition for the MOSFET current. External diodes (D5 and D6) connected in antiparallel to each MOSFET are also inserted to allow an additional path for the sharing of the lamp current with the MOSFET (channel or intrinsic diode) during the negative drain current conduction phase and in particular during the start-up phases when the average lamp current levels can be higher than the steady state working condition as a consequence of the cold state of the board and lighting load.

At 230 V_{AC} input main voltage conditions, the minimum and maximum duration of the settable duty cycles are approximately equal to 20% and 82% respectively of the whole half line cycle.

For a positive mains half cycle, the lamp current passes through:

- **Q1** working on the first-quadrant operation or forward conduction with positive current
- **Q2** working on the third-quadrant operation and reverse conduction current (through channel resistance or intrinsic diode)
- **D6** working on forward biasing condition

For negative mains half cycle, the lamp current passes through:

- **Q2** working on the first-quadrant operation or forward conduction with positive current;

- **Q1** working on the third-quadrant operation and reverse conduction current (through channel resistance or intrinsic diode);
- **D5** working on forward biasing condition.

A dead time for the current across the MOSFETs also occurs when the gate driving voltage signal is zero and remains in this state until the end of the half line cycle with no current flowing in the lamp.

1.1.1 Digital control logic

The following digital control logic stage functional diagram shows the interconnection of the three 3-input NOR gate PINS and the relative PIN descriptions.

Figure 3: Digital control logic functional diagram

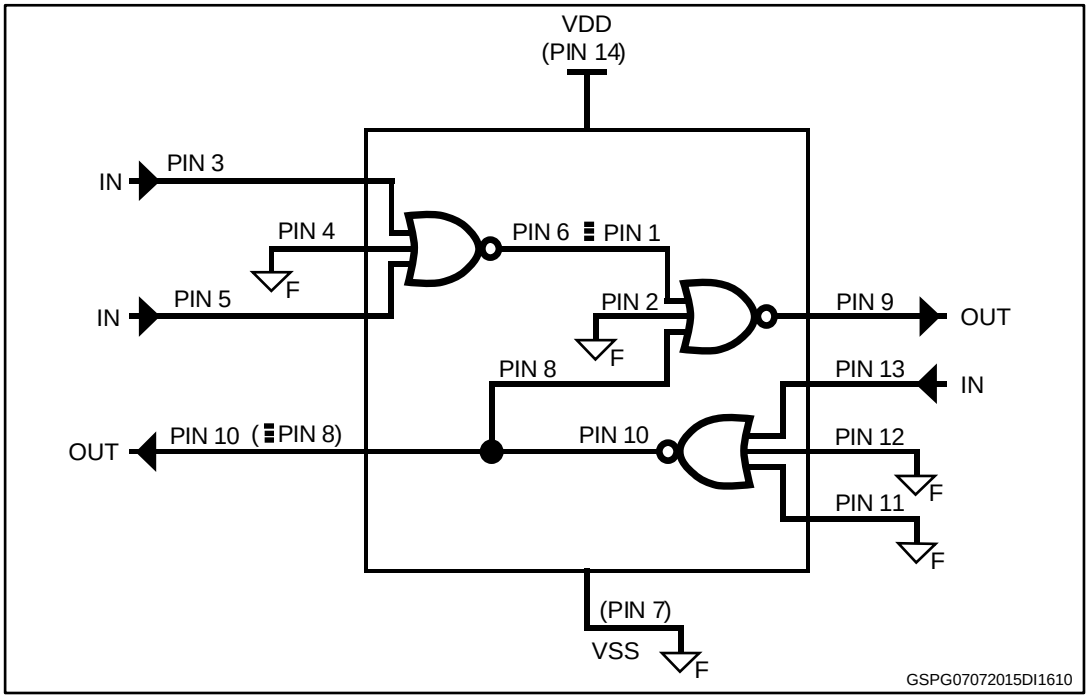


Table 1: Pin description

Pin no.	Name and function
3, 5, 13	Data inputs
9, 10 (≡ 8)	Data outputs
1 ≡ 6	Intermediate connection
2, 4, 11, 12	Connected to GND
7	Negative supply voltage V_{SS} to GND
14	Positive supply voltage to V_{DD}

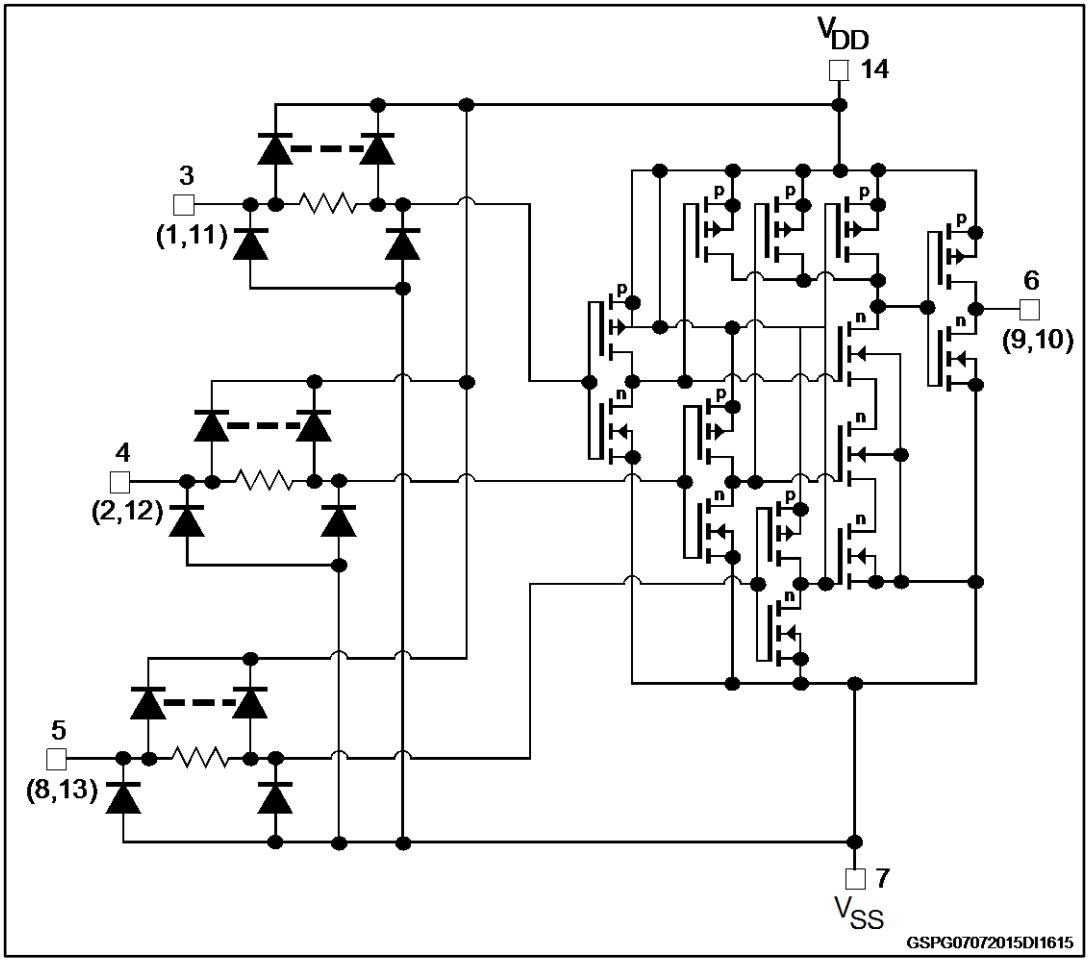
The digital control is implemented by a logic circuit with 3 inputs and 2 outputs and the associated logic function (calculating the correlation between each output and the inputs) can be expressed via the following mathematical expressions (where I_x and O_y indicate the respective input and output PINs to the logic circuit):

Equation 1

$$\begin{cases} O_9 = (I_3 + I_5) \cdot I_{13} \\ O_{10} = \overline{I_{13}} \end{cases}$$

All inputs are protected by a CMOS protection network as shown in the figure below, referring to the single triple input NOR gate where the numbers in parentheses are terminal numbers for the other gates (refer to the CMOS NOR gate CD4025B datasheet).

Figure 4: Single triple input NOR gate schematic



Therefore, for all the logic inputs, the voltage range (with reference to V_{SS} = 0 V pin voltage) is from -0.5 V to V_{DD} +0.5 V, where the positive supply voltage V_{DD}= V_{CC} – VD7 and the maximum dc voltage signal V_{CC} (generated by the supply stage) is clamped to +15 V by a Zener diode between V_{CC} and the negative supply voltage pin (V_{SS}) of the logic.

The following truth table describes the Boolean function with all the possible operating conditions (or states) that the logic circuit can theoretically assume in the steady state working condition and expressed as correlations between inputs and outputs with binary symbols 0 and 1.

Table 2: Truth Table of the logic states

Truth table						State	Working phase	Operating condition
	Inputs			Outputs				
Pin	3	5	13	9	10			
Logic values	0	0	0	0	1	1	Steady state (positive and negative main voltage envelope)	MOSFET on state
	0	0	1	0	0	2	Steady state (positive and negative main voltage envelope)	MOSFET off state (first phase)
	0	1	0	0	1	3	X	
	0	1	1	1	0	4	Steady state (negative main voltage envelope)	MOSFET off state (second phase)
	1	0	0	0	1	5	X	
	1	0	1	1	0	6	Steady state (positive main voltage envelope)	MOSFET off state (second phase)
	1	1	0	0	1	7	X	
	1	1	1	1	0	8	X	

In the above table, the symbol X indicates that the input combinations referring respectively to STATES 3, 5, 7 and 8 never occur during regular dimmer operation and therefore can be ignored.

The real operational states are:

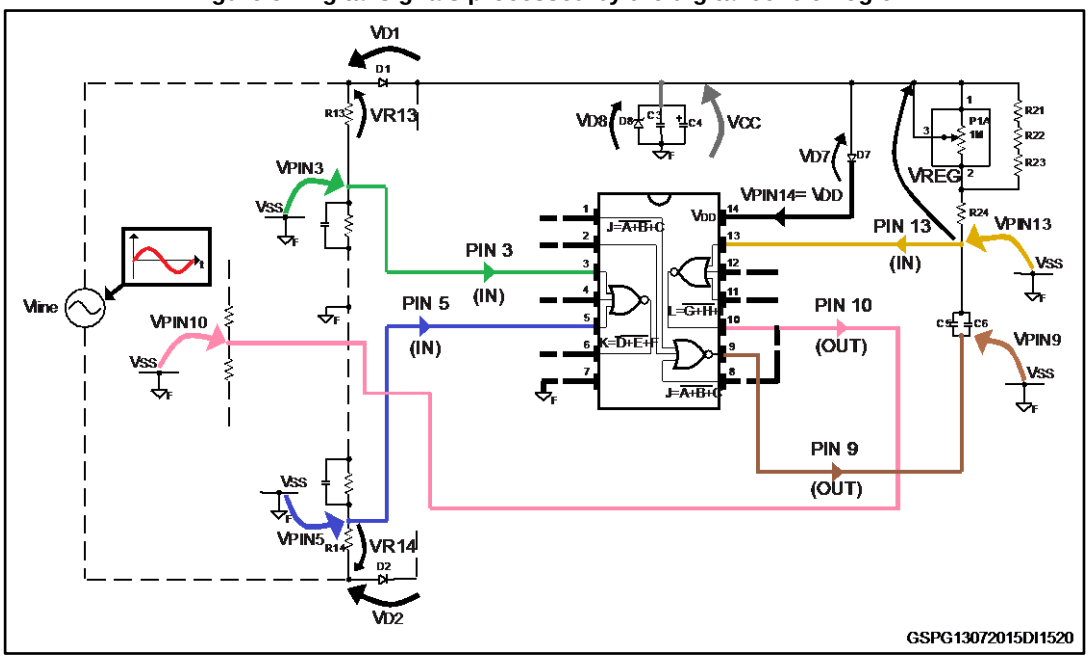
- STATE 1: occurs during the steady on-state operation of the MOSFETs
- STATES 2, 4 and 6: occur during the steady off-state operation of the MOSFETs

All the operating conditions for the above states can also occur during the dimmer startup phases when a low biasing condition for the driving voltage V_{DR} at the output of the digital control logic circuit imposes an inadequate gate-to-source voltage V_{GS} (lower than the nominal value of ~ 14 V) because the supply voltage V_{DD} still hasn't reached the steady state value of 15 V during its rise in the startup transient.

The supply stage voltage signal and all the input/output data from/to the Triple 3-input NOR gate logic circuit are detailed below and distinguished in *Figure 5: "Digital signals processed by the digital control logic"* as digital signals of the logic circuit functionality:

- Supply stage: voltage signal V_{CC}
- Input data to the logic circuit:
  - signals from cross detection stage: voltage signals V_{PIN3} and V_{PIN5} at PIN3 and PIN5 respectively
  - signal from timing control stage: voltage signal V_{PIN13} at PIN13
- Output data from the logic circuit:
  - signal to gate driving stage: voltage signal V_{PIN10} at PIN10
  - signal to timing control stage: voltage signal V_{PIN9} at PIN9

Figure 5: Digital signals processed by the digital control logic



The theoretical waveforms and command sequences from/to the logic circuit are depicted in *Figure 6: "Theoretical waveforms and command sequences"* together with the input main voltage variation under steady state working conditions (STATE 2 is not included as it is a fast transitory in comparison to the others), with:

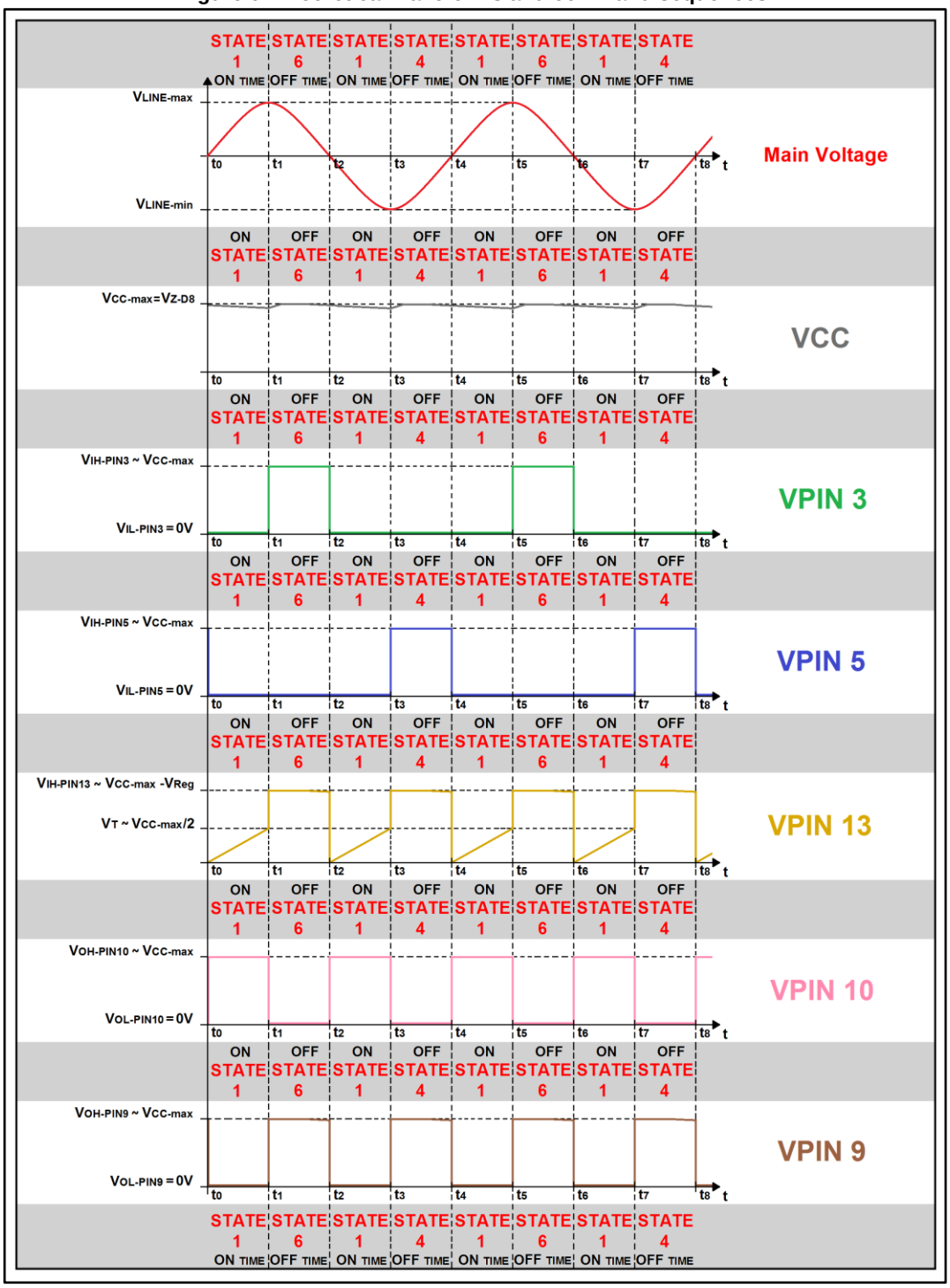
- $V_{LINE-min}$, $V_{LINE-max}$ = maximum and minimum values of the main voltage
- VZ-D8 = D8 diode breakdown voltage (equal to 15 V with a tolerance of 20 %)
- V_{CC-max} = maximum value of the supply voltage V_{CC} (with $V_{CC} = V_{DD}+V_{D7}\sim V_{DD}$)
- V_{REG} = Voltage drop on the whole resistive regulation stage with the resistive potentiometer and the other series and parallel resistances (R21, R22, R23 and R24)
- $V_{IH-PIN3}$, $V_{IH-PIN5}$, $V_{IH-PIN13}$ = high voltage levels of the input data at PIN3, PIN5 and PIN13 (with $V_{IH-PIN3} = V_{IH-PIN5}\sim V_{CC\ max}$ by neglecting the voltage drops on the resistances R13/R14 and on the diodes D1/D2/D7; $V_{IH-PIN13}\sim V_{CC\ max}-V_{REG}$)
- V_T = the threshold value (set to around $V_{CC\ max}/2$) of each NOR gate input
- $V_{OH-PIN9}$, $V_{OH-PIN10}$ = high voltage levels of the output data at PIN9 and PIN10 (with $V_{OH-PIN9} = V_{OH-PIN10} \sim V_{CC\ max}$)

Moreover, for all the low voltage levels of the input (V_{PIN3}, V_{PIN5} and V_{PIN13}) and output (V_{PIN9} and V_{PIN10}), the data is assumed to be:

Equation 2

$$V_{IL-PIN3} = V_{IL-PIN5} = V_{IL-PIN13} = V_{OL-PIN9} = V_{OL-PIN10} = V_{SS} = 0\ V$$

Figure 6: Theoretical waveforms and command sequences



1.2 Steady-state stage-wise circuit analysis

In a trailing edge phase-cut dimmer, the MOSFETs are turned on when the line voltage (and therefore the current through the devices) passes through zero during the ascendant or descendent slopes of its respective positive or negative envelopes. The dimmer uses a timing control and regulation circuit to turn the current supply to the fixture on and off at

regular intervals, typically 100 or 120 times per second (for 50 Hz or 60 Hz line frequencies), too fast to be perceived by the human eye.

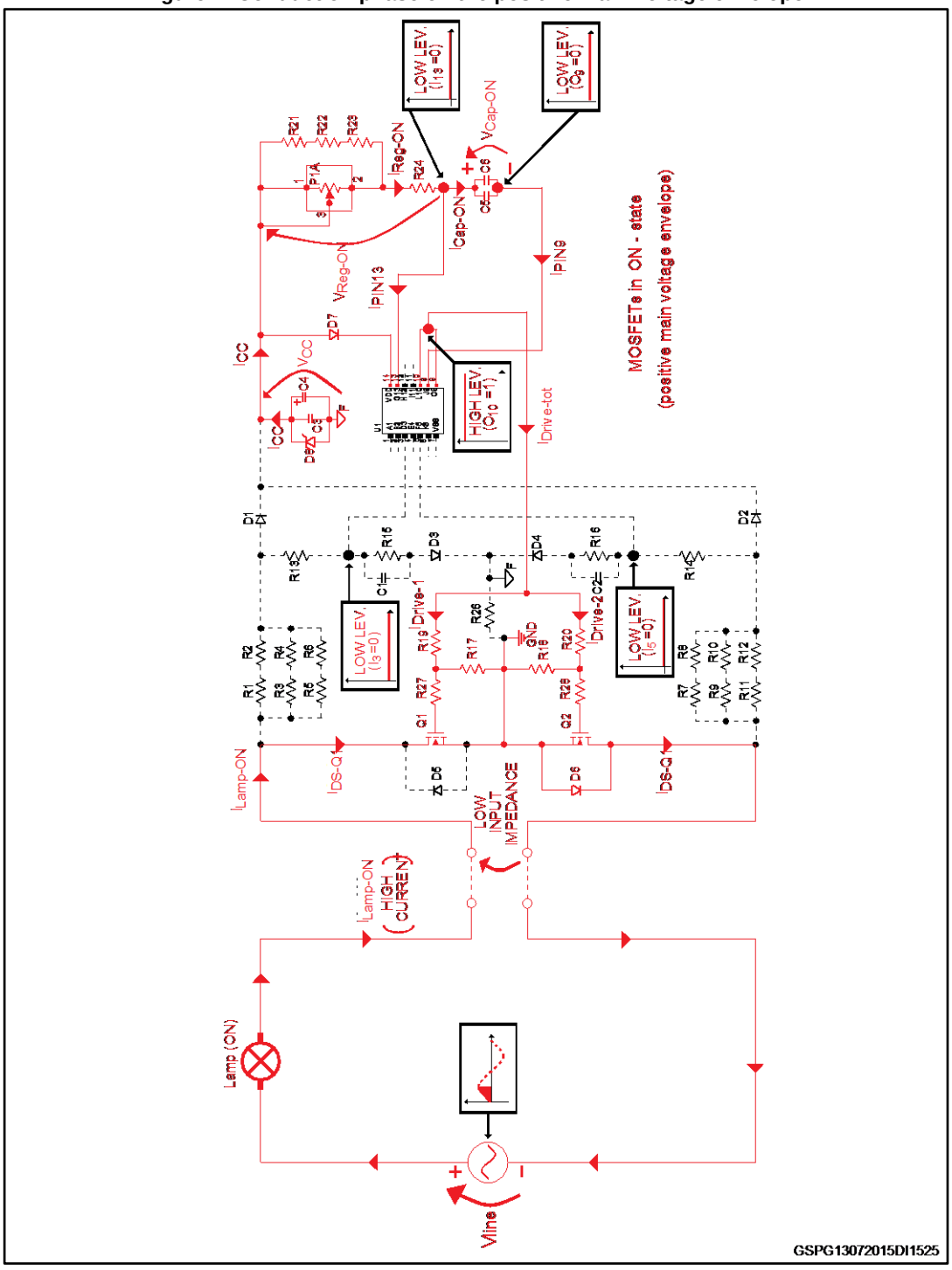
The circuit implements two STF17N62K3 MOSFETs as switches: when the switches are simultaneously turned on, a significant current flows through the devices and the lamp, while when the switches are simultaneously turned off, negligible current flows through the circuit. The amount of time in which the current is on determines the brightness or dimming effect of the lamp. In fact, by turning the switch on and off twice every line cycle, the rms voltage applied to the lamp is reduced from 230 V_{AC} to a lower value, so the rms current that flows through the lamp is also reduced and produces less light.

During the dimmer startup phases, the MOSFETs working in the on state may operate under a low biasing condition for the gate driving voltage signal because the supply voltage V_{CC}, such as all the input/output logic circuit PINs, hasn't properly reached the nominal voltage of ~15 V.

This section provides a comprehensive description of the trailing edge phase cut dimmer circuit operation through a stage-by-stage circuit analysis under steady state conditions, divided into sequential functional phases according to the variation over a period of the main voltage starting from the time instant at zero voltage value on the ascendant slope of the positive envelope. For simplification purposes, STATE 2 is not included (considered a fast transitory compared to the others during the normal operation) and the leakage currents flowing on the diodes working in reverse-bias operation are neglected.

- **Conduction phase on the positive main voltage envelope (STATE 1):** the zero crossing detection network recognizes the instant when the main line passes through the zero value on the ascendant voltage slope because all the three input signals to the digital control logic circuit V_{PIN3}, V_{PIN5} and V_{PIN13} are at the same low voltage detected as zero logic level conditions (respectively I3=0, I5=0 and I13=0). In this case, the turn on phase of the two MOSFETs is instantaneously activated by the logic circuit that applies a high logic level signal (O10=1, V_{DR}=$V_{OH\text{-}PIN10}$ ~$V_{CC\ max}$) at the output of the PIN10 for the resistive driving network to the gates, maintaining a zero logic level output at PIN9 (09 = 0, V_{PIN9} = 0 V).
  Due to the slow discharging transient of the supply stage (i.e., paralleled capacitances C3 and C4) through the regulation stage (with the resistive potentiometer and the other series and parallel resistances R21, R22, R23 and R24), the voltage V_{PIN13} increases during the whole conduction phase via the charging current $I_{REG\text{-}ON}$ on the capacitive node corresponding to PIN13. Therefore, the conduction phase lasts for the time required for the voltage on PIN13 (V_{PIN13}) to reach the threshold value of around $V_{CC\ max}$/2 starting from the zero value condition.

Figure 7: Conduction phase on the positive main voltage envelope



- **Turn-off phase on the positive main voltage envelope (STATE 2 and STATE 6):**
  - **STATE 2**: when the voltage V_{PIN13} of the input signal at PIN13 reaches the threshold value V_T~V_{ccmax}/2, the following changes occur in sequence:
    a. input signal V_{PIN13} changes its status detected by the digital control logic from low logic level (I13=0) to high logic level (I13=1);
    b. output signal V_{PIN10} changes its status from high logic level (O10=1, V_{PIN10}~V_{ccmax}) to zero logic level (O10=0, V_{PIN10} = 0 V).

Under this operating condition, the voltage signal V_{DR} applied to the resistive driving network for the MOSFET gates is turned off instantly.

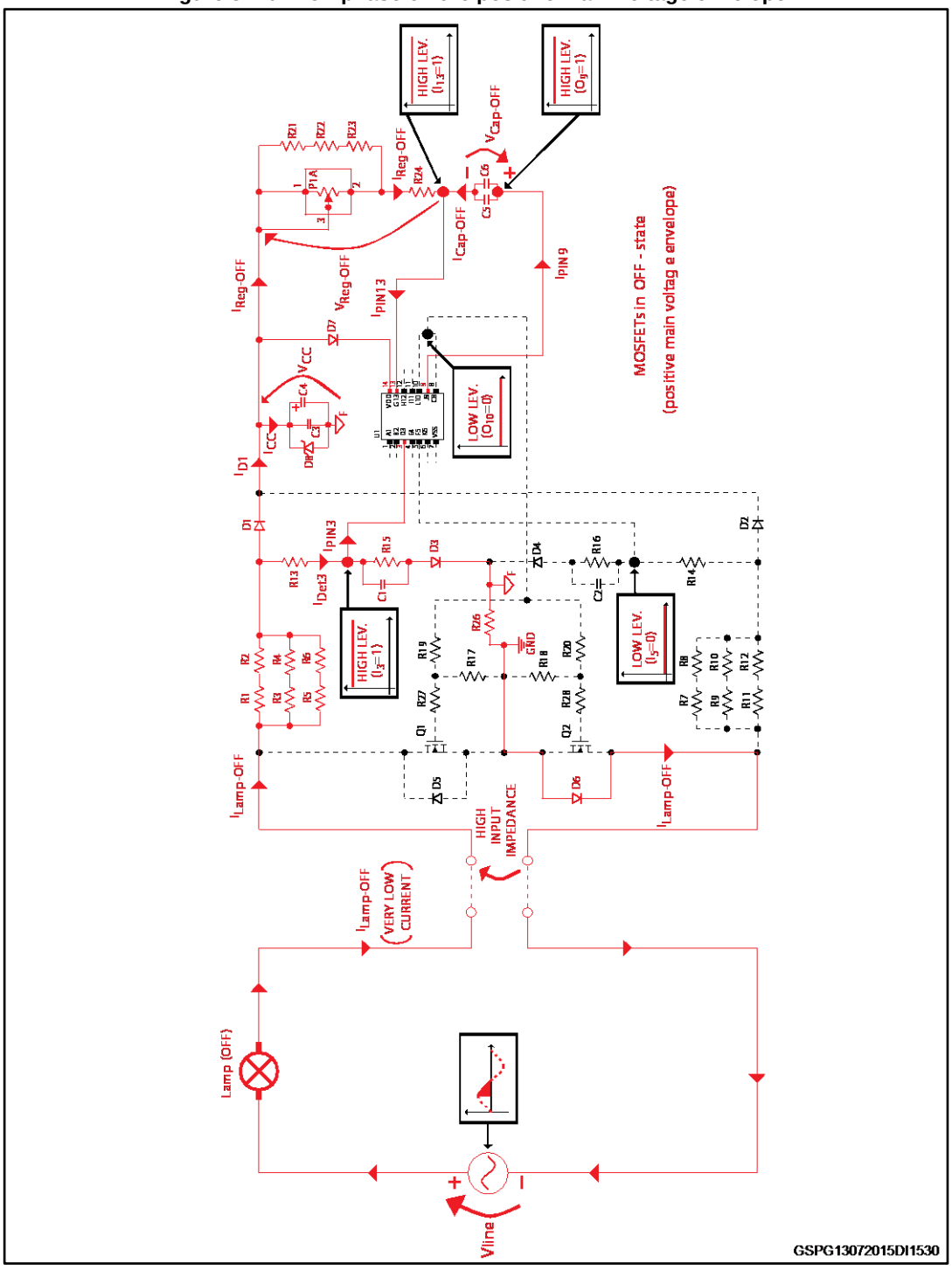
  - **STATE 6:** As a consequence of the disabled condition for driving the MOSFETs, the charge of the capacitance C1 placed on the cross detection network with a current I_{DET-3} becomes involved and the following changes occur in sequence:
    a. input signal V_{PIN3} changes its status from low logic level (I3=0) to high logic level (I3=1, V_{PIN3}~ $V_{CC\ max}$)
    b. output signal V_{PIN9} changes its status from zero logic level to high logic level (O9=1, V_{PIN9}~$V_{CC\ max}$)
    c. input signal V_{PIN13} instantly rises to $V_{IH-PIN13}$ = $V_{CC\ max}$ – V_{reg} and a very low discharge current $I_{REG-OFF}$ continues to flow from the supply stage (paralleled capacitances C3 and C4) towards the node associated with PIN13 involving full discharge and voltage polarity inversion phases sequentially on paralleled capacitances C5 and C6.

When the main voltage reaches zero during its positive descendant slope, the following changes occur in sequence:

1. capacitance C1 is fully discharged and the input signal V_{PIN3} changes status from high logic level (I3=1 associated with V_{PIN3}~ $V_{CC\ max}$) to zero logic level (I3=0)
2. output signal V_{PIN9} changes status to zero logic level (O9=0), as the input signal V_{PIN5} is at low logic level (I5=0)
3. input signal V_{PIN13} instantly passes from high to zero logic level condition.

This last operating (STATE 1) condition, with all the three V_{PIN3}, V_{PIN5} and V_{PIN13} input signals at the same zero logic level condition (I3=0, I5=0 and I13=0), sets the digital control logic circuit for the new conduction phase in the next half main cycle.

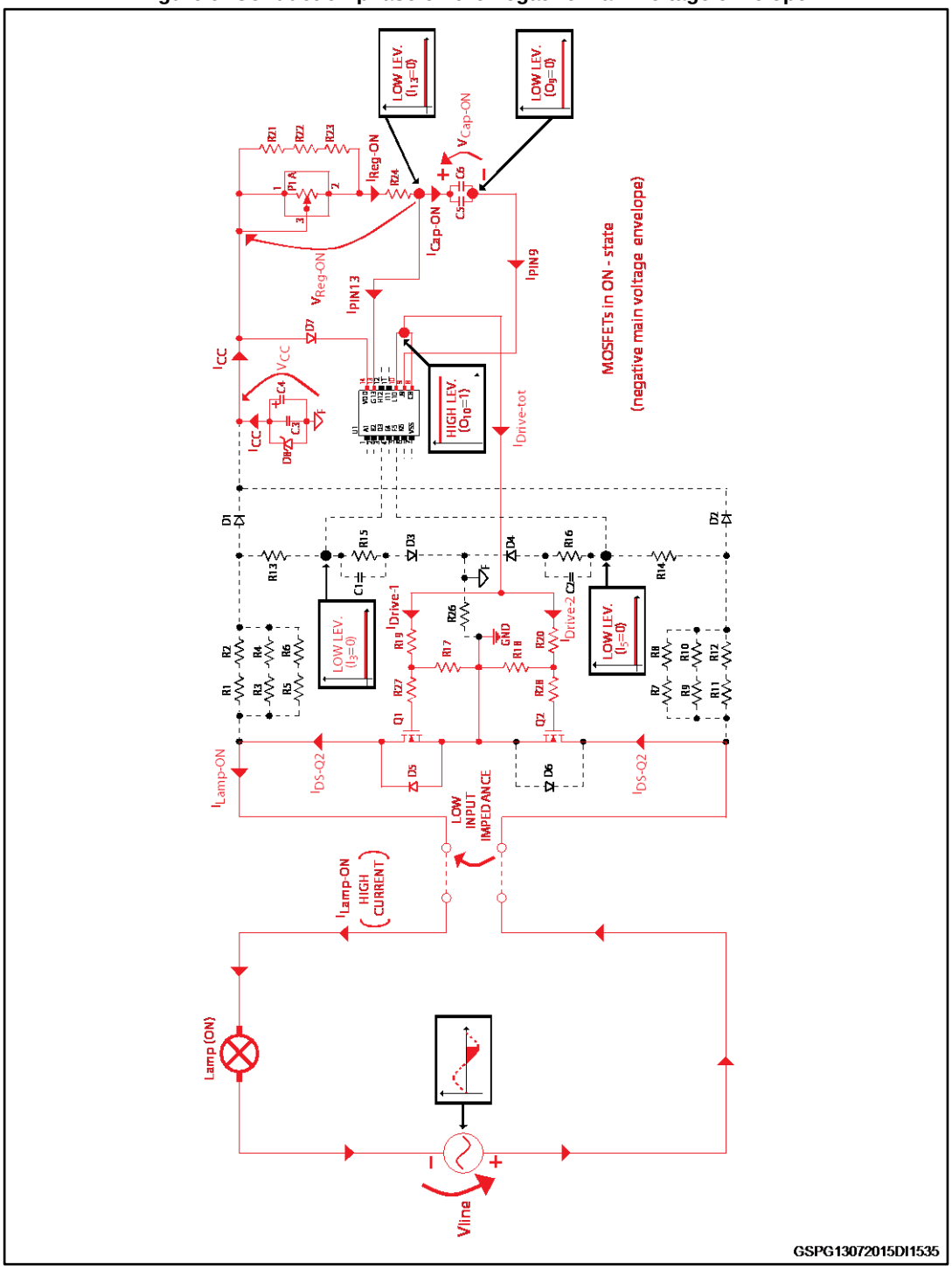
Figure 8: Turn-off phase on the positive main voltage envelope



- **Conduction phase on the negative main voltage envelope (STATE 1):** the zero crossing detection network recognizes the instant when the main line passes through the zero value on the descendant voltage slope because all the three input signals to the digital control logic circuit V_{PIN3}, V_{PIN5} and V_{PIN13} are at the same low voltage detected as zero logic level conditions (respectively I3=0, I5=0 and I13=0). In this case, the turn-on phase of the two MOSFETs is instantaneously activated by the logic circuit that applies a high logic level signal to the output of PIN10 (O10=1,

V_{DR}=V_{PIN10}~$V_{CC\ max}$) for the resistive driving network to the gates, maintaining the output at PIN9 at zero (09=0,V_{PIN9} = 0 V).
Due to the slow discharging transient of the supply stage (paralleled capacitances C3 and C4) through the regulation stage (resistive potentiometer and the series and parallel resistances R21, R22, R23 and R24), the voltage V_{PIN13} rises during the whole conduction phase via the charging current I_{REG-ON} on the capacitive node associated with PIN13. Therefore, the conduction phase lasts for the period required for V_{PIN13} to reach the threshold value of around V_{ccmax} /2 starting from the zero value condition.

Figure 9: Conduction phase on the negative main voltage envelope



- **Turn-off phase on the negative main voltage envelope (STATE 2 and STATE 4)**:
  - **STATE 2:** when the input signal voltage V_{PIN13} reaches the threshold value V_T~V_{ccmax}/2, the following changes occur in sequence:
  a. input signal V_{PIN13} changes its status detected by the digital control logic from low logic level (I13=0) to high logic level (I13=1)
  b. output signal V_{PIN10} changes its status from high logic level (O10=1, V_{PIN10}~V_{ccmax}) to zero logic level (O10=0, V_{PIN10} = 0 V)

Under this operating condition, the voltage signal V_{DR} applied to the resistive driving network for the MOSFET gates is instantly turned off.

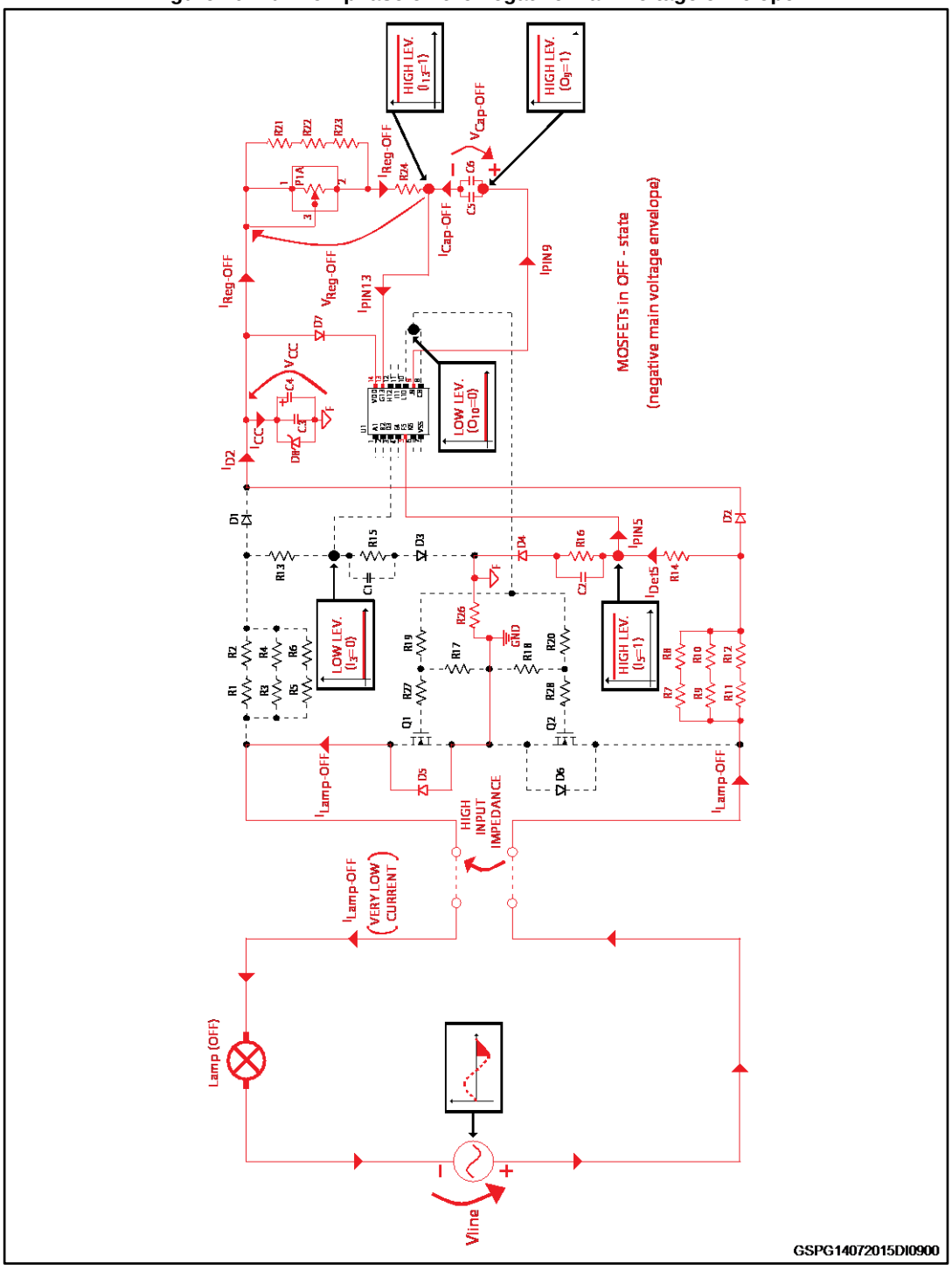
- **STATE 4:** as a consequence of the disabled condition for driving the MOSFETs, the charge of capacitance C2 placed on the cross detection network with current I_{DET-5} becomes involved and the following changes occur in sequence:
  a. input signal V_{PIN5} changes its status from the low logic level (I5=0) to the high logic level condition (I5=1, V_{PIN5}~ V_{ccmax})
  b. output signal V_{PIN9} changes from zero to high logic level (O9=1, V_{PIN9}~V_{ccmax})
  c. input signal V_{PIN13} voltage instantly rises to $V_{IH-PIN13}$ = V_{ccmax} – V_{reg} and a very low discharge current $I_{REG-OFF}$ continues to flow from the supply stage (paralleled capacitances C3 and C4) towards the node relating to PIN13 involving the full discharge and voltage polarity inversion phases sequentially on the paralleled capacitances C5 and C6.

When the main voltage reaches zero during its negative ascendant slope, the following changes occur in sequence:

1. capacitance C2 is fully discharged and input signal V_{PIN5} changes from high logic level (I5=1, V_{PIN5}~ V_{ccmax}) to zero logic level (I5=0)
2. output signal V_{PIN9} changes to zero logic level (O9=0), as the input signal V_{PIN3} is in the low logic level condition (I3=0)
3. input signal V_{PIN13} instantly passes from the high to zero logic level.

This last operating (STATE 1) condition with all the three input signals V_{PIN3}, V_{PIN5} and V_{PIN13} at the same zero logic level (respectively I3=0, I5=0 and I13=0) sets the digital control logic circuit for the new conduction phase in the next half main cycle.

Figure 10: Turn-off phase on the negative main voltage envelope



2 Operating conditions and selected components

2.1 Basic features

This board is designed to dim resistive or capacitive lighting loads available for domestic or industrial use. The main features of this dimmer are:

- operation for 2-wire wall dimmer
- trailing-edge control only (compatible with all lamps commonly found on the market)
- operation on 110 V_{rms} or 230 V_{rms} line voltage (±10 %) and 50 Hz or 60 Hz line frequency
- dimmable power range (without heatsinks mounted on MOSFETs)
  - 40 W to 300 W for 230 V_{rms} line
  - 15 W to 90 W for 110 V_{rms} line
- maximum operating ambient temperature: 50 °C
- power efficiency @ Max power - 230 V_{AC} > 95%
- power factor @ Max power > 0.98
- control and regulation interface with a switched type single linear rotary potentiometer
- supported loads
  - dimmable CFL/LED lamps
  - incandescent bulbs with halogen technology
  - electronic low voltage transformers dimmable by trailing edge phase control

2.2 MOSFET

The STF17N62K3 15.5 A, 620 V SuperMESH3 MOSFET in a TO-220 full package is the most suitable device for the requirements of this trailing edge phase cut dimmer switch application operating at line frequency (50/60 Hz) thanks to its high total input capacitance (C_{iss}=3100 pF @ V_{DS} = 50 V) and sufficiently low on-resistance at operating currents.

The main features of STF17N62K3 are:

- extremely low on-resistance: $R_{DS(on)\ max}$ = 0.34 Ω with V_{GS} = 10 V and I_D = 7.5 A at T_C = 25 °C
- high avalanche capability with I_{AR} = 15.5 A and E_{AS} = 260 mJ
- extremely high dv/dt capability: dv/dt = 9 V/ns with I_{SD} ≤ 15.5 A, di/dt ≤ 400 A/µs
- zener-protected.

2.3 Triple 3-inputs CMOS NOR gate

The CMOS NOR gate CD4025B (pin-to-pin compatible with ST's HCF4025BE 14-lead dual in-line CMOS gate logic device in a plastic SO-14 micropackage) fits very well with the light dimmer application requirements by performing the control of the board.

Its main features are:

- propagation delay time: t_{PD} = 60 ns (typ.) at V_{DD} = 10 V, C_L = 50 pF
- buffered inputs and outputs
- standardized symmetrical output characteristic
- 100 % tested for maximum quiescent current at 20 V
- 5 V, 10 V and 15 V parametric ratings
- maximum input current of 1 µA at 18 V over full package temperature range; 100 nA at 18 V and 25 °C

- noise margin (over full package temperature range): 1 V at V_{DD}=5 V, 2 V at V_{DD}=10 V and 2.5 V at V_{DD}=15 V.

2.4 Linear rotary potentiometer

A single linear rotary potentiometer equipped with a mechanical switch which opens the circuit at minimum setting is used to implement lamp current dimming and power regulation with on/off power switch and up/down dimming functions.

The main characteristics include:

- resistance range (LAW): 1 kΩ to 1 MΩ
- resistance tolerance: ±20 % (±10 % per selection)
- rated dissipation at 40 °C: 0.4 W
- limiting element voltage: 500 V DC or AC RMS
- terminal resistance: 5 Ω maximum
- noise (ENR): 2 % maximum
- mechanical rotation: 300°
- operating temperature range: -25 to +70 °C

3 Board performances

3.1 Experimental test and results @ 230VAC

The MOS-based dimmer solution includes two STF17N62K3 MOSFETs connected in anti-series configuration and a single linear potentiometer to set the turn-on time (or duty cycle) of the devices as in the following three operating conditions representing the minimum, medium and maximum levels of lamp current dimming and input power absorbed by the board:

- minimum power: ~2.0 ms (or ~20 % of duty cycle in the semiperiod)
- medium power: ~4.5 ms (or ~45 % of duty cycle in the semiperiod)
- maximum power: ~8.2 ms (or ~82 % of duty cycle in the semiperiod)

The following figures show the waveforms acquired on the steady state operation with 300 W halogen technology incandescent bulbs at 230 V_{AC} input mains for the working conditions described above for the MOSFETs.

The waveforms were acquired by scope with the signal color codes:

- Q1 drain current: signal ID1 = yellow
- Q2 drain current: signal ID2 = blue
- Q1 drain-source voltage: signal VDS1 = red
- Q2 drain-source voltage: signal VDS2 = green

Figure 11: Steady state operation with ~2.0 ms turn-on time @ minimum input power

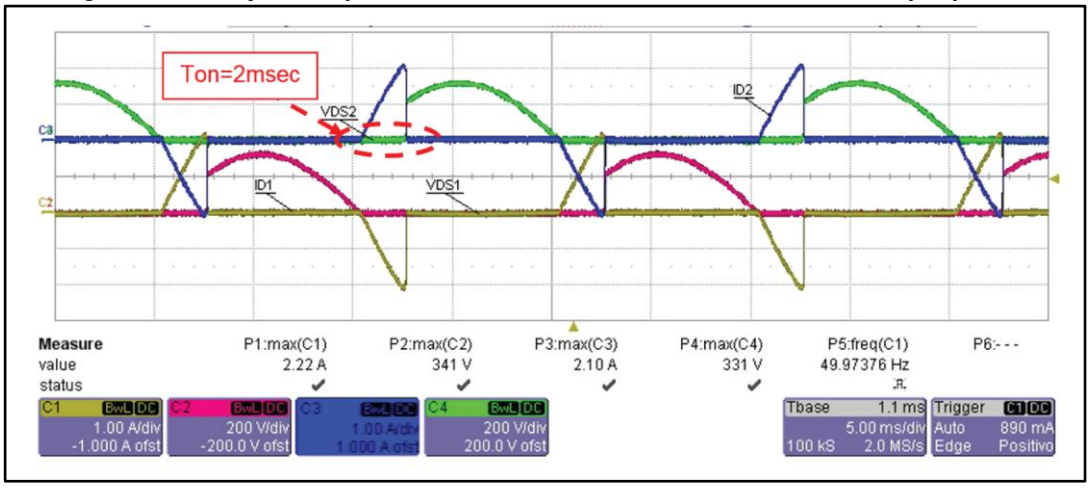


Figure 12: Steady state operation with ~4.5 ms turn-on time @ medium input power

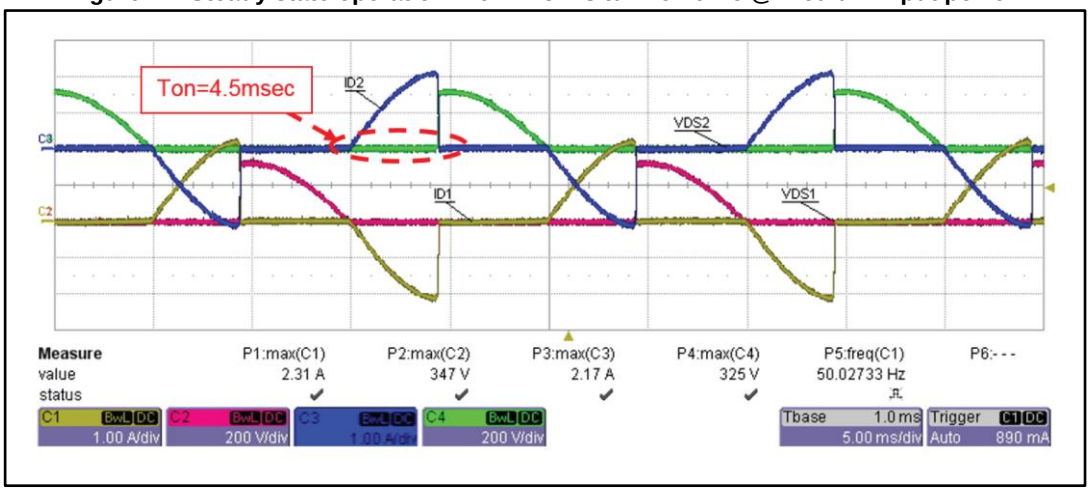
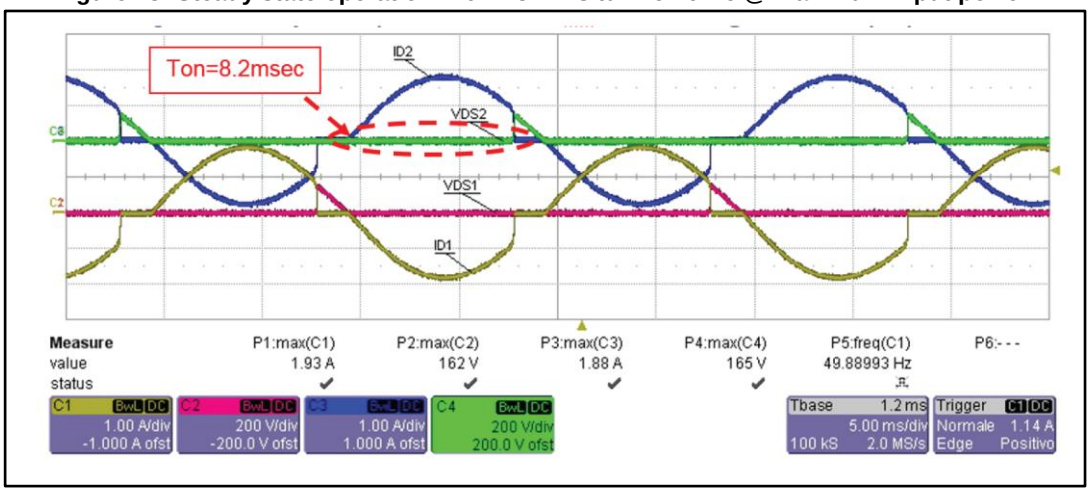


Figure 13: Steady state operation with ~ 8.2 ms turn-on time @ maximum input power



The following figures show the waveforms acquired for the input signals to the digital logic circuit, respectively the voltages on the pins PIN3 (V_{PIN3}) and PIN5 (V_{PIN5}) together with the 230 V_{AC} input mains, during the steady state operation with halogen technology incandescent bulbs at the minimum, medium and maximum input power conditions.

Waveforms were acquired by scope with the following signal color codes:

- input signal on the PIN3: voltage V_{IN3} = green
- input signal on the PIN5: voltage V_{IN5} = yellow
- input main voltage: signal V_{Line} = red

Figure 14: Voltage signals VPIN3 and VPIN5 in steady state operation @ minimum input power

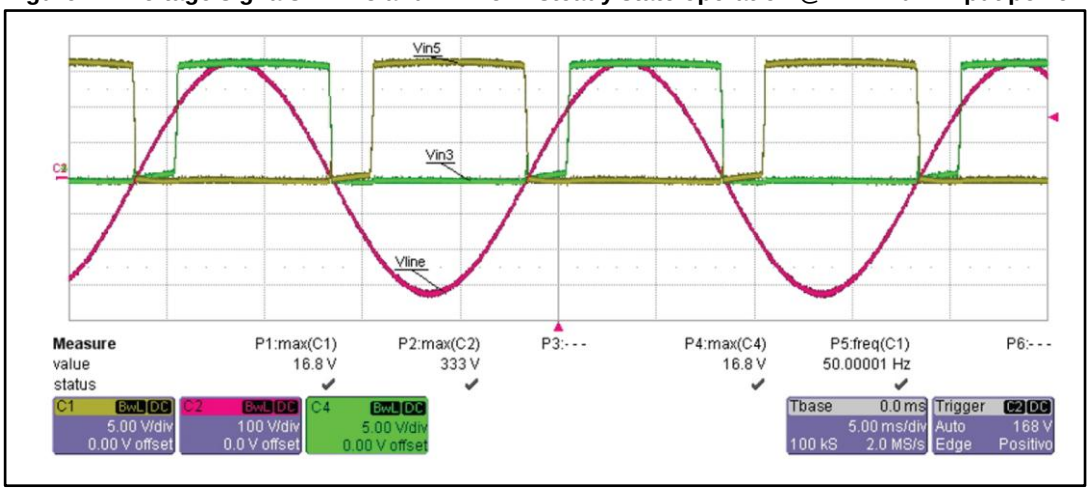


Figure 15: Voltage signals VPIN3 and VPIN5 in steady state operation @ medium input power

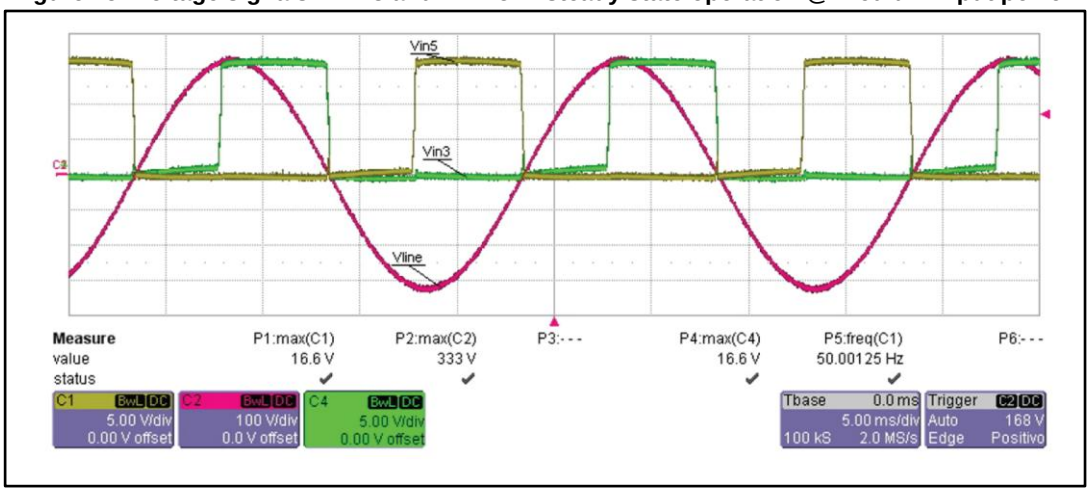
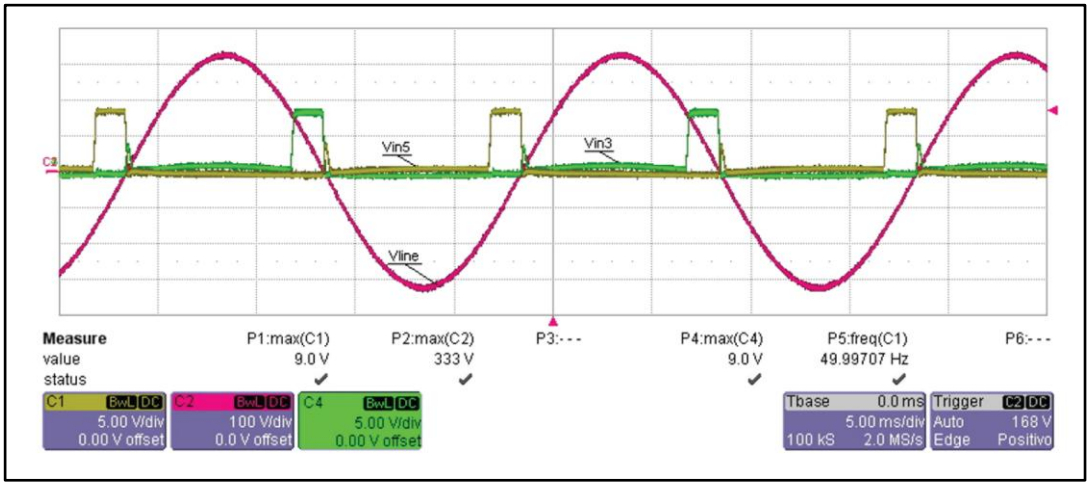


Figure 16: Voltage signals VPIN3 and VPIN5 in steady state operation @ maximum input power

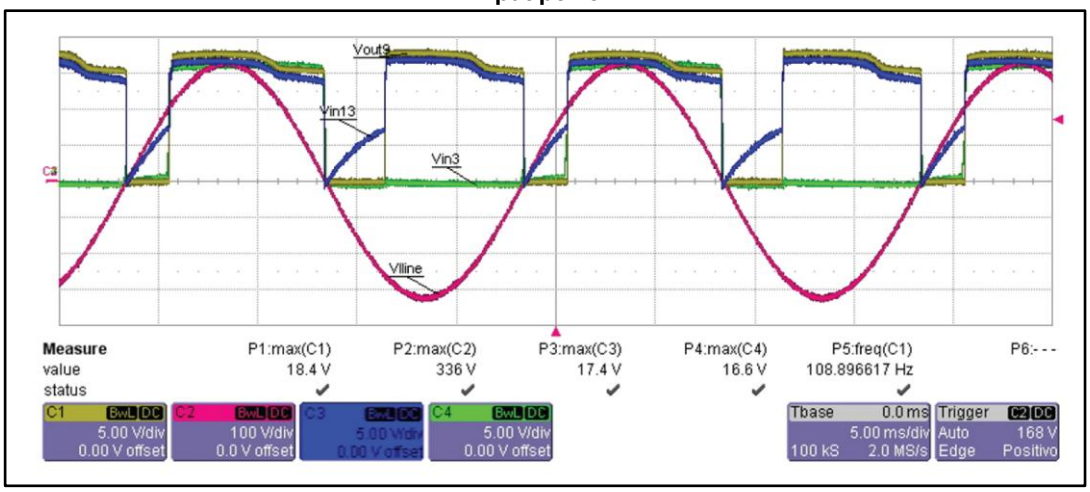


The figure below shows the waveforms acquired for the digital logic circuit input and output signals, respectively the voltages on the pins PIN3 (V_{PIN3}), PIN13 (V_{PIN13}) and PIN9 (V_{PIN9}) together with the 230 V_{AC} input mains during the steady state operation with halogen technology incandescent bulbs at the minimum input power condition and 230 V_{AC} input mains.

Waveforms were acquired by scope with the following signal color codes:

- input signal on the PIN3: voltage V_{IN3} = green
- input signal on the PIN13: voltage V_{IN13} = blue
- output signal on the PIN9: voltage V_{OUT9} = yellow
- input main voltage: signal V_{Line} = red

Figure 17: Voltage signals VPIN3, VPIN9 and VPIN13 in steady state operation @ minimum input power

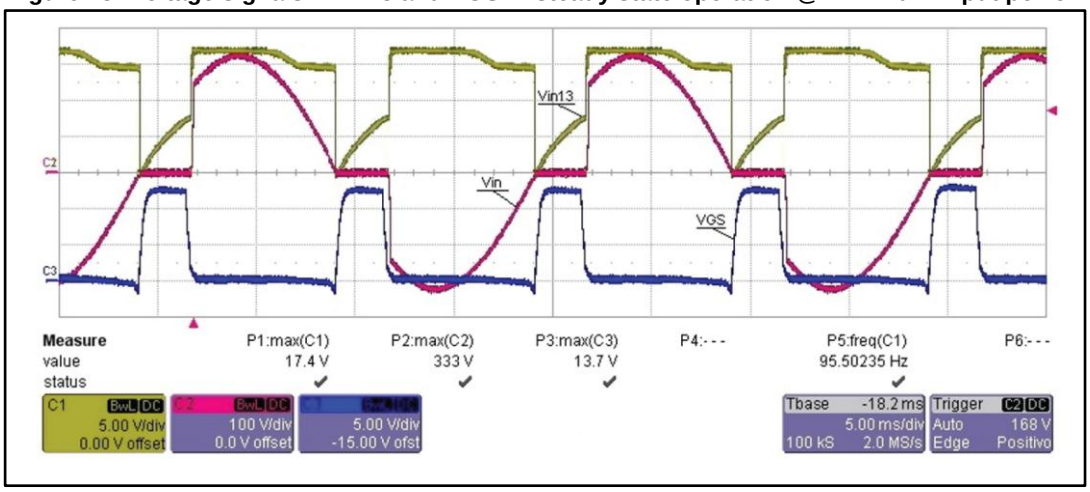


The following figure shows the waveforms acquired respectively for the input digital logic circuit signal of the voltage on PIN13 (V_{PIN13}), the gate-to-source voltage signal V_{GS} and the dimmer input voltage signal V_{in} during the steady state operation with halogen technology incandescent bulbs at the minimum input power condition and 230 V_{AC} input mains.

Waveforms were acquired by scope with the following signal color codes:

- input signal on the PIN13: voltage V_{IN13} = yellow
- gate-source voltage: signal V_{GS} = blue
- dimmer input voltage: signal V_{IN} = red

Figure 18: Voltage signals VPIN13 and VGS in steady state operation @ minimum input power



As can be seen, the MOSFET gate-source voltage is set to approx. 14 V during the conduction phases in order to keep the channel of the devices activated while crossed by the lamp current.

3.2 Electromagnetic compatibility test

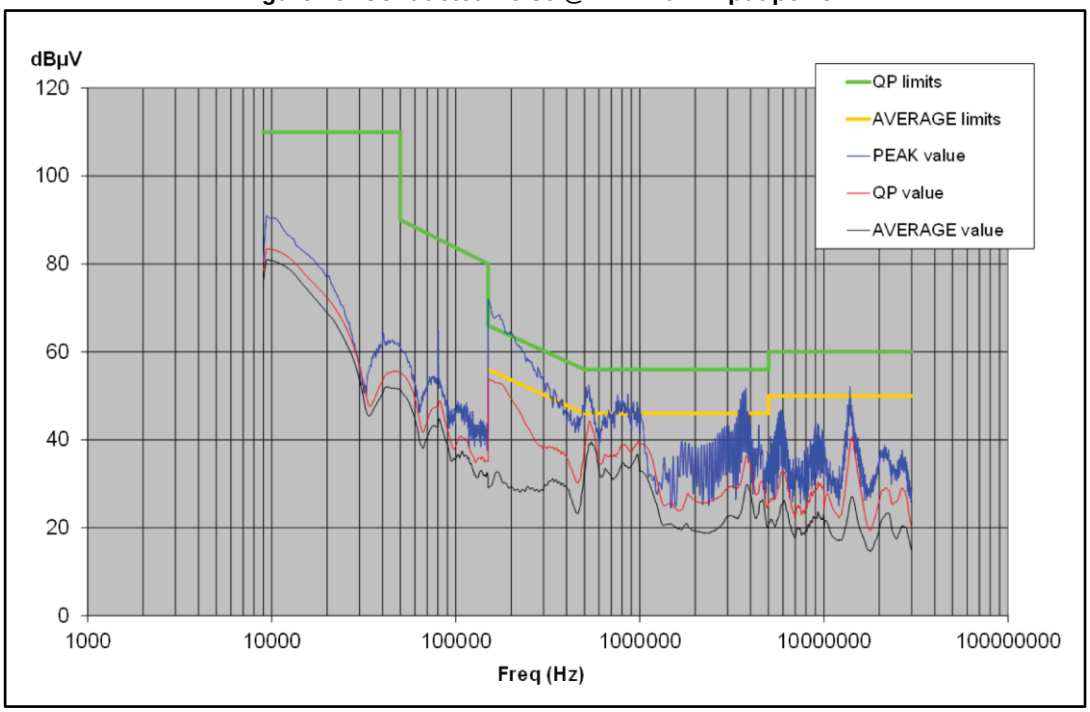
3.2.1 EMC conducted noise compliance according to EN 55015

Conducted emission noise was tested according to standard **EN 55015** under the following conditions:

- 230 V_{RMS} - 50 Hz mains voltage
- 300 W/230 V_{AC} incandescent bulbs with halogen technology
- tests were carried out with the rotary potentiometer set to different rotation angles corresponding to different conduction angles/times of the MOSFETs and input power levels absorbed by the dimmer

The following figure gives the measurement of the maximum conducted noise level reached for the minimum input power level condition (40 W).

Figure 19: Conducted noise @ minimum input power



The above figure demonstrates that the conducted emission noise measured at the minimum input power condition (i.e., worst case for the generation of the EMI disturbances) was compliant with the EN55015 electronic standard specifications, with the QP and AV detectors always below the corresponding QP and AV limits in the frequency range from 9 kHz to 30 MHz. As can be seen, thanks to the appropriate setting of the resistances on the gate driving network to the MOSFETs, no LC noise input filter is needed to meet the European EMC standard regulation in force for the conducted disturbances.

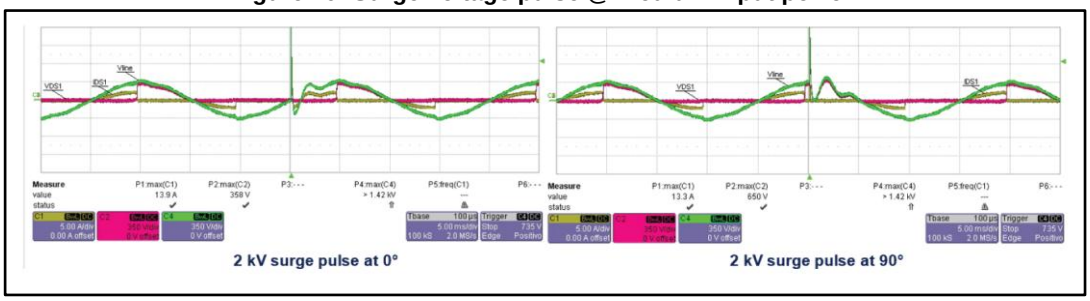
3.2.2 Surge voltage immunity test

Surge immunity tests were carried out on the MOS-based dimmer in order to analyze the board performance when sequences of high energy but relatively slow transient overvoltages are applied on the power lines. The tests were performed according to the standard IEC 61000-4-5 relating to the immunity requirements by applying voltage surges of amplitudes equal to 2 kV in both positive and negative polarities with different phase angles shifted in relation to the input main voltage.

A 300 W/230 V_{AC} halogen technology incandescent bulbs is connected in series to the board running under normal operating conditions at 230V_{AC} and 50Hz frequency.

The figure below shows the STF17N62K3 MOSFET response during the tests performed when a 2 kV surge pulse with positive polarity is applied to the AC power port in differential mode (symmetrical configuration as line-to-line between the phase and neutral lines) with 0º and 90º shifted phase angles respectively under medium input power working conditions for the dimmer. The waveforms acquired by scope for the MOSFET Q1 are the drain-source voltage (VDS1 signal in red), the drain-source current (IDS1 signal in yellow) and the input main voltage (V_{Line} signal in green).

Figure 20: Surge voltage pulse @ medium input power



The MOSFET STF17N62K3 was able to withstand the surge pulses without any failure condition and the dimmer continued to operate normally without any temporary degradation or loss of functionality and with automatic return to normal operation after the disturbance ceased.

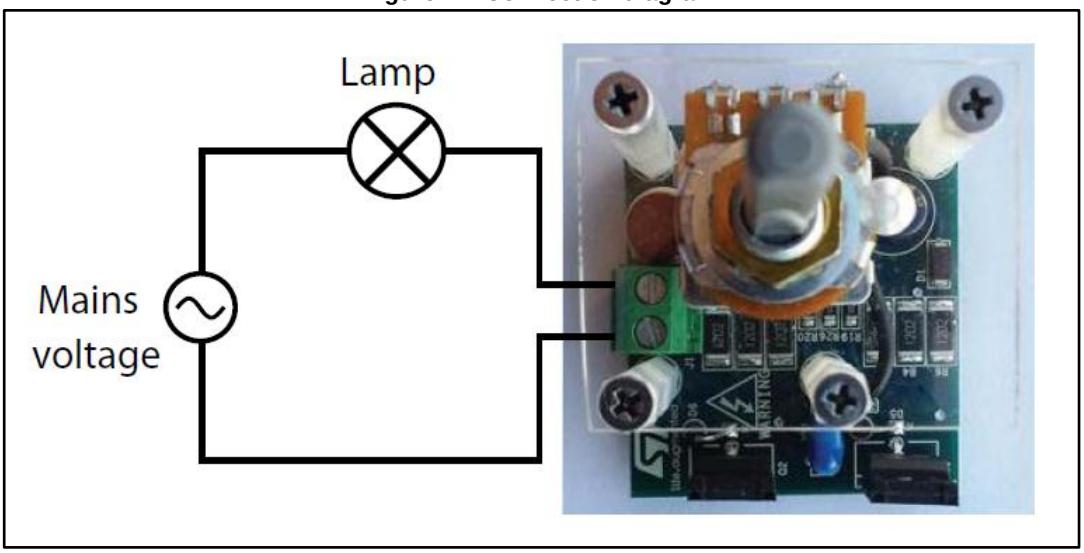
4 Getting started

4.1 Board connection

The figure below shows the connection diagram of the STEVAL-ILD005V1 to the lamp to be dimmed.

Please unplug the circuit from the line before setting the different connections.

Figure 21: Connection diagram



1. header J1 is used to connect the two-wire dimmer to the mains in series with the lamp
2. terminals T1 or T2 of the Header J1 can either be connected to the lamp or directly to the mains

Appropriate connection of the lamp to mains neutral or line depends on the applicable electrical safety regulations, even if the lamp must usually be connected to neutral.

4.2 User interface

The user interface consists of a rotative potentiometer with integrated ON/OFF switch:

1. the ON/OFF switch is used to turn the dimmer board and lamp on and off
2. the clockwise rotation of the potentiometer up to the maximum rotational angle (representing the maximum resistive value) allows continuous power absorption and light emission modification by increasing lamp brightness up to the maximum intensity level
3. the anticlockwise rotation of the potentiometer up to the minimum rotational angle (representing the minimum resistive value) allows continuous power absorption and light emission modification by decreasing lamp brightness down to the minimum intensity level

4.3 Steps for board testing

Follow this procedure to use the STEVAL-ILD005V1 board:

1. connect one lamp terminal to one J1 header terminal (T1 or T2) as shown in *Figure 21: "Connection diagram"*
2. connect the other lamp terminal to a plug of the 230 Vac AC power source switched off
3. connect the other J1 terminal to the other plug of the 230Vac AC power source switched off
4. switch the 230Vac AC power source on
5. if the potentiometer switch opens the circuit in the OFF position, close the switch by rotating the potentiometer clockwise to turn the dimmer board and lighting load on

At this point, the STEVAL-ILD005V1 is working correctly if:

- the lamp brightness increases by rotating the potentiometer clockwise
- the lamp brightness decreases by rotating the potentiometer in anticlockwise
- the lamp brightness remains stable when no rotation is performed

4.4 Safety instruction

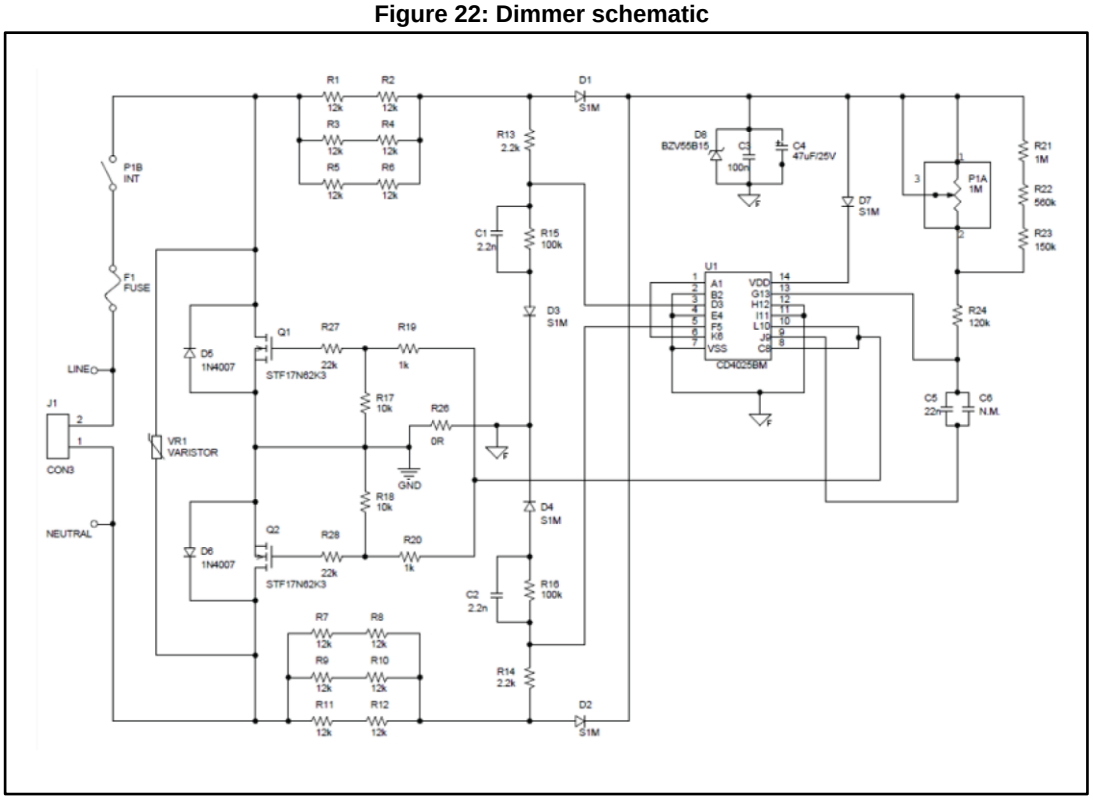
Follow this procedure to use the STEVAL-ILD005V1 board:

Waring: The high voltage levels used to operate the MOS-based dimmer evaluation board could present a serious electrical shock hazard. This evaluation board must be used in a suitable laboratory by qualified personnel only, familiar with the installation, use, and maintenance of electrical power systems.

The STEVAL-ILD005V1 evaluation board is designed for demonstration purposes only, and shall not be used either for domestic installation or for industrial installation.

5 Dimmer schematic

Figure 22: Dimmer schematic



A 5 A/250 V_{AC} fuse F1 is mounted to protect MOSFETs in case of lamp flash-overs or accidental short-circuits.

6 Board layout and silkscreen

Figure 23: Component layout – top and bottom assembly

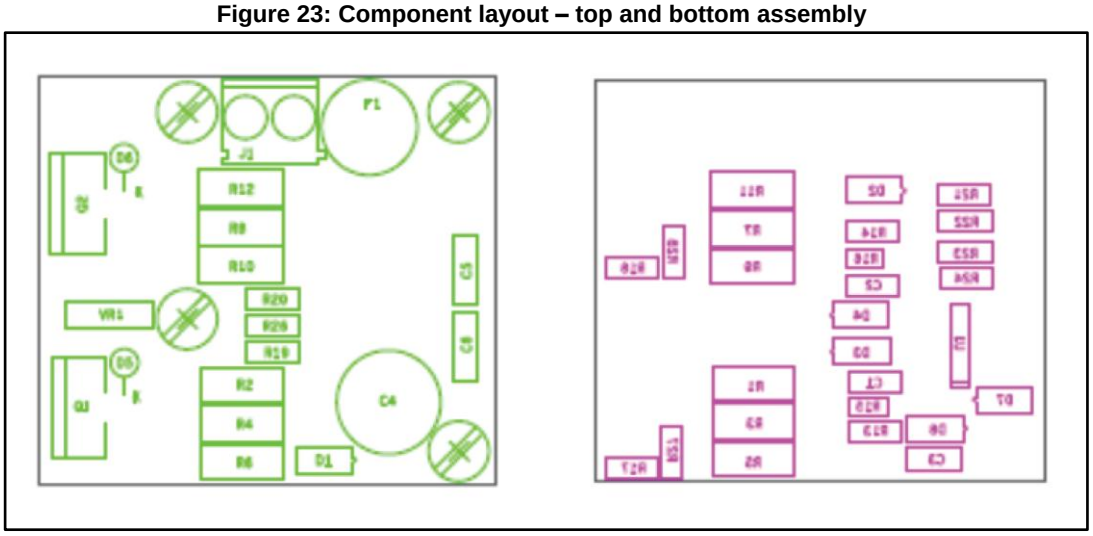
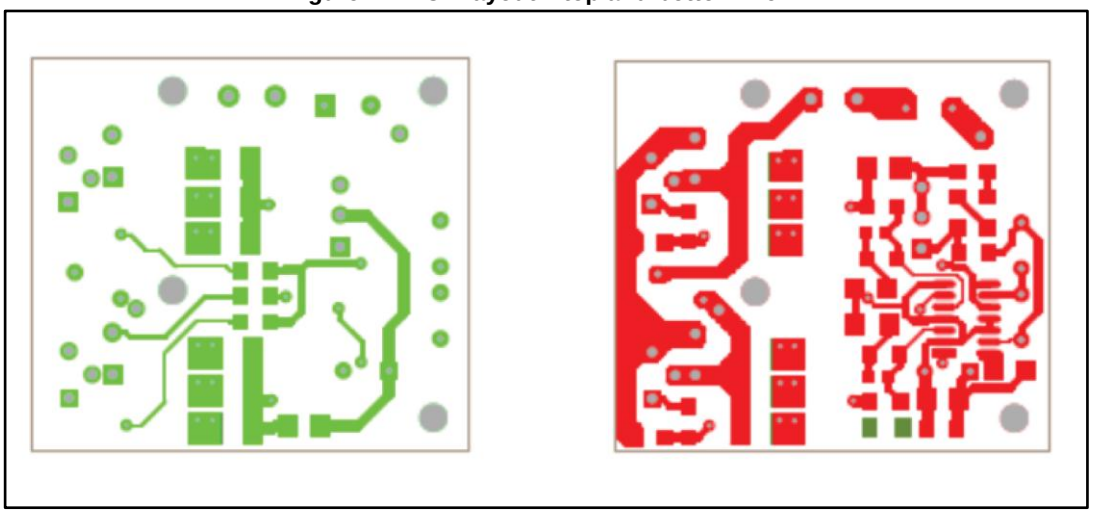


Figure 24: PCB layout – top and bottom view



7 Bill of material

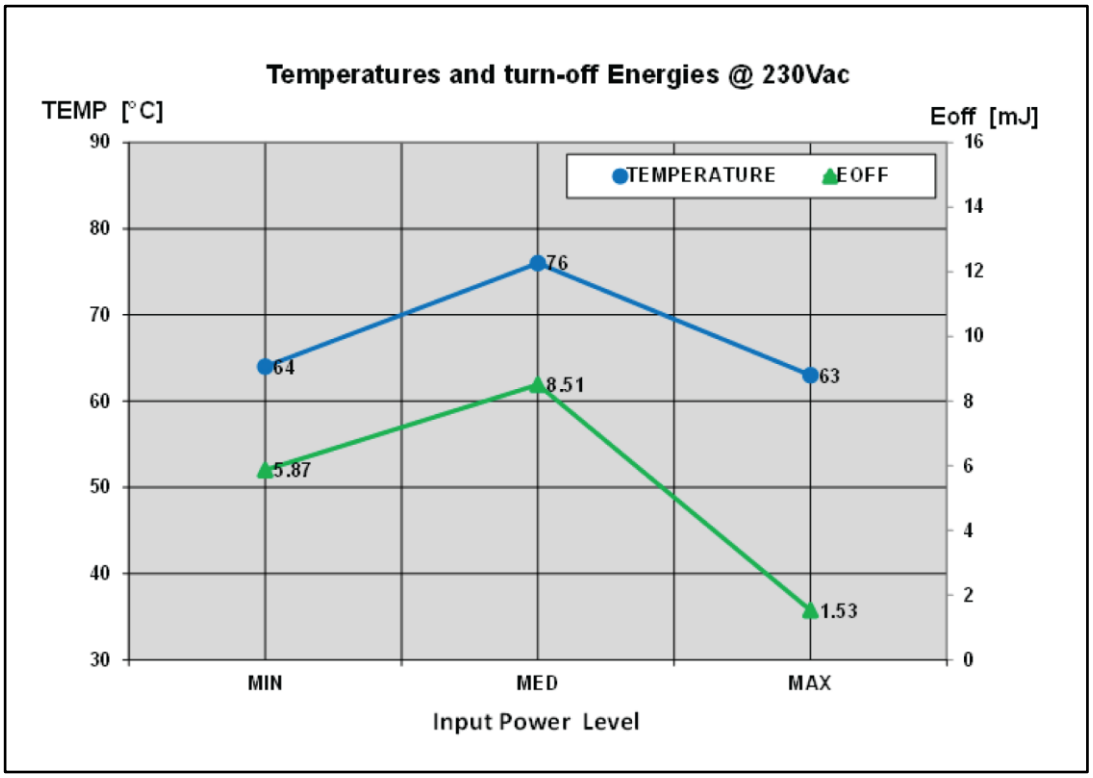
Table 3: Bill of material

Reference	Part / value
U1	CD4025BM
Q1, Q2	STF17N62K3
P1A/P1B	1 MΩ/0.4 W
R1, R2, R3, R4, R5, R6, R7, R8, R9 R10, R11, R12	12 kΩ / 2 W
R13, R14	2.2 kΩ / 0.25 W
R15, R16	100 kΩ / 0.125 W
R17, R18	10 kΩ / 0.25 W
R19, R20	1 kΩ / 0.25 W
R21	1 MΩ / 0.25 W
R22	560 kΩ / 0.25 W
R23	150 kΩ / 0.25 W
R24	120 kΩ / 0.25 W
VR1	Varistor / 420 V
R26	0 Ω / 0.25 W
R27, R28	22 kΩ / 0.25 W
D1, D2, D3, D4, D7	S1M
D5, D6	1N4007
D8	BZV55B15
C1, C2	2.2 nF / 0.25 W
C4	47 µF / 25V
C3	100 nF / 0.25 W
C5	22 nF / 100V_{CC}
C6	N.M.
Rfuse	5 A / 250 V_{AC}
FUSE HOLDER	6.3 A / 250 V_{AC}
J1	2-pin PCB screw terminal block

8 Temperatures and turn-off energies

The figure below shows the different temperatures and turn-off switching energies measured for the STF17N62K3 MOSFETs working under the three different operating conditions for minimum, medium and maximum levels of lamp current dimming and input power absorbtion by the board connected to 300 W/230 V_{AC} halogen technology incandescent bulbs.

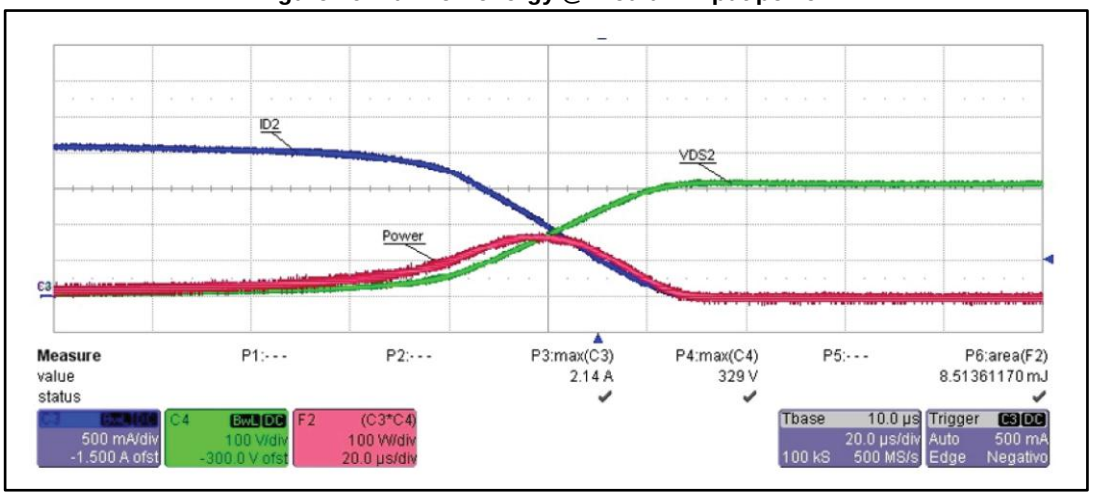
Figure 25: Temperatures and turn-off energies @ 230 VAC



The maximum case temperatures (approx. 76 °C without heatsinks) are reached in free air conditions (at 25 °C room temperature) for the medium input power level operation and can be reduced by mounting appropriate heatsinks in contact with the MOSFETs. Switching losses can be reduced by decreasing the original value of the two gate drive resistances R27 and R28 (set to 22 kΩ) to speed up the turn-off switching transients. This modification implies a new noise emission condition for the conducted disturbances introduced by the dimmer and may require the use of an appropriate EMI input filter to guarantee compliance with the EN55015 standard.

The following figure depicts the turn-off transient detail for MOSFET Q2 switching under the medium input power operating condition.

Figure 26: Turn-off energy @ medium input power



9 Conduction times calculation

Assuming a sinusoidal envelope over the period T = 1/freq for the current lamp waveform under normal steady state conditions, as in:

Equation 3

$$I_{lamp}(t) = I_{lamp\_MAX} \cdot \sin(2\pi \cdot freq \cdot t) \quad \text{for } 0<t<T_{COND} \text{ and } T/2<t<T/2+T_{COND}$$

by neglecting the voltage drops on the $R_{DS(on)}$ channel resistances and on the forward biased antiparallel diodes during the MOSFET conduction phases, we can consider the mains voltage entirely applied on the lamp and therefore express the power P_{IN} for $D = \frac{T_{COND}}{T}$ and conduction time T_{COND} thus:

Equation 4

$$P_{IN} = \frac{I_{lamp\_MAX} \cdot V_{main\_MAX}}{\pi}\left[\pi \cdot D - \left(\frac{1}{2} \cdot sin(2\pi \cdot D) \cdot cos(2\pi \cdot D)\right)\right]$$

For a 90° MOSFET conduction angle, $D = \frac{T_{COND}}{T} = \frac{1}{4}$, so:

Equation 5

$$P_{IN\_90deg} = \frac{1}{4} \cdot I_{lamp\_MAX} \cdot V_{main\_MAX}$$

The max value I_{lamp_MAX} for the current lamp signal (equalt to the maximum dimmer input current I_{IN_MAX}) can be expressed with the following formula where P_{IN_90deg} is the input power level at 90° MOSFET conduction angle and V_{main_MAX} is the maximum mains voltage value:

Equation 6

$$I_{lamp_{MAX}} = \frac{4 \cdot P_{IN\_90deg}}{V_{main\_MAX}}$$

By inserting:

$P_{IN\_90deg} = P_{IN\_MED} + \Delta\% \cdot P_{IN\_MED} \cong 158W$ with P_{IN_MED} = 150 W and Δ % = 5 %

and

$V_{main\_MAX} = 230 \cdot \sqrt{2}V$

We obtain:

Equation 7

$$I_{lamp\_MAX} = \frac{4 \cdot 158}{230 \cdot \sqrt{2}} \cong 1.94A$$

The rms value of the lamp current I_{lamp_RMS} (equal to the rms value of the dimmer input current I_{IN_RMS}) can be expressed with the following formula where P_{IN_MAX} is the maximum input power, V_{main_RMS} is the rms value of the mains voltage and PF_{MAX} is the power factor at the maximum input power:

Equation 8

$$I_{lamp\_RMS} = I_{IN\_RMS} = \frac{P_{IN\_MAX}}{V_{main\_RMS} \cdot PF_{MAX}}$$

By imposing the following conditions for maximum input power operation:

- P_{IN_MAX} = 300 W
- V_{main_RMS} = 230 V
- PF_{MAX} = 0.98

We obtain:

Equation 9

$$I_{lamp\_RMS} = \frac{300}{230 \cdot 0.98} = 1.33A$$

The following formula correlates I_{lamp_MAX} with I_{lamp_RMS} in the phase cut dimming principle with a lamp current I_{lamp} having sinusoidal profile where $D = \frac{T_{COND}}{T}$ for MOSFET conduction time T_{COND}:

Equation 10

$$I_{lamp\_MAX} = \frac{I_{lamp\_RMS}}{\sqrt{D - \frac{sin(4\pi D)}{4\pi}}}$$

Which can be reformulated thus:

Equation 11

$$\sqrt{D - \frac{sin(4\pi D)}{4\pi}} = \left(\frac{I_{lamp\_RMS}}{I_{lamp\_MAX}}\right)$$

Where:

Equation 12

$$\frac{I_{lamp\_RMS}}{I_{lamp\_MAX}} = \frac{1.33}{1.94} = 0.686$$

With an appropriate choice for T_{COND} = 8.2 ms:

Equation 13

$$D = \frac{T_{COND}}{T} = \frac{8.2\ ms}{20\ ms} = 0.41$$

and by inserting this value in $\sqrt{D - \frac{sin(4\pi D)}{4\pi}}$ for *Equation 11*, we obtain:

Equation 14

$$\sqrt{D - \frac{sin(4\pi D)}{4\pi}} - \left(\frac{I_{lamp\_RMS}}{I_{lamp\_MAX}}\right) \cong 0.694 - 0.686 = 8 \cdot 10^{-3}$$

Therefore, from the result obtained in the above equation, the time T_{COND} = 8.2 ms is a good approximation of the right value of the MOSFET conduction time during maximum input power conditions.

Assuming a linear envelope in the period T=1/freq for the current and voltage lamp waveforms during normal steady state operation at minimum input power, as in:

Equation 15

$$I_{lamp}(t) = \frac{I_{lamp\_MAX}}{T_{COND}} \cdot t \quad \text{for } 0<t<T_{COND} \text{ and } T/2<t<T/2+T_{COND}$$

Equation 16

$$V_{lamp}(t) = \frac{V_{lamp\_MAX}}{T_{COND}} \cdot t$$

for 0<t<T_{COND} and T/2<t<T/2+T_{COND}

In the above equation, by neglecting the voltage drops on the $R_{DS(on)}$ channel resistances and on the forward biased antiparallel diodes during the MOSFET conduction phases, we can express V_{lamp_MAX} for the voltage lamp signal as a function of the mains voltage thus:

Equation 17

$$V_{lamp\_MAX} = 230 \cdot \sqrt{2} \cdot \sin(2\pi \cdot freq \cdot T_{COND})$$

As D = T_{COND}/T, the lamp power for the minimum input power condition can be expressed as:

Equation 18

$$P_{IN\_MIN} = \frac{2}{3} \cdot I_{lamp\_MAX} \cdot V_{lamp\_MAX} \cdot D$$

By imposing the following minimum input power working conditions:

- P_{IN_MIN} = 40 W
- V_{main_RMS} = 230 V
- PF_{MIN} = 0.31

we calculate the rms value of the lamp current I_{lamp_RMS} (the rms value of the dimmer input current I_{IN_RMS}) with *Equation 8*:

Equation 19

$$I_{lamp\_RMS} = I_{IN\_RMS} = \frac{P_{IN\_MIN}}{V_{main\_RMS} \cdot PF_{MIN}} = \frac{40}{230 \cdot 0.31} = 0.561$$

The following formula correlates I_{lamp_MAX} with I_{lamp_RMS} in the phase cut dimming principle, with lamp current I_{lamp} having a linear variation profile where D=T_{COND}/T for MOSFET conduction time T_{COND}:

Equation 20

$$I_{lamp\_MAX} = \frac{I_{lamp\_RMS}}{\sqrt{\frac{2}{3} \cdot D}}$$

Substituting *Equation 17* and *20* into *18*, we obtain:

Equation 21

$$V_{lamp\_MAX} \cdot D = \frac{3}{2} \cdot \frac{P_{IN\_MIN}}{I_{lamp\_MAX}} \Rightarrow \sqrt{D} \cdot sin(2\pi \cdot D) = \frac{\sqrt{3}}{2} \cdot \frac{P_{IN\_MIN}}{I_{lamp\_RMS} \cdot V_{main\_RMS}}$$

where:

Equation 22

$$\frac{\sqrt{3}}{2} \cdot \frac{P_{IN\_MIN}}{I_{lamp\_RMS} \cdot V_{main\_RMS}} = \frac{\sqrt{3}}{2} \cdot \frac{40}{0.561 \cdot 230} = 0.268$$

With an appropriate choice for T_{COND} = 2.0 ms:

Equation 23

$$D = \frac{T_{COND}}{T} = \frac{2\ ms}{20\ ms} = 0.1$$

and by substituting this value into $\sqrt{D} \cdot \sin(2\pi \cdot D)$ of *Equation 21*, we obtain:

Equation 24

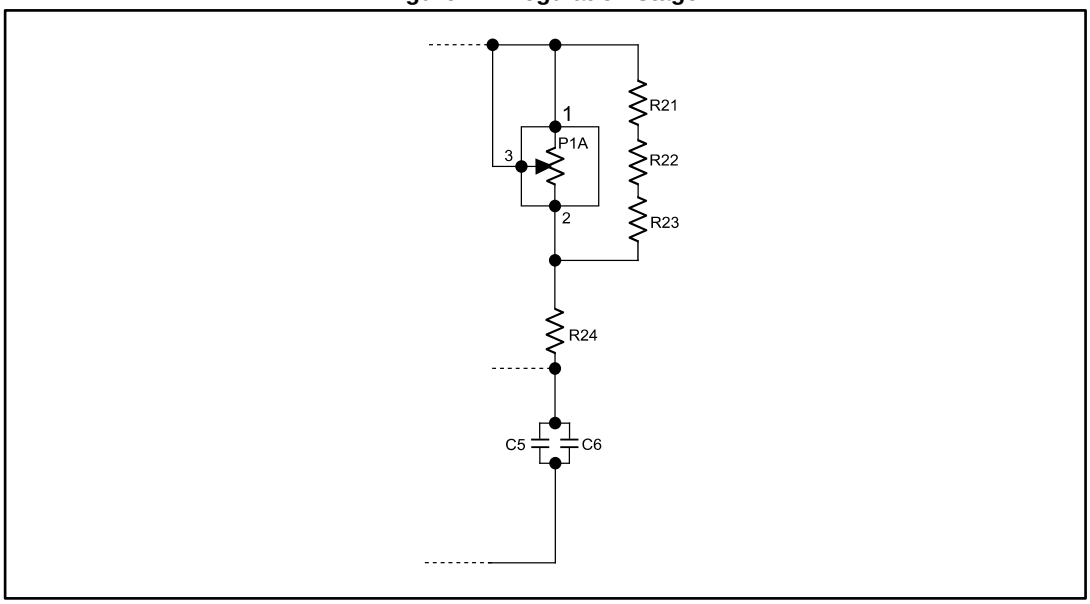
$$\sqrt{D} \cdot sin(2\pi \cdot D) - \frac{\sqrt{3}}{2} \cdot \frac{P_{IN\_MIN}}{I_{lamp\_RMS} \cdot V_{main\_RMS}} \cong 0.185 - 0.268 = -8 \cdot 10^{-2}$$

Therefore, from the above equation, the time T_{COND} = 2.0 ms is a good approximation of the right value of the MOSFET conduction time under minimum input power conditions.

10 Regulation stage setting

To calculate the potentiometer resistance variation range and magnitude of the other passive components (resistances and capacitances) of the dimmer regulation stage, we can analyze the conduction phases of the MOSFETS at minimum and maximum levels of power absorbed in input.

Figure 27: Regulation stage



In both phases, the supply stage electrolytic capacitance C4 (set to 47µF) discharges on the capacitive section of the regulation stage (C5 and C6 paralleled) through the resistive section with the potentiometer and resistances R21, R22, R23 and R24. During this discharge transient of capacitance C4, the two capacitances C5 and C6 are charging and increase the voltage level up to the NOR gate input threshold voltage V_T, set to around $V_{CCmax}/2$.

The condition of reaching the threshold V_T corresponds with the duration time of the conduction phase set by the potentiometer for that specific lamp dimming functionality before the beginning of the MOSFET turn-off phase.The law governing the charging transient of the regulation stage capacitive section during the MOSFET conduction phases at both minimum and maximum input power conditions is given by the formula for the charge of a capacitor in an RC series circuit supplied by a constant voltage generator, generally expressed as:

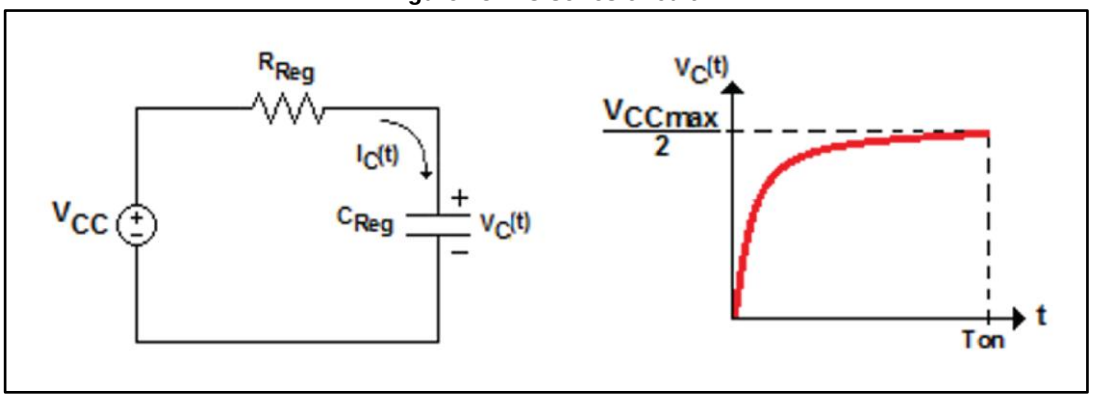
Equation 25

$$V_C(t) = (V_C(0) - V_{CC}) \cdot e^{-t/\tau} + V_{CC}$$

where:

- $V_C(t)$ is the voltage on the two paralleled capacitances C5 and C6 of the regulation stage
- $V_C(0)$ is the voltage at time t = 0 on the two paralleled capacitances C5 and C6 of the regulation stage
- V_{CC} is the voltage on the supply stage electrolytic capacitance C4
- $\tau = R_{reg}.C_{reg}$ is the time constant of the circuit, where R_{reg} is the equivalent resistance of the resistive section with the potentiometer and resistances R21, R22, R23, R24 and $C_{reg} = C_5||C_6$

Figure 28: RC series circuit



Due to the high value of the electrolytic capacitance C4 (set to 47µF) and the low current levels flowing on the regulation stage during the C4 discharge phase, we can assume the supply stage voltage V_{CC} to be constant during the charging phase of the capacitive section $C_{reg} = C_5||C_6$.

So, by inserting Vc(0) = 0, Equation 25 is reduced to:

Equation 26

$$V_C(t) = V_{CC} \cdot \left(1 - e^{-t/\tau}\right)$$

We can reformulate in terms of the τ parameter thus:

Equation 27

$$\tau = \frac{t}{ln\left(\frac{V_{CC}}{V_{CC} - V_C(t)}\right)}$$

Moreover, as the voltage level on C5 and C6 always rises during the MOSFET conduction phase up to the NOR gate input threshold voltage V_T (set to around $V_{CCmax}/2$), we can assume:

$V_C\ (T_{ON}) = V_{CC}/2$

for the MOSFET conduction time t = T_{ON} so Equation 27 becomes:

Equation 28

$$\tau = R_{reg} \cdot C_{reg} = \frac{T_{ON}}{ln(2)}$$

For the minimum input power condition, T_{ON}= 2 ms and so:

Equation 29

$$R_{reg\_min} \cdot C_{reg} = \frac{2 \cdot 10^{-3}}{ln(2)} = 2.88msec$$

By selecting R_{reg_min} = 120 kΩ for the equivalent resistance of the regulation stage resistive section at minimum input power:

Equation 30

$$C_{reg} = \frac{2.88 \cdot 10^{-3}}{120 \cdot 10^{3}} \cong 24\ nF$$

And therefore capacitance $C_{reg} = C_5||C_6$ = 22 nF is chosen for the design at the minimum input power condition.

At the maximum input power condition, due to the long time constant for the charging transient, we consider a linear variation for the voltage on the two paralleled capacitances C5 and C6 of the regulation stage; therefore, Equation 26 can be transformed into the following linearized form:

Equation 31

$$V_C(t) = \frac{I_{Reg-max}}{C} \cdot t$$

where for t = T_{ON}:

- $V_C(T_{ON}) = V_{CC}/2$
- I_{reg_max} can be chosen as the current at the t = 0 to equal $I_{reg\_max} = V_{CC}/R$.

By substituting these two conditions in Equation 31, for T_{ON}= 8.2 ms we obtain:

Equation 32

$$R_{reg\_max} \cdot C_{reg} = 2 \cdot T_{ON} \Rightarrow R_{reg\_max} = \frac{2 \cdot T_{ON}}{C_{reg}} = \frac{2 \cdot 8.2 \cdot 10^{-3}}{22 \cdot 10^{-9}} = 745\ k\Omega$$

The variability range of the equivalent resistance R_{reg} is therefore:

Equation 33

$$120\ k\Omega \leq R_{reg} \leq 745\ k\Omega$$

The following values were therefore chosen for the potentiometer and resistances R21, R22, R23, R24 of the regulation stage resistive section:

- potentiometer = 1 MΩ
- R21 = 1 MΩ, R22 = 560 kΩ, R23 = 150 kΩ, R24 = 120 kΩ

Using these resistances, the actual variation range for the equivalent resistance R_{reg} becomes:

Equation 34

$$120\ k\Omega \leq R_{reg} \leq 751\ k\Omega$$

11 Experimental test and results @ 110Vac

The following figures show the waveforms acquired under steady state operation with 90 W halogen technology incandescent bulbs at 110 V_{AC} input mains for the above mentioned operating conditions for the MOSFETs.

Waveforms were acquired by scope with the following signal color codes:

- Q1 drain current: signal ID1= yellow
- Q2 drain current: signal ID2 = blue
- Q1 drain-source voltage: signal VDS1 = red
- Q2 drain-source voltage: signal VDS2 = green

Figure 29: Steady state operation @ 110 VAC and minimum input power

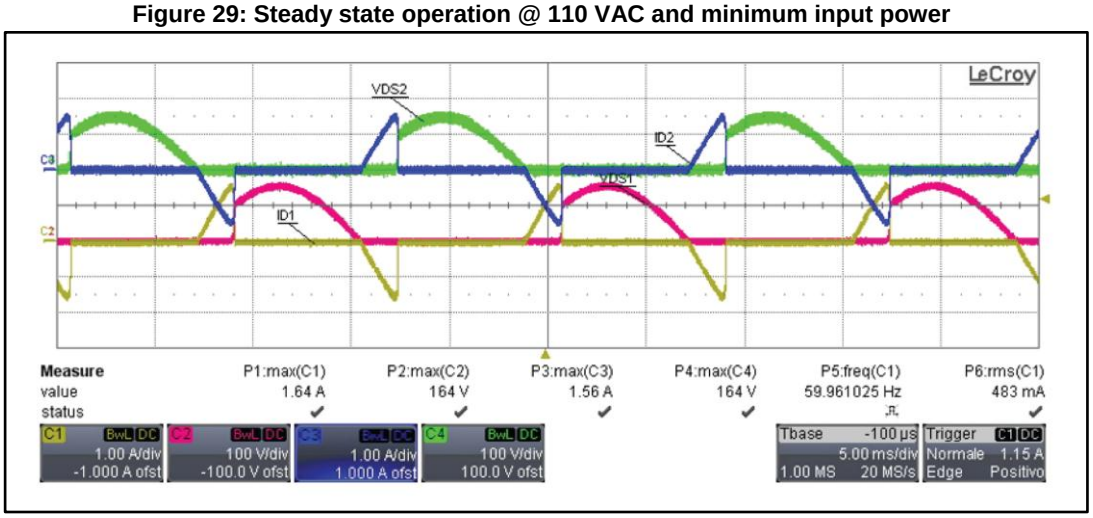


Figure 30: Steady state operation @ 110 VAC and medium input power

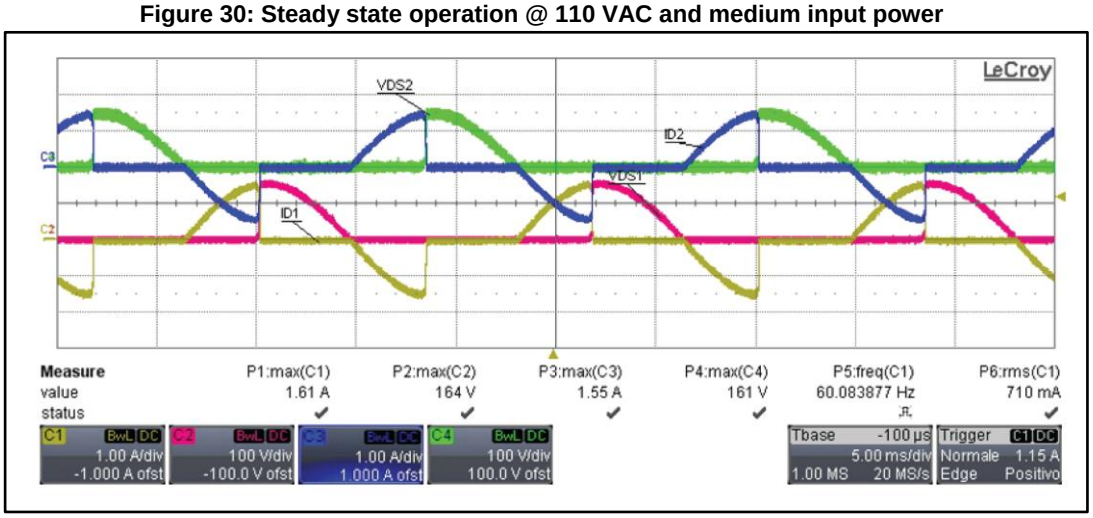
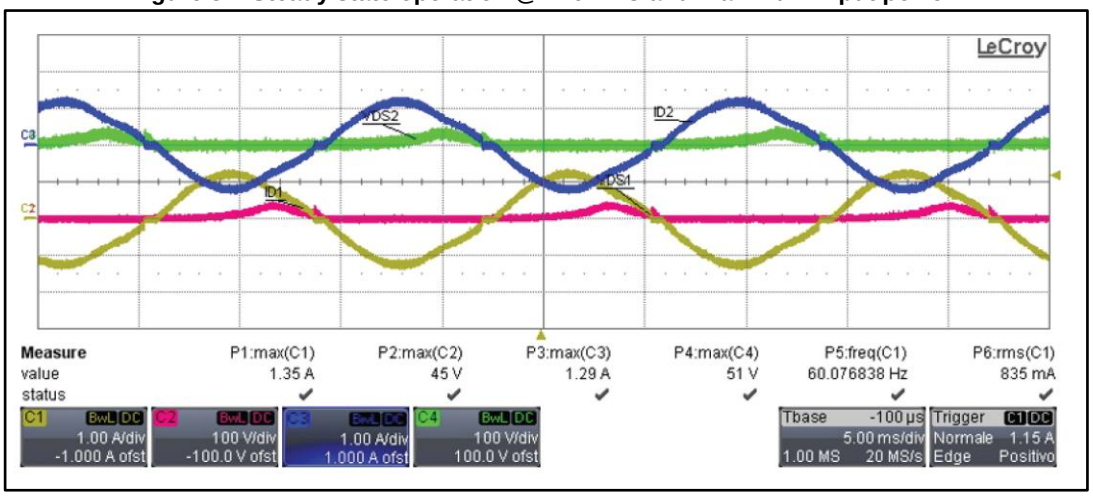
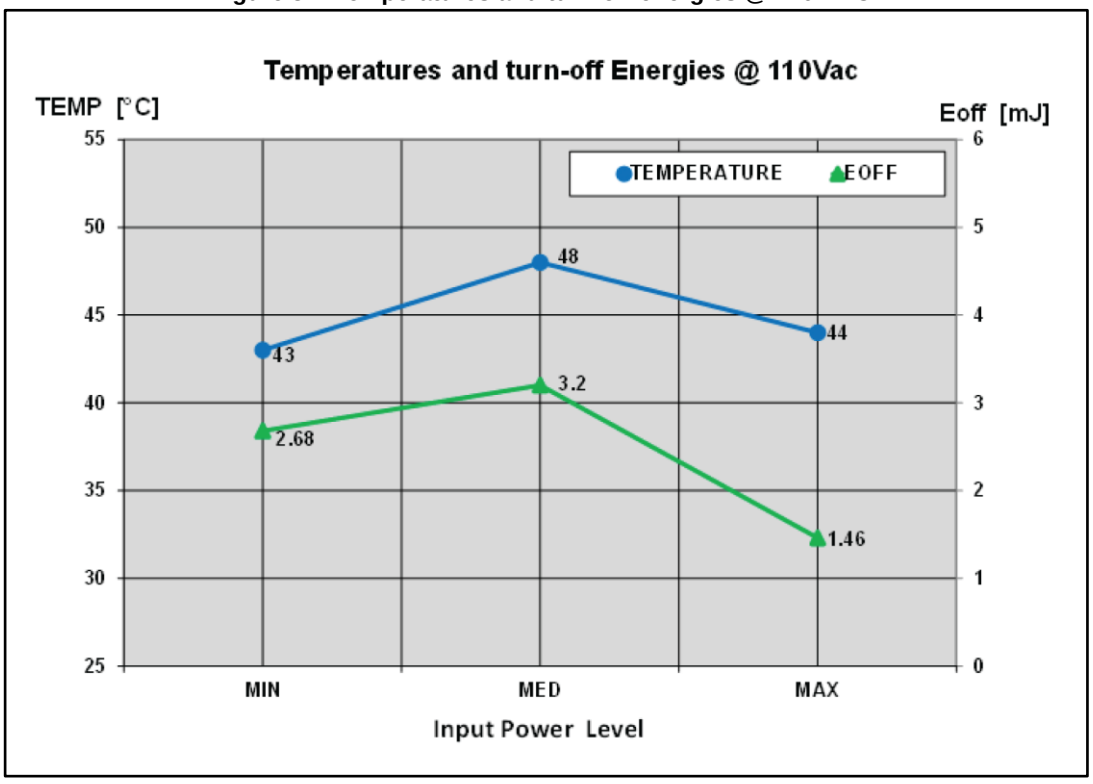


Figure 31: Steady state operation @ 110 VAC and maximum input power



The figure below shows the different temperatures and turn-off switching energies measured for the STF17N62K3 MOSFETs working under minimum, medium and maximum operating conditions for lamp current dimming and input powers absorbed by the board connected to 90 W/110 V_{AC} halogen technology incandescent bulbs.

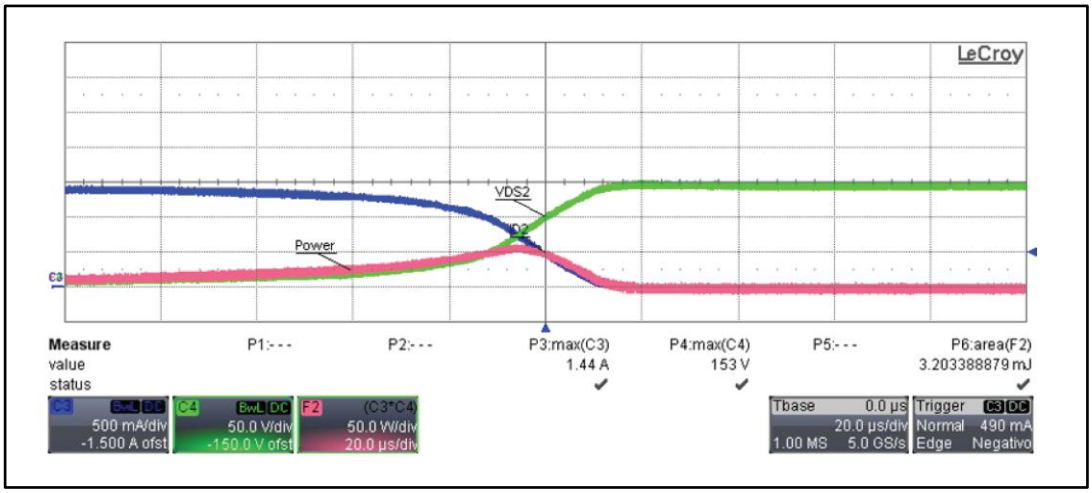
Figure 32: Temperatures and turn-off energies @ 110 VAC



The maximum case temperatures (~48 °C without heatsinks) are reached in free air conditions (25 °C room temperature) for the medium input power level operation with the original setting of 22 kΩ.

The following figure details the turn-off transient for MOSFET Q2 switching during medium input power operation.

Figure 33: Turn-off energy@ medium input power



12 Conclusion

The STEVAL-ILD005V1 evaluation board implements a trailing edge operation mode for 2-wire analog wall dimmers with flicker-free dimming and no audible noise performance for dimmable R-C lighting loads in the power range from 40 W to 300 W at 230 V_{AC} input mains, by using a triple 3-input NOR gate to perform gate driving, zero crossing and timing control functions and a switched type single linear rotary potentiometer as the control interface. Thanks to the electrical characteristics of the STF17N62K3 MOSFET with high C_{iss} values and low $R_{DS(on)}$ values at the operating currents, this MOS-based dimmer solution is able to meet the European EMC standard for conducted emission noise (EN55015), without requiring any bulky LC input filters, relying instead on appropriate setting for the resistances of the gate driving network to the active devices. At the same time, the MOSFETs show satisfactory thermo-electrical performance without any heatsink components in contact with the case and the 620 V breakdown voltage ensures good margins for passing surge immunity tests with up to 2 kV voltage pulses, in compliance with the IEC61000-4-5 standards.

13 Revision history

Table 4: Document revision history

Date	Version	Changes
12-Aug-2015	1	Initial release.

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